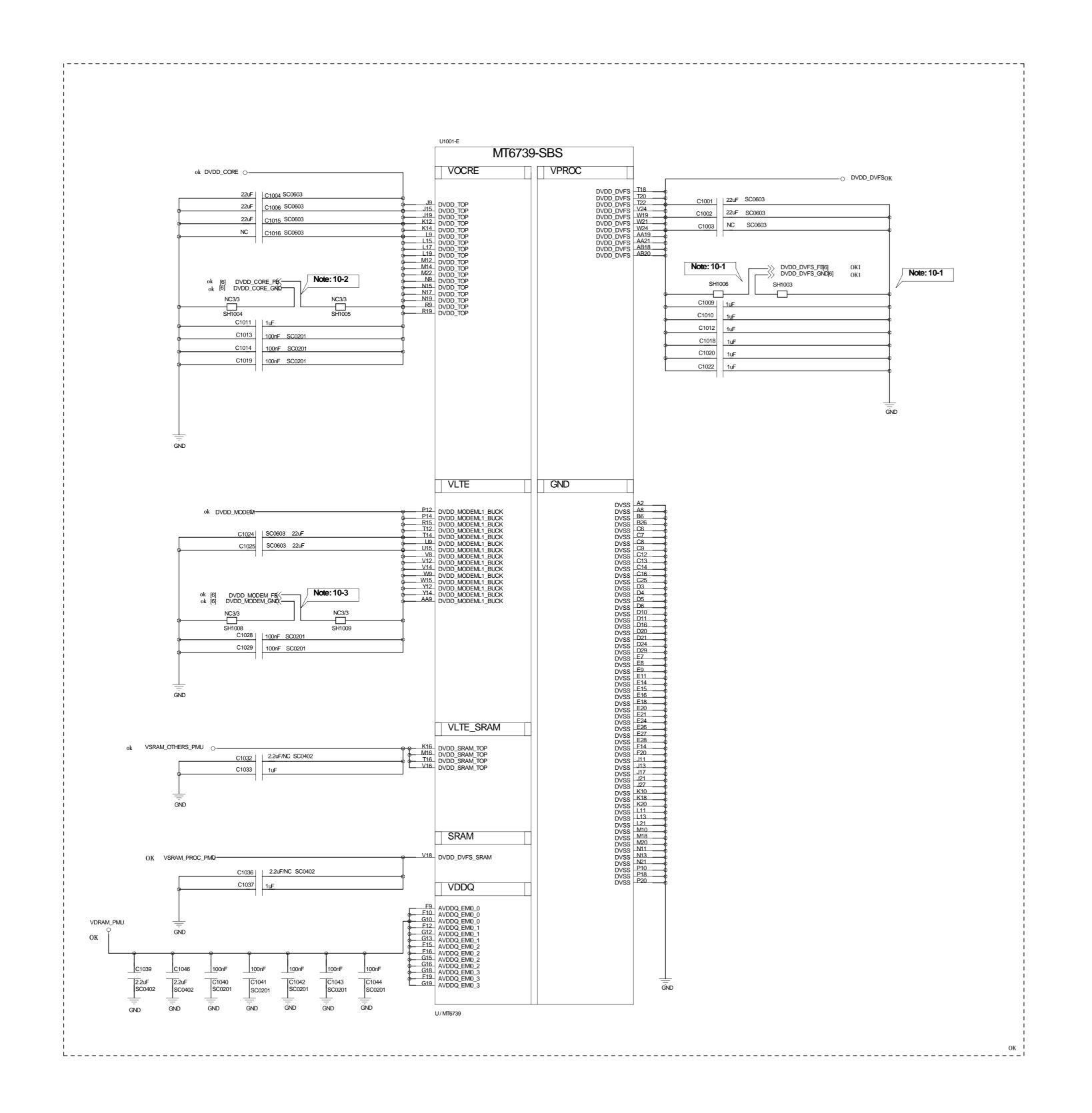
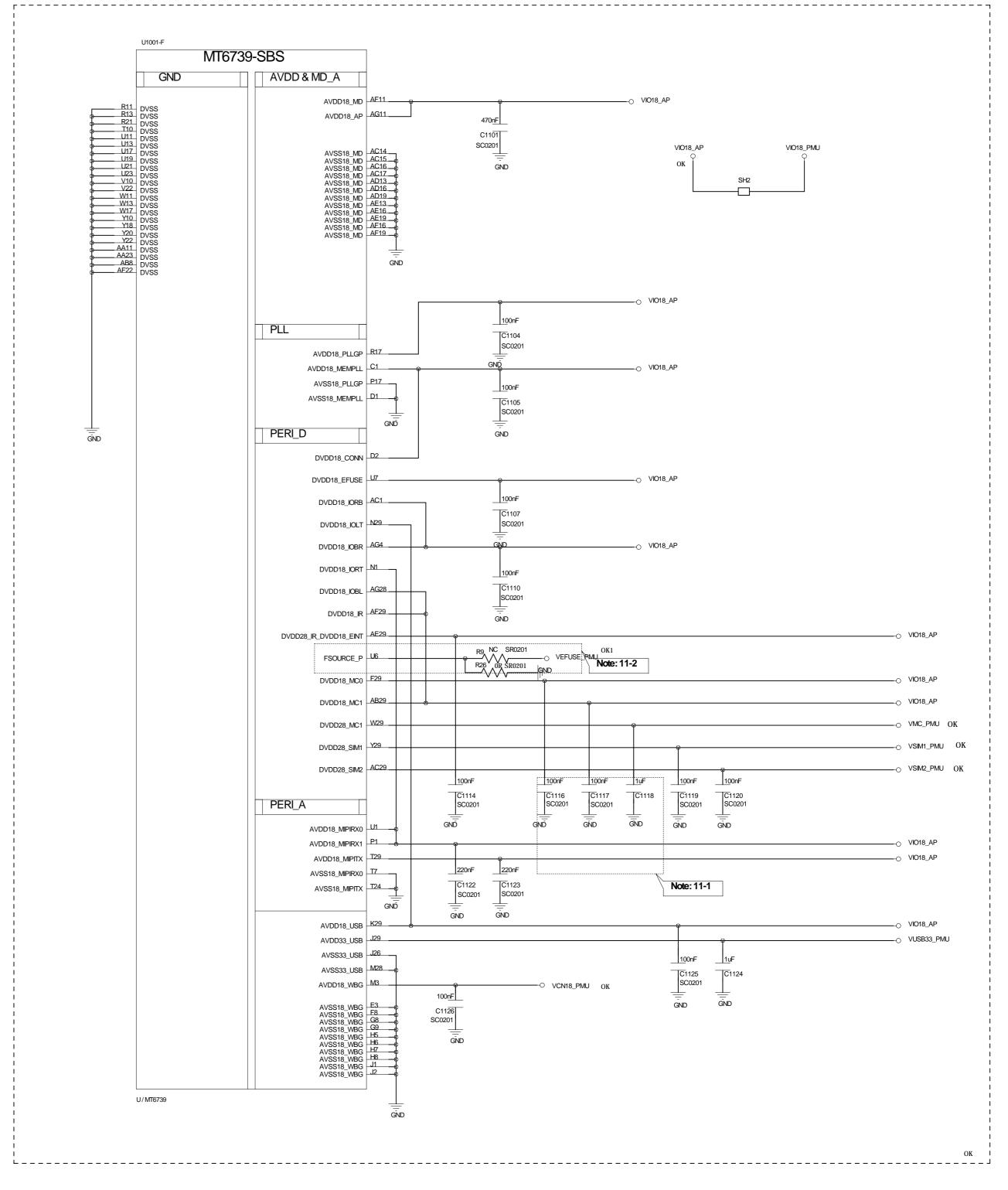


i_{|------}





Schematic design notice of "10_BB_POWER_PDN" page.

Note 10-1: Differential pair of DVDD_DVFS remote sense
Remote sense trace with GND shielding to PMIC (Differential)
must be close to BB's ball

Note 10-2: Differential pair of DVDD_TOP remote sense must be Remote sense trace with GND shielding to PMIC (Differential)

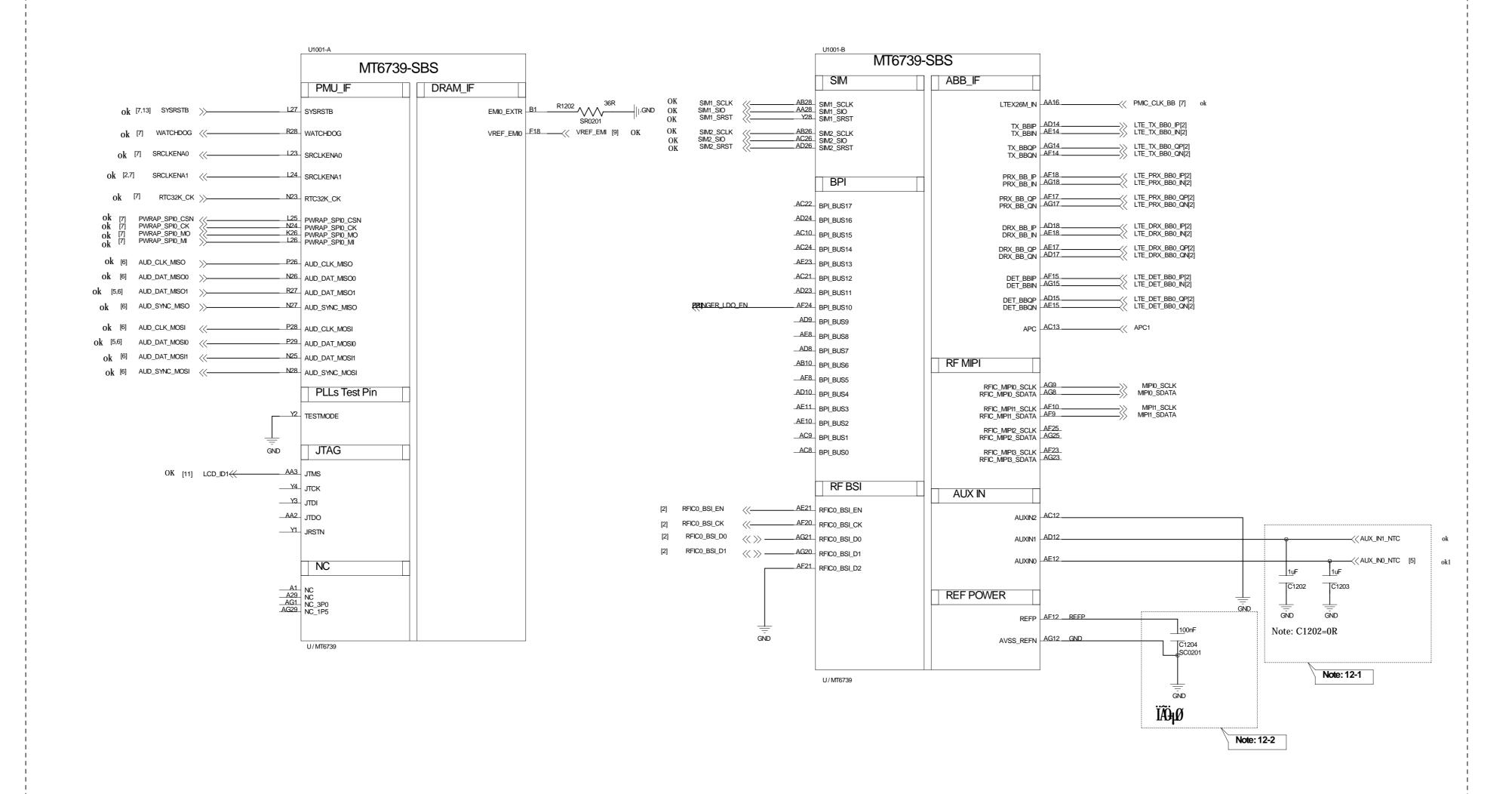
Note 10-3: Differential pair of DVDD_MODEML1_BUCK remote sense must be Remote sense trace with GND shielding to PMIC (Differential) close to BB's ball.

Schematic design notice of "11_BB_ POWER_PDN"

Note 11-1: C1116 close to DVDD18_MC0, Distance less than 150mil C1117 close to DVDD18_MC1, Distance less than 150mil C1118 close to DVDD28_MC1, Distance less than 150mil

Note 11-2:

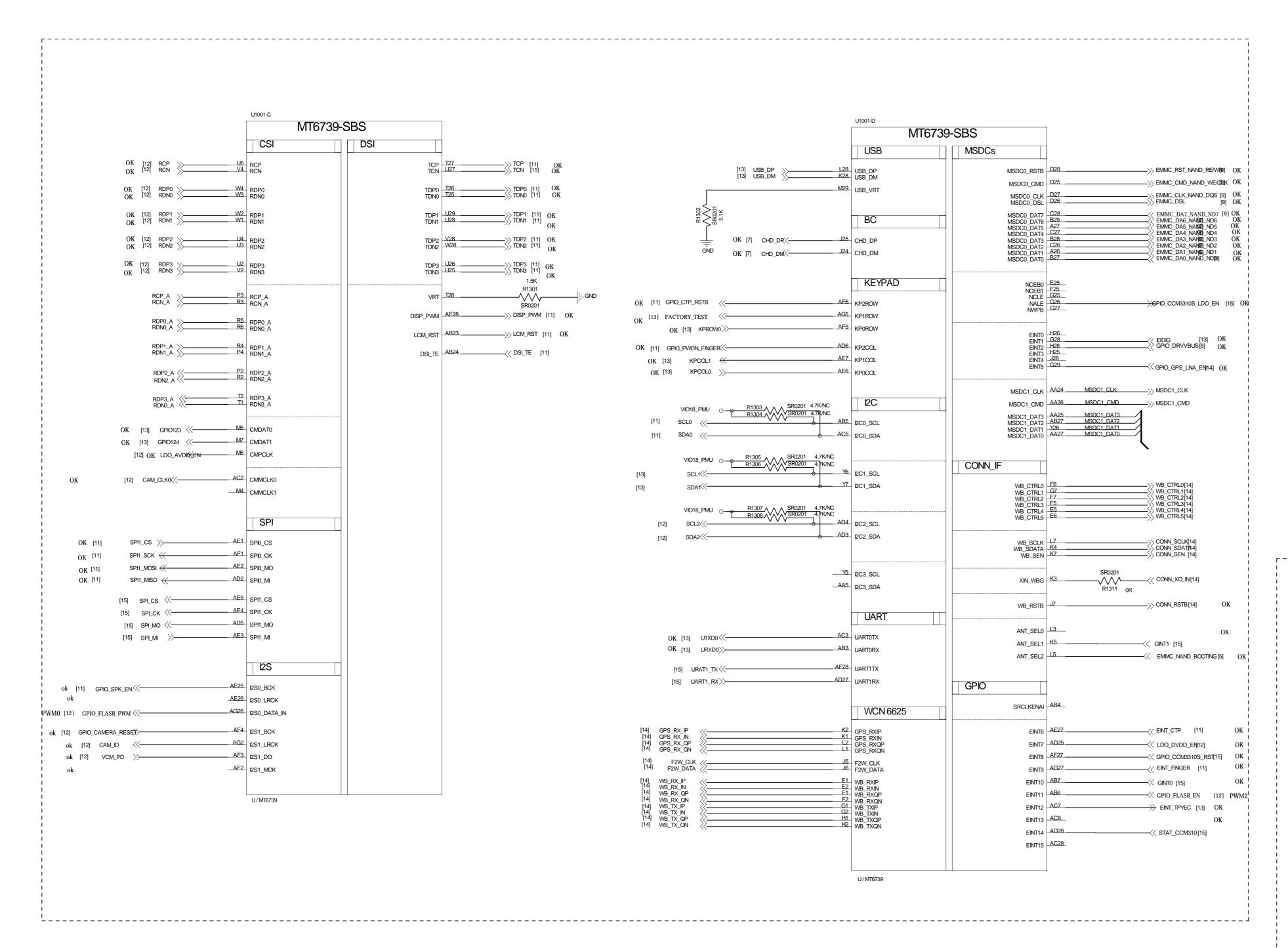
FSOURCE_P(EFUSE)
(1)FSOURCE_P EFUSE power(VEFUSE) should be
only for EFUSE usage(not share with other application)
(2)W/I EFUSE program, VEFUSE need luf bypass cap
(pls refer to ; §LDO output voltage/current table; ")
(3)W/O EFUSE program, VEFUSE bypass cap should be NC.



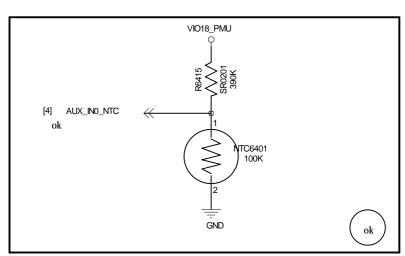
Schematic design notice of "12_BB_1" page.

Note 12-1: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

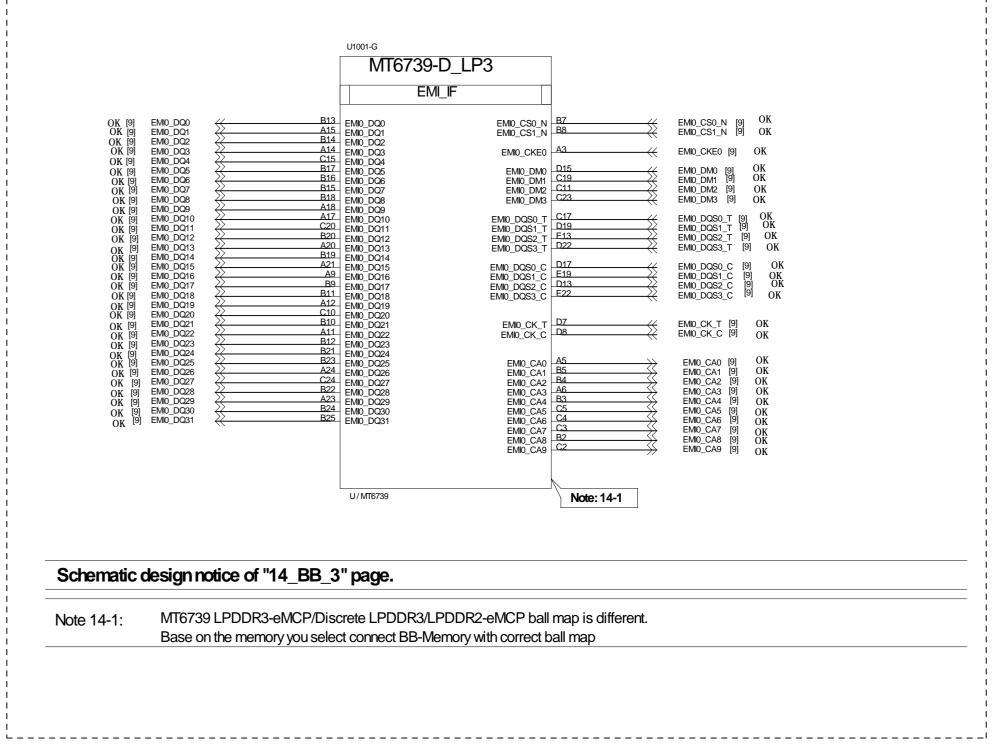
ote 12-2: The de-coupling cap. for REFP (AF12 ball) have to be placed as close to BB as possible.

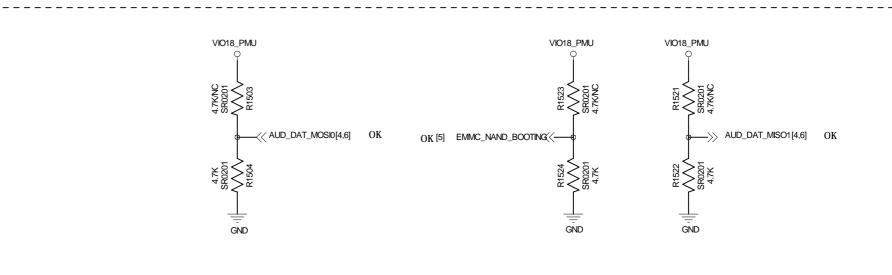


Thermistor / To sense board level temperature



Distance to AP is 5~7mm and away form other heat resource 10mm~12mm





Schematic design notice of "15_BB_HW_Trap" page.

Note 15-1: AUD_DAT_MOSI0 is JTAG feature in bootstrap.

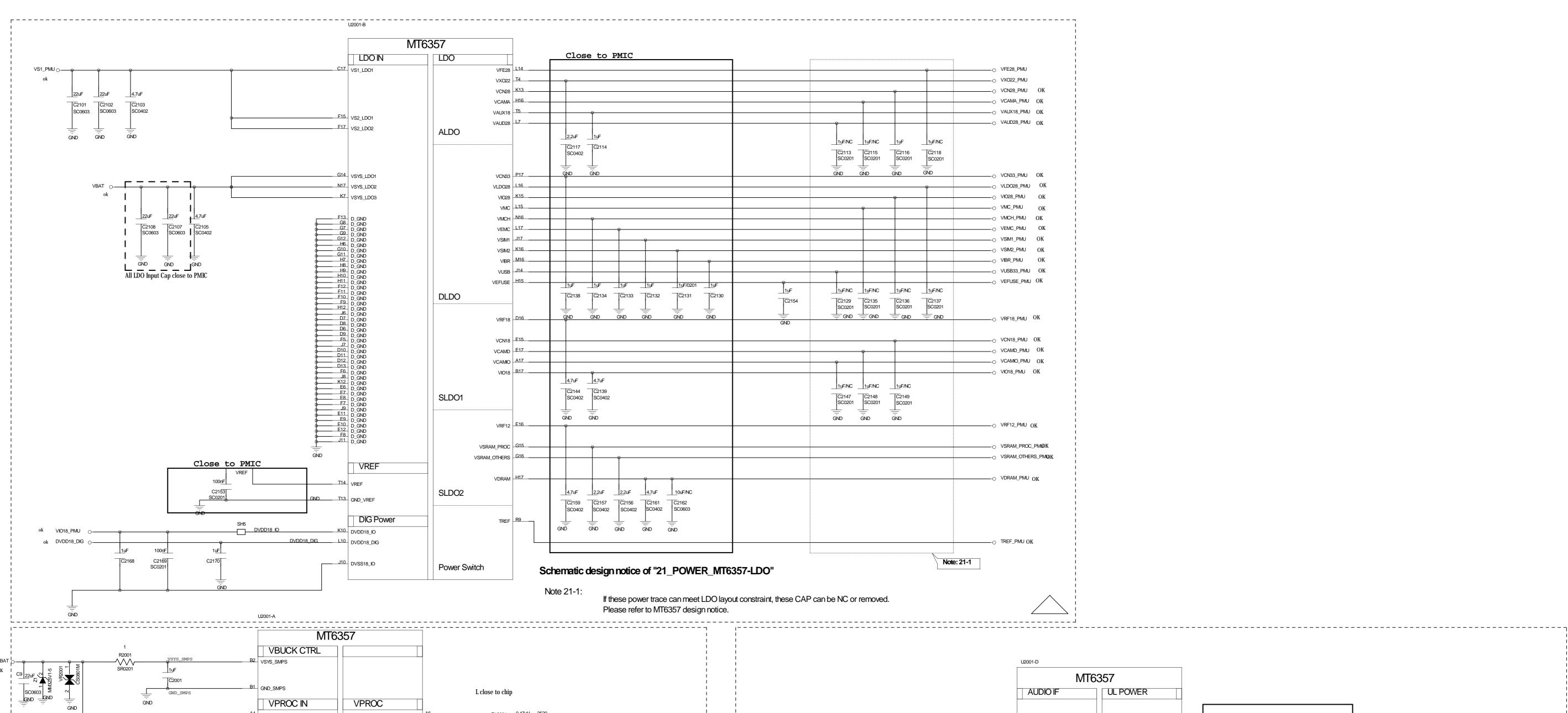
[AUD_DAT_MOSIO default status is LO]

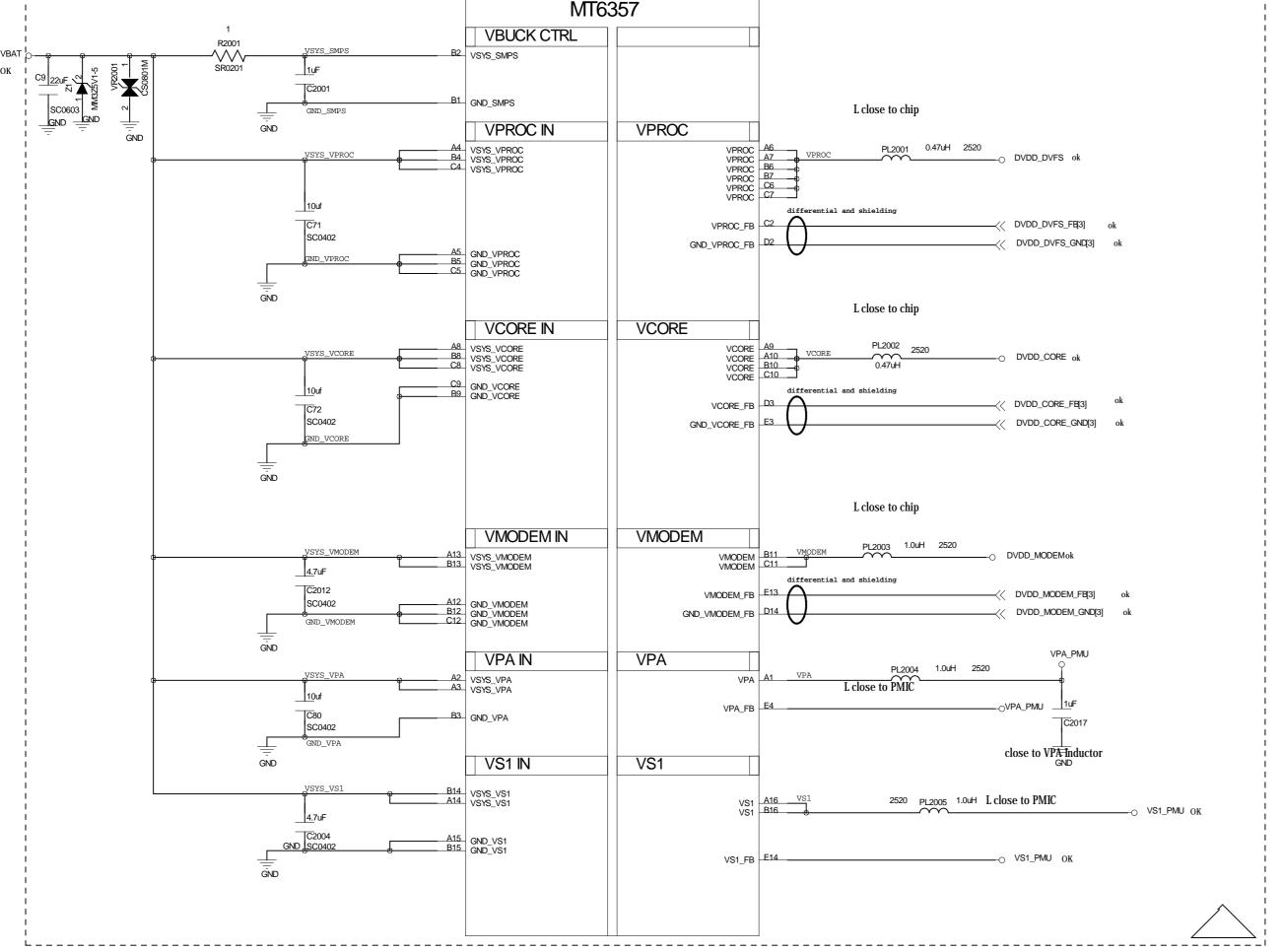
AUD_DAT_MOSI0	Mode	Note
LO	Default	N/A
Н	Aux Func. trap_MD_JTAG_AP_JTAG	MD JTAG = CMDAT0/CMDAT1/CMPCLK/CMMCLK/CMMCLK1

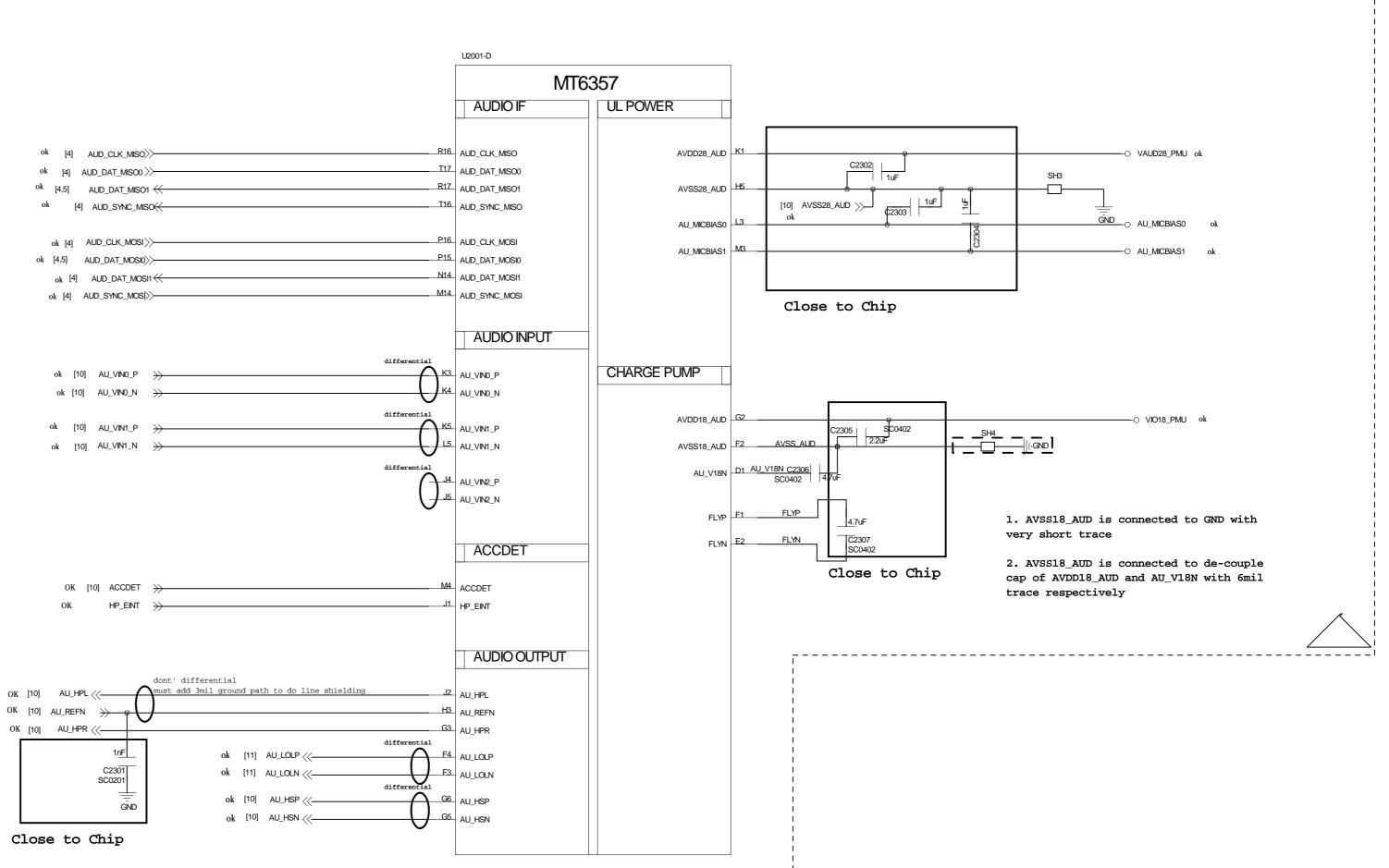
Note 15-2: ANT_SEL2 and AUD_DAT_MISO1 is storage booting feature in bootstrap. [ANT_SEL2 default status is LO] [AUD_DAT_MISO1 default status is LO]

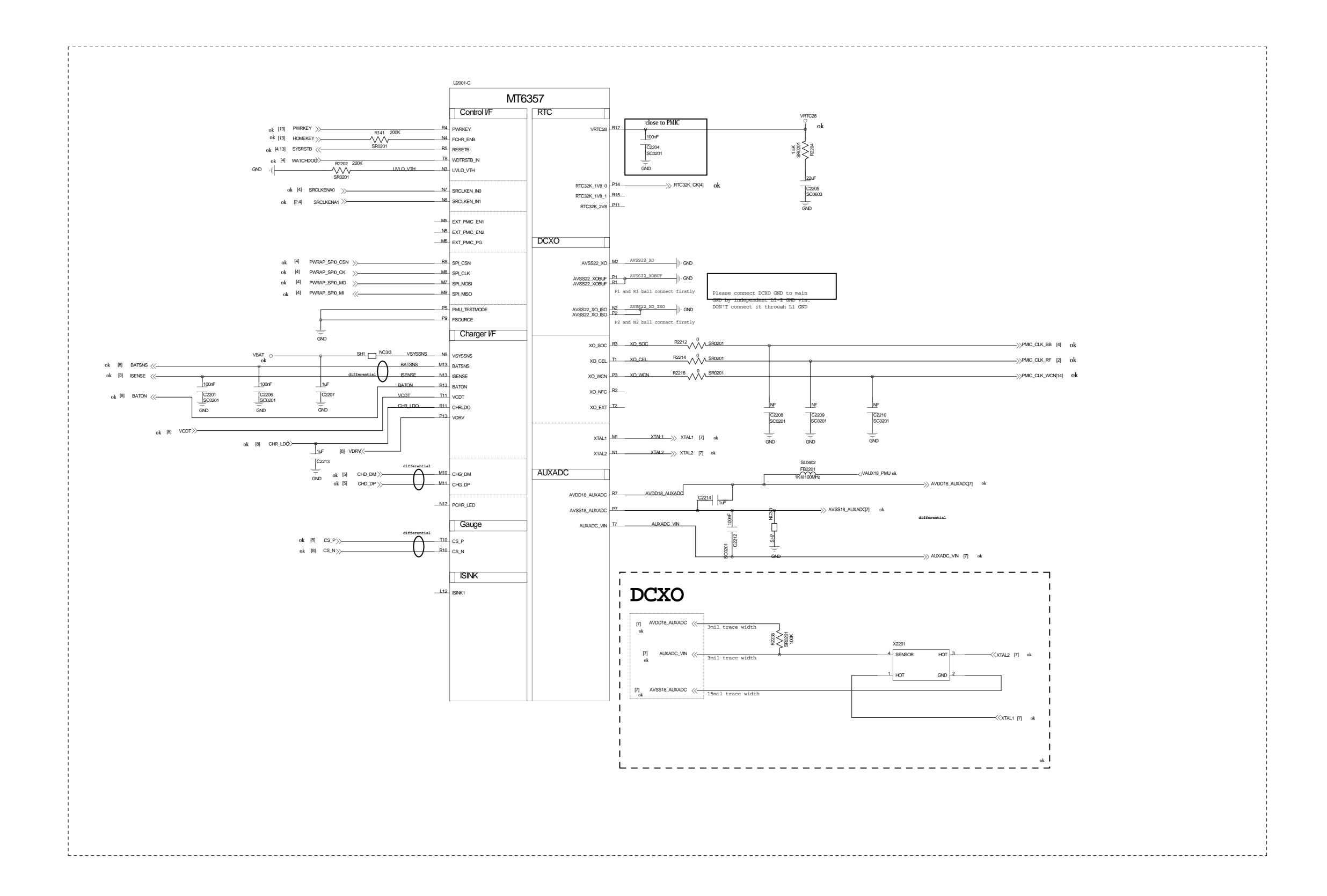
(EMMC_NAND_BOOTING)

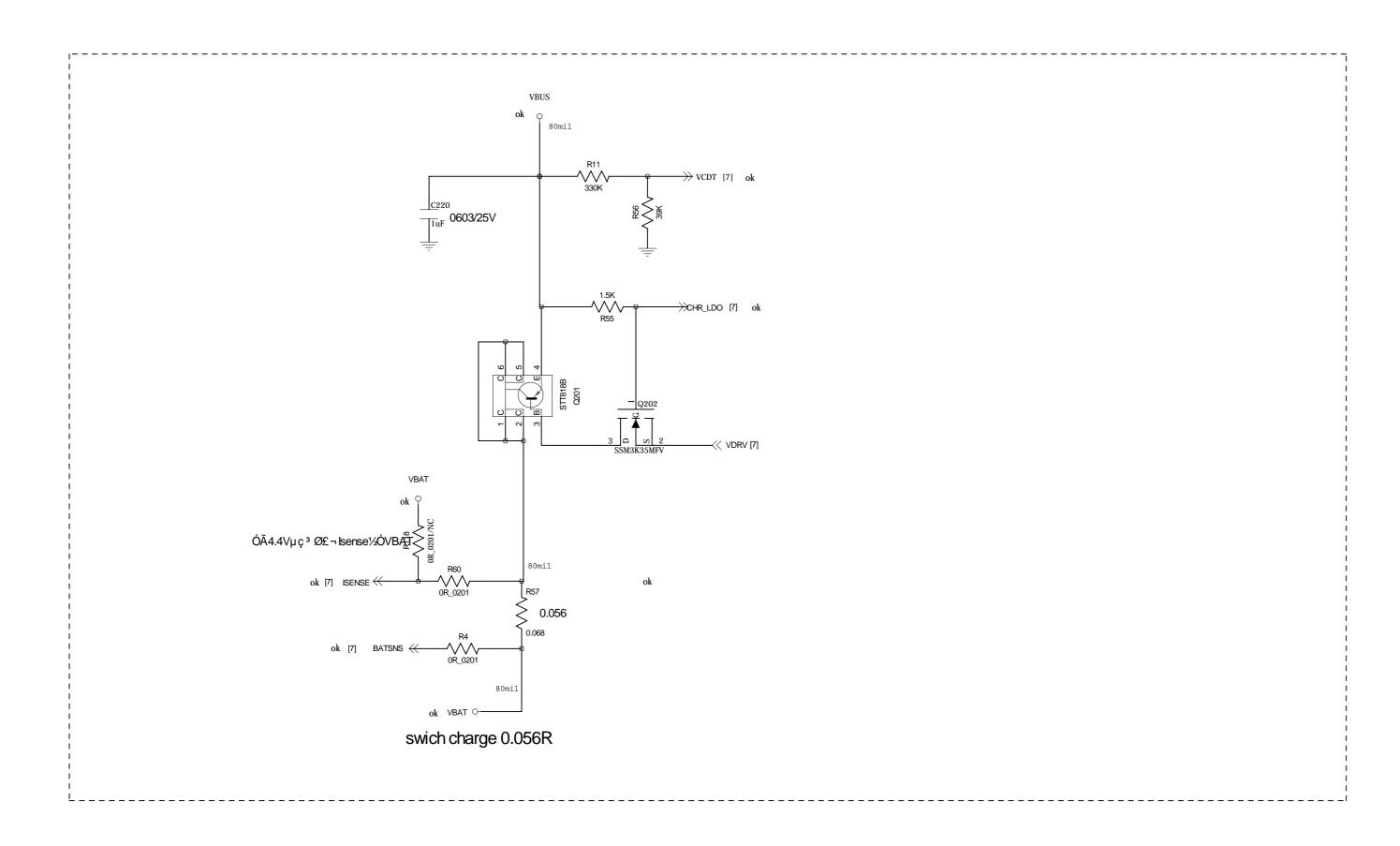
ANT_SEL2	AUD_DAT_MISO1	Storage Booting
Н	LO	TLC Boot
Н	Н	SLC Boot
LO	LO	eMMC Boot
LO	H	N/A



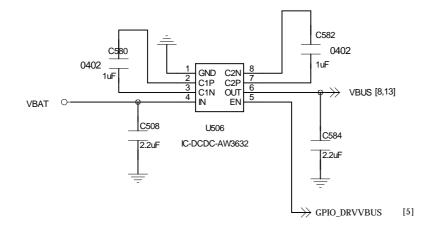


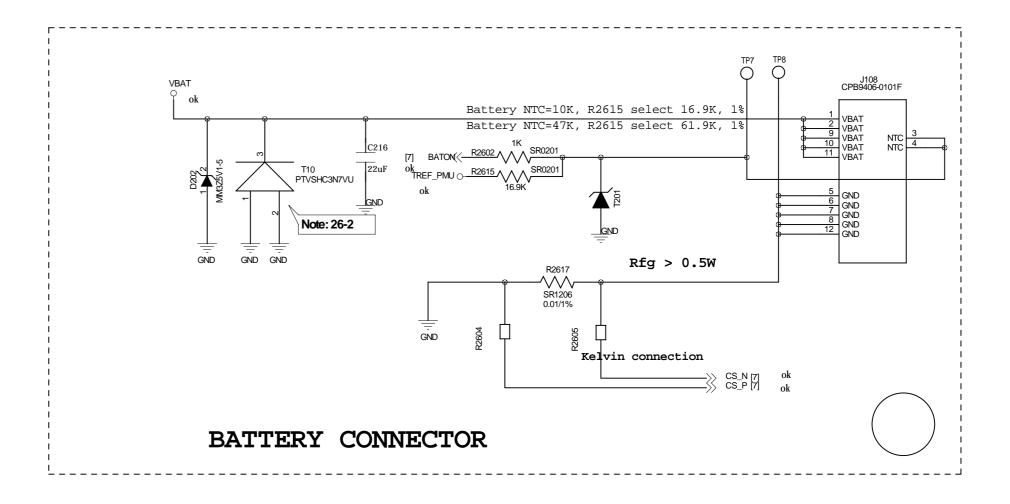


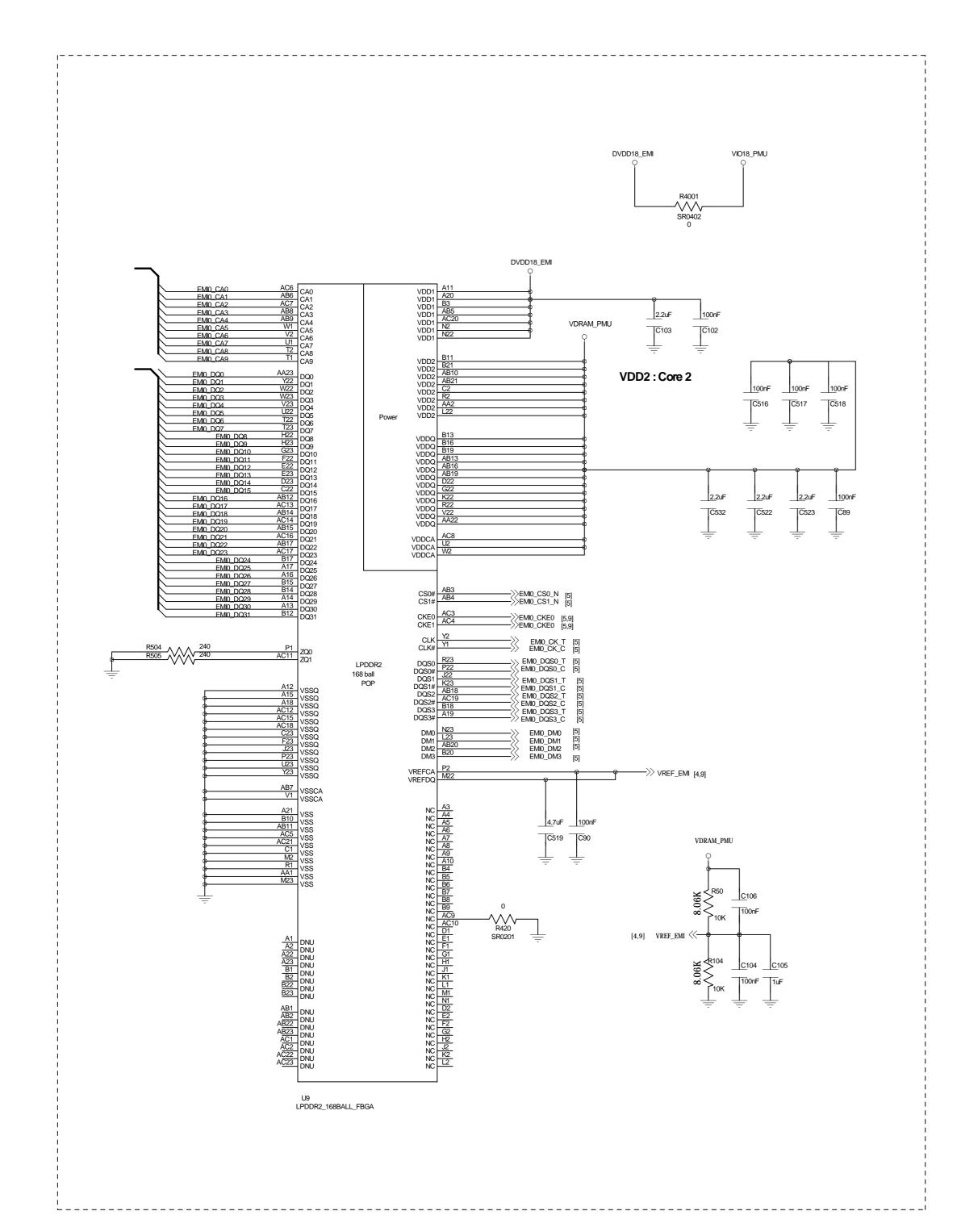


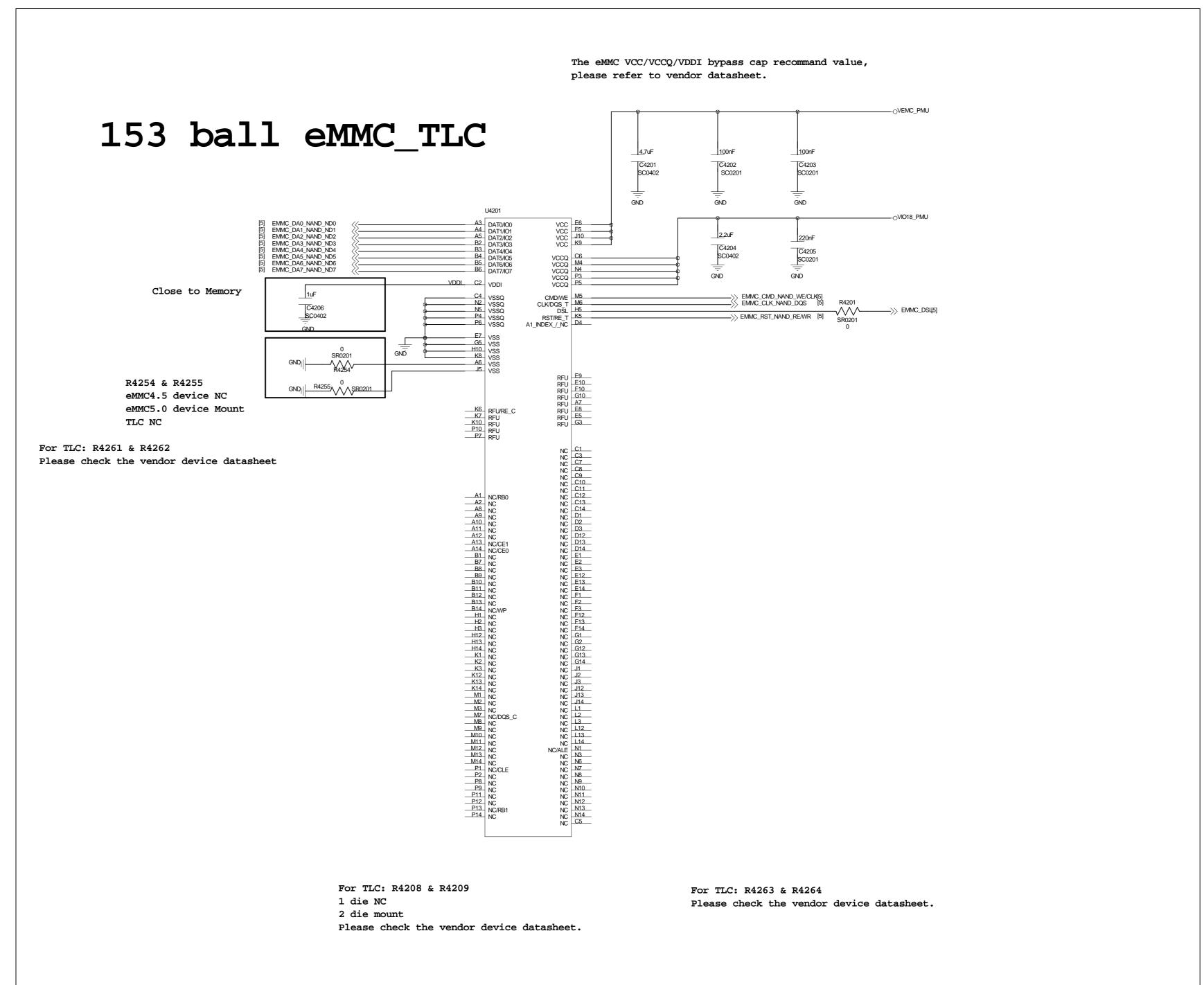


OTG IC



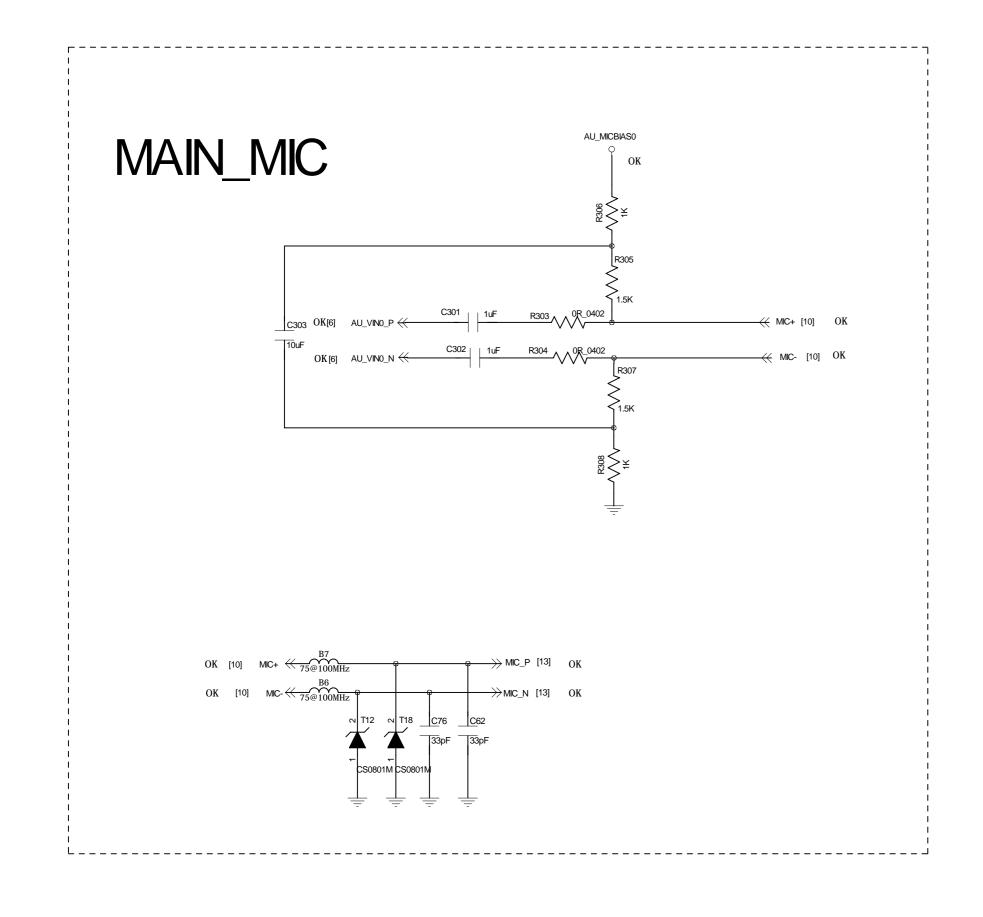


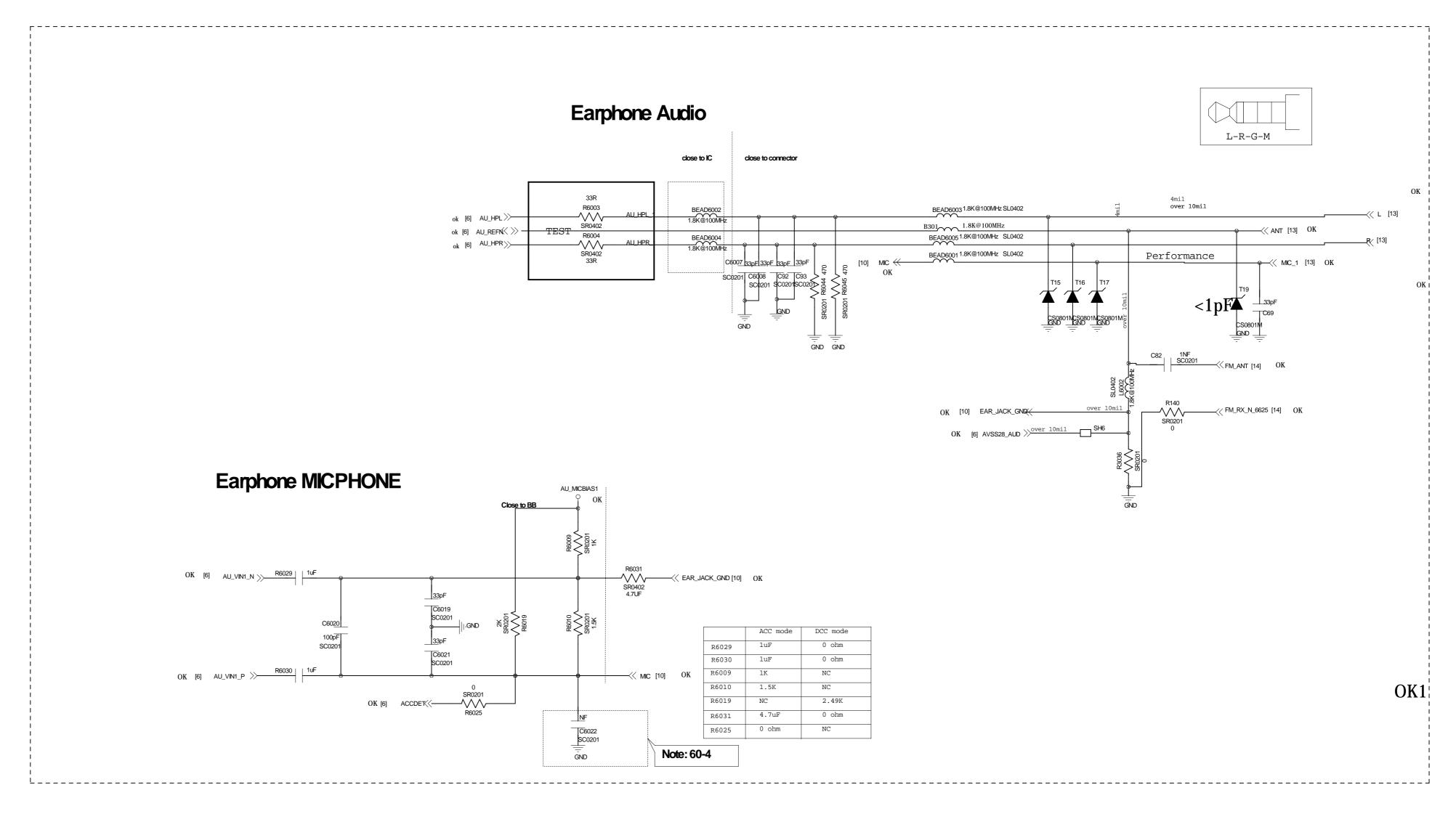


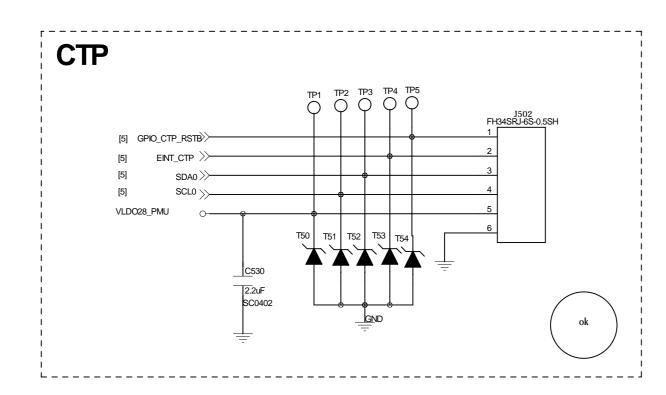


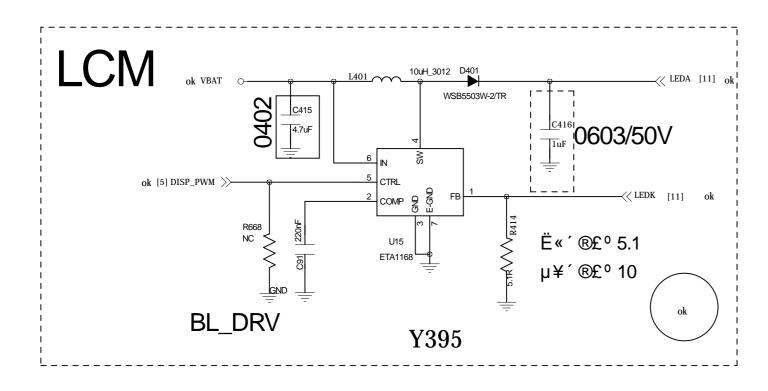
OK

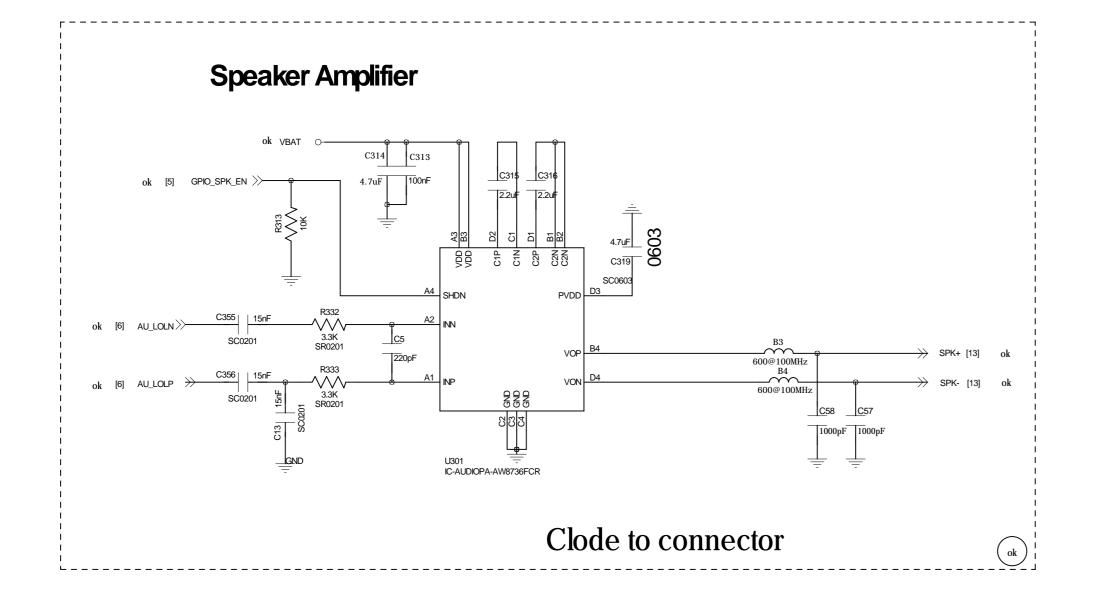


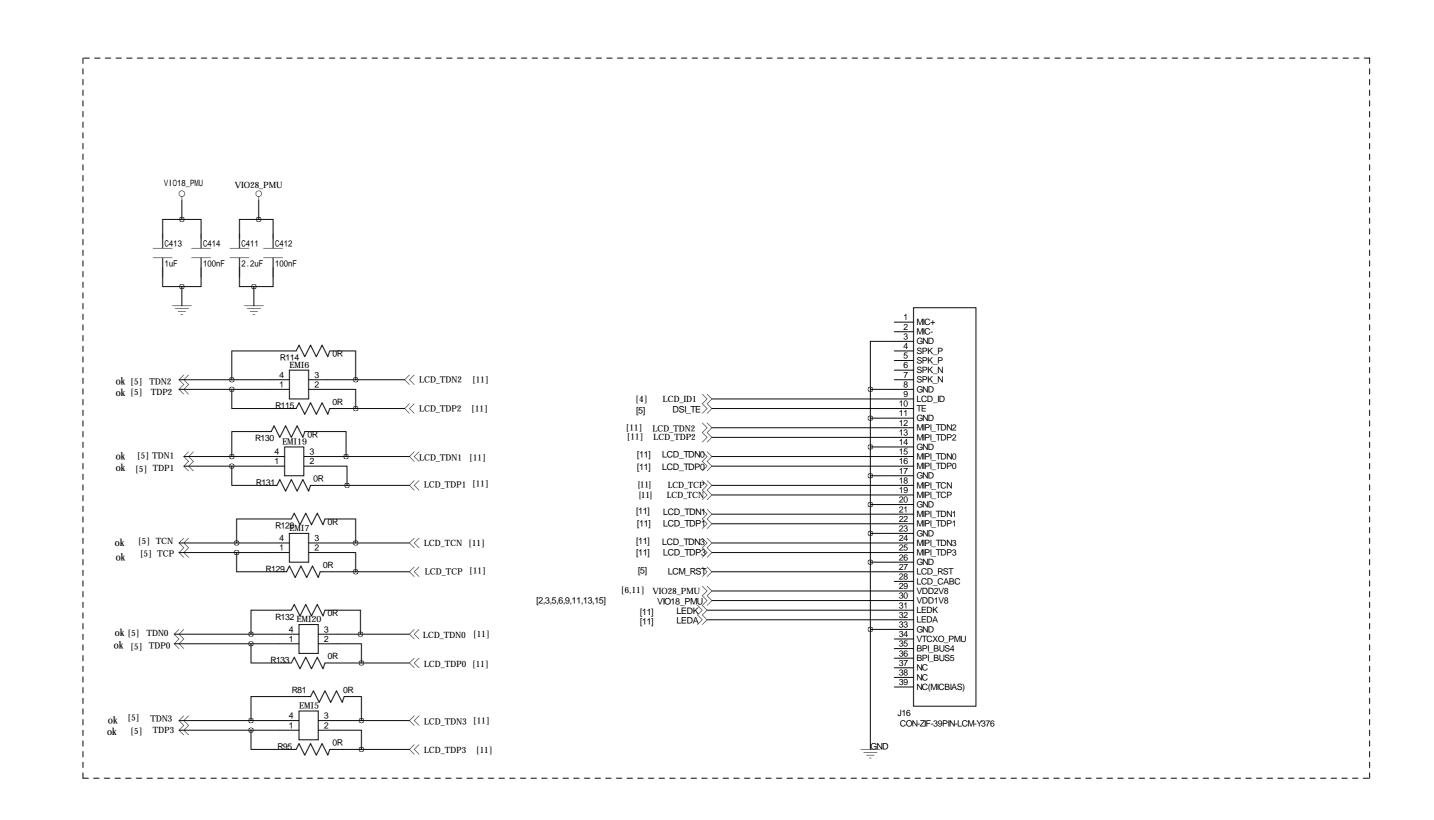


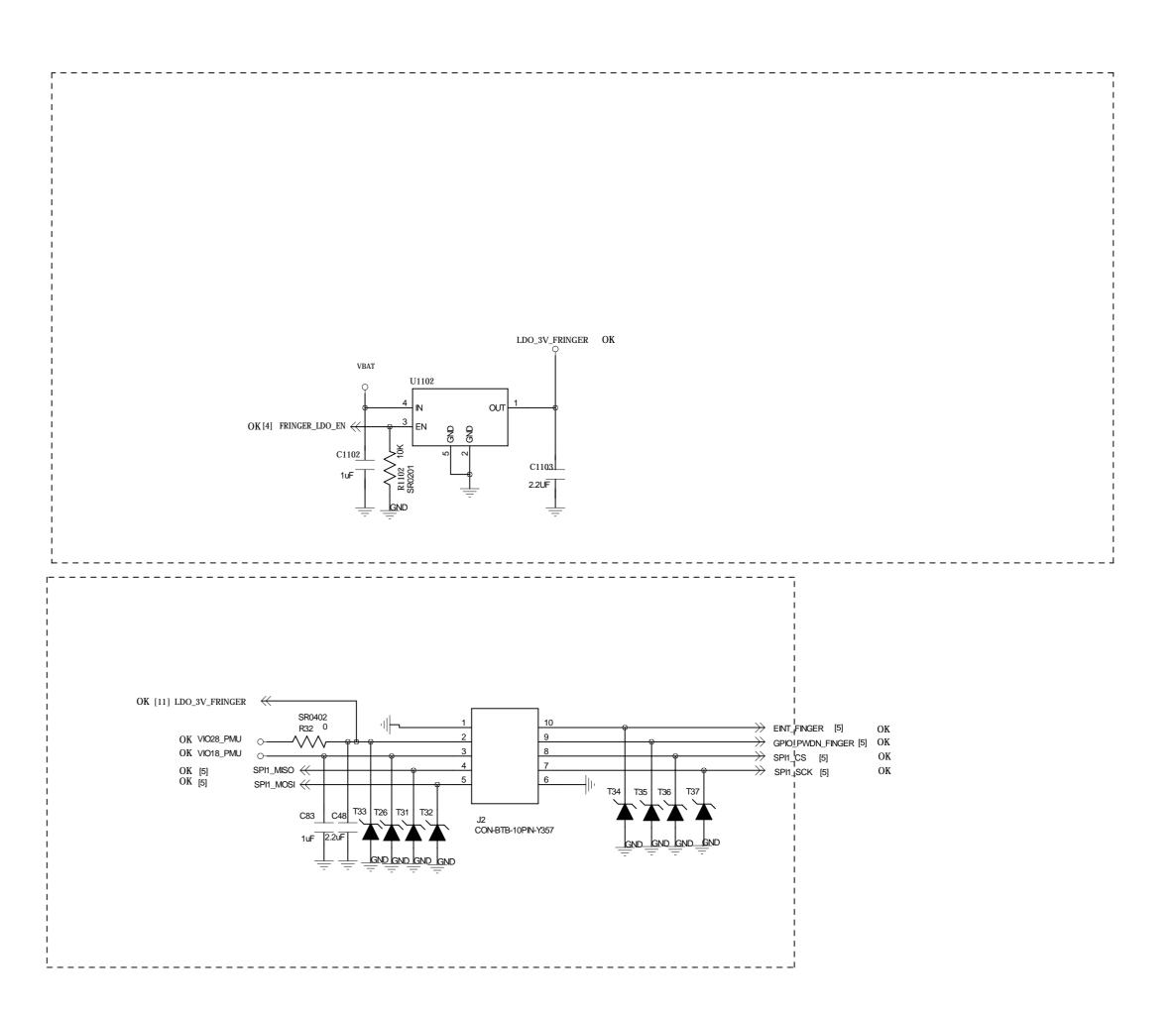




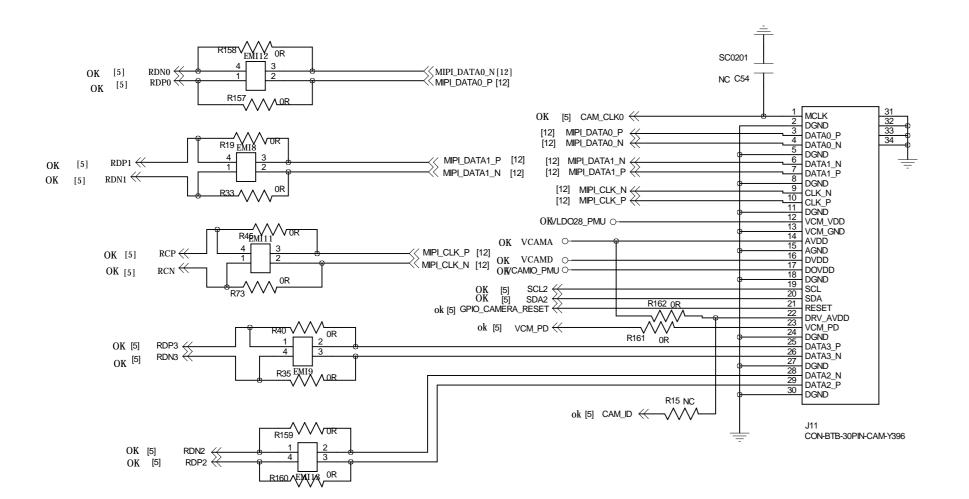


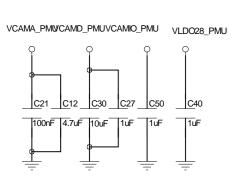




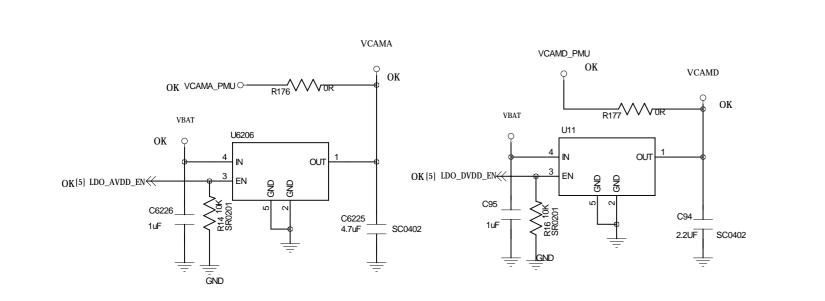


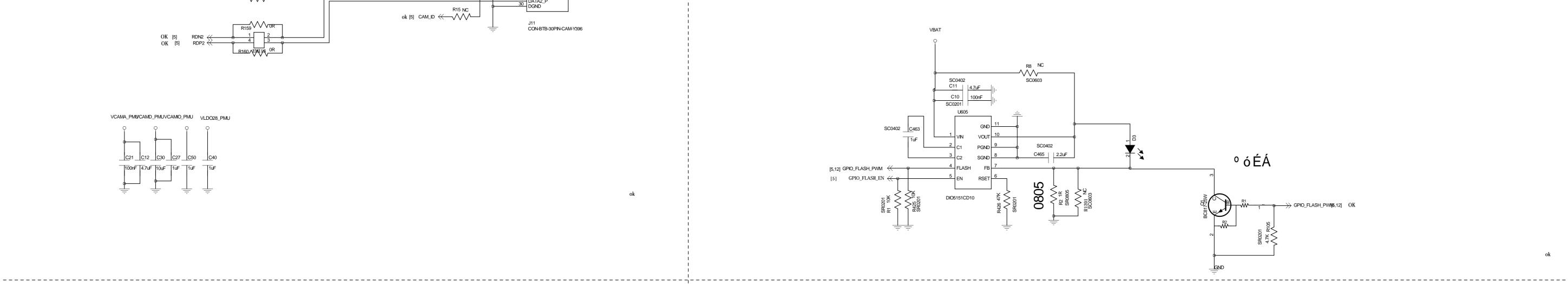
MAIN_REAR





SUB_REAR





SUB_FRONT

