ENGR-241 Passive Filters Lab

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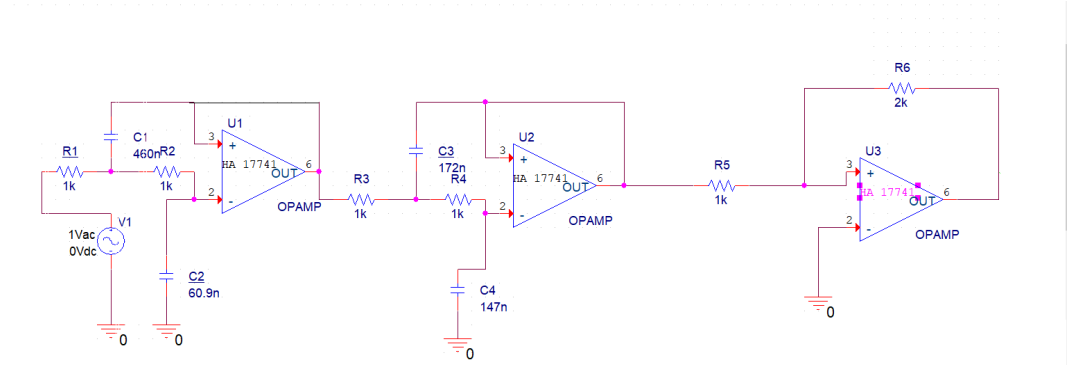
Overview

For this lab we designed and constructed an active Butterworth Low Pass Filter with a cutoff frequency of 1KHz and a passband gain of 6 dB. The circuit was designed to have a minimum of 70dB of attenuation at 10KHz. We disgned and tested the circuit using Orcad prior to building the circuit. We then built and observed the output on the oscilloscope to ensure we met the design requirements.

Circuit Diagrams



Calculations

The calculations for this lab required us to determine the number of stages needed to meet the attenuation specifications of 70dB at 10KHz. We then calculated the values for the capacitors using scaling and choosing a resistor value of 1k Ω.

1. Approximate the number of stages needed to attain 70dB of attenuation.

Given:
$f_s = 10KHz$
$f_p = 1KHz$

$n = \frac{-0.05A_s}{log(f_s/f_p)}$
$n = \frac{-0.05 \cdot -70}{log(10KHz/1KHz)} = 3.5$

=>four stages should provide the required attenuation

2. Using the roots from the Butterworth n^{th} order polynomial table, calculate the roots of the polynomials for a fourth order filter.

Given: $(s^2+0.765s+1)(s^2+1.848s+1)$
$C_1 = 2.61F$
$C_2 = 0.38F$
$C_3 = 1.08F$
$C_4 = 0.924F$

3. Using the values found above, scale the capacitors for the selected resistor value.

$R' = k_m R = 1k\Omega$
$k_f = \frac{\omega_c'}{\omega_c} = 2000\pi$

$C' = \frac{C}{k_m k_f}$
$C_1' = \frac{C_1}{k_m k_f} = \frac{2.614F}{2000\pi \cdot 1000} = 416.0nF$
$C_2' = \frac{C_2}{k_m k_f} = \frac{0.3825F}{2000\pi \cdot 1000} = 60.9nF$
$C_3' = \frac{C_3}{k_m k_f} = \frac{1.08F}{2000\pi \cdot 1000} = 171.9nF$
$C_4' = \frac{C_4}{k_m k_f} = \frac{0.924F}{2000\pi \cdot 1000} = 147.1nF$

Data Table

Frequency(Hz)	V_{out}(ideal)	V_{out}(observed)	% Diff
100	$10V$	$10.05V$	0.5%
250	$10.1V$	$10.0V$	-0.99%
500	$10.3V$	$9.6V$	-6.80%
600	$10.3V$	$9.25V$	-10.19%
700	$10.2V$	$8.75V$	-14.22%
800	$9.6V$	$8V$	-16.67%
900	$8.5V$	$7V$	-17.65%
1k	$7V$	$5.7V$	-11.63%
1.1k	$5.4V$	$4.6V$	-8.0%
1.2k	$4V$	$3.65V$	-8.75%
1.3k	$3V$	$2.8V$	-6.67%
1.5k	$1.8V$	$1.9V$	5.56%
2k	$530mV$	$700mV$	32.07%
3k	$111mV$	$200mV$	80.2%
4k	$33mV$	$75mV$	127%
5.5k	$10mV$	$32.5mV$	225%

Procedure

The circuit was more involved than others we built in the class. We were able to successfully design the circuit in the first week of the lab, which involved running simulations with our calculated values to ensure we would meet the design criteria. We then built the circuit using