Experiment – 5

Aim of the experiment

To design and implement combinational logic circuit to test half adder, full adder, half subtractor and full subtractor.

Objective –

To verify and implement the combinational logic circuit of half adder, full adder, half subtractor and full subtractor.

Apparatus required –

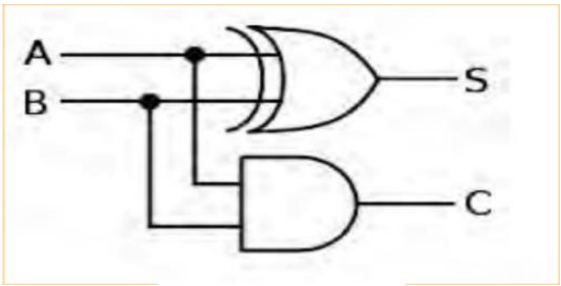
Serial No	Items	Specifications
1..	Project Board	
2.	IC's 7404 7408 7432 7486	 Hex Inverter Quad 2 I/p AND gate Quad 2 I/P OR gate Quad 2 I/P Ex-or gate

Theory –

1.Half adder - It can add 2 bits.

Expression for sum :– S = A'B+AB'=A⊕B

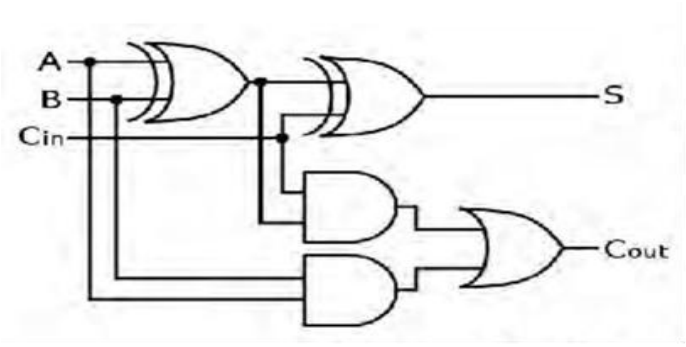
Expression for carry :- C = AB



Truth Table for Half Adder:

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2.Full adder- It can add 3 bits.



Expression for sum –

S=A′B′C+A′BC′+AB′C′+ABC

= C(A′B′+AB)+ C′(A′B+AB′)

=C(A⊕B)′+C′(A⊕B)

= A⊕B⊕C

Expression for carry -

C=A′BC+AB′C+ABC′+ABC

=A(CB′+BC) +BC=A(B⊕C) + BC

Truth Table for Full Adder:

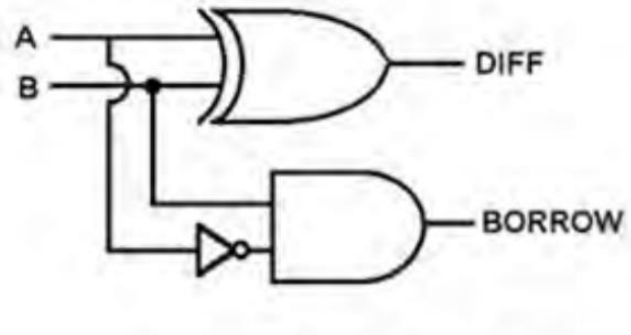
3.Half subtractor – It can subtract 2 bits.

Truth Table For Half Subtractor:

A	B	Difference	Borrow
0	0	0	0
0	1	1	1
0	0	1	0
0	1	0	0

Expression for difference, Diff = A′ B + A B′= A⊕B

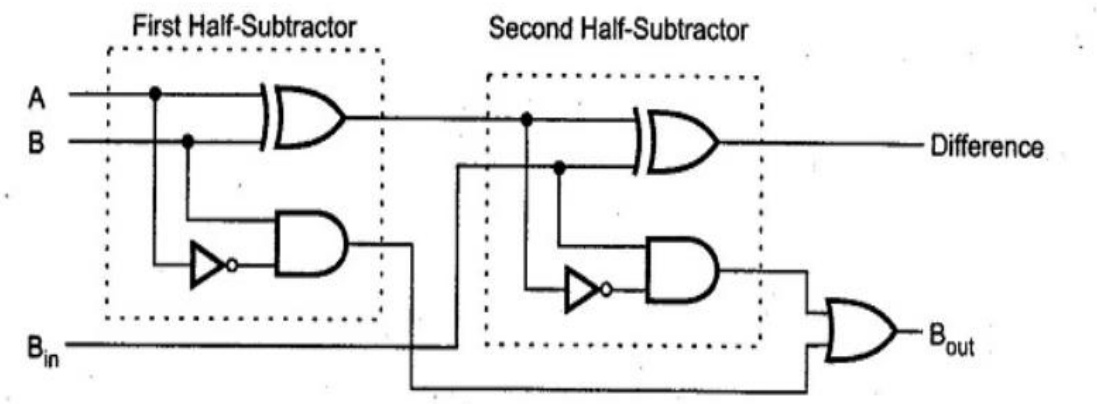
Expression for borrow, Borrow = A′ B



4.Full subtractor –: It can subtract 3 bits.

Truth Table for Full Subtractor:

A	B	C	Difference	Carry
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Expression for difference, Diff = A′ B′C+ABC′+AB′C′+ABC

=C (A′B ′+AB) + C′(A′B+AB′)= C(A⊕B)′+C′(A⊕B)

=A⊕B⊕C

Expression for borrow, Borrow = A ′B′ C + A′ B C′ + A′ B C + ABC

=C(A⊕B)′+A′B

Observation-

(Draw the observation tables in High and Low format)

1.Adder:

i)Half adder:

ii)Full adder:

2.Substractor:

i)Half Subtractor:

ii)Full Subtractor:

Conclusion-