CLAMPER

A clamper is an electronic circuit that changes the DC level of a signal to the desired level without changing the shape of the input signal.

Types of clamper ⇒

It's of 3 types :- a) Positive
b) Negative
c) Biased

* The clamper is otherwise known as level shifter or DC restorer.

* Steps to solve clamper circuit ⇒

↳ Start the analysis by considering the input half-cycle which makes the diode forward biased.

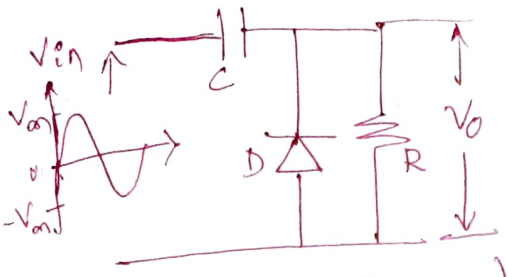
↳ During that half, capacitor will store its maximum charge. Then calculate capacitor voltage (V_c) and output voltage (V_o).

↳ During another half, diode is reverse biased (open). Hence, capacitor will try to discharge the previously stored charge to the other component.

↳ The ~~input~~ output voltage should be equal to input voltage.

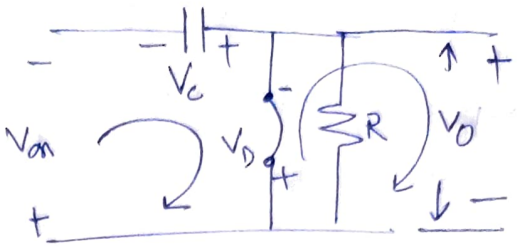
a) Positive clamper ⇒ it shifts the input signal towards the positive side or upward.

↳ circuit consists of a diode, a resistor and a capacitor.



(Positive clamper)

During -ve half cycle, diode is forward biased. So, the capacitor will store its max.



(a)

By applying the loop eqn in i/p side,

$$-V_m + V_C + V_D = 0$$

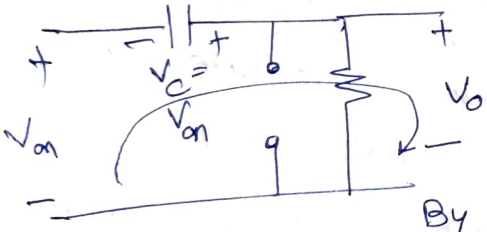
$$\Rightarrow V_C = V_m \quad (\text{if } V_D = 0)$$

(Ideal diode is used)

By applying loop eqn in o/p side,

$$-V_D - V_o = 0 \Rightarrow \boxed{V_o = V_D = 0} \Rightarrow \text{for -ve half.}$$

During +ve half-cycle, Diode is reverse biased. Hence signal appears at the output as shown in fig (b).



(b)

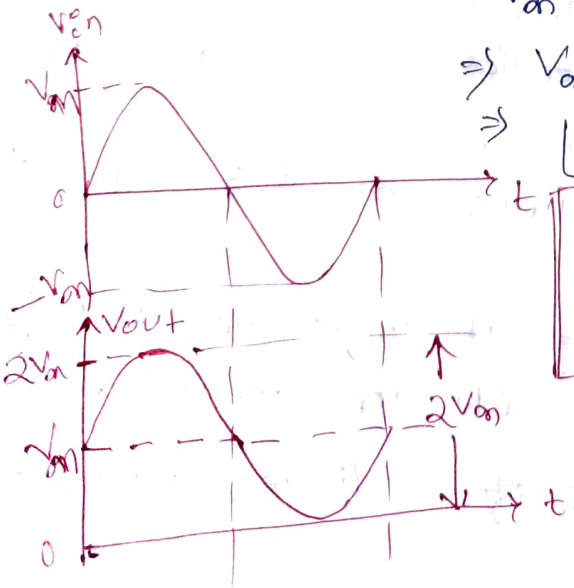
Input current directly flows towards the output.

By applying loop eqn,

$$V_m + V_C - V_o = 0$$

$$\Rightarrow V_m + V_m = V_o$$

$$\Rightarrow \boxed{V_o = 2V_m} \rightarrow \text{for +ve half}$$



for sine & △ wave,

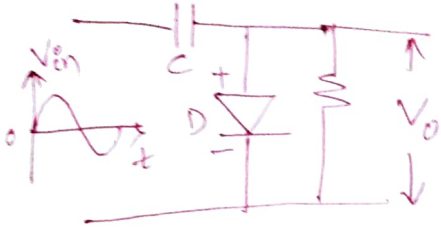
Baseline = $\frac{\text{+ve half } V_o + \text{negative half } V_o}{2}$

for this

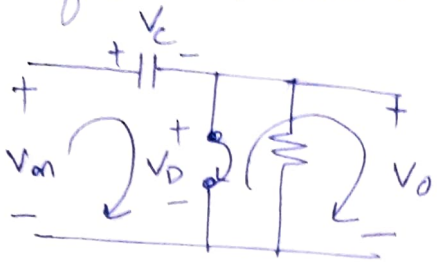
$$= \frac{2V_m}{2} = V_m$$

b) Negative clamper →

It shifts the waveform to negative side.



During +ve half cycle, diode is forward biased.

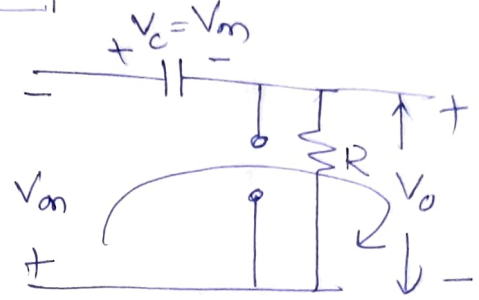


$$V_{in} - V_c - V_D = 0$$

$$\Rightarrow \boxed{V_{in} = V_c}$$

$$V_D - V_o = 0 \Rightarrow \boxed{V_o = V_D = 0}$$

During -ve half cycle, Diode is reverse biased and hence the signal appears at the output.

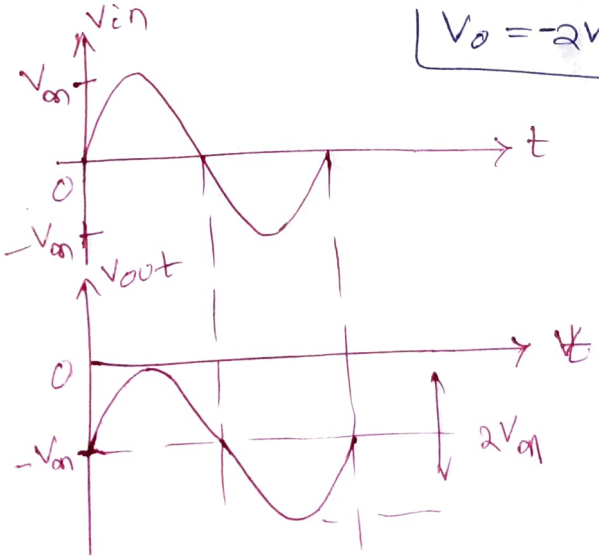


→ Diode does not allow current through it. The charge stored in capacitor is discharged.

$$-V_{in} - V_c - V_o = 0 \Rightarrow V_o = -V_{in} + V_c$$

$$= -V_{in} + V_{in}$$

$$\boxed{V_o = -2V_{in}}$$



Baseline = $\frac{0 + (-2V_m)}{2} = -V_m$

Applications :-

- Used as dc restorer
- as voltage multipliers
- for protection of amplifier
- Used as base-line Stabilizer