Experiment – 8

Aim of the experiment –

To study the operation of SR and D flip flops.

Apparatus required -

- Flip flop kit
- Connecting wires

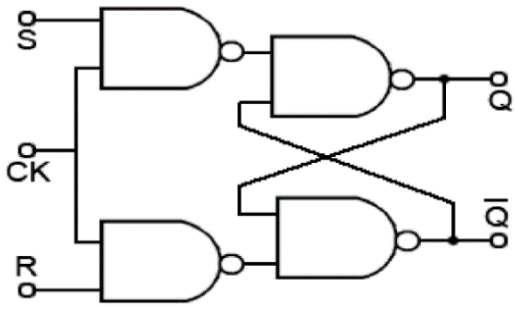
Theory -

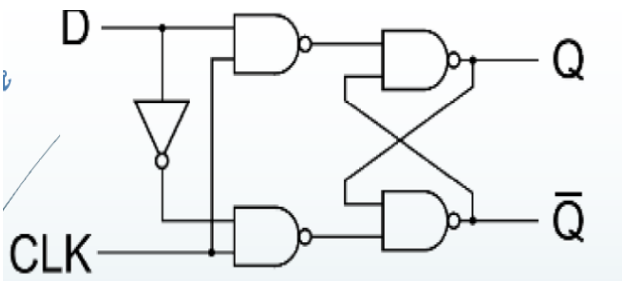
SR flip flop –

A SR flip flop is an arrangement of logic gates that maintain a stable output even after the inputs are turned off. This simple flip flop circuit has a set input(S) and a reset input (K). The set input causes the output 0(top output) and 1(bottom output). The reset causes the vice - versa (top – 1bottom – 0).

S R Truth table -

clk	S	R	Qn+1	$\bar{Q}$n+1	Operatios
0	x	x	Qn	$\bar{Q}$n	No change
1	0	0	Qn	$\bar{Q}$n	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	1	1	Invalid





D flip flop –

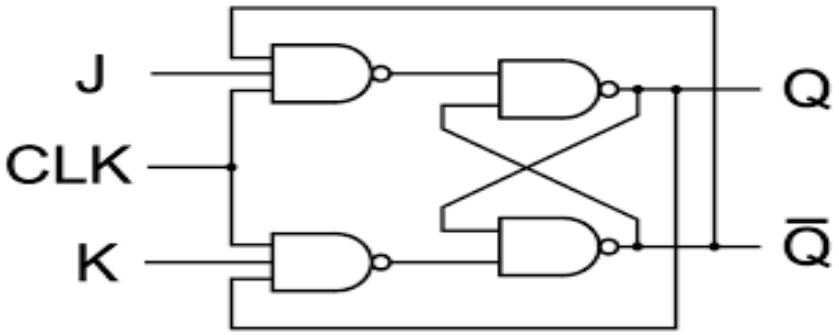
It is also known as a "data" or "delay" flip - flop.The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (low to high or high to low). The output shows the current stored values.

D Truth table –

clk	D	Qn+1	$\bar{Q}n+1'$	condition
0	X	Qn	Qn′	No change
1	0	0	1	Reset
1	1	1	0	Set

J K flip flop –

The JK flip-flop augments the behavior of the SR flip-flop (J=Set, K=Reset) by interpreting the J = K = 1 condition as a "flip" or toggle command. The combination J = 1, K = 0 is a command to set the flip-flop; the combination J = 0, K = 1 is a command to reset the flip-flop; and the combination J = K = 1 is a command to toggle the flip-flop.



J K Truth table –

J	K	Qn+1	$\bar{Q}$n+1′	CONDITION
x	x	Qn	Qn′	No change
0	0	Qn	Qn′	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	Qn′	Qn	Toggle

OBSERVATION:

Draw the observation table as per truth table in high and low format.

CONCLUSION: