EXPERIMENT NO-5

01.AIM OF THE EXPERIMENT: -

To study and verify different logic gates.

02.OBJECTIVE: -

To familiarize with circuit implementations using ICs and test the behavior of different logic gates.

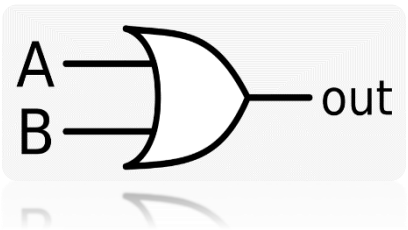
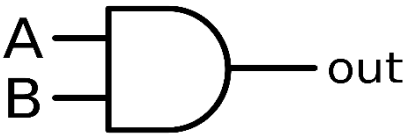
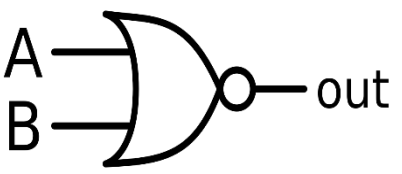
03.COMPONENTS REQUIRED: -

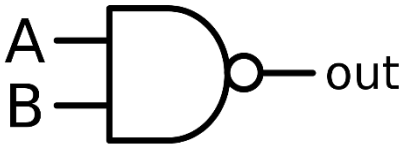
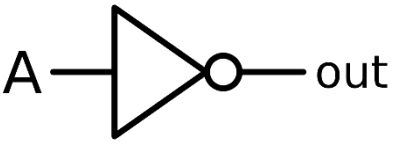
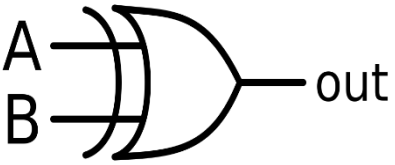
- Digital bread board / Project board
- Connecting patch chords
- IC 7400, IC 7408, IC 7432, IC 7402, IC 7404, IC 7486

04.THEORY: -

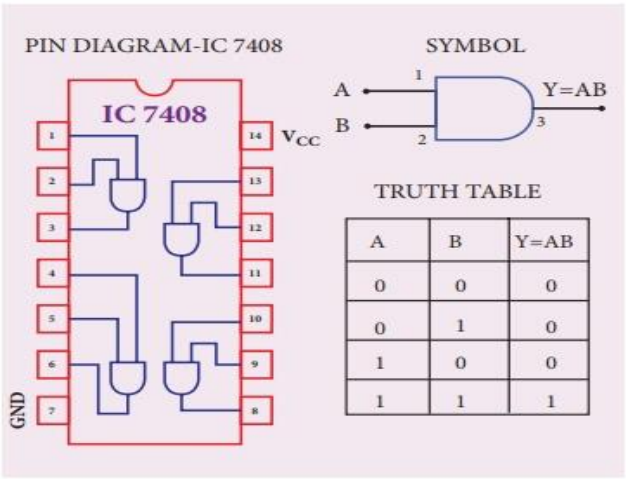
The basic logic gates are the building blocks of more complex logic circuits. These logic gates perform the basic Boolean function such as AND, OR, NAND, NOR, Inversion, Exclusive OR and Exclusive NOR.

These basic logic gates are implemented as small scale integrated circuits (IC) on as part of more complex medium scale (MSI) on very large scale (VLSI) integrated circuits. Digital IC gates are classified not only by their logic operation but also the specific logic-circuit family to which they belong. Each family has its own basic electronic circuit upon which more complex digital circuits and functions are developed.

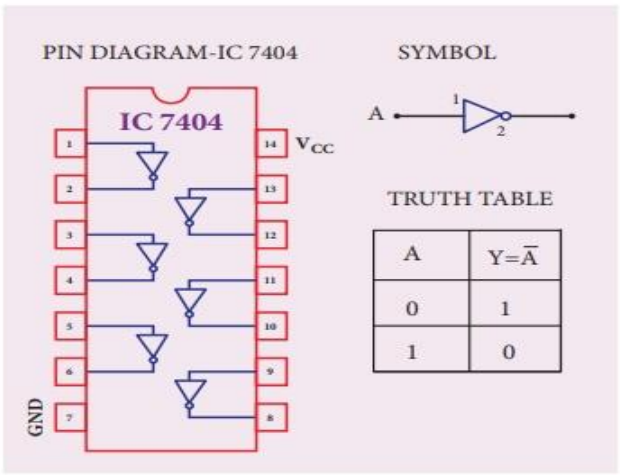
Gate	Description	Truth Table			Logic Symbol
OR	The output is active high if any one of the input is in active high stable. Mathematically, **Q=A=B**	A	B	Output	
		0	0	0	
		0	1	1	
		1	0	1	
		1	1	1	
AND	The output is active high only if both the inputs are in active high state. Mathematically, **Q=A.B**	A	B	Output	
		0	0	0	
		0	1	0	
		1	0	0	
		1	1	1	
NOR	The output is active high only if both the inputs are in active low state. Mathematically, **Q=(A+B)'**	A	B	Output	
		0	0	1	
		0	1	0	
		1	0	0	
		1	1	0	

Gate	Description	Truth Table			Logic Symbol
NAND	The output is active high only if any one of the inputs is in active low state. Mathematically, **Q=(A.B)'**	A	B	Output	
		0	0	1	
		0	1	1	
		1	0	1	
		1	1	0	
NOT	In this gate the output is opposite to the input state. Mathematically, **Q=(A)'**	A		Output	
		0		1	
		1		0	
XOR	The output is active high only if any one of the input is in active high state. Mathematically, **Q=A'B+AB'**	A	B	Output	
		0	0	0	
		0	1	1	
		1	0	1	
		1	1	0	

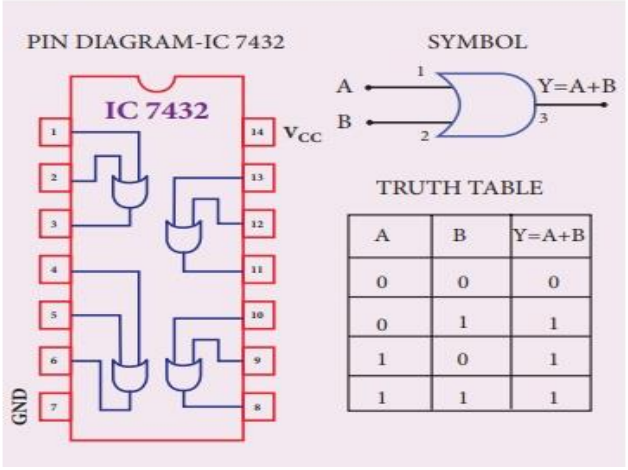
AND Gate:



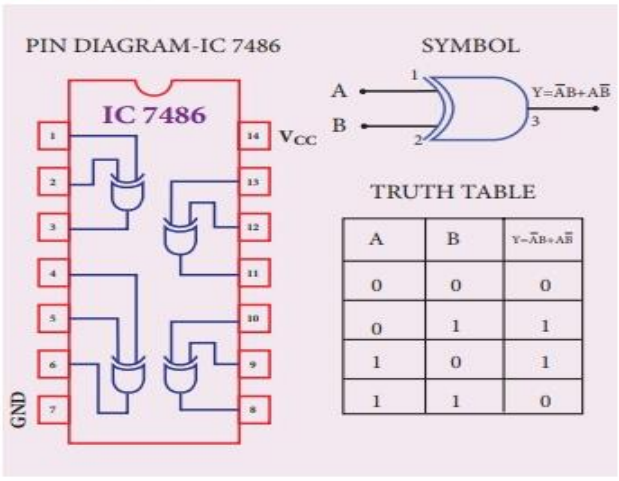
NOT Gate:



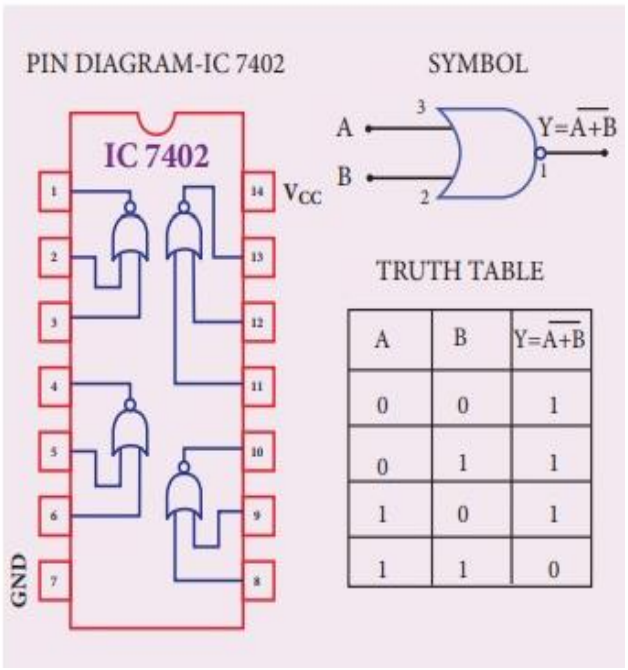
OR Gate:



X-OR Gate :

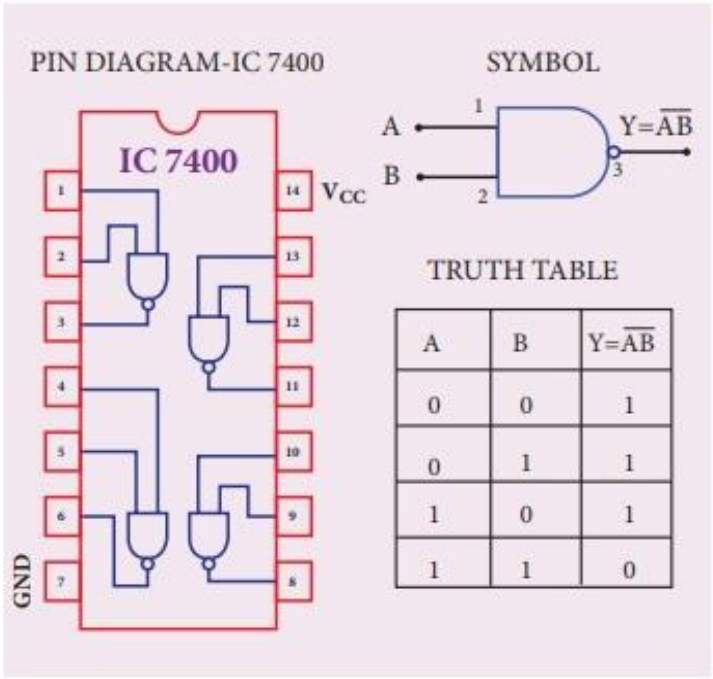


NOR Gate:



A	B	Y=A+B
0	0	1
0	1	1
1	0	1
1	1	0

NAND Gate:



A	B	Y=AB
0	0	1
0	1	1
1	0	1
1	1	0

05.CONCLUSION: -