UNIT-III

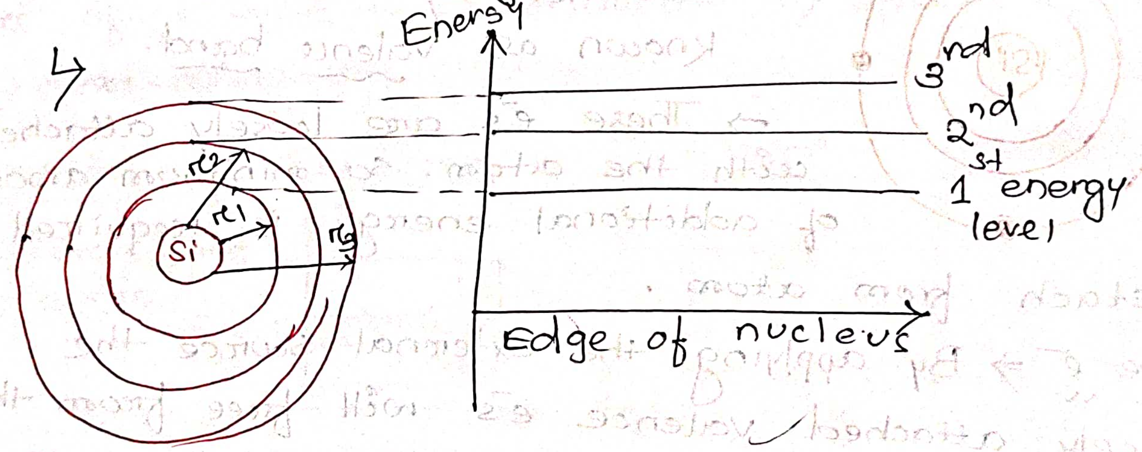
Semiconductor diodes

Introduction →

* Electronics is defined as the branch of engineering which deals with the flow of e^-s in a vacuum or semiconductor by applying some external electric or magnetic field.

* An atom consists of -vely charged e^-s surrounding a dense nucleus that contains +vely charged photons & electrically neutral neutrons.

* Energy level ⇒ Within the ~~atomic~~ atomic structure of each & every isolated atom there are specific energy levels associated with each shell & orbiting e^-.



↳ When e^- jump from lower orbit to higher orbit, it gain some energy & vice-versa.

↳ Each orbit gives some energy to the e^-. So, each individual level is known as discrete energy level.

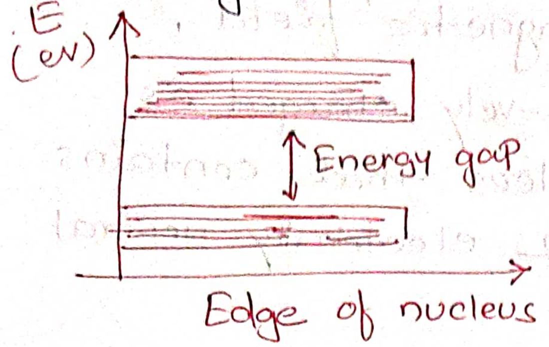
↳ The representation of energy level for an single isolated atom by a horz. line is known as energy-level diagram.

↳ Energy can be measured by electronvolt (eV). It's defined as the amount of energy required by the e^- to move in an orbit through a potential difference of 1V.

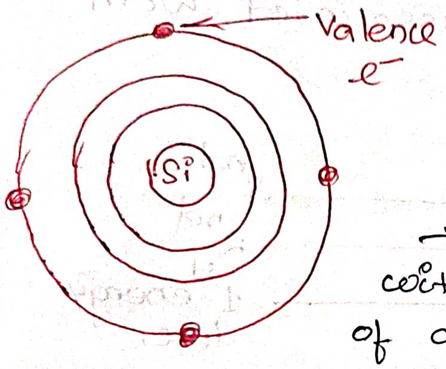
$1\ eV = 1.602 \times 10^{-19}\ C \times 1\ V$

$\{1\ eV = 1.602 \times 10^{-19}\ \text{joule}\}$

Energy band → The representation of the solid by the range of energy is known as energy band diagram.



Valence electron → It's defined as the outermost e⁻ present in the outermost orbit.



→ The range of energies obtained by valence e⁻s are known as Valence band.

→ These e⁻s are loosely attached with the atom. So, minimum amount of additional energy is required to detach from atom.

Free e⁻ ⇒ By applying the external source the loosely attached valence e⁻s will free from the atom & move within the solid. So, these e⁻s are known as free e⁻s.

→ These e⁻s are responsible for conductivity in a solid.

Conduction band → The range of energies possessed by free e⁻s are known as conduction band.

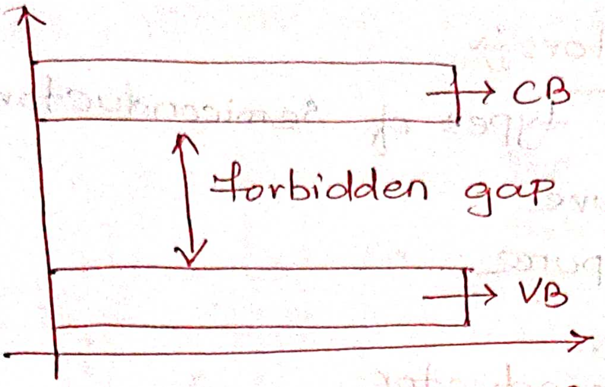
→ Otherwise known as empty band in min^m energy.

⇒ It's always partially filled by free e⁻s. But VB is completely filled by valence e⁻!

② **Forbidden energy gap** → This is the gap between the Valency band & Conduction band.

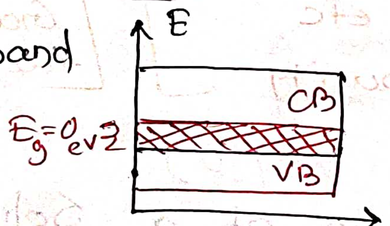
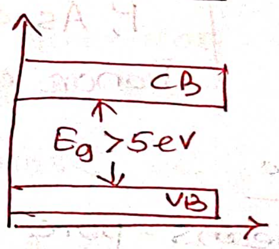
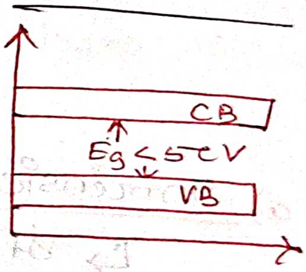
→ There is no free e^- present in this gap.

→ Electron jump from lower band (VB) to upper band (CB), if the supplied energy is max. as compared to forbidden energy (E_g).



Classification of materials ⇒

Depending upon the properties, materials are of 3 types :- i) Conductor ii) Insulator iii) Semi-conductor.

Properties	Conductor	Insulator	Semi-conductor
i) Energy-band diagram			
	In case of Conductor, no forbidden energy gap is present. Hence, e^-s can easily jump from VB to CB and Provide I.	E_g is larger, Hence, max amount of external supply is required to move valence e^- to CB.	For pure Si, $E_g = 1.1\ ev$; for Ge $E_g = 0.78\ eV$
ii) Conductivity (σ)	More	Negligible	In between
iii) Resistivity (ρ)	less	More	In between

Properties	Conductor	Insulator	Semi-cond'
No. of Valence e^-	<4	>4	$=4$
e.g	Au, Cu, Al	Rubber, wood, Plastic, glass	Si, Ge, Arsenic, In

Types of Semiconductors :-

There are two types of semiconductors :

a) Intrinsic or pure

b) Extrinsic or Impure

a) Intrinsic :-

Semiconductor

- Intrinsic
  - Pure form of Ge, Si
- Extrinsic
  - N-type
    - Pentavalent Impurity
    - P, As, Sb etc
    - Donor impurity
  - P-type
    - Trivalent
    - Ga, B, In, Al
    - Acceptor

(Byju)

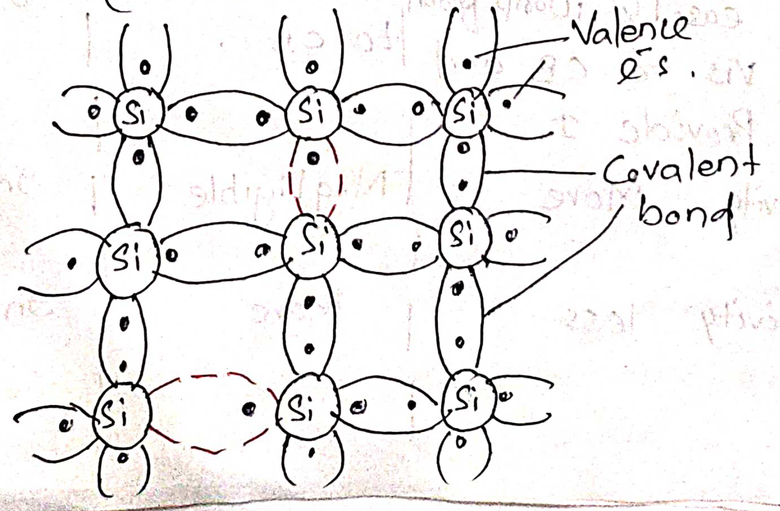
a) Intrinsic :-

↳ It means pure form of a Solid.

↳ It's made up of only a single type of element.

↳ Ge & Si are the most common type of intrinsic Semiconductor elements. They have 4 Valence e^- (tetravalent).

↳

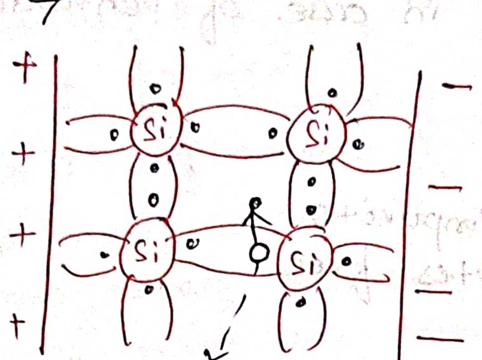


(3)

↳ At absolute 0° temperature, the covalent bonds are very strong and valence e^-s are tightly bounded with the neighbouring atom by forming C.B. Hence, Semiconductor behaves as a perfect insulator.

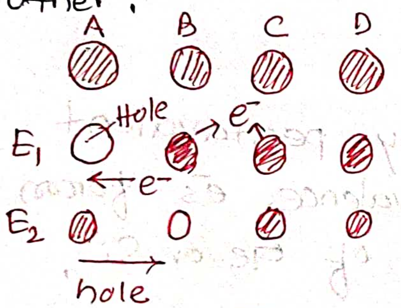
↳ With the increase in temp. few valence e^-s jump into CB by breaking the CB. These e^-s acts free e^-s, which is responsible for the current conduction.

↳



The empty energy state behind the movement of e^- in VB is known as hole. This is an absense of e^-. So, it's considered as positively charged particle.

↳ The movement of e^- & hole is opposite to each other.



* The direction of e^- is from B to A and direction of hole is from A to B,

In intrinsic SC,

$\boxed{\text{No. of } e^- = \text{No. of hole}}$

let $n \rightarrow$ no. of e^-

$P \rightarrow$ no. of holes

$\boxed{n = P}$ $\boxed{\therefore n = P = n_i}$

n_i = intrinsic S.C

b) Extrinsic Semiconductor →

(Intrinsic + impurity = Extrinsic)

→ The conductivity of S.C can be improved by introducing a small number of impurities.

→ The process of adding impurity atoms to the pure S.C is called Doping.

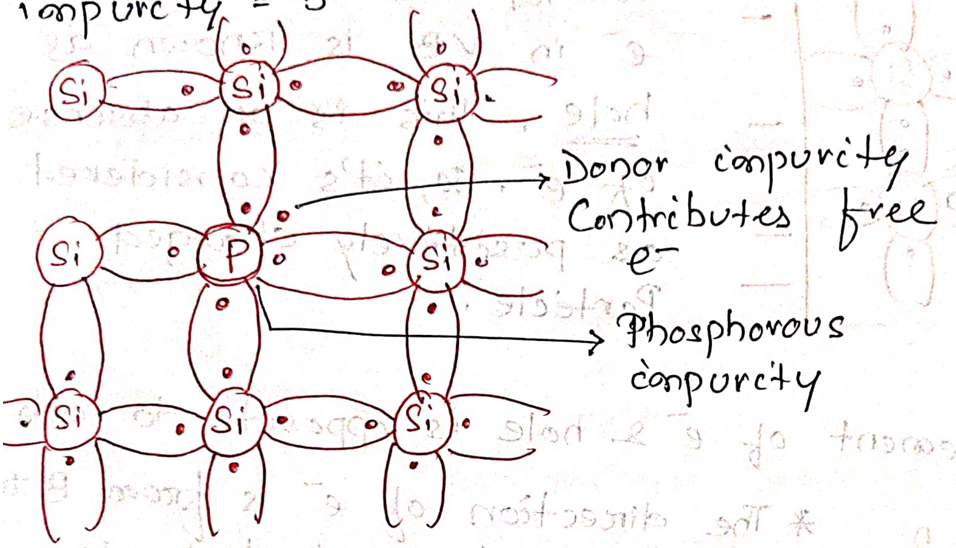
⇒ And the impurities are known as dopant.

⇒ An extrinsic semiconductor can be further classified into:

* N-type
* P-type

i) N-type :- An n-type material is created by introducing impurity elements that have 5 valence e^-s (Pentavalent) such as antimony, arsenic & phosphorus.

↳ The no. of valence e^- in case of pentavalent impurity = 5



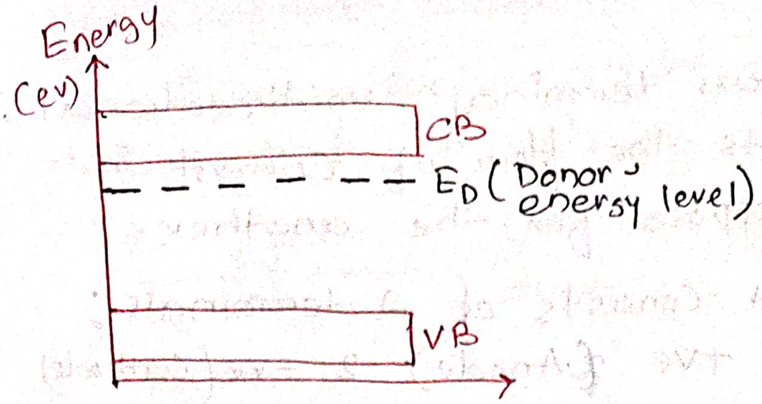
(n-type)

⇒ When a pure S.C (Ge or Si) is doped by pentavalent impurity then, 4 e^-s out of 5 valence e^-s form covalent bonds with the 4 e^-s of Ge or Si.

⇒ The 5^{th} e^- of dopant is set free. Thus, the impurity atom donates a free e^- for conduction is called 'Donor'.

⇒ Since the no. of free e^- ↑ by the addition of an impurity, the -ve charge carriers increase. Hence, it's called n-type sc.

⇒ As conduction is due to a large no. of free e^-s, the e^-s in the n-type s.c are the majority carriers & holes are the minority carrier.

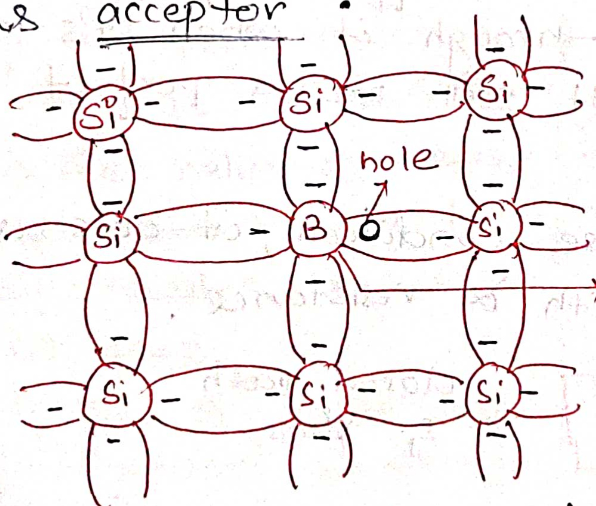


ii) P-type :-

* When a pure s.c is doped with a trivalent impurity (B, Al, In, Ga) then ~~3 valence e⁻s~~ p-type s.c is formed.

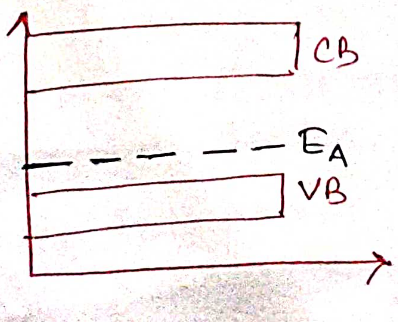
* No. of valence e^- = 3

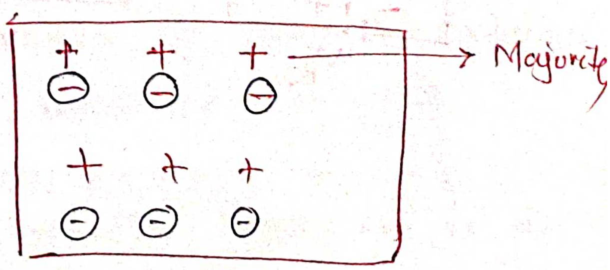
* When trivalent impurities are added the Si atom, then valence e⁻s are making covalent bond with the neighbouring atom. But the 4^{th} covalent bond is incomplete. So, it can accept or receive 1 e^- to complete covalent bond. Hence, these impurity atoms are known as acceptor.



↳ The resulting vacancy is called a hole. With the ↑ in the no. of impurities, the holes are increased. Hence, it's known as p-type sc.

→ As conduction is due to a large number of holes, the holes in the p-type are MAJORITY Carriers & e⁻s are MINORITY Carrier,





Ideal diode →

↳ Diode is a two terminal, unidirectional device which permits the flow of current in one direction and oppose for the another direction.

↳ It consists of 2 terminals: +ve (Anode) & −ve (cathode)

(Symbol)

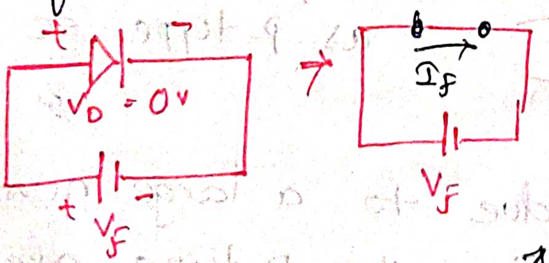
↳ the electric current always flows from anode to cathode.

↳ If the positive terminal of the battery is connected to the p-type S.C & −ve terminal is to n-type, then diode is said to be forward biased.

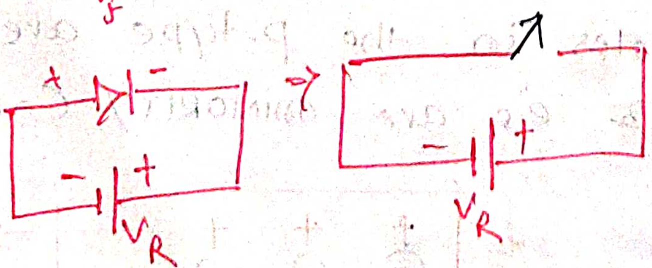
↳ Similarly, if +ve of the battery is connected to the n-type S.C & −ve to p-type, the diode is known as reverse biased.

↳ An ideal diode does not offer any resistance to the flow of current through it when it's in forward biased mode. It will be a perfect conductor.

↳ Under reverse biase condition, it acts as a perfect insulator with ∞ resistance.



closed path ⇒ I_F flows

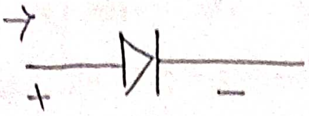


open path
I_R 0 μA

(5)

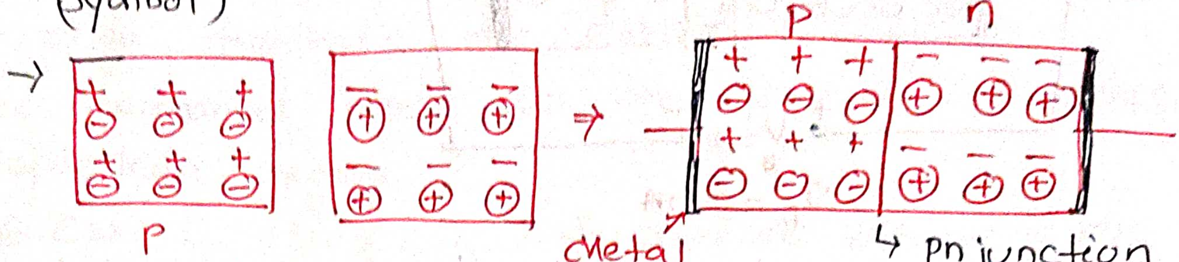
Semiconductor diode →

Semiconductor diodes are two-terminal devices that consists of a p-n junction.

→ 

Direction of arrow indicates the direction of current.

(Symbol)

→ 

→ The junction is not a physical separation between p & n-type but it is an electrical boundary/separation betn these two s.c.

→ Silicon & Ge are used for the fabrication of pn diode. But Si is preferably used because.

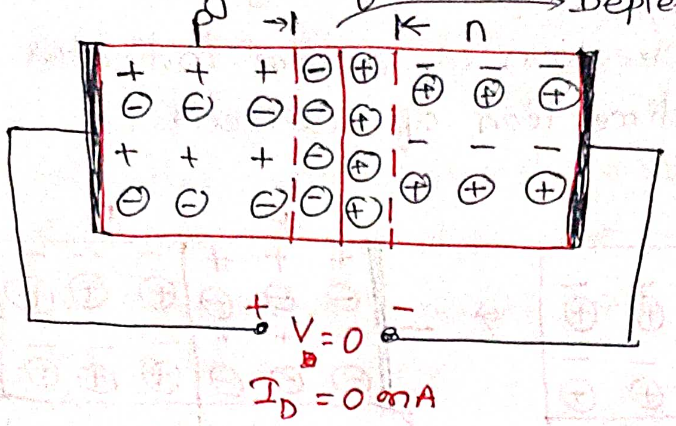
Si	Ge
i) The peak inverse voltage (PIV) is 1000V.	i) PIV is 400V.
ii) The value of reverse saturation current in Si doubles at 10°c rise in temp.	ii) Value doubles at 8°c rise in temp.
iii) The Si-diode can withstand upto 200°c.	iii) It can withstand upto 100°c.

Physical Operation of a pn junction diode →

i) Pn junction diode under Zero-biased condition →

Biasing is the process in which external DC source (Voltage) is connected to the particular device.

↳ The closer the minority carrier is to the junction, the greater is the attraction force the layer of −ve ions and the less is the opposition offered by the +ve ions in the depletion region of n-type.



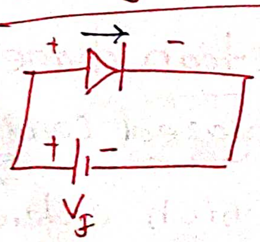
→ The movement of holes from p to n-side due to the diffusion (higher concentration to lower conc.). Similarly, free $\bar{e}$s are diffused from n to p.

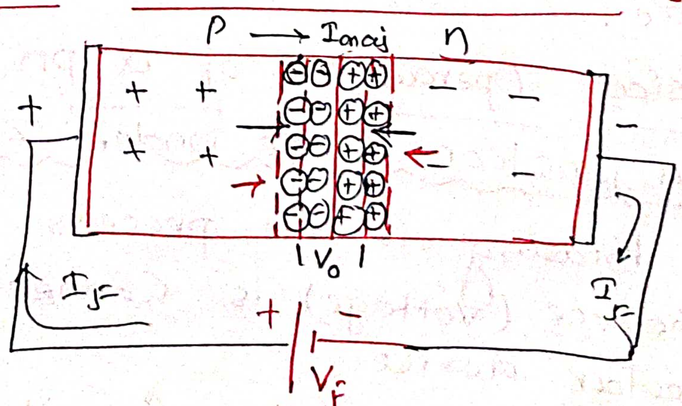
→ Due to diffusion, the free $\bar{e}$ try to recombine with hole and create an $\bar{e}$-hole pair. The process is known as recombination.

→ Due to recombination, the fixed ions are collected across pn junction. Due to its nature, they can't take part in the cond' of current. The region contain all the depleted fixed ion $\bar{e}$s known as depletion region. It's otherwise known as space-charge region.

→ The width of depletion region depends on the doping level.

b) pn junction diode under forward bias →





6/ When the +ve terminal of the battery is connected ~~to~~ to p-side & the -ve terminal of the battery is to n-side, that condition is known as forward-bias.

* In forward bias, the positive terminal repel all the majority charge carrier (holes) from p-side towards the depletion region. ||^{rly} -ve terminal repels all the free e^- towards depletion region.

* Case-1 if $V_f < V_0$ (Forward dc voltage is less than barrier potential)

The depletion region acts as a barrier for the movement of hole & e^-. So, the carriers cann't pass through the depletion region & deposited across the region.

So current conduction is not possible from p to n.

$\therefore$ $I = 0A$

* Case-2 ($V_f > V_0$)

When forward voltage exceeds the barrier potential (V_0) then depletion region gets weaker and the diffused holes & e^-s enter to the depletion region.

Here, holes & e^-s make the recombination process with +ve & -ve ions. So the width of the depletion region is reduced.

The current flow due to majority charge carrier is known as forward current (I_F).

The V-I relationship betn forward bias & reverse bias can be expressed by

$$i = I_S\left(e^{V_D/nV_T} - 1\right) \quad -(1)$$

∵ i = forward current (I_f)

I_S = reverse saturation current

V_D = Applied Voltage

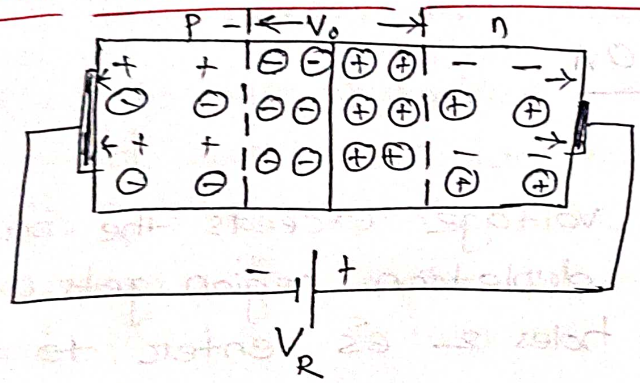
V_T = Thermal Voltage $= \frac{KT}{q}$

(K = Boltzmann's const = 1.38×10^{-23} J/K
T = Abs. temp in k = 273 + temp in °C)

n = Emission coefficient, which is a function of the operating conditions & physical construction.

= 1 for Ge, 2 for Si.

c) Under reverse-bias condition → ($V_D < 0V$)



↳ When +ve terminal of the battery is connected to its n-side & -ve terminal to the p-side of the diode, then the condition is known as reverse bias.

↳ All the majority charge carriers are attracted towards the battery terminals. Majority holes & ēs are movable in nature. So, the fixed ions are deposited near the depletion region. Hence, the width of the depletion region is increased.

→ There is no current due to the majority carrier because the movement of charge carriers are away from the depletion region.

(7) But due to minority Carrier, a small amount of Current is produced in the diode. This is known as reverse saturation Current (I_0).

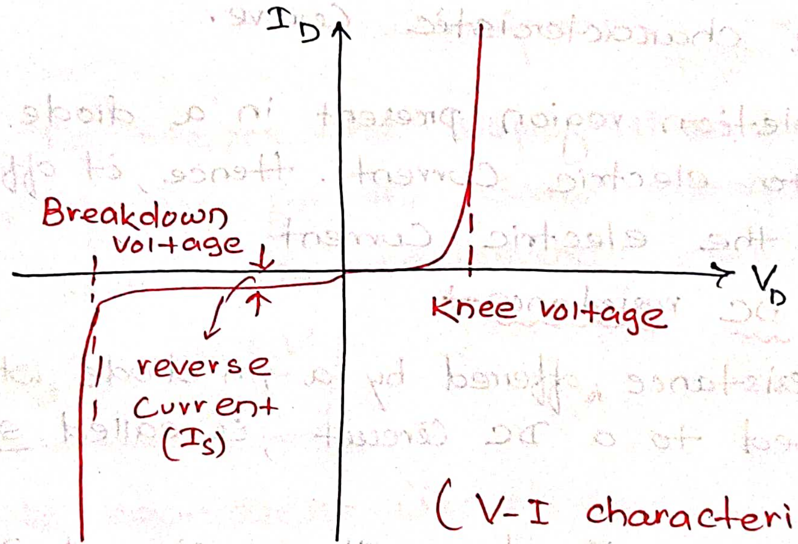
↳ The reverse voltage at which pn junction breaks is known as breakdown voltage.

Breakdown region :→

When the reverse voltage (V_R) will ↑ Continuously, then at a particular point I_s will increase suddenly. This is known as breakdown effect of a pn junction diode.

* There are two types of breakdown effect occurs in a diode.

a) Zener breakdown
b) Avalanche breakdown



(V-I characteristic)

* a) When the value of reverse voltage (V_R) is ↑ cont, then W_{dep} will increase. It'll provide greater barrier potential (V_0) across the depletion region. It's create the diffused minority Carrier in p & n side. There is large no. of minority Carrier which provides Saturation Current (I_s). The voltage at which breakdown occurs is known as Zener breakdown & the voltage is known as Zener Voltage (V_z).

16)

* When V_R will ↑ in a heavy amount, then due to the repulsion on the minority carrier, they will collide with the other atoms & due to the higher momentum they will break the covalent bond.

↳ Due to this higher momentum, the collision process will continue upto its highest value. This continuous process is known as avalanche breakdown.

↳ Here, the no. of minority carrier is increased due to the higher velocity.

Resistance levels →

As the operating point of a diode moves from one region to another the resistance of the diode will also change due to the nonlinear shape of the characteristic curve.

* The depletion region present in a diode acts like barrier to electric current. Hence, it offers resistance to the electric current.

a) Static or DC resistance →

The resistance offered by a pn diode when it's connected to a DC circuit, is called static resistance.

↳ It is also defined as the ratio of DC voltage applied across diode to the DC current flowing through the diode.

↳ The resistance offered by pn diode under forward biased condition is denoted as R_f.

$$\boxed{R_f = \frac{\text{DC Voltage}}{\text{DC Current}} = \frac{V_D}{I_D}}$$

8)

b) Dynamic or AC resistance ⇒

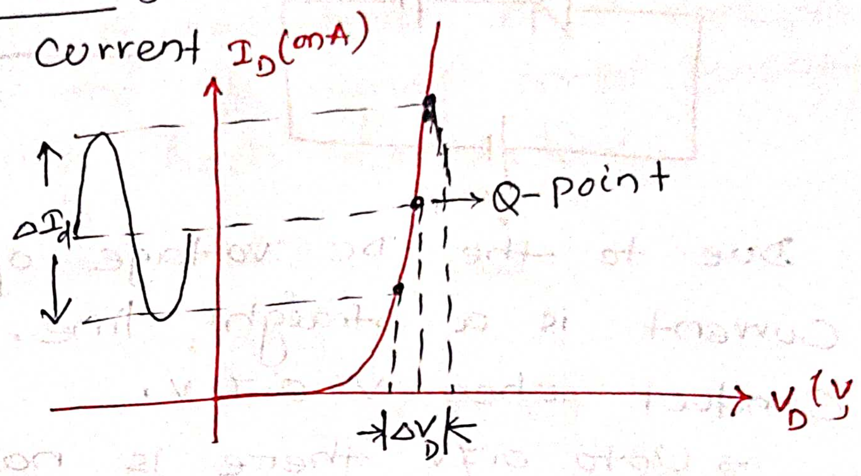
↳ It's the resistance offered by p-n diode when AC voltage is applied.

↳ In AC circuit, charge carriers or current does not flow in single direction. It flows in both forward & reeverese direction.

↳ It's also defined as the ratio of change in voltage to the change in I. It's denoted as r_f.

$$r_f = \frac{\text{change in voltage}}{\text{change in current}}$$

or $\boxed{r_d = \frac{\Delta V_d}{\Delta I_d}}$



* The steeper the slope, the lower is the value of ΔV_d for the same change in ΔI_d & the lower is the resistance.

$\boxed{r_d = \frac{26\,mV}{I_D}}$

Diode equivalent Circuits ⇒

It's the combination of different elements depends upon the proper requirement in a system.

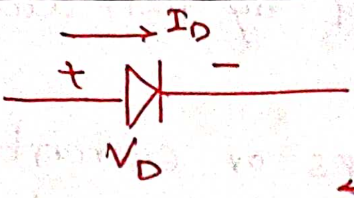
↳ 3 different types of equivalent circuits are designed for pn junction diode

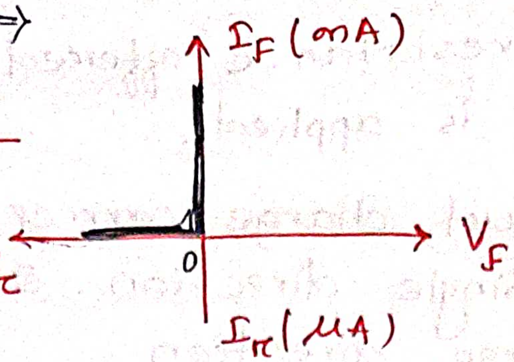
a) Ideal equivalent circuit

b) Simplified "

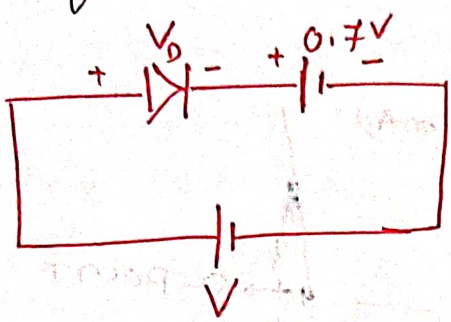
c) piecewise-linear "

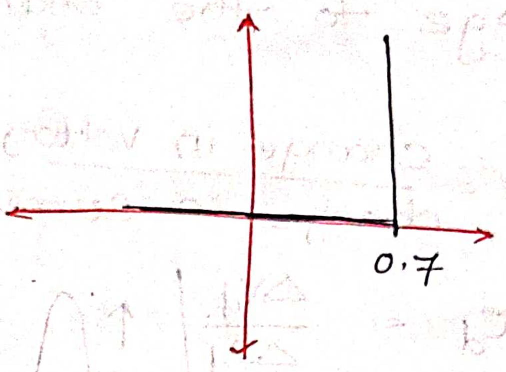
a) Ideal circuit ⇒





b) Simplified Circuit ⇒

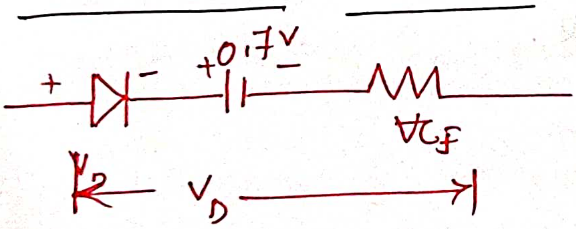




Due to the DC voltage of 0.7 the forward Current is a straight line. The diode will Conduct when V = 0.7 V.

→ Upto 0.7V, there is no current within the circuit.

c) Piecewise – Linear ⇒



It defines the resistance level of the device when it's in on state.

↳ The ideal diode is included to establish the unidirectional Current conduction.

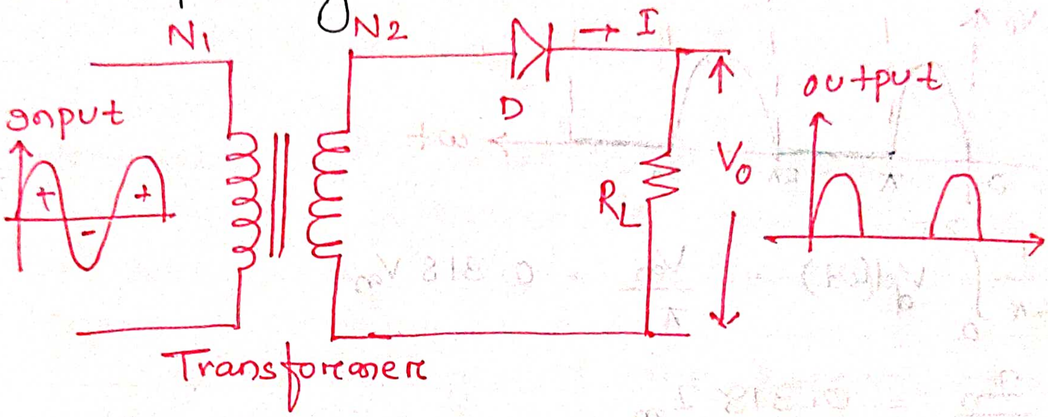
$$r_f = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt to pt}}$$

Rectifier → It's an electronic device which Converts input AC signal into output Pulsating DC signal.

Rectifier
- Half-wave
- full-wave
  - Centre tapped
  - Bridge

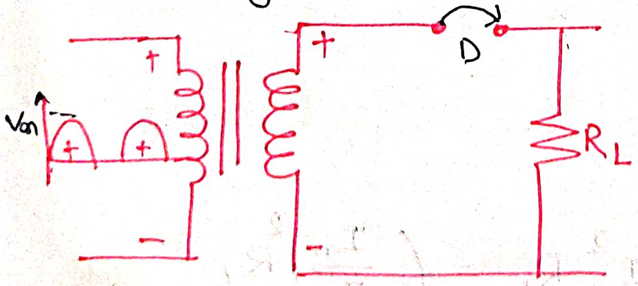
a) Half-wave rectifier →

It is a type of rectifier which converts only one half of the i/p signal into pulsating DC depending upon diode Connection.



Working Principle →

a) During +ve half-cycle →



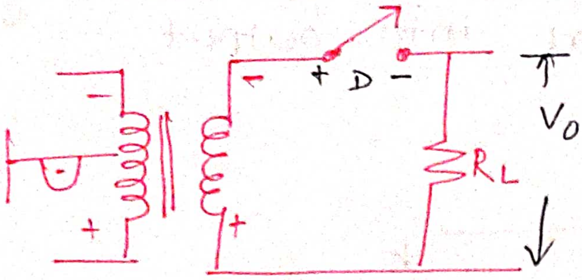
During +ve half cycle only +ve halves are Considered across the transformer winding.

→ Diode is forward biased and allows current through the Circuit.

→ The resistor placed at the o/p consumes the DC Current generated by diode. The o/p DC Voltage or Current is measured across R_L.

→ The o/p voltage is equal to V_{in} for +ve half. i.e $\boxed{V_0 = V_{in}}$

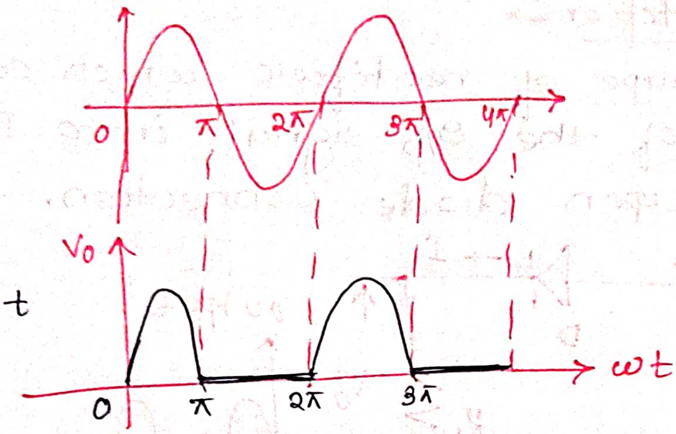
b) During -ve half →



During -ve half cycle, diode is reverese biased or open. Hence, there is no current through the circuit.

so $\boxed{V_0 = 0V}$

Waveform :- v_i



$$V_{dc} = \frac{1}{2\pi}\int_0^{2\pi} V_d\, d(\omega t) = \frac{V_m}{\pi} = 0.318\, V_m$$

$$I_{dc} = \frac{I_m}{\pi} = 0.318\, I_m$$

$$\Rightarrow I_{dc} = 0.318\left(\frac{V_m}{r_f + R_L}\right)$$

$$V_{rms} = \frac{V_m}{2} = 0.5\, V_m$$

$$I_{rms} = \frac{I_m}{2} = 0.5\, I_m$$

$$\eta = \frac{P_o}{P_{in}}, \quad P_{out} = P_{dc} = I_{dc}^2 R_L = \left(\frac{I_m}{\pi}\right)^2 R_L$$

$$P_{in} = I_{rms}^2 (r_f + R_L)$$

$$\boxed{\eta = 0.406 \text{ or } 40.6\%}$$

Ripple factor → In dc signal, some unwanted ac components are present known as ripple.

$$r.f = \frac{I_{ac}}{I_{dc}} \text{ or } \frac{V_{ac}}{V_{dc}}$$

b) Full-wave rectifier :→

A rectifier circuit that rectifies both +ve & -ve half cycles can be known as FWR.

→ It's divided into 2 types :-

a) Center-tapped

b) Bridge

a) Center-tapped →

Here requirements are :-

i) Center-tap transformer

ii) two-diodes

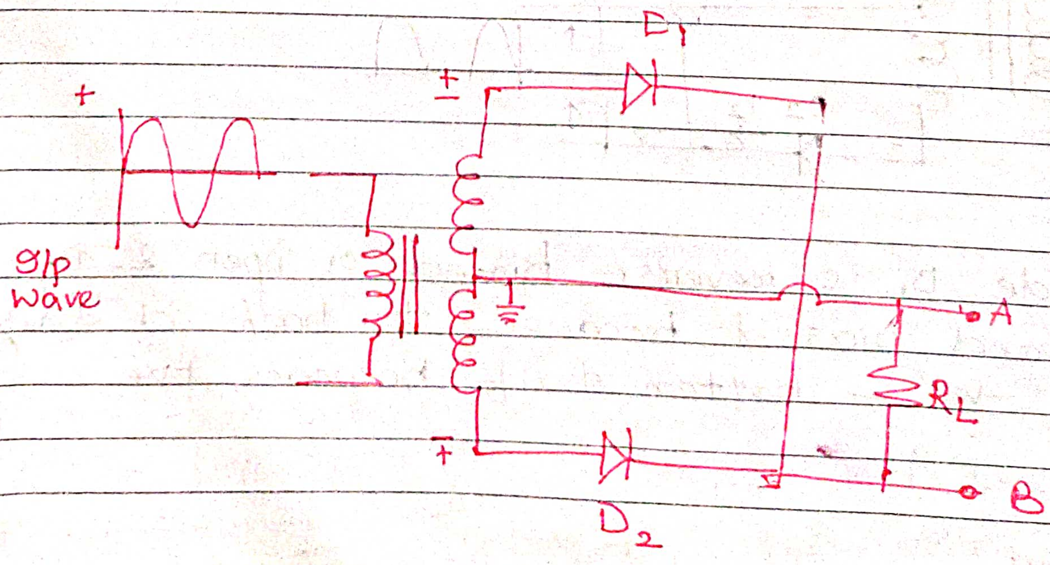
iii) Load-resistor (R_L)

Features :- a) The tapping is done by drawing a lead at the mid-point on the secondary winding. This winding is divided into 2 equal halves.

b) The voltage at the tapped mid-point is zero.

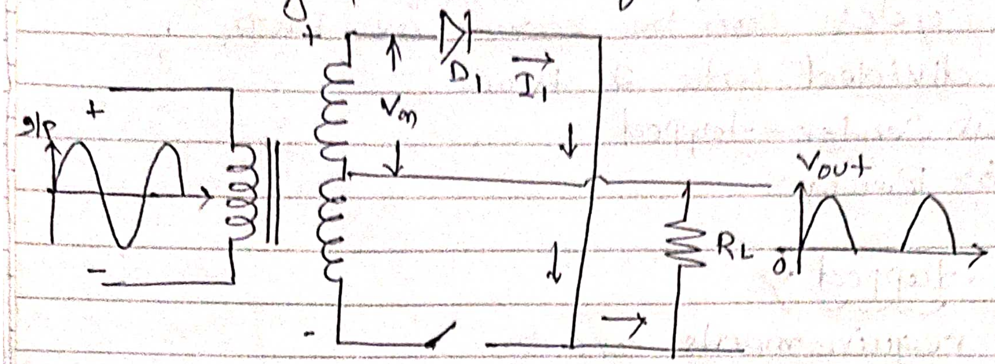
c) The center-tapping provides two separate o/p voltages which are equal in magnitude but opposite in polarity.

b) i:- Circuit diagram :-



Working :-

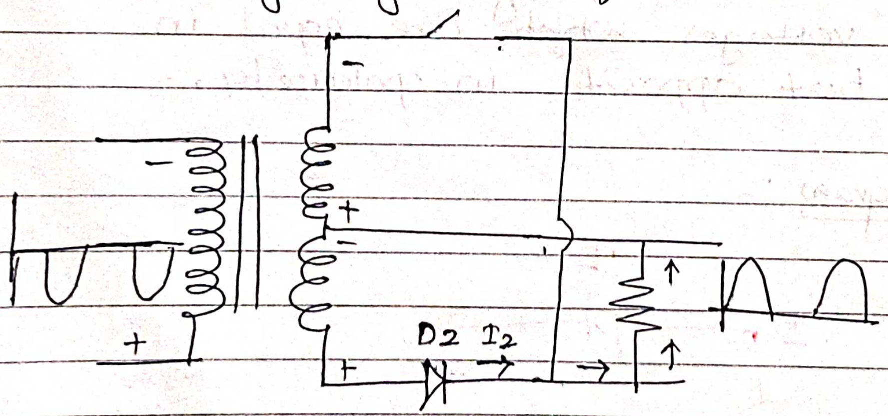
a) During positive half-cycle :-



During +ve half, only +ve half is given as input to the primary winding. Diode D_1 is forward biased as it's connected to the top of 2nd ary winding. Diode D_2 is reverse biased as it's connected to bottom of the Secondary winding.

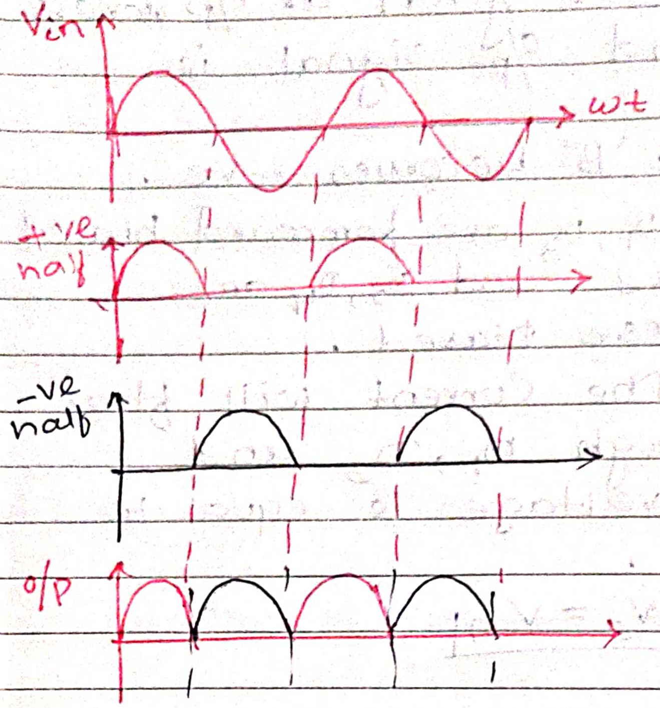
$D_1 \rightarrow$ Short circuit and current will flow through it and o/p will be +ve half.

b) During negative half-cycle :-

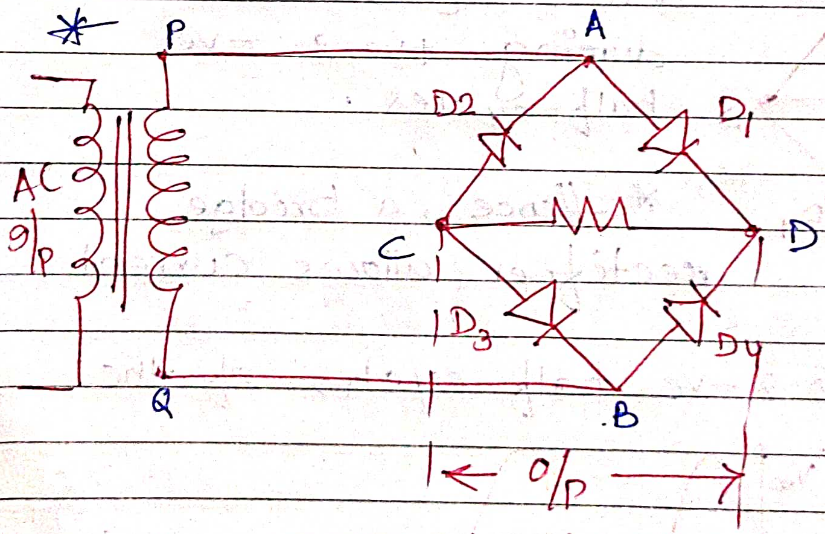


Diode D_1 is reverse biased or open & D_2 is forward biased because top half of 2nd ary becomes -ve & bottom half becomes +ve.

Waveform :-



b) Bridge rectifier → It is defined as a type of FWR that uses 4 diodes in a bridge circuit to convert ac current to dc current.

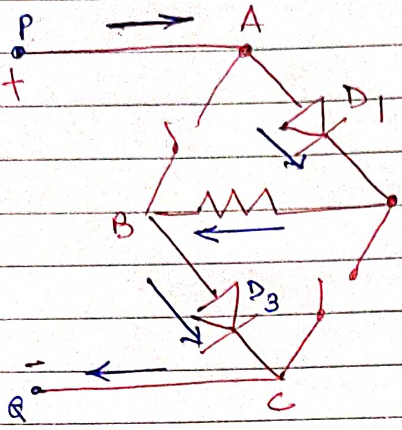


→ It consists of 4 diodes D_1, D_2, D_3 & D_4 and load resistor R_L. The 4 diodes are arranged in such a way that only 2 diodes conduct electricity during each half-cycle. D_1 & D_3 are conducting during +ve half and D_2 & D_4 are conducting during -ve half cycle.

Working :-

i) When +ve half-cycle is given as i/p across terminal A & B ~~the~~ and o/p signal is obtained across R_L.

→ 'A' becomes +ve & 'B' becomes −ve.

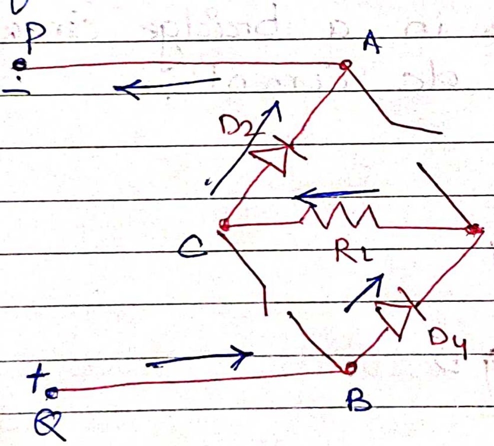


→ Diode D_1, D_3 are forward biased or close and D_2, D_4 are reverese biased.

→ The Current will flow through D_1, D_3 and o/p voltage is equal to V_m.

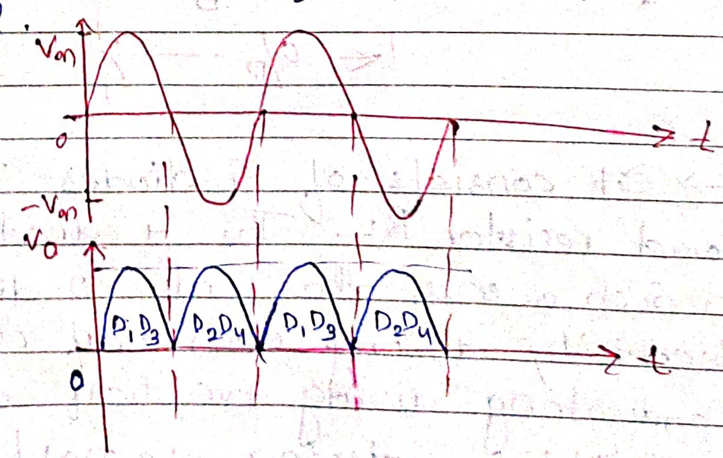
$$\boxed{V_0 = V_m}$$

ii) When −ve half-cycle, Point P becomes −ve w.r.t Q. It makes diode D_2, D_4 forward biased while D_1, D_3 reverse biased.



* The Current flow across R_L is same during +ve & −ve half-cycles.

* Hence, a bridge rectifier allows current during both +ve & −ve half cycles of the i/p AC signal.



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Peak Inverse Voltage → (PIV)

Whenever two of the diodes are being in parallel to the secondary of the transformer, the max secondary voltage across " appears at the non-conducting diodes which make the PIV of the rectifier ckt. Hence, the PIV is the max. voltage across the secondary winding i.e

$$\boxed{PIV = V_m}$$

Advantages :- i) No need of center-tapping

ii) DC o/p voltage is twice that of center-tap rectifier.

iii) PIV of diodes is of the half-value that of center-tap.

iv) Design is easier.

Equations :-

i) $V_{dc} = \frac{1}{T}\int_0^T V_a(\omega t)$

$= \frac{1}{\pi}\int_0^{\pi}(V_m \sin\omega t)\, d(\omega t)$

$$\boxed{V_{dc} = \frac{2V_m}{\pi}} \quad \text{or} \quad \boxed{V_{dc} = 0.636\, V_m}$$

ii) $I_{dc} = \frac{2I_m}{\pi}$ or $0.636\, I_m$

for center-tap $I_m = \frac{V_m}{V_f + R_L}$

for bridge, $I_m = \frac{V_m}{2V_f + R_L}$

iii) $V_{rms} = \sqrt{\frac{1}{T}\int_0^T V_d^2(\omega t)}$

$= \sqrt{\frac{1}{\pi}\int_0^{\pi}(V_m \sin \omega t)^2 d\omega t}$

$= \frac{V_m}{\sqrt{2}}$ or $0.707 V_m$

$I_{rms} = \frac{I_m}{\sqrt{2}}$ or $0.707 I_m$

iv) $\eta = \frac{P_{out}}{P_{in}} = I_{dc}^2 R_L = \left(\frac{2I_m}{\pi}\right)^2 R_L$

$P_{in} = I_{rms}^2 (R_f + R_L)$. $P_{out} = \frac{I_m^2}{2}(R_f + R_L)$

$= \left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_L)$

$\eta = P_{out} / P_{in}$

$= \frac{8}{\pi^2}$ or 0.81 or 81%

v) ripple factor $r.f = \frac{I_{ac}}{I_{dc}} = 0.483$

vi) ~~Form~~ factor $= \frac{I_{rms}}{I_{dc}} = 1.1$

Q-1) An ac voltage of peak value 20v is Connected in series with a Si diode & load resistance of 500 Ω. If the forward resistance of diode is 10 Ω. Find i) peak Current through diode ii) Peak o/p voltage what will be these values if the diode is assumed to be ideal?

D. $V_{in} = 20V$

$R_L = 500\,\Omega$

$r_f = 10\,\Omega$

Si diode $V_0 = 0.7V$

13.

i) $V_f = V_0 + (I_f)_{peak}(r_f + R_L)$

$\Rightarrow \dfrac{V_f - V_0}{r_f + R_L} = I_f \Rightarrow I_f = \dfrac{20 - 0.7}{10+500} = 37.8\ mA$

ii) Peak o/p voltage $= (I_f)_{peak} \times R_L = 37.8\ mA \times 500$
$= 18.9\ V$

Ideal diode, $V_0 = 0$ & $r_f = 0$ so

$V_f = I_f \times R_L \Rightarrow I_f = \dfrac{V_f}{R_L} = \dfrac{20}{500} = 40\ mA$

Peak o/p volt $= 40\ mA \times 500 = 20\ V$

2) A HWR uses a diode with internal resistance of $100\ \Omega$. If input ac signal is 220 V (rms) & $R_L = 2\ kV$. Calculate I_m, I_{dc}, I_{rms}, V_{dc}, P_{dc} & η.

Given :-

$R_L = 2\ kV$, $r_f = 100\ \Omega$, $V_i = 220\ V (rms)$
$\Rightarrow V_m = 220\sqrt{2}$
$= 311.1$

i) $I_m = \dfrac{V_m}{R_L + r_f} = \dfrac{311.1}{2000+100} = 0.148$

ii) $I_{dc} = \dfrac{I_m}{\pi} = \dfrac{0.148}{\pi}$ (or 0.318×0.148
$= 0.047$)

iii) $I_{rms} = 0.5\ I_m = 0.074\ A$

iv) $V_{dc} = V_m/\pi = 0.318\ V_m = 98.96$

v) $P_{dc} = I_{dc}^2 R_L = (0.047)^2 \times 2000 =$

vi) $\eta = 0.406 \left(\dfrac{1}{1 + \frac{r_f}{R_L}}\right)$

$= 0.386$
$= 38.6\%$

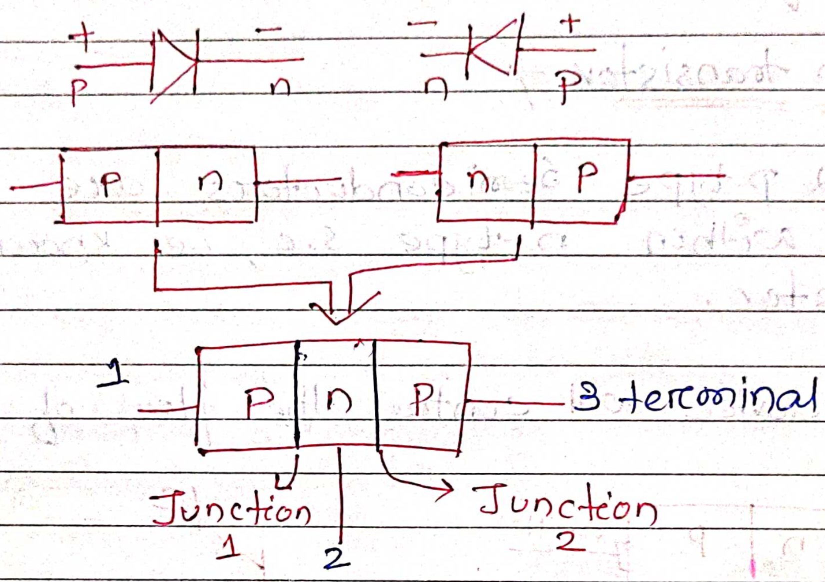
Bipolar Junction Transistors (BJT)

Introduction :-

A transistor is a 3 terminal Semiconductor device that regulates current / voltage flow and acts as a switch for signals.

* Bipolar means both e^- & holes are implemented in this fabrication process.

* It has two P-n junction.



Construction →

↳ Transistor is formed by connecting two diodes back to back. Hence, it has two PN junctions.

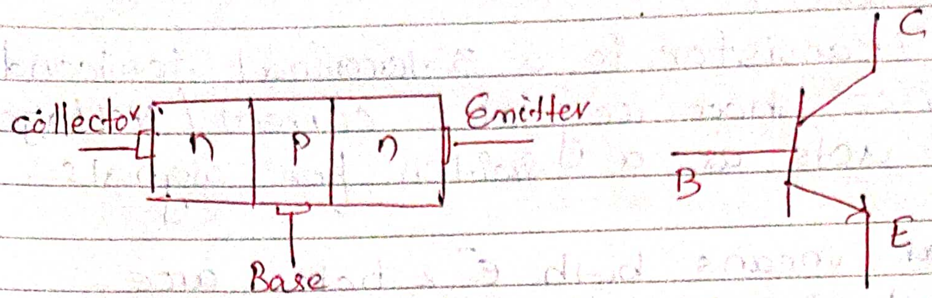
↳ 3 terminals are drawn out of 3 Semiconductor materials present in it.

↳ There are 2 types of transistors:-

a) npn b) pnp

a) npn :- When two n-type of s.c are sandwiched or implemented with a p-type semiconductor, it's known as npn transistor.

↳ It's basically used to amplify weak signals to strong signals.

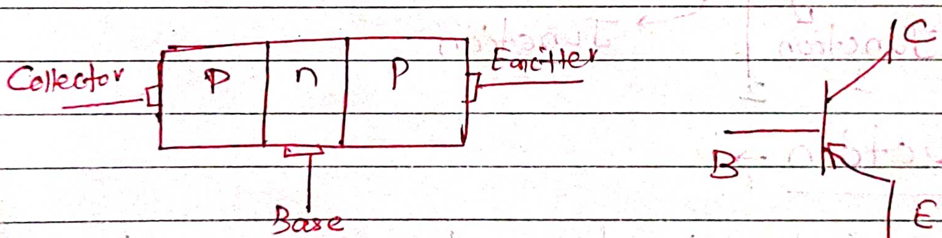


* In npn transistor, the e's move from the emitter to collector region resulting in the formation of current in the transistor.

*(b) P-n-p transistor ⇒

↳ When a p-type semiconductors are sandwiched within n-type s.c, i.e known as pnp transistor.

↳ The device will control the flow of current.



Terminals :→ It has 3 terminals :-

a) Emitter b) Base c) Collector

a) Emitter :→ Emits the majority charge carrier from 1 end to another end because
→ It's heavily doped.

* The width of emitter area is more to emit sufficient amount of majority carrier.

* It's represented by an arrow mark near the terminal.

* Always forward biased w.r.t base.

3

b) Base :→ It's present as the middle part in the BJT Symbol.

* It's lightly doped as compared to E & C.

* The area of base is thin, It passes most of the charge Carriers to collector.

c) Collector :→ Its function is to collect the Carriers.

* It's a bit larger in size than emitter & base. It's moderately doped.

* Reverse biased w.r.t base.

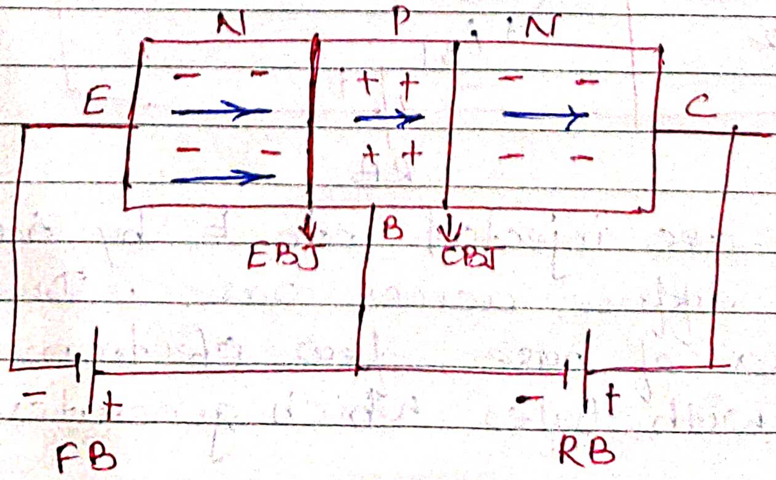
Transistor Operation →

There are 4 mode of operation in a BJT. Depending upon the diode configuration →

i) Active ii) Cut-off iii) Saturation
iv) Reverse - active

Modes of operation		EBJ	CBJ
i) Active	⇒	F.B	R.B
ii) Cut-off	⇒	R.B	R.B
iii) Saturation	⇒	F.B	F.B
iv) Reverse-active	⇒	R.B	F.B

i) Working of npn transistor :-



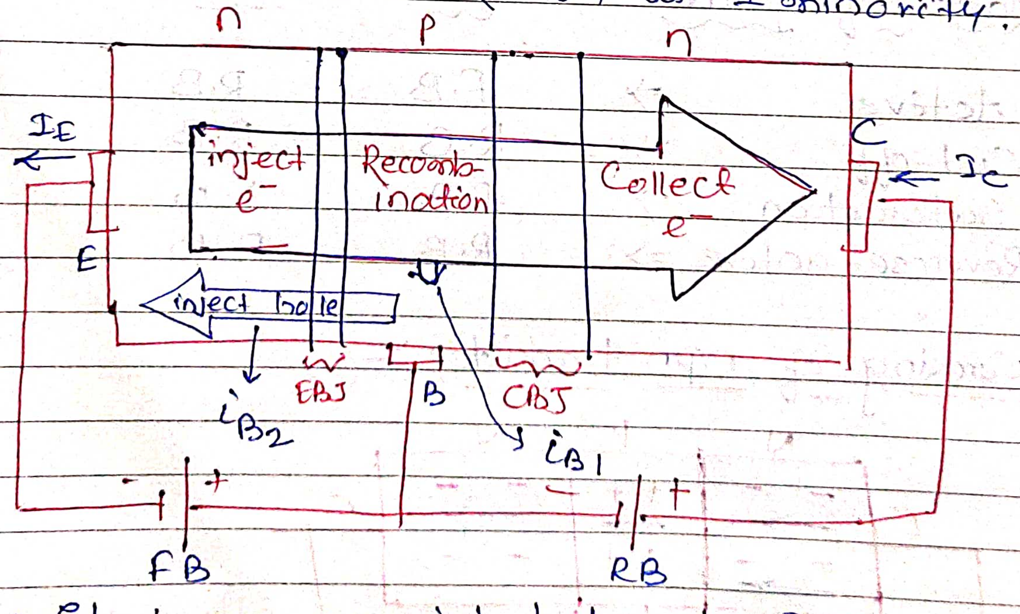
↳ The emitter of npn is made by n-type material, hence the majority Carriers are electrons.

↳ When EBJ is forward biased, the $\bar{e}$s will move from the n-type region towards p-type region and the minority Carriers holes moves towards n-type region.

↳ It decreases the width of EBJ.

↳ ~~The~~ As E has more area as compared to base, no. of $\bar{e}$ is more. So, the Current produced in the Circuit can be considered as flow of $\bar{e}$s. EBJ will give more amount of Current due to majority Charge-carrier which is known as $I_{majority}$.

↳ When CBJ is reverse-biased, there is no Current due to majority Carrier, but due to minority Carrier Small amount of Current is produced, which is known as $I_{minority}$.



* Electrons are injected into E by supply voltage. It'll diffuse across base. Due to the thin area of base, few electrons are recombined with holes which generates current i_{B_1}.

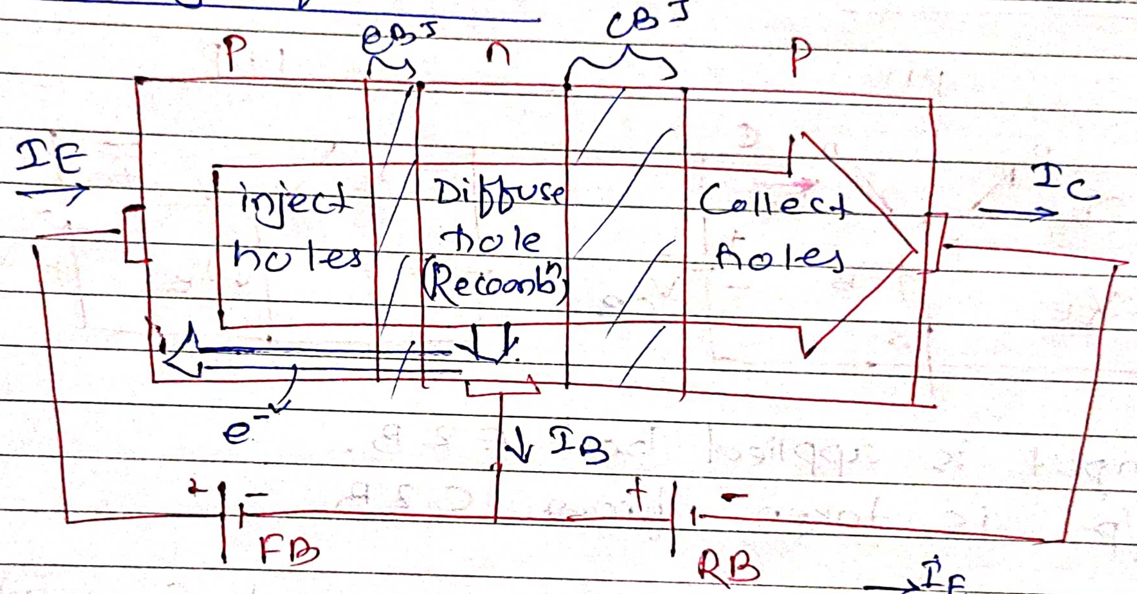
3.

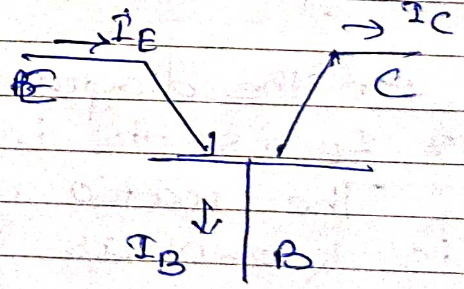
* Remaining e's are collected across Collector. In this area, no current is produced due to the reverse-biased condition. It only collects the free-e's coming from E, which is known as Collector Current (i_c).

* Due to +ve terminal (FB), majority carriers of P-side will repel towards n-side which is emitter region. This current component due to hole is known as i_{B_2}.

$$\boxed{I_E = I_B + I_C}$$

ii) Working of PNP





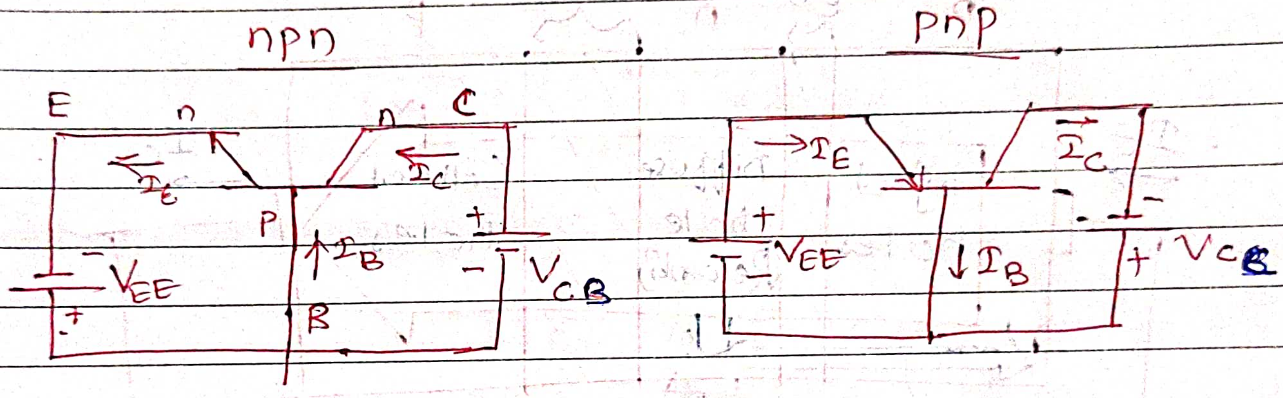
Transistor Configuration ⇒

Depending upon the terminal, the configurⁿ is of 3 types :-

i) Common - base (CB)
ii) Common emitter (CE)
iii) Common collector (CC)

The word 'common' stands for the terminal which is present both in input & output side.

a) Common-base



Input is applied betⁿ E & B.
O/P is taken from C & B

In the diagram, I_C is the output current & I_E is the input current.

The ratio of o/p current to i/p current is known as current amplification factor (α).

$$\alpha_{dc} = \frac{I_C}{I_E} \quad -(1)$$

$\Rightarrow I_C = \alpha I_E$ As $I_E << I_C$ so

$\alpha < 1$

$I_C = I_{C\,majority} + I_{C\,minority} \quad -(2)$

(4)

When CBJ is reverse-biased & EBJ is open condition, the I_s is known as I_{CO} (Collector Current when E is open).

I_{CO} can be represented as I_{CBO} (collector to base current) when emitter is open.

$$\boxed{I_C = \alpha I_E + I_{CBO}} \quad \text{— (3)}$$

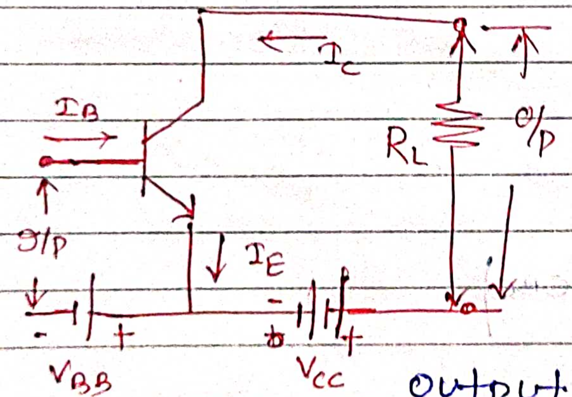
$$= \alpha(I_C + I_B) + I_{CBO}$$

$$\Rightarrow I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$\Rightarrow I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$\Rightarrow \boxed{I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}} \quad \text{— (4)}$$

b) Common-emitter →



* Emitter is connected between C & B hence its name is Common emitter.
* Input ckt is connected between E & B and output ckt is taken from the C & E.

* Current amplification factor is defined as the ratio of the o/p & i/p Current in a CE configurⁿ.

* In CE amplification, the o/p current is I_C & I/p current is I_B.

$$\boxed{\beta = \frac{I_C}{I_B}}$$

$$\alpha = \frac{I_C}{I_E} = \frac{I_C}{I_C + I_B}, \quad \beta = \frac{I_C}{I_B}$$

By dividing I_B in numerator & denominator,

$$\alpha = \frac{(I_C/I_B)}{\left(\frac{I_C + I_B}{I_B}\right)} = \frac{\beta}{1+\beta}$$

$$\Rightarrow \boxed{\alpha = \frac{\beta}{1+\beta}}$$

$$\beta = \frac{I_C}{I_B} = \frac{I_C}{I_E - I_C}$$

Dividing by I_E,

$$\beta = \frac{(I_C/I_E)}{\left(\frac{I_E - I_C}{I_E}\right)} \Rightarrow \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

We know that,

$$I_C = \alpha I_E + I_{CBO}$$

$$= \alpha(I_C + I_B) + I_{CBO}$$

$$\Rightarrow I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$\Rightarrow \boxed{I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}}$$

In CE configuration,

$\left(\frac{1}{1-\alpha}\right) I_{CBO}$ is denoted as I_{CEO}

$$\left(\frac{1}{1-\alpha}\right) I_{CBO} = I_{CEO}$$

where I_{CEO} is the current from collector to emitter when base is open.

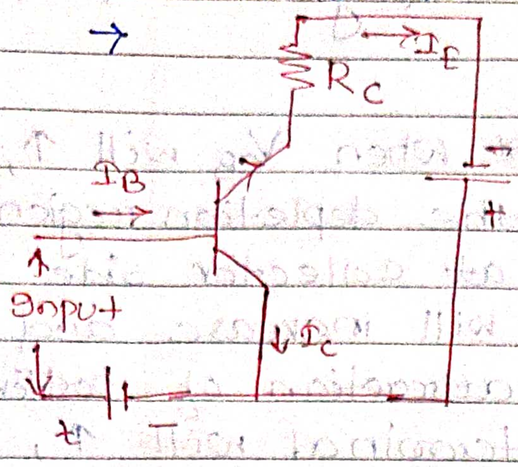
$$\boxed{I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + I_{CEO}}$$

5).

c) Common-collector →

→ Collector is common betⁿ E & B i.e.

→



* It's defined as the ratio of the o/p current to i/p current.

* $\boxed{\gamma = \frac{I_E}{I_B}}$

* $I_E = I_C + I_B$

→ $I_B = I_E - I_C$

$$\gamma = \frac{I_E}{I_E - I_C}$$

by dividing I_E in numerator & denominator

$$= \frac{(I_E / I_E)}{\left(\frac{I_E - I_C}{I_E}\right)} = \frac{1}{1-\alpha} \Rightarrow \boxed{\gamma = \frac{1}{1-\alpha}}$$

Relationship betⁿ α, β & γ →

$$\alpha = \frac{I_C}{I_E}, \quad \beta = \frac{I_C}{I_B}, \quad \gamma = \frac{I_E}{I_B}$$

$$\gamma = \frac{1}{1-\left(\frac{\beta}{1+\beta}\right)} = \frac{1+\beta}{1+\beta-\beta} \Rightarrow \boxed{\gamma = 1+\beta}$$

$$\beta = \frac{\alpha}{1-\alpha} = \alpha\left(\frac{1}{1-\alpha}\right) = \alpha \cdot \gamma$$

$$\boxed{\beta = \alpha\gamma}$$

Current-Voltage characteristics →

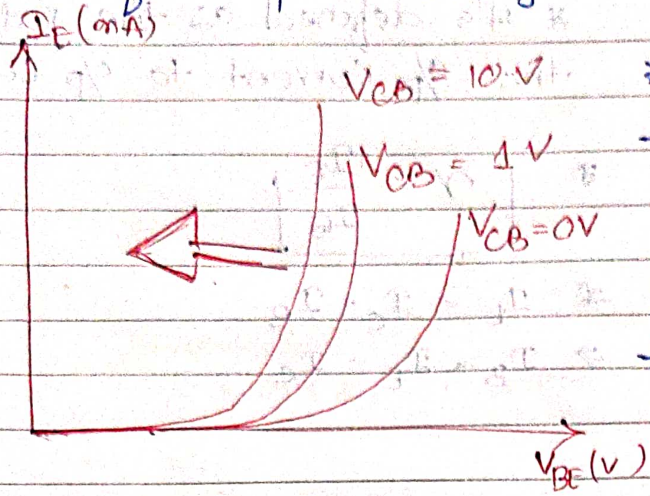
The V-I characteristics is depending on i/p & o/p Parameters :-

i) Input characteristic

ii) Output

In CB Configuration,

i) Input char. :→ It's the curve between i/p current & i/p voltage by taking constant value of output voltage.

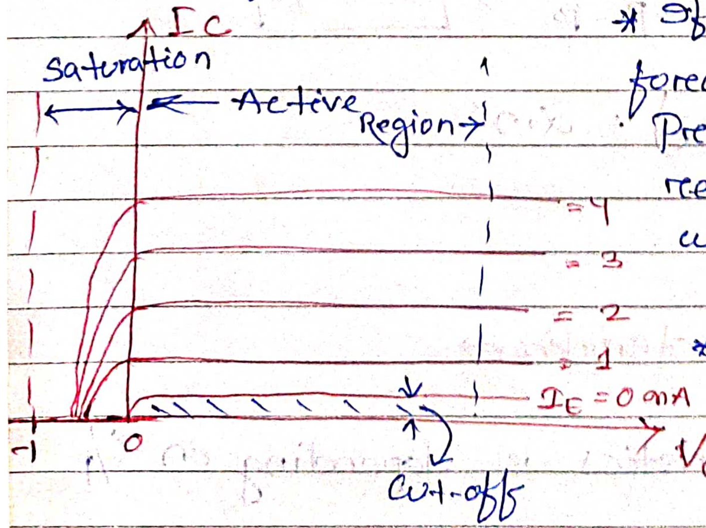


* When V_{CB} will ↑, the depletion region at collector side will increase and attraction of positive terminal will ↑, the movement the charge carrier.

↳ Due to the large no. of charge carrier at Collector side, I_C will increase. Then $\lfloor I_E = I_C \rfloor$, Hence, I_E will ↑. So, in the input char. the curves will move to inward or towards y-axis (I_E).

Input R = $\frac{\Delta V_{BE}}{\Delta I_E}$ (Quite Small)

ii) Output char :- At o/p char, the curve is bet^n o/p voltage & o/p Current by taking constant value of I_E.



* If $I_E=0$ i.e when no forward current is Present, then due to the reverse-bias CBJ I_{CO} will flow across junction.

* $I_E \simeq I_C$. So $I_C=0$, it's Known as cut-off region.

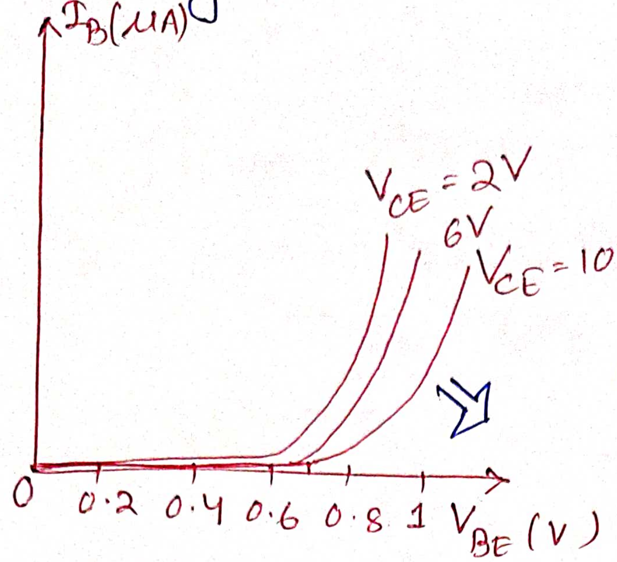
When values of V_{CB} is increased, the I_C becomes Constant as indicated by straight horz. Curves.

→ I_C is independent of V_{CB} & depends on I_E.

6.

In Common-emitter,

a) Input char :→ Graph between V_{BE} & I_B by taking constant value of V_{CE}.



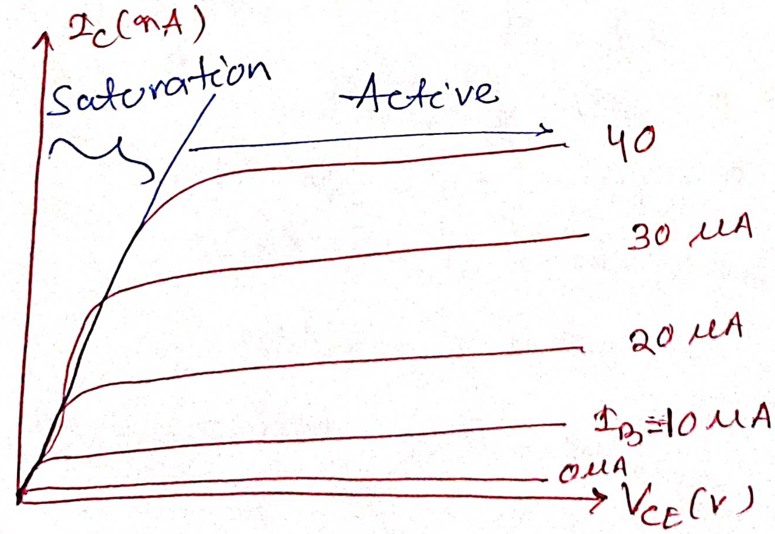
→ I_B ↑ with the increase in V_{BE}.

→ When V_{BE} & V_{CE} both are 0V, No Current is present in the circuit.

The ratio of change in V_{BE} to the change in base current at constant V_{CE} is known as input resistance.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at const. } V_{CE}$$

b) Output char :- The curve is in betn I_C & V_{CE} at a const. I_B is called o/p char in CE conf.



As $\beta = \frac{I_C}{I_B}$

$I_C >> I_B$

i.e $\boxed{\beta >> 1}$

So, o/p char. will not give linear graph.

*

7

1) In a transistor $I_C = 0.98\,mA$, $I_B = 20\,\mu A$. find
i) I_E ii) α, β

i) $I_E = I_C + I_B$

$= (0.98 \times 10^{-3}) + (20 \times 10^{-6})$

$= 1\,mA$

ii) $\beta = \dfrac{I_C}{I_B}$

$= \dfrac{0.98\,mA}{20\,\mu A}$

$= 0.049 \times 10^{3}$

$= 49$

$\alpha = \dfrac{I_C}{I_E}$

$= \dfrac{0.98\,mA}{1\,mA}$

$= 0.98$

2) In a CB connection, Current amplification factor is 0.9. If the emitter current is 1 mA, find the value of I_B.

$\alpha = 0.9$, $I_E = 1\,mA$

$\alpha = \dfrac{I_C}{I_E} \Rightarrow I_C = \alpha I_E = 0.9 \times 1 = 0.9\,mA$

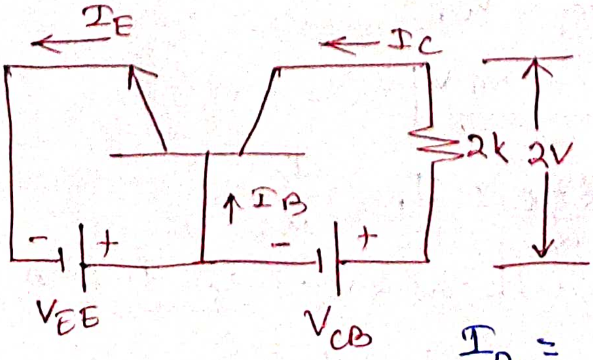
$I_B = I_E - I_C = 1 - 0.9 = 0.1\,mA$

3) In CB, $I_C = 0.95\,mA$, $I_B = 0.05\,mA$. find α.

$I_E = I_B + I_C = 0.05 + 0.95 = 1\,mA$

$\alpha = I_C / I_E = 0.95/1 = 0.95$

4) In a CB Connection $\alpha = 0.95$. The voltage drop across $2\,k\Omega$ resistance which is connected in the collector is 2V. find the base current.



$\alpha = 0.95$

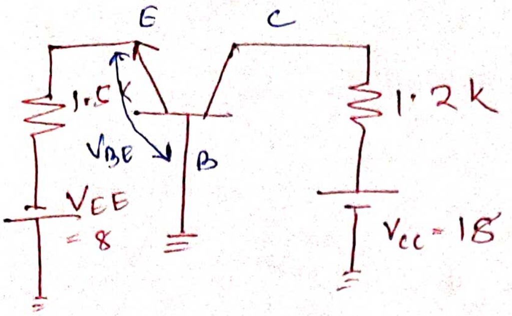
$I_C = \dfrac{2V}{2k} = 1\,mA$

$\alpha = \dfrac{I_C}{I_E} \Rightarrow I_E = \dfrac{1}{0.95}$

$= 1.05\,mA$

$I_B = I_E - I_C = 1.05 - 1 = 0.05\,mA$

5) For the CB circuit, determine I_C & V_{CB}. Assume the transistor to be of Si.



Since the transistor is Si,

$$V_{BE} = 0.7 \text{ E}$$

Applying KVL,

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

$$\Rightarrow V_{BE} + I_E R_E = V_{EE}$$

$$\Rightarrow I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{8 - 0.7}{1.5K} = 4.87 \text{ mA}$$

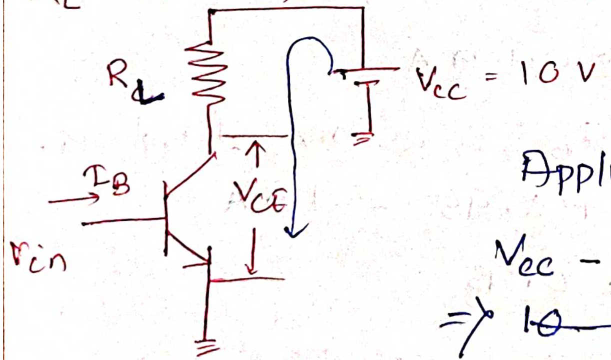
$$\underline{I_C \simeq I_E = 4.87 \text{ mA}}$$

$$V_{CC} \simeq I_C R_C + V_{CB}$$

$$\Rightarrow V_{CB} = V_{CC} - I_C R_C = 18 - (4.87 \times 10^{-3} \times 1.2 \times 10^{+3})$$

$$= 12.16 \text{V}$$

6) A transistor is Connected in CE Confⁿ. where $V_{CC} = 10$V, $R_L = 1$ KΩ, Voltage drop across $R_L = 2.2$V, $\alpha = 0.98$. Determine V_{CE} & I_B.



$V_{CC} = 10$V

$R_L = 1$ K

Applying KVL in o/p side,

$$V_{CC} - I_C R_L - V_{CE} = 0$$

$$\Rightarrow \cancel{10 - I_C \cdot 1k - V_{CE} = 0}$$

$$\Rightarrow V_{CC} - V_L - V_{CE} = 0$$

$$\Rightarrow 10 - 2.2 = V_{CE}$$

$$\Rightarrow \boxed{V_{CE} = 7.8 \text{V}}$$

$$\alpha = \frac{I_C}{I_E} \Rightarrow \cancel{I_E = \frac{I_C}{\alpha}} \cdot I_E = \frac{I_C}{\alpha}.$$

so $I_C R_L \doteq V_L \Rightarrow I_C \cdot 1k = 2.2\text{V} \Rightarrow \underline{I_C = 2.2 \text{mA}}$

so $I_E = \frac{2.2 \text{ mA}}{0.98} = \underline{2.244}$ $\quad I_B = I_E - I_C = 0.044$