```
library ieee;
use ieee.std_logic_1164.all;
 entity mux4_1 is
   port(
     A,B,C,D: in std_logic;
     s0,s1: in std_logic;
     z: out std_logic);
   end mux4_1;

architecture  mux4_1_logic of mux4_1 is
component mux_1
port(
     A,B: in std_logic;
     S: in std_logic;
     Y: out std_logic);
   end component;
  signal temp1,temp2 : std_logic;

begin
  u1: mux_1 port map(A,B,s0,temp1);
 u2: mux_1 port map(C,D,s0,temp2);
 u3: mux_1 port map(temp1,temp2,s1,z);
end mux4_1_logic;
```