```
Library IEEE;
use ieee.std_logic_1164.all;



entity FULL_ADDER is
port (A, B, CIN: in std_logic; SUM, COUT: out std_logic);
end FULL_ADDER;



architecture FA_mixed of FULL_ADDER is
component XOR2
port (A, B: in std_logic; Z: out std_logic);
end component;
signal S1:std_logic;
begin
X1: XOR2 port map (A, B, S1 );
SUM <= S1 xor CIN;
process (A, B, CIN)
variable T1, T2, T3: std_logic;
begin
T1 :=A and B;
T2 := B and CIN;
T3:=A and CIN;
COUT <= T1 or T2 or T3;
end process;



end FA_mixed;
```