```
library IEEE;
use IEEE.std_logic_1164.all;
entity mux_1 is
 port(
 S,A,B : in std_logic;
  Y : out std_logic);
end mux_1;
-- Architecture definition
architecture muxLogic of mux_1 is
component not_1
 port(A : in std_logic; Y:out std_logic);
 end component;
 component orgate_1
 port(A,B : in std_logic; Y :out std_logic);
 end component;
 component and_1
 port(A,B : in std_logic; Y :out std_logic);
 end component;
 signal s1,s2,s3 : std_logic;
 begin
 u1: not_1 port map(S,s1);
 u2: and_1 port map(s1,A,s2);
 u3: and_1 port map(B,S,s3);
 u4: orgate_1 port map(s3,s2,Y);
end muxLogic;
```