## C:/altera/90/modelsim\_ase/examples/Halfadder.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
entity halfadder is
  port(A,B : in std_logic; sum,carry :out std_logic);
end halfadder;
-- Architecture definition
architecture halfadderLogic of halfadder is
  begin
sum <= A xor B;
carry <= A and B;
end halfadderLogic;</pre>
```

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