```
library IEEE;
use IEEE.std_logic_1164.all;
entity kesh_decod1 is
 port(
      A: in std_logic;
      B: in std_logic;
      D0,D1,D2,D3:out std_logic);
end kesh_decod1;
-- Architecture definition
architecture keshav_decod_Logic of  kesh_decod1 is
component not_1
 port(A: in std_logic; Y:out std_logic);
 end component;
 component And_2
 port(A,B : in std_logic; Y :out std_logic);
 end component;
 signal s0,s1:std_logic;
 begin
 u1: not_1 port map(A,s0);
 u2: not_1 port map(B,s1);
 u3: And_2 port map(s0,s1,D0);
 u4: And_2 port map(s0,B,D1);
 u5: And_2 port map(A,s1,D2);
 u6: And_2 port map(A,B,D3);
end keshav_decod_Logic;
```