```
library IEEE;
use IEEE.std_logic_1164.all;
entity fulladder is
 port(A,B,C : in std_logic; sum,carry :out std_logic);
end fulladder;
-- Architecture definition
architecture fulladderLogic of fulladder is
component halfadder
 port(A,B : in std_logic; sum, carry :out std_logic);
 end component;
 component orgate_1
 port(A,B : in std_logic; Y :out std_logic);
 end component;
 signal s1,s2,s3 : std_logic;
 begin
 u1: halfadder port map(A,B,s1,s2);
 u2: halfadder port map(s1,C,sum,s3);
 u3: orgate_1 port map(s3,s2,carry);
end fulladderLogic;
```