```
Library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity BPS4 is
port( A,B: in std_logic_vector(3 downto 0);
sum: out std_logic_vector(3 downto 0);
Cin : in std_logic;
Cout: out std_logic);
end BPS4;
architecture arc_BPS4 of BPS4 is
component fulladder
port( a,b,c: in std_logic;
sum, carry: out std_logic);
End component;
signal c1, c2, c3 : std_logic;
signal TMP : std_logic_vector(3 downto 0);

begin
 TMP <= ((not(B)) + "0001");
U0: fulladder port map(A(0),TMP(0), Cin, sum(0),c1);
U1: fulladder port map(A(1),TMP(1), c1, sum(1),c2);
U2: fulladder port map(A(2),TMP(2), c2, sum(2),c3);
U3: fulladder port map(A(3),TMP(3), c3, sum(3),Cout);
end arc_BPS4;
```