```
library IEEE;
use IEEE.std_logic_1164.all;
entity fullsub is
 port(A,B,Bin : in std_logic; Dout,Bout :out std_logic);
end fullsub;
-- Architecture definition
architecture fullsubLogic of fullsub is
component halfsub
 port(A,B : in std_logic; D,BO :out std_logic);
 end component;
 component orgate_1
 port(A,B : in std_logic; Y :out std_logic);
 end component;
 signal s1,s2,s3 : std_logic;
 begin
 u1: halfsub port map(A,B,s1,s2);
 u2: halfsub port map(s1,Bin,Dout,s3);
 u3: orgate_1 port map(s3,s2,Bout);
end fullsubLogic;
```