```
Library ieee;
use ieee.std_logic_1164.all;
entity mul_2 is
port( A,B: in std_logic_vector(1 downto 0);
p: out std_logic_vector(3 downto 0)
);
end mul_2;
architecture arc_mul_2 of mul_2 is
component halfadder
port( A,B: in std_logic;
sum, carry: out std_logic);
End component;
component And_2
port( A,B: in std_logic;
Y: out std_logic);
End component;

signal s1, s2, s3,c1 : std_logic;
begin
U0: And_2 port map(A(0),B(0),p(0));
U1:  And_2 port map(A(1),B(0), s1);
U2: And_2 port map(A(0),B(1), s2);
U3: halfadder port map(s1,s2,p(1),c1);
U5: And_2 port map(A(1),B(1),s3);
U6: halfadder port map(s3,c1,p(2),p(3));
end arc_mul_2;
```