```
library IEEE;
use IEEE.std_logic_1164.all;
entity fulladder is
 port(A,B,C : in std_logic; sum,carry :out std_logic);
end fulladder;
-- Architecture definition
architecture fulladderLogic of fulladder is
signal X,Y,Z: std_logic;
 begin
 X <= A XOR B;
 sum <= X XOR C;
  Y <= X and C;
  Z <= A and B;
 carry<= Y OR Z;

end fulladderLogic;
```