```
library ieee;
use ieee.std_logic_1164.all;
entity kesh_encod1 is
  port(
    D: in std_logic_vector(3 downto 0);
    A,B:out std_logic);
end kesh_encod1;
architecture kesh_encod_Logic of kesh_encod1 is
component or_1
  port(
    A,B:in std_logic;
    Y:out std_logic);
end component;
  begin
u1:or_1 port map(D(2),D(3),A);
u2:or_1 port map(D(1),D(3),B);
end kesh_encod_Logic;
```