```
library ieee;
use ieee.std_logic_1164.all;

entity halfbi is
port(a, b : in bit;
sum, carry : out bit);
end halfbi;

architecture halfa2 of halfbi is
begin
p1: process(a,b)
begin
if a & b = "00" then
sum <= '0';
carry <= '0';
elsif a & b = "01" or a & b = "10" then
sum <= '1';
carry <= '0';
else
sum <= '0';
carry <= '1';
end if;
end process;
end halfa2;
```