```
library IEEE;
use IEEE.std_logic_1164.all;

entity halfadder is
 port(A,B : in std_logic; sum,carry :out std_logic);

end  halfadder;
-- Architecture definition
architecture halfadderLogic of halfadder is
component Xor_1
   port(A,B : in std_logic; Y :out std_logic);
 end component;
 component And_1
   port(A,B : in std_logic;  Y :out std_logic);
 end component;
 begin
 u1: Xor_1 port map(A,B,sum);
 u2: And_1 port map(A,B,carry);
end halfadderLogic;
```