```
library IEEE;
use IEEE.std_logic_1164.all;
entity half_sub is
 port(A,B : in std_logic; D,BO :out std_logic);
end half_sub;
-- Architecture definition
architecture half_subLogic of half_sub is
component xor_1
 port(A,B : in std_logic; Y :out std_logic);
 end component;
 component and_1
 port(A,B : in std_logic; Y :out std_logic);
 end component;
 component not_1
   port(A : in std_logic;
    Y: out std_logic);
end component;
signal s: std_logic;
 begin
 u1: xor_1 port map(A,B,D);
 u2: not_1 port map(A,s);
 u3: and_1 port map(s,B,BO);
end half_subLogic;
```