```
library IEEE;
use IEEE.std_logic_1164.all;
entity kesh_multi1 is
 port(
      A: in std_logic_vector ( 1 downto 0);
      B: in std_logic_vector ( 1 downto 0);
      C :out std_logic_vector (3 downto 0));
end kesh_multi1;
-- Architecture definition
architecture keshav_multi_Logic of  kesh_multi1 is
component halfadder
 port(A,B : in std_logic; sum,carry:out std_logic);
 end component;
 component And_2
 port(A,B : in std_logic; Y :out std_logic);
 end component;
 signal s0,s1,s2,s3:std_logic;
 begin
 u1: And_2 port map(A(0),B(0),C(0));
 u2: And_2 port map(A(0),B(1),s0);
 u3: And_2 port map(A(1),B(0),s1);
 u4: halfadder port map(s0,s1,C(1),s3);
 u5: And_2 port map(A(1),B(1),s2);
 u6: halfadder port map(s2,s3,C(2),C(3));
end keshav_multi_Logic;
```