```
library IEEE;
use IEEE.std_logic_1164.all;

-- Entity declaration

entity And_2 is

    port(A : in std_logic;      -- AND gate input
         B : in std_logic;      -- AND gate input
         Y : out std_logic);    -- AND gate output

end And_2;

-- Architecture definition

architecture andLogic of And_2 is

 begin

    Y <= A AND B;

end andLogic;
```