

```
library IEEE;
use IEEE.std_logic_1164.all;
entity halfadder is
  port(A,B : in std_logic; sum,carry :out std_logic);
end halfadder;
-- Architecture definition
architecture halfadderLogic of halfadder is
  begin
    sum <= A xor B;
    carry <= A and B;
  end halfadderLogic;
```