8051 Microcontroller: Organization

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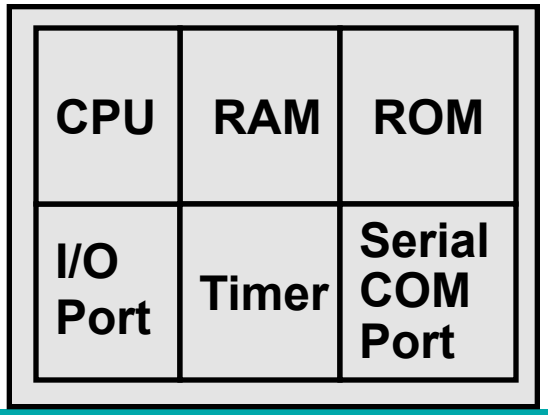
EE-309: Microprocessors

Lecture 4 (27 July 2014)

CADSL

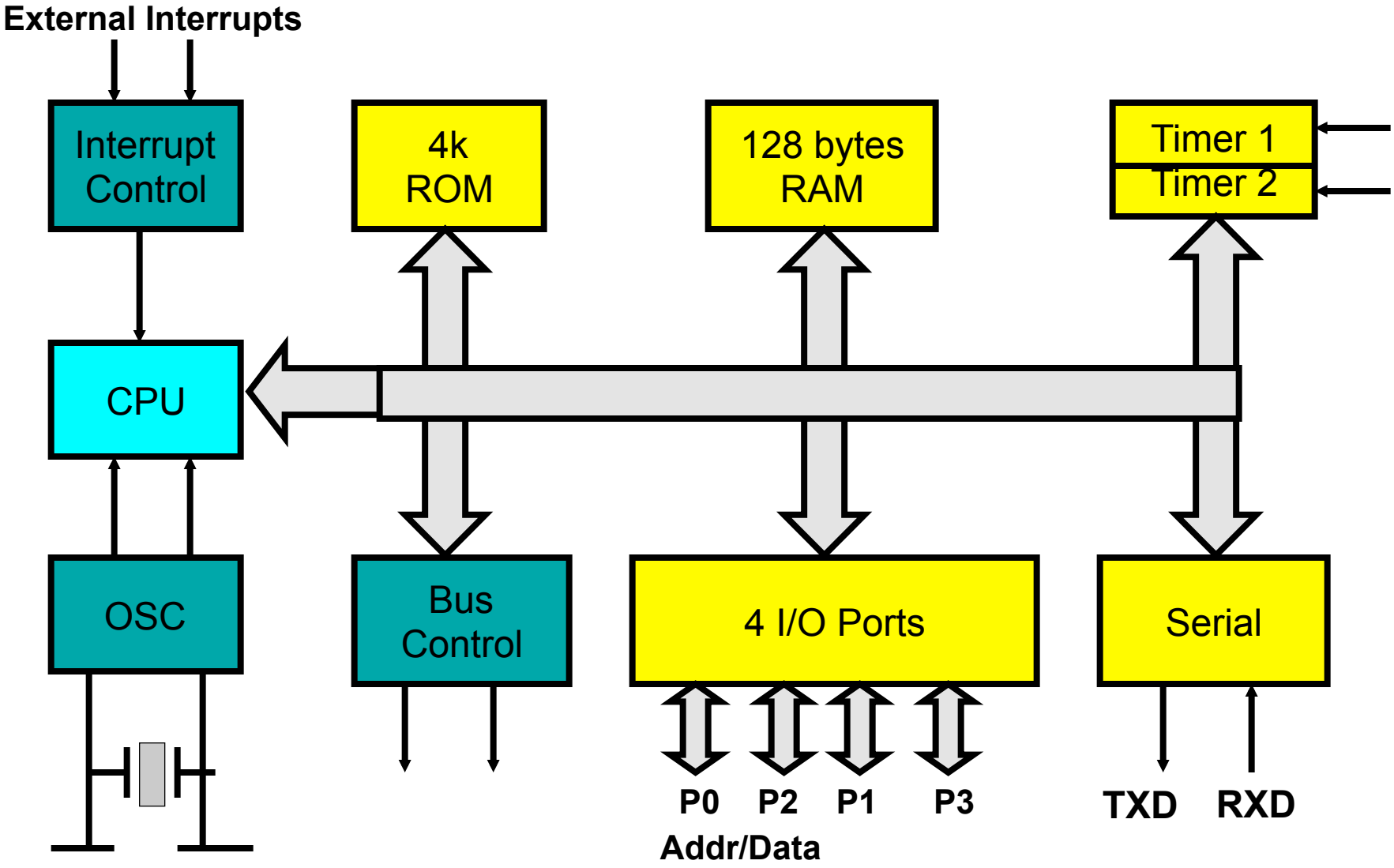
8051 Basic Component

- 4K bytes internal ROM
- 128 bytes internal RAM
- Four 8-bit I/O ports (P0 - P3).
- Two 16-bit timers/counters
- One serial interface



A single chip Microcontroller

Block Diagram

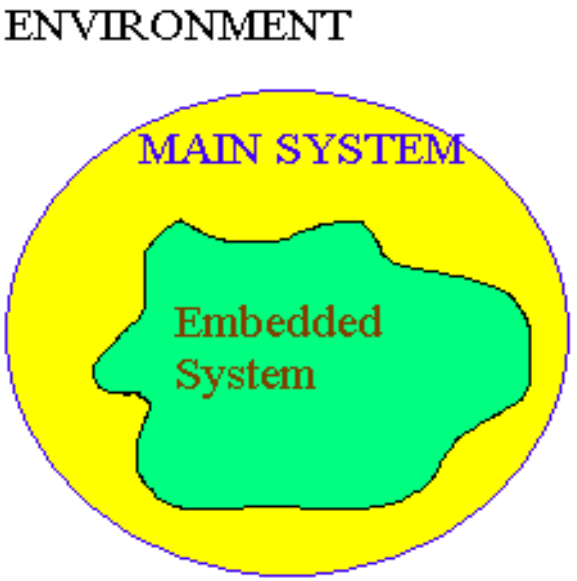


Other 8051 features

- only 1 On chip oscillator (external crystal)
- 6 interrupt sources (2 external , 3 internal, Reset)
- 64K external code (program) memory(only read)PSEN
- 64K external data memory(can be read and write) by RD,WR
- Code memory is selectable by EA (internal or external)
- We may have External memory as data and code

Embedded System
(8051 Application)

- An embedded system is closely integrated with the main system
- It may not interact directly with the environment
- For example – A microcomputer in a car ignition control



❖ An embedded product uses a microprocessor or microcontroller to do one task only

❖ There is only one application software that is typically burned into ROM

Criteria for Choosing a Microcontroller

- meeting the computing needs of the task efficiently and cost effectively
  - speed, the amount of ROM and RAM, the number of I/O ports and timers, size, packaging, power consumption
  - easy to upgrade
  - cost per unit
- availability of software development tools
  - assemblers, debuggers, C compilers, emulator, simulator, technical support
- wide availability and reliable sources of the microcontrollers

Comparison of the 8051 Family Members

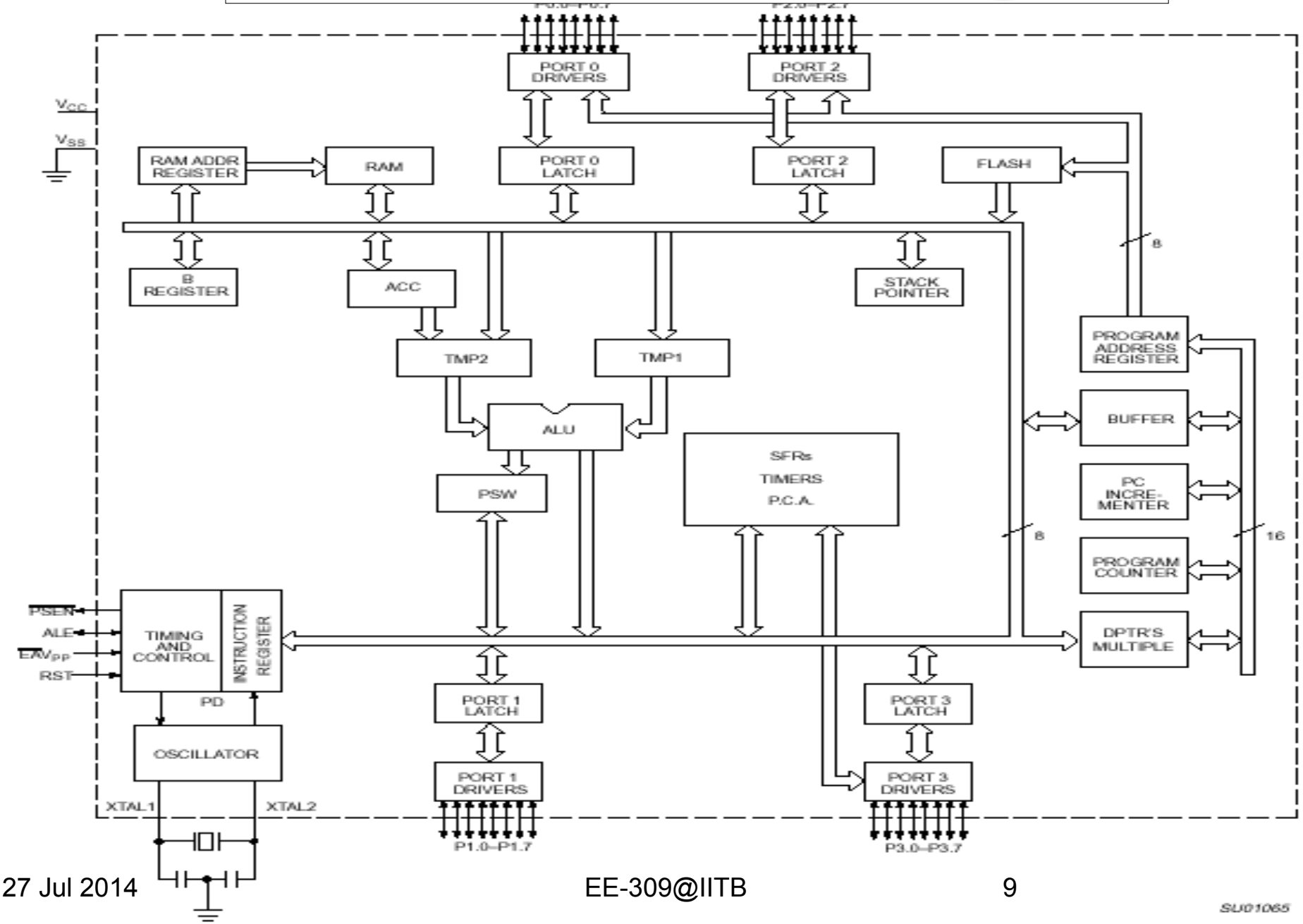
- ROM type
  - 8031 no ROM
  - 80xx mask ROM
  - 87xx EPROM
  - 89xx Flash EEPROM
- 89xx
  - 8951
  - 8952
  - 8953
  - 8955
  - 898252
  - 891051
  - 892051
- Example (AT89C51,AT89LV51,AT89S51)
  - AT= ATMEL(Manufacture)
  - C = CMOS technology
  - LV= Low Power(3.0v)

Comparison of the 8051 Family Members

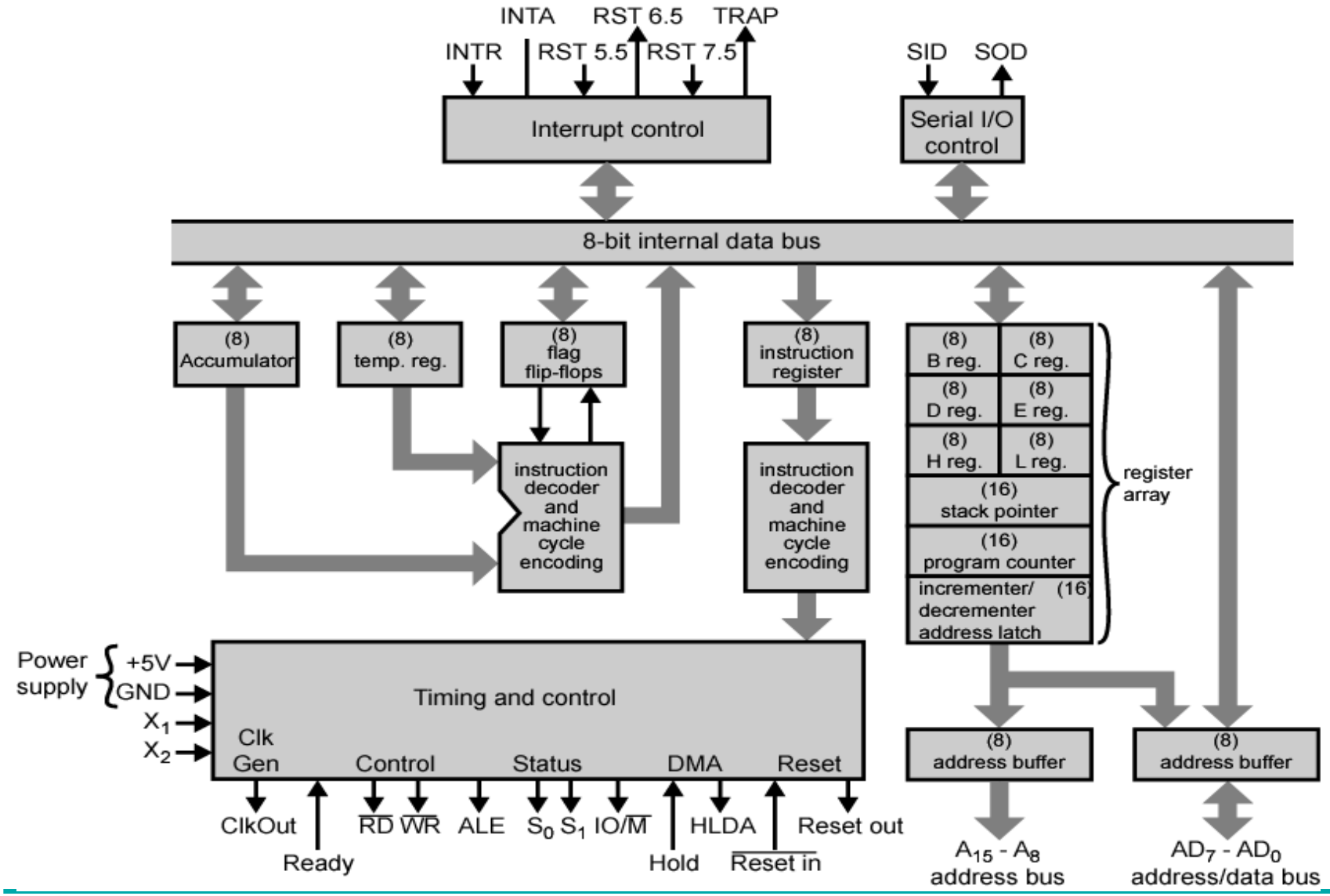
89XX	ROM	RAM	Timer	Int Source	IO pin	Other
8951	4k	128	2	6	32	-
8952	8k	256	3	8	32	-
8953	12k	256	3	9	32	WD
8955	20k	256	3	8	32	WD
898252	8k	256	3	9	32	ISP
891051	1k	64	1	3	16	AC
892051	2k	128	2	6	16	AC

WD: Watch Dog Timer
AC: Analog Comparator
ISP: In System Programable

8051 Internal Block Diagram



Intel 8085 CPU Block Diagram



8051 Schematic Pin out

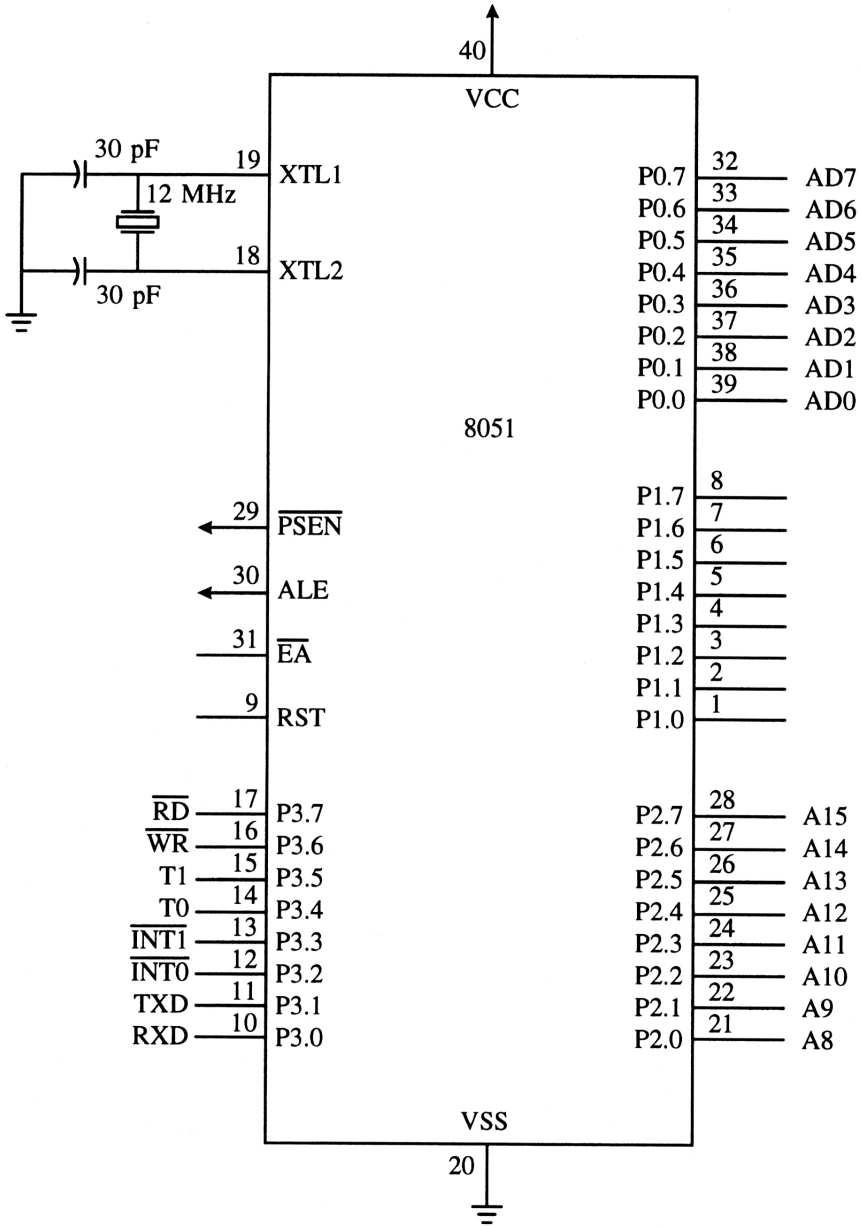
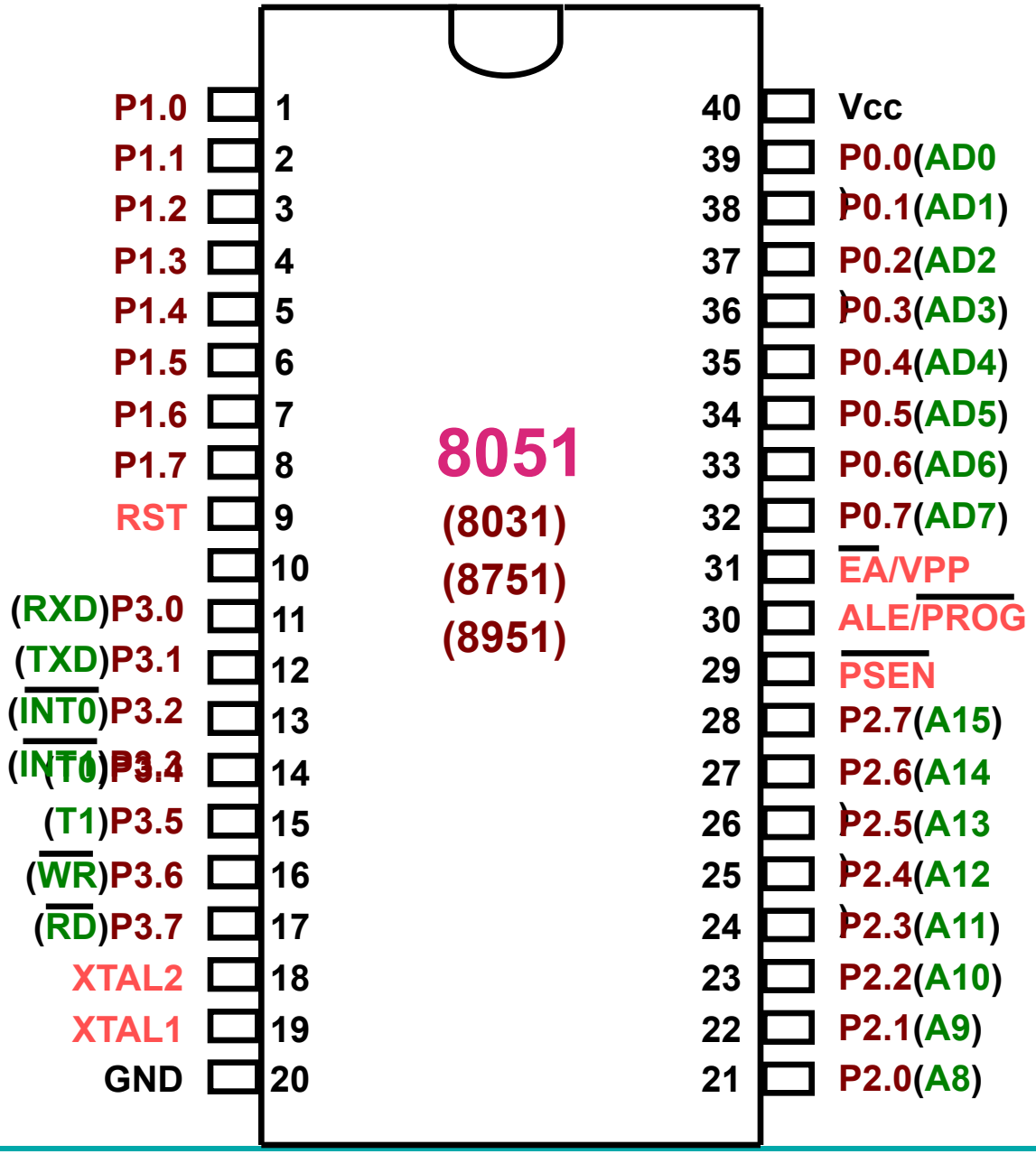


FIGURE 2–2
8051 pinouts

8051 Foot Print



Important Pins (IO Ports)

- **One of the most useful features of the 8051 is that it contains four I/O ports (P0 - P3)**

- Port 0 （pins 32-39）：P0（P0.0～P0.7）
  - 8-bit R/W - General Purpose I/O
  - Or acts as a multiplexed low byte address and data bus for external memory design
- Port 1 （pins 1-8） ：P1（P1.0～P1.7）
  - Only 8-bit R/W - General Purpose I/O
- Port 2 （pins 21-28）：P2（P2.0～P2.7）
  - 8-bit R/W - General Purpose I/O
  - Or high byte of the address bus for external memory design
- Port 3 （pins 10-17）：P3（P3.0～P3.7）
  - General Purpose I/O
  - if not using any of the internal peripherals (timers) or external interrupts.
- **Each port can be used as input or output (bi-direction)**

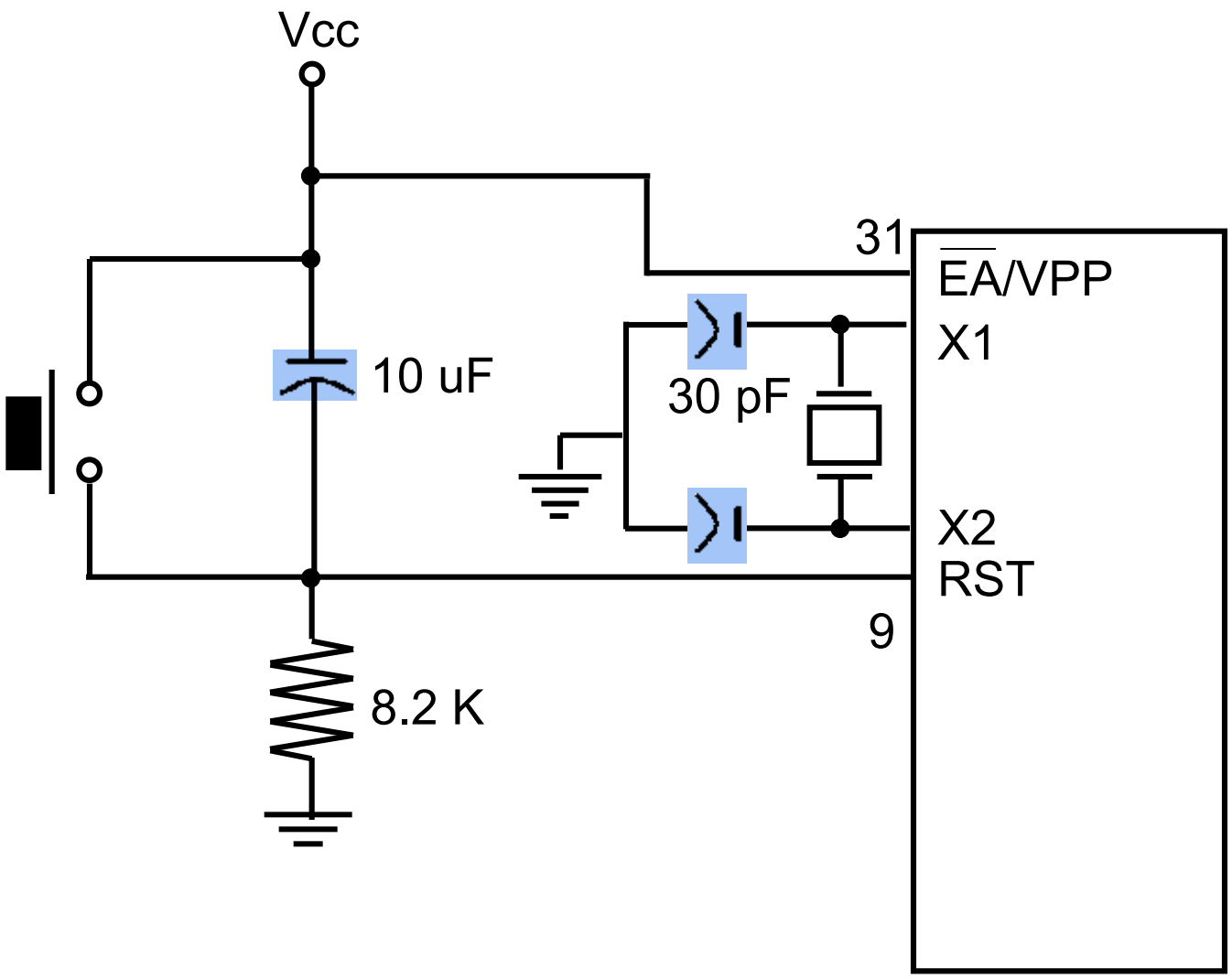
Port 3 Alternate Functions

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

Pins of 8051

- RST(pin 9)：reset
  - input pin and active high (normally low)
    - The high pulse must be high at least 2 machine cycles.
  - power-on reset
    - Upon applying a high pulse to RST, the microcontroller will reset and all values in registers will be lost.
    - Reset values of some 8051 registers
  - power-on reset circuit

Power-On RESET



RESET Value of Some 8051 Registers

Register	Reset Value
PC	0000
ACC	0000
B	0000
PSW	0000
SP	0007
DPTR	0000

RAM are all zero

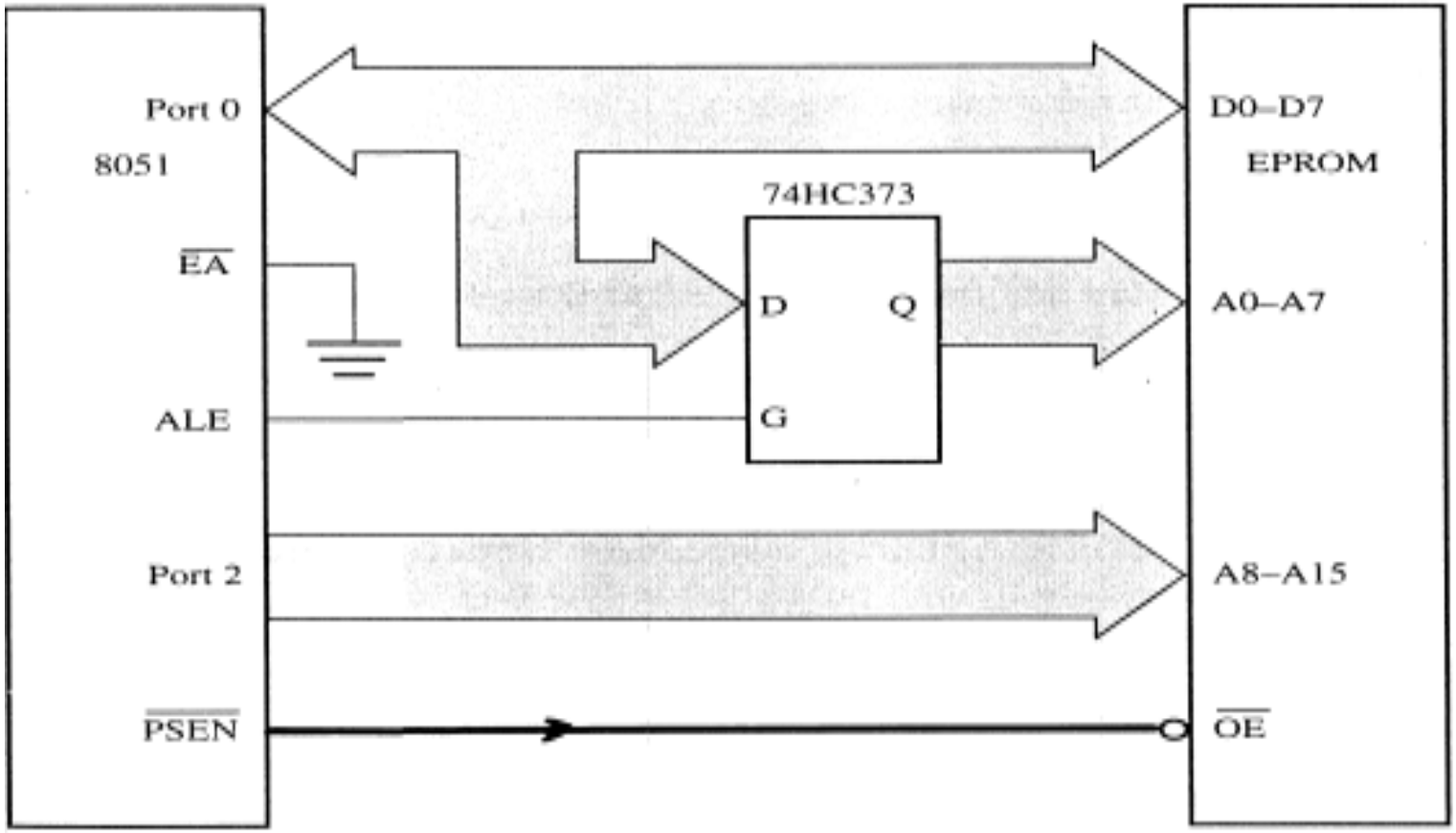
CADSL

Pins of 8051

- /EA（pin 31)：external access
  - There is no on-chip ROM in 8031 and 8032 .
  - The /EA pin is connected to GND to indicate the code is stored externally.
  - /PSEN & ALE are used for external ROM.
  - For 8051, /EA pin is connected to Vcc.
  - “/” means active low.
- /PSEN（pin 29）：program store enable
  - This is an output pin and is connected to the OE pin of the ROM.

Address Multiplexing for External Memory

Accessing external code memory



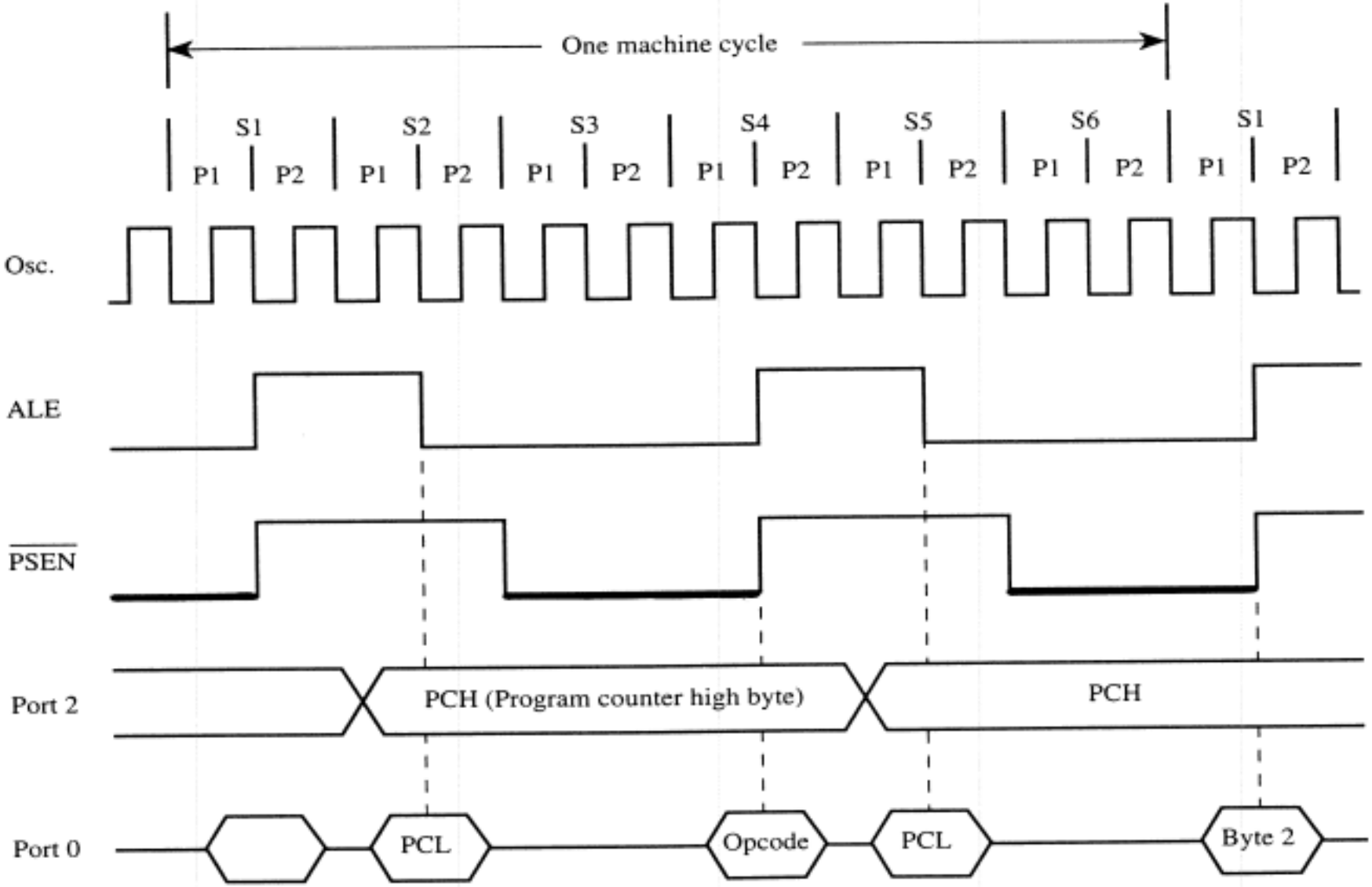


FIGURE 2–9
Read timing for external code memory

Overlapping External Code and Data Spaces

- Allows the RAM to be
  - written as data memory, and
  - read as data memory as well as **code memory**.
- This allows a program to be
  - downloaded from outside into the RAM as data, and
  - executed from RAM as code.

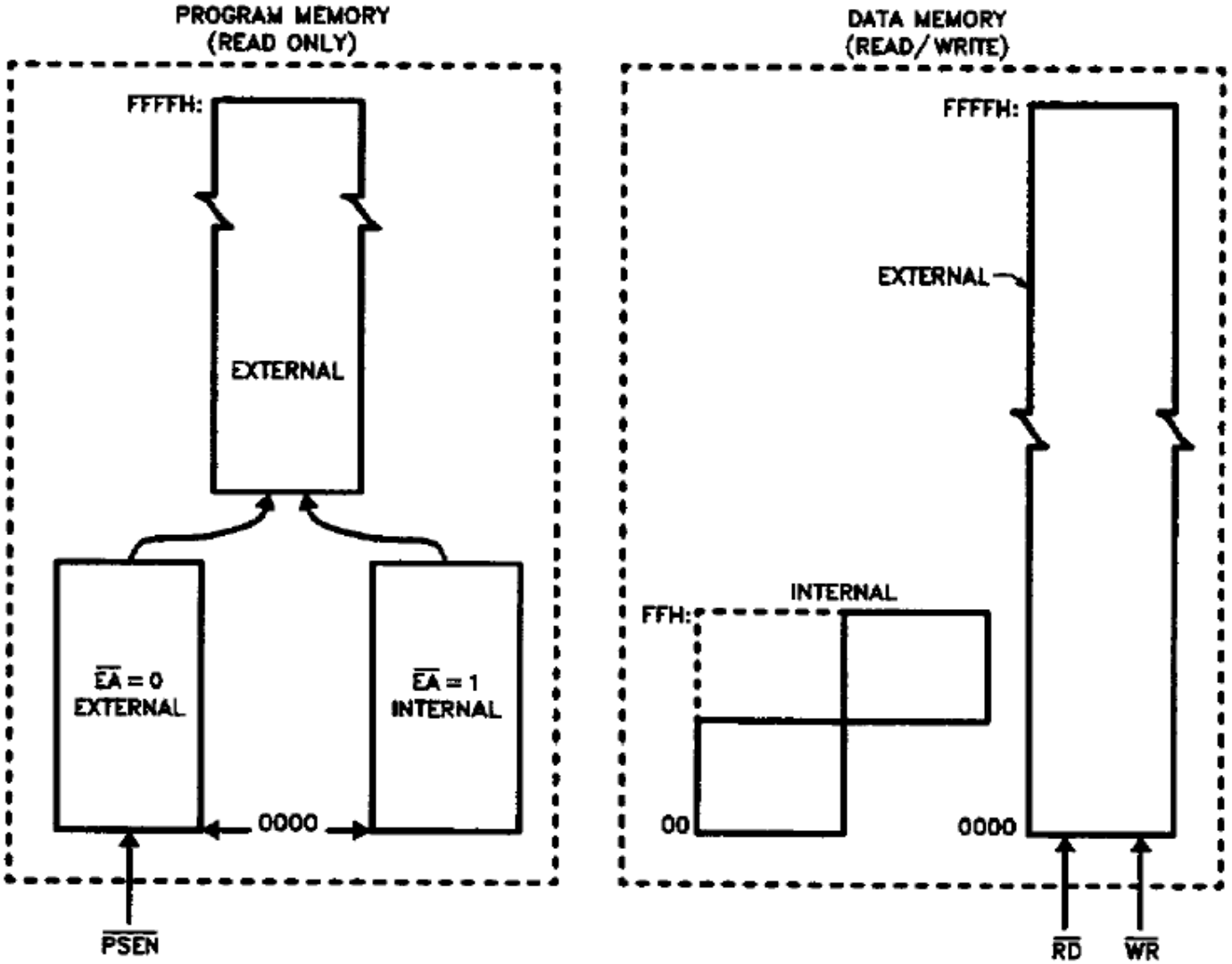
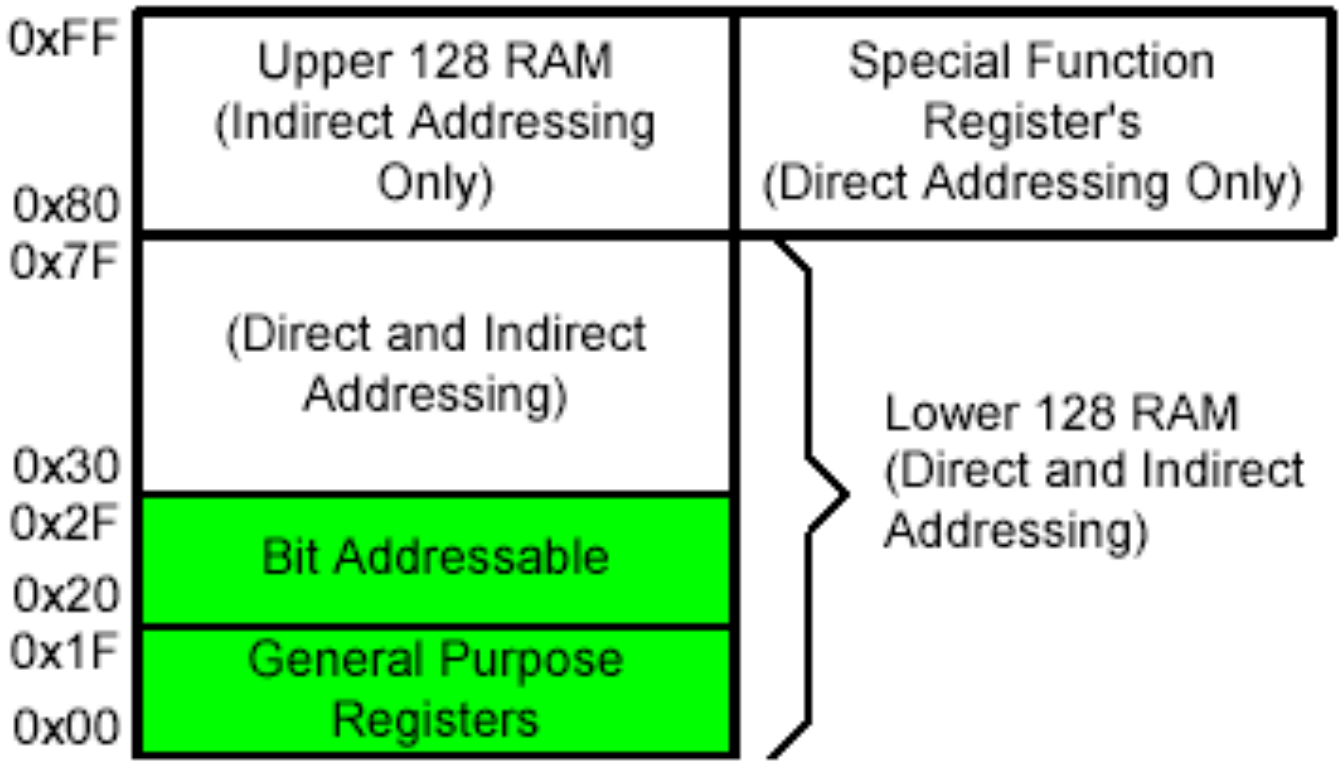
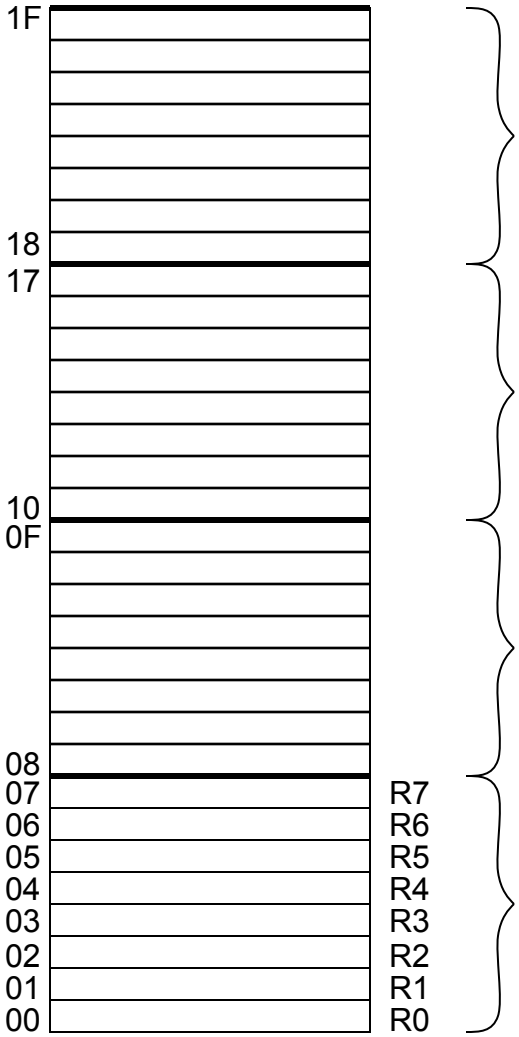


Figure 2. MCS®-51 Memory Structure

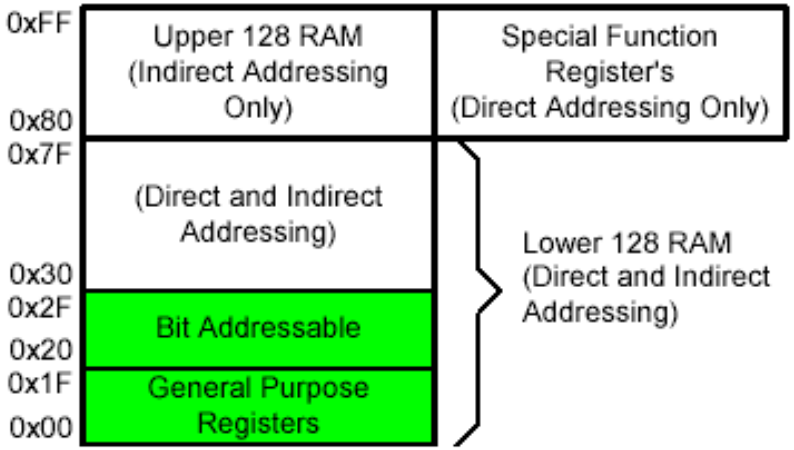
On-Chip Memory
Internal RAM



Registers



Four Register Banks
Each bank has R0-R7
Selectable by psw.2,3



Register Banks

- Active bank selected by PSW [RS1,RS0] bit
- Permits fast "context switching" in interrupt service routines (ISR).

Bit Addressable Memory

2F	7F							78
2E								
2D								
2C								
2B								
2A								
29								
28								
27								
26								
25								
24								
23						1A		
22								10
21	0F							08
20	07	06	05	04	03	02	01	00

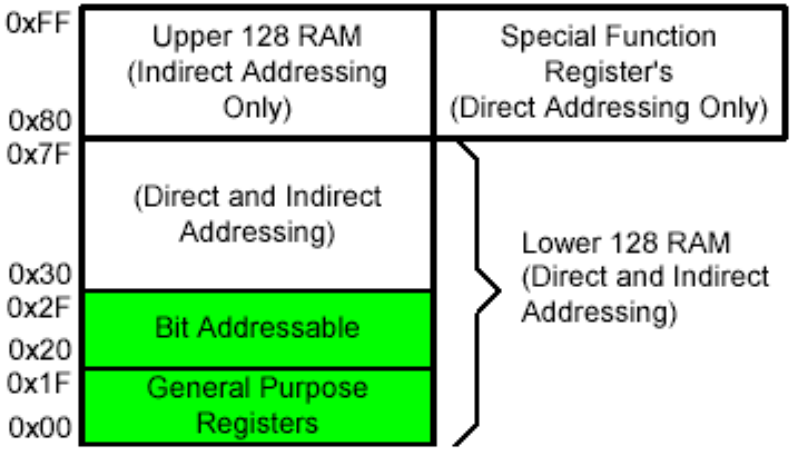
20h – 2Fh (16 locations X 8-bits = 128 bits)

Bit addressing:

mov C, 1Ah

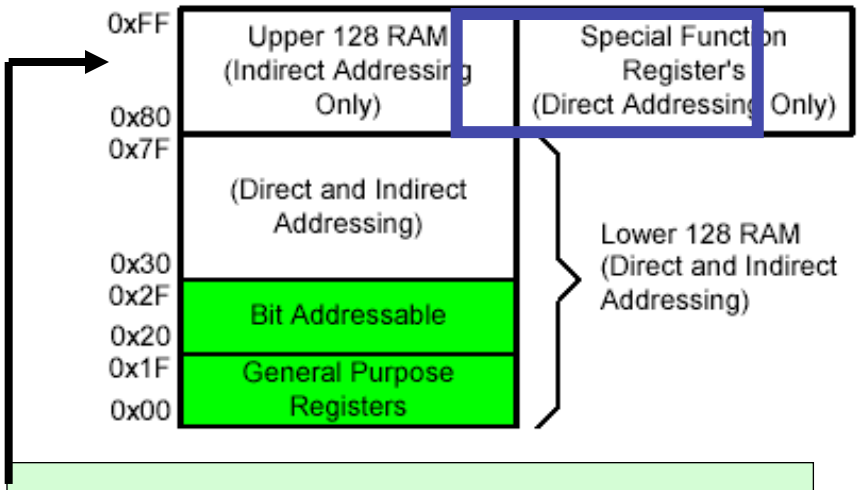
or

mov C, 23h.2



Special Function Registers

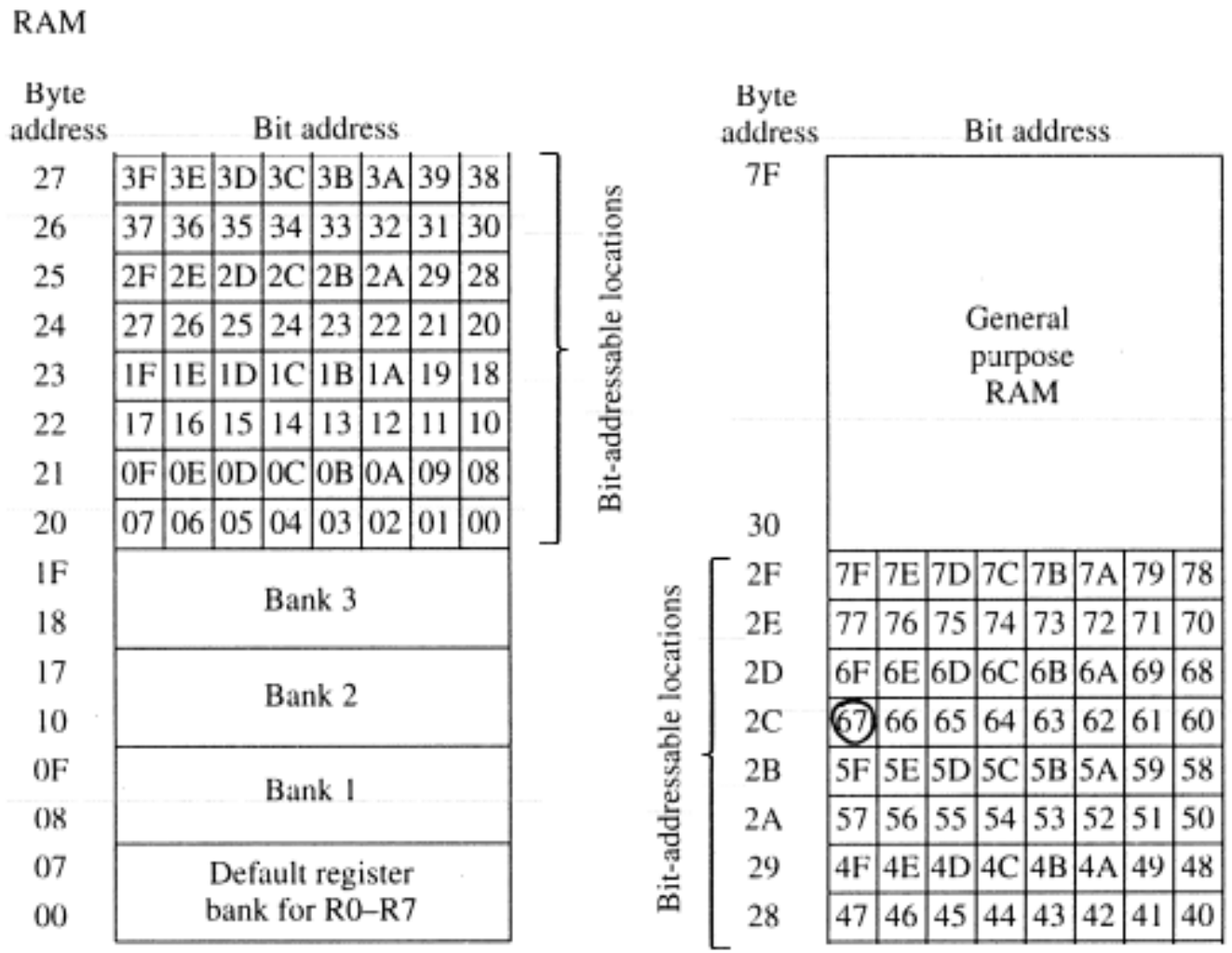
- DATA registers
- CONTROL registers
  - Timers
  - Serial ports
  - Interrupt system
  - Etc.



Addresses 80h – FFh

Direct Addressing used to access SPRs

On-chip RAM


RAM
Byte address
Bit address
27 3F 3E 3D 3C 3B 3A 39 38
26 37 36 35 34 33 32 31 30
25 2F 2E 2D 2C 2B 2A 29 28
24 27 26 25 24 23 22 21 20
23 1F 1E 1D 1C 1B 1A 19 18
22 17 16 15 14 13 12 11 10
21 0F 0E 0D 0C 0B 0A 09 08
20 07 06 05 04 03 02 01 00
Bit-addressable locations
1F
18
Bank 3
17
10
Bank 2
0F
08
Bank 1
07
00
Default register bank for R0–R7
Byte address
Bit address
7F
General purpose RAM
30
Bit-addressable locations
2F 7F 7E 7D 7C 7B 7A 79 78
2E 77 76 75 74 73 72 71 70
2D 6F 6E 6D 6C 6B 6A 69 68
2C 67 66 65 64 63 62 61 60
2B 5F 5E 5D 5C 5B 5A 59 58
2A 57 56 55 54 53 52 51 50
29 4F 4E 4D 4C 4B 4A 49 48
28 47 46 45 44 43 42 41 40

Special Function Registers

Byte address	Bit address								
98	9F	9E	9D	9C	9B	9A	99	98	SCON
90	97	96	95	94	93	92	91	90	P1
8D	not bit addressable								TH1
8C	not bit addressable								TH0
8B	not bit addressable								TL1
8A	not bit addressable								TL0
89	not bit addressable								TMOD
88	8F	8E	8D	8C	8B	8A	89	88	TCON
87	not bit addressable								PCON
83	not bit addressable								DPH
82	not bit addressable								DPL
81	not bit addressable								SP
80	87	86	85	84	83	82	81	80	P0

Byte address	Bit address								
FF									
F0	F7	F6	F5	F4	F3	F2	F1	F0	B
E0	E7	E6	E5	E4	E3	E2	E1	E0	ACC
D0	D7	D6	D5	D4	D3	D2	–	D0	PSW
B8	–	–	–	BC	BB	BA	B9	B8	IP
B0	B7	B6	B5	B4	B3	B2	B1	B0	P3
A8	AF	–	–	AC	AB	AA	A9	A8	IE
A0	A7	A6	A5	A4	A3	A2	A1	A0	P2
99	not bit addressable								SBUF

SPF: Prog. Status Word

PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

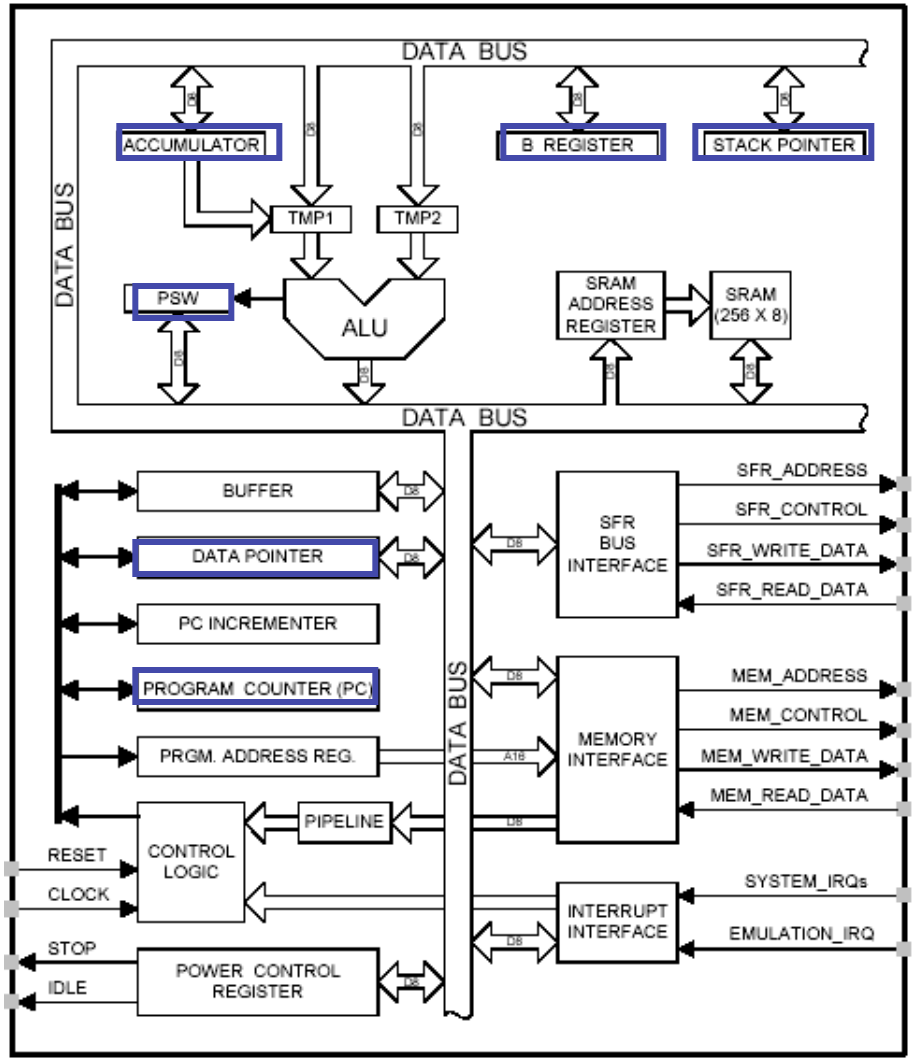
CY	AC	F0	RS1	RS0	OV	—	P

CY	PSW.7	Carry Flag.
AC	PSW.6	Auxiliary Carry Flag.
F0	PSW.5	Flag 0 available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1 (SEE NOTE 1).
RS0	PSW.3	Register Bank selector bit 0 (SEE NOTE 1).
OV	PSW.2	Overflow Flag.
—	PSW.1	User definable flag.
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of '1' bits in the accumulator.

NOTE:
1. The value presented by RS0 and RS1 selects the corresponding register bank.

RS1	RS0	Register Bank	Address
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

8051 CPU Registers



- A (Accumulator)
- B
- PSW (Program Status Word)
- SP (Stack Pointer)
- PC (Program Counter)
- DPTR (Data Pointer)

Used in assembler instructions

Thank You