Project report by:

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Introduction-

In present days we are confronting numerous issues with the current vehicle parking system. As we have to park our vehicle physically and there is no control in this procedure it makes an enormous obstacle.

Peoples can park their vehicles any places they need to, leading to unmanaged traffic. Population is growing in our country and so is the growing traffic.

So, we need a safe and secure parking system to assign the right way and minimizes the waste of time for trying to find out free parking space.

Objective-

This project is to implement a car parking system in Verilog.

As far we are progressing with time for this old car parking system, we face wastage of time and some economic losses.

Thus, we require an answer to solve this problem. The goal of this project is to give an opportunity to avoid manual car parking system.



Design-

- Our project will work using the finite state machine model.
- A finite state machine (sometimes called a finite state automaton) is a computation model that can be implemented with hardware or software and can be used to simulate <u>sequential logic</u> and some computer programs. Finite state machines can be used to model problems in many fields including mathematics, artificial intelligence, games, and linguistics.
- State machines are spoken to utilizing state charts. The yield of a state machine is an element of the information and the present state. It is easy to design and gives the designer great flexibility when the designer needs to weak the design either for speed or area optimization.

Features-

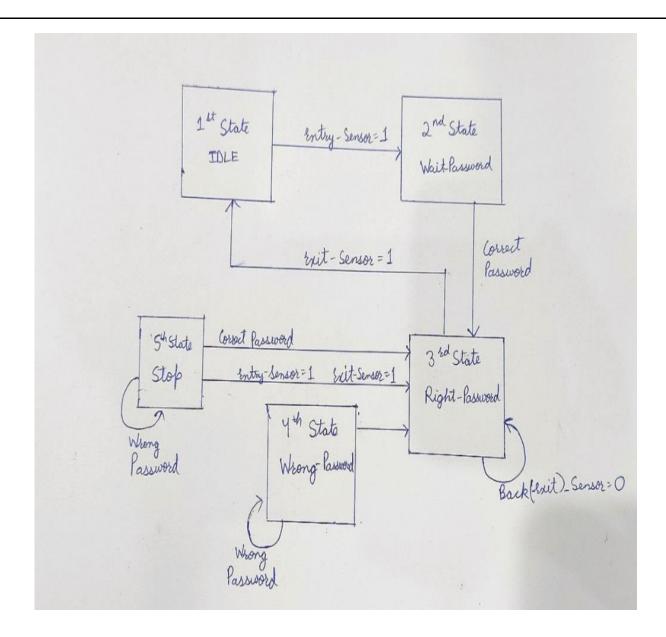
- It uses a moore machine which is a finite-state machine whose output values are determined only by its current state. This is in contrast to a Mealy machine, whose output values are determined both by its current state and by the values of its inputs.
- Model provides an efficient use of time and resources for parking.
- Use of IR Sensors: The IR Sensors gives the FPGA the pulse which considers an input to be detected. The vehicle is allowed into the parking lot only if the password is entered. If the entered password is correct then the vehicle is preceded to park or else the gate will remain closed. During exit, the IR Sensors provide the pulse to the FPGA which assumes that an input is detected and that the car is only exited from the parking lot after the password has been entered correctly.

Terminals of the state machine

Signal Name	Direction	Description
Jock	Input	Clock input to the state machine
Reset	Input	Reset elignal to reset the state machine to know state
Front Sensor	Input	Detect the coming valuables vehicles
Back Sensor	Input	Detect the car into the car park
Posswood 2	Input	Gale is opened to let the our who can pouck
Password a	Input	if pars_ s is incorrect it will there again & let the core into the core park.
Green LED	output	fsm turns to seight pass state; a concern i
Redled	output	wring pass store A if the next car is coming before parking the current car than RED LED to be blinking Display 7-segment LED
HEX 1	output	Display 7- segment LED
HEX 2	oculput	Display 7- Segment LEO

State Diagram

Each of five states is worked according to their program, as indicated by the boxes. The looping arrow at each state indicates that the system remain in that state under the condition defined by the associated expression. Each of the arrows going from one state to the next state indicates a state transition under the condition defined by the associated expression.



Module description-

- Initially, the state is Idle.If there is a vehicle coming detected by the enter sensor, State is switched to Wait for 4 cycles.
- The car will input the password in this state; if the password is correct, the gate is opened to let the car get in the car park and state turns to Right, Green LED will start blinking.
- Otherwise, state turns to Wrong, a Red LED will start blinking and it requires the car to enter the password again until the password is correct.

- When password is right the car gets into the parking zone detected by the exit sensor and there is the next car coming, The state is switched to Stop and the Red LED will be blinking so that the next car will be noticed to stop and enter the password.
- After the car passes the gate and gets into the parking area, the state returns to Idle.

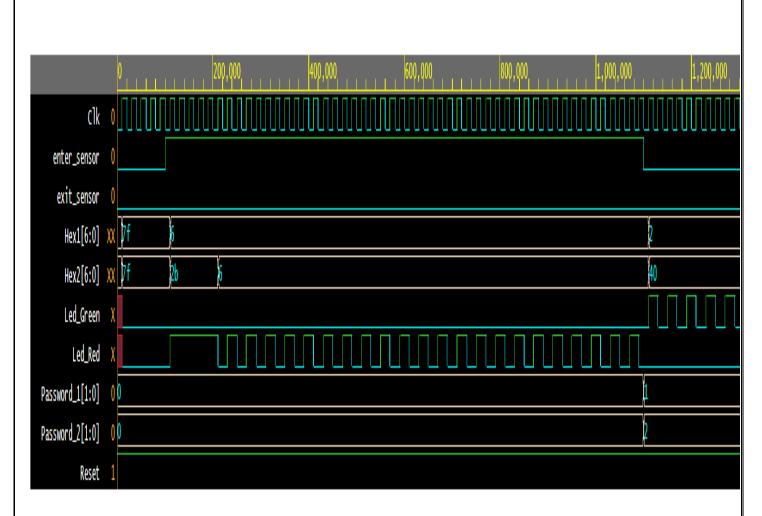
Therefore, output for car parking system is dependent on the password which is in the entry gate. The gate will open or not according to the password accurateness, FSM is used to do the whole system.

Validation-

We have added the display which helps us validating our results by showing Led's and sensor states.

```
Outputs-- Green Led: 0, Red Led: 1
Inputs--Sensor.enter: 1, Sensor.exit: 0
Inputs--Sensor.enter: 1,Sensor.exit: 0
                                         Outputs-- Green Led: O, Red Led: O
Inputs--Sensor.enter: 1, Sensor.exit: 0
                                         Outputs-- Green Led: 0.Red Led: 1
Inputs--Sensor.enter: 1,Sensor.exit: 0
                                         Outputs-- Green Led: O, Red Led: O
Inputs--Sensor.enter: 1,Sensor.exit: 0
                                         Outputs-- Green Led: 0, Red Led: 1
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                                         Outputs-- Green Led: 0, Red Led: 0
Inputs--Sensor.enter: 0,Sensor.exit: 0
Inputs--Sensor.enter: 0, Sensor.exit: 0
                                         Outputs-- Green Led: 1, Red Led: 0
                                         Outputs-- Green Led: 0, Red Led: 0
Inputs--Sensor.enter: 0,Sensor.exit: 0
Inputs--Sensor.enter: 0,Sensor.exit: 0
                                         Outputs-- Green Led: 1, Red Led: 0
```

Results-



Simulation output for car entry and exit password requirement

Conclusion-

The goal of this project was to develop an effective smart car parking system which increases productivity, reduces costs and speeds up market time. It gives security to the parking ground. Computerized car parking systems lessen the issue in parking grounds and road turned parking lot. We designed a moore fsm model for it, learnt about its features, implemented it in Verilog and verified our results. Overall, it provided a great learning experience and hopefully we can implement it in real life.