CSEN2011	COMPUTER ORGANIZATION AND	L	T	Р	S	J	С
	ARCHITECTURE	2	1	0	0	0	3
Pre-requisite	Digital Logic Circuits	•					
Co-requisite	None						
Preferable exposure	None						

# UNIT 1 Register Transfer and Micro operations:

8 hours

Register transfer language, register transfer, bus and memory transfers, arithmetic micro-operations, logic micro-operations, shift micro-operations, arithmetic logic shift unit

### UNIT 2 Basic Computer Organization and Design

11 hours

Basic Computer Organization and Design Instruction codes, computer registers, computer instructions, timing and control, instruction cycle, memory-references instructions, input-output and interrupt, complete computer description. Design ofthe basic computer, Design of accumulator logic. Micro programmed Control: Control memory, address sequencing, micro program example, Design of control unit.

### UNIT 3 Central Processing Unit

10 hours

**Central Processing Unit**: Introduction, general register organization, stack organization, instruction formats, addressing modes, data transfer and manipulation, program control.

Pipeline and Parallel Processing: Parallel processing, pipelining, arithmetic pipeline, instruction pipeline.

**Computer Arithmetic**: Introduction, addition and subtraction, decimal arithmetic unit, Booth's multiplication algorithm.

### UNIT 4 Input-Output Organization

8 hours

Peripheral devices, I/O Interface, Asynchronous Data Transfer, Modes of Transfer, Priority Interrupt, DMA, I/O Processor, Serial Communication.

## **UNIT 5** Memory Organization

8 hours

Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memories, Cache Memory, Virtual Memories, Memory Management Hardware

## TextBooks:

1. M. Morris Mano, Computer System Architecture, 3/e, Pearson education, 2008

### References:

- 1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization, 5/e, McGraw Hill, 2001
- 2. John P. Hayes, Computer Architecture and Organization, 3/e, McGraw Hill, 1998.
- 3. William Stallings, Computer Organization and Architecture, 6/e, Pearson PHI, 2012.

## **CO-PO Mapping:**

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	2	1	1	2									1	2	2
CO2	2	2	2	2		2			2				1	2	2
CO3	1	2	1	2					2				2	2	2
CO4	1	1	1	2									2	2	2
CO5	1	1	2	2									2	2	2

Note: 1 - Low Correlation 2 - Medium Correlation 3 - High Correlation