Full_Adder

DSD:

DIGITAL SYSTEM DESIGN

SUBMITTED BY:

Kondrolla Dinesh Reddy

(2020BTechCSE040)

FACULTY GUIDE:

Dr. Devika Kataria

Institute of Engineering and Technology

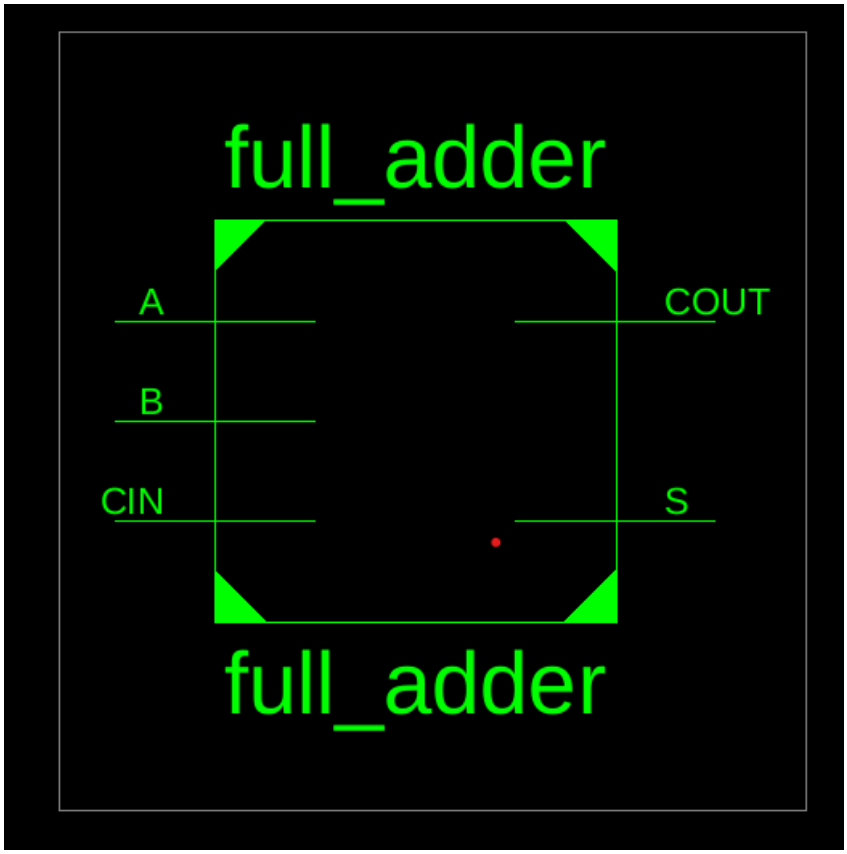
JK Lakshmipat University, Jaipur

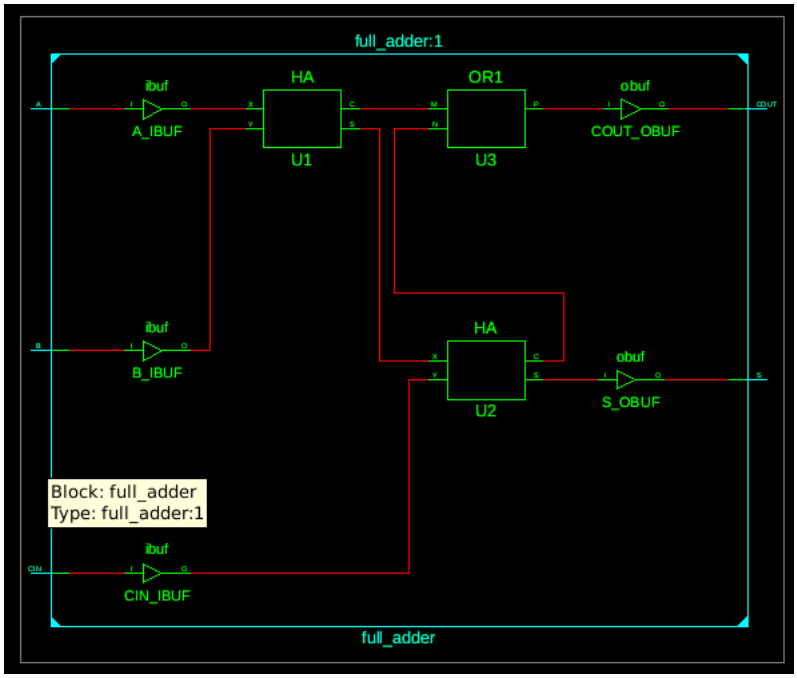
March 2022

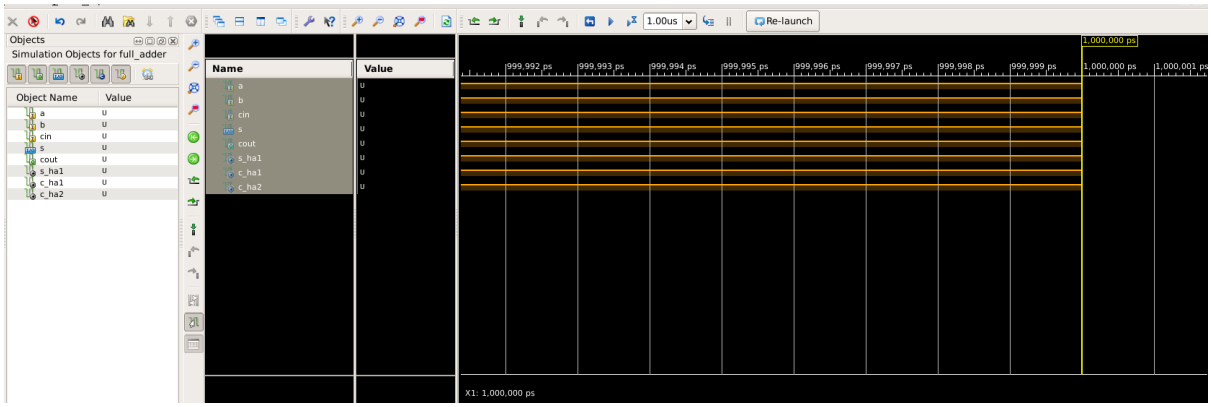
Design a full adder using tow half adders and OR gate. Use structural Programming.

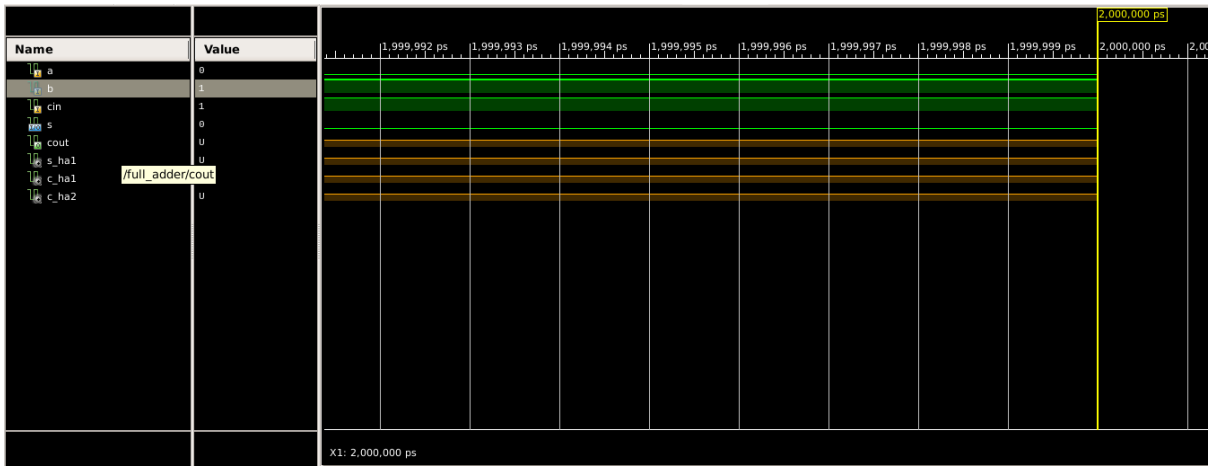
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--use UNISIM.VComponents.all;
                                                        --KOndrolla Dinesh Reddy
entity full_adder is
Port ( A,B,CIN : in  STD_LOGIC;
       S    :INOUT STD_LOGIC;
                                    COUT : out  STD_LOGIC);
end full_adder;
architecture Behavioral of full_adder is
SIGNAL S_HA1,C_HA1,C_HA2:STD_LOGIC;
COMPONENT HA is
   Port ( X,Y : in  STD_LOGIC;
          S,C : out  STD_LOGIC);
end COMPONENT;
component OR1 is
   Port ( M,N : in  STD_LOGIC;
          P : out  STD_LOGIC);
end component;
begin
U1:HA PORT MAP(X=>A,Y=>B,  S=>S_HA1,C=>C_HA1);
U2:HA PORT MAP(X=> S_HA1,Y=>CIN,S=>S,C=>C_HA2 );
U3:OR1 PORT MAP (M=>C_HA1,N=>C_HA2,P=>COUT);
end Behavioral;
```

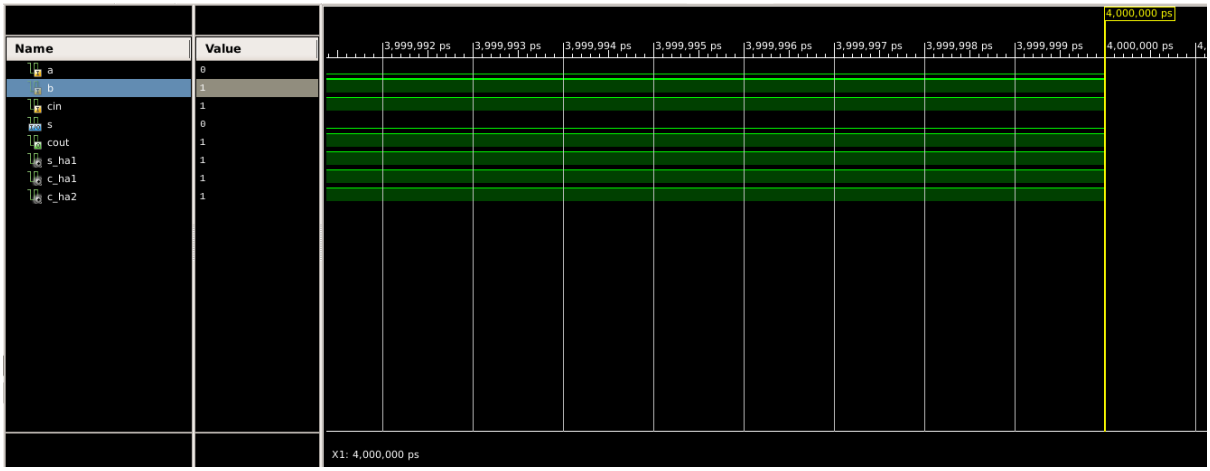
```
30  --use UNISIM.VComponents.all;
31                                          --KOndrolla Dinesh Reddy
32  entity full_adder is
33  Port ( A,B,CIN : in  STD_LOGIC;
34             S     :INOUT STD_LOGIC;
35              COUT : out  STD_LOGIC);
36  end full_adder;
37
38  architecture Behavioral of full_adder is
39  SIGNAL S_HA1,C_HA1,C_HA2:STD_LOGIC;
40  COMPONENT HA is
41      Port ( X,Y : in  STD_LOGIC;
42             S,C : out  STD_LOGIC);
43  end COMPONENT;
44  component OR1 is
45      Port ( M,N : in  STD_LOGIC;
46            P : out  STD_LOGIC);
47  end component;
48  begin
49  U1:HA PORT MAP(X=>A,Y=>B,   S=>S_HA1,C=>C_HA1);
50  U2:HA PORT MAP(X=> S_HA1,Y=>CIN,S=>S,C=>C_HA2 );
51  U3:OR1 PORT MAP (M=>C_HA1,N=>C_HA2,P=>COUT);
52
53
54  end Behavioral;
```




full_adder:1
ibuf
A_IBUF
HA
U1
OR1
U3
obuf
COUT_OBUF
COUT
ibuf
B_IBUF
HA
U2
obuf
S_OBUF
S
Block: full_adder
Type: full_adder:1
ibuf
CIN_IBUF
full_adder


Objects
Simulation Objects for full_adder
Object Name
Value
a
b
cin
s
cout
s_ha1
c_ha1
c_ha2
Name
Value
Re-launch
1.00us
1,000,000 ps
X1: 1,000,000 ps


Name
Value
a
b
cin
s
cout
s_ha1
c_ha1
c_ha2
/full_adder/cout
2,000,000 ps
X1: 2,000,000 ps


Name
Value
a
b
cin
s
cout
s_ha1
c_ha1
c_ha2
0
1
1
0
1
1
1
1
3,999,992 ps
3,999,993 ps
3,999,994 ps
3,999,995 ps
3,999,996 ps
3,999,997 ps
3,999,998 ps
3,999,999 ps
4,000,000 ps
X1: 4,000,000 ps