Course Title and Code: Computer Architecture and Organization: CS1107	
Hours per Week	**L-T-P: 3-0-2**
Credits	**4**
Students who can take	B. Tech. CSE IV

Course Objectives: To study the basic organization and architecture of digital computers (CPU, memory, I/O, software). Discussions will include digital logic and microprogramming. Learners would be able to program to optimize cache hit and estimate cost of different hardware for the number systems. Such knowledge leads to better understanding and utilization of digital computers, and can be used in the design and application of computer systems or as foundation for more advanced computer-related studies.

Course Outcome:

On successful completion of this course, the students should be able to:

CS1107.1. Draw the functional block diagram of single bus architecture of a computer and describe the function of the instruction execution cycle, RTL interpretation of instructions, addressing modes, instruction set.

CS1107.2. Summarize and compare different computer systems.

CS1107.3. Categorize different types of computers based on Instruction set Architecture.

CS1107.4. Develop assembly language programs for multiplication, division, and I/O interface using 8086.

CS1107.5. Given a CPU organization and instruction, design a memory module and analyze its operation by interfacing with the CPU.

CS1107.6. Write a flowchart for Concurrent access to memory and cache coherency in Parallel Processors and describe the process.

CS1107.7. Given a CPU organization, assess its performance, and apply design techniques to enhance performance using pipelining, parallelism and RISC methodology.

CS1107.8. Analyze the performance of pipeline and cache-based systems.

CS1107.9. Design algorithms to optimize hit-rate in cache memory.

CS1107.10. Program and estimate the execution time of arithmetic functions using different number systems.

Prerequisites		**Basics of Computer Networks**
Sr. No	**Specifications**	**Marks**
1	Attendance	Nil
2	Assignment	**10**
3	Class Participation	Nil
4	Quiz	**20**
5	Theory Exam-I	Nil
6	Theory Exam-II	**20**
7	Theory Exam-III	**30**
8	Report-I	Nil
9	Report-II	Nil
10	Report-III	Nil
11	Project-I	Nil
12	Project-II	Nil
13	Project-III	Nil
14	Lab Evaluation-I	**10**
15	Lab Evaluation-II	**10**
16	Course Portfolio	Nil
17	Presentation	Nil
18	Viva	Nil

	Total (100)	**100**
Re-Test Evaluation		
	Theory Exam-III	**30**
	Total:	**30**

Course Syllabi (Theory):

Unit I: BASIC STRUCTURE OF COMPUTERS: Functional units, Basic operational concepts, Bus structures, Performance and metrics, Number Systems, Instructions and instruction sequencing, Hardware-Software Interface, x86 Architecture, Instruction set architecture, Addressing modes, RISC, CISC. ALU design, Fixed point and floating-point operations.

Unit II: BASIC PROCESSING UNIT: Fundamental concepts, Execution of a complete instruction, Multiple bus organization, Hardwired control, Micro programmed control, Nano programming.

Unit III: PIPELINING: Basic concepts, Data hazards, Instruction hazards, Influence on instruction sets, Data path and control considerations, Performance considerations, Exception handling.

Unit IV: MEMORY SYSTEM: Basic concepts, Memory Hierarchy, Semiconductor RAM, ROM, Speed, Size and cost, Cache memories, Improving cache performance, Virtual memory, Memory management requirements, Associative memories, Secondary storage devices.

Unit V: I/O ORGANIZATION: Accessing I/O devices, Programmed Input/Output, Interrupts, Direct Memory Access, Buses, Interface circuits, Standard I/O Interfaces (PCI, SCSI, USB), I/O devices and processors.

Text Books:

- Mano, M. Morris. "Computer system architecture, 1993." Prentice Hall 3: 299.
- Stallings, William. Computer organization and architecture: designing for performance. Pearson Education India, 2003.

Reference Books:

- Patterson, David A., and John L. Hennessy. Computer Organization and Design MIPS Edition: The Hardware/Software Interface. Newnes, 2013.
- Hayes, John P. Computer architecture and organization. McGraw-Hill, Inc., 2002.
- Heuring, Vincent P., Harry Frederick Jordan, and Miles Murdocca. Computer systems design and architecture. Addison-Wesley, 1997.

Course Outcome	Correlation with program outcomes															Correlation with program specific outcomes	
	PO 1	PO 2a	PO 2b	PO 2c	PO 3a	PO 3b	PO 3c	PO 4a	PO 4b	PO 4c	PO 5a	PO 5b	PO 6	PO 7a	PO 7b	PSO-1	PSO -2
CS1107.1		1		1				1				1				2	
CS1107.2	1		1			1								1			2
CS1107.3		1					1				1						
CS1107.4			1		1				1	1			1			1	
CS1107.5	1							1				1		1			2
CS1107.6		1		2			1				1				1	1	
CS1107.7	1		1		1				1			1					
CS1107.8		2				2								1		1	2
CS1107.9			1		1			1				1				2	
CS1107.10	1								1				1		1		2

Course Plan

Week/ Month	1	**2**	**3**	**4**

1	Week 1 Contents • Introduction to the course and evaluation scheme. • Number Systems – Decimal, Binary, Octal, Hexadecimal • 1's and 2's complements Quiz I	Week 2 Contents Functional units, Basic operational concepts, Bus structures, Performance and metrics, • Introduction to Microprocessor • 8086 architecture and pin diagram **Lab Activity** Quiz II	Week 3 Contents Instructions and instruction sequencing, Hardware-Software Interface Quiz 2 **Lab Activity**	Week 4 Contents • Instructions and instruction sequencing, Introduction to 8086 Emulator • Introduction 8086 instruction set **Lab Activity** Assignment I **Course feedback I**
2	Week 5 Contents • Fundamental concepts, Execution of a complete instruction • Addressing modes • Hardwired control Unit Quiz III **Lab Activity**	Week 6 Contents • Software Control Unit • . 8086 instruction set Assignment 2 **Lab Activity**	Week 7 Contents • RISC, CISC • Fixed point and floating point operations • Array and String in 8086 **Lab Activity**	Week 8 Contents • Basic concepts of memory system, Memory Hierarchy, Semiconductor RAM, ROM, Speed, Size and cost **Lab Activity** **Course feedback II**

3	Week 9 Contents • Cache memories • Virtual memory **Lab Activity** **Theory Exam II**	Week 10 Contents • Associative memories • Secondary storage devices. **Lab Activity** Assignment 3	Week 11 Contents • Basic concepts of pipelining, Data hazards, • Instruction hazards, Influence on instruction sets • Data path and control considerations **Lab Activity**	Week 12 Contents • Performance considerations, Exception handling • pipelining **Lab Activity** Assignment 4 **Course feedback III**
4	Week 13 • I/O ORGANIZATION: Accessing I/O devices, • Programmed Input/Output, Interrupts, • Direct Memory Access, Buses	Week 14 • Standard I/O Interfaces (PCI, SCSI, USB), • I/O devices and processors.	**Theory Exam III**	

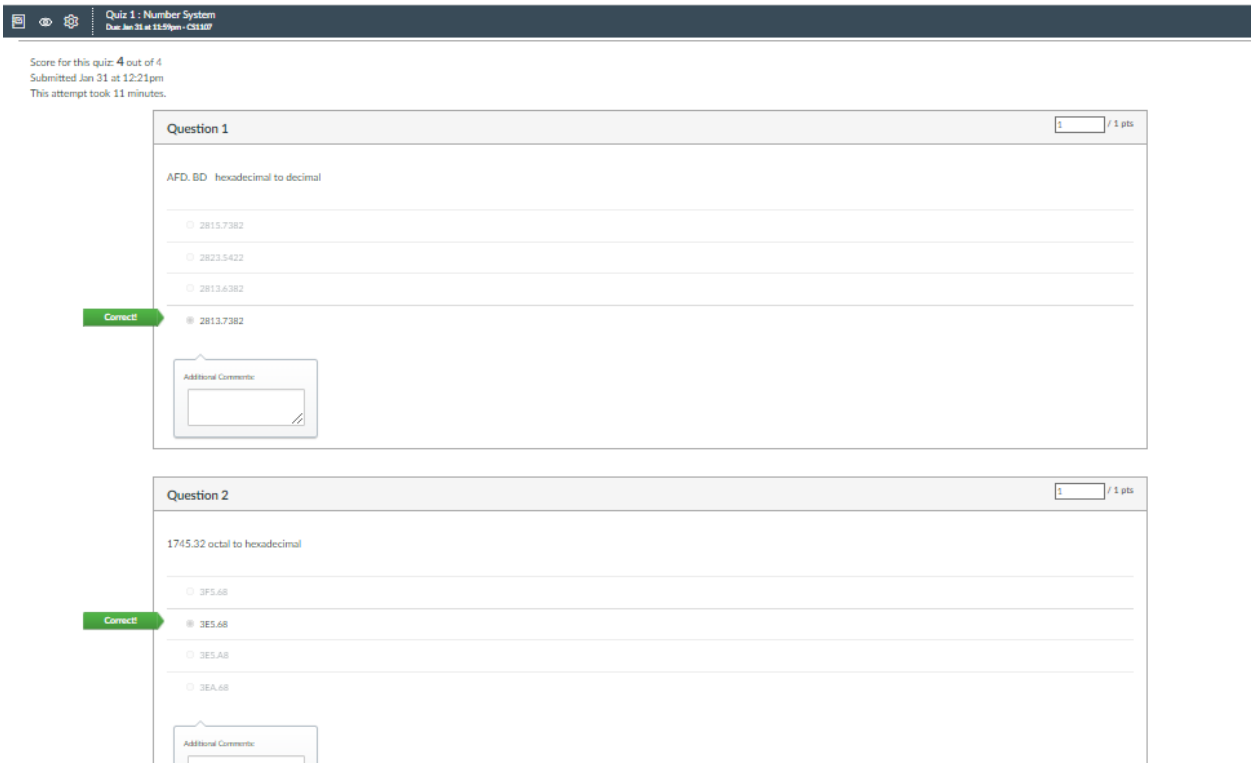
Assignment 1

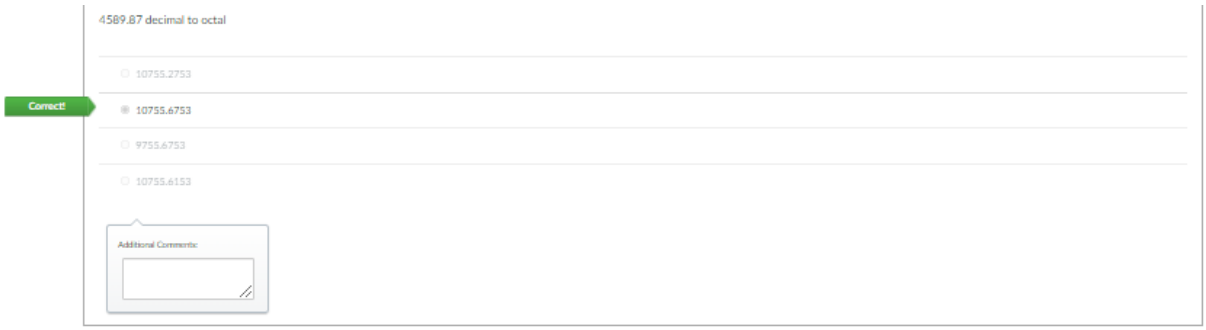
1. Draw the architecture diagram and pin diagram of 8086 and explain it properly.
2. WAP to add a series of 5 bytes stored in memory 20000H to 20004 H. Store the result immediately after the series. (use LOOP instruction, no need of string instruction)
3. WAP to do the 8 bit multiplication. Using MUL instruction

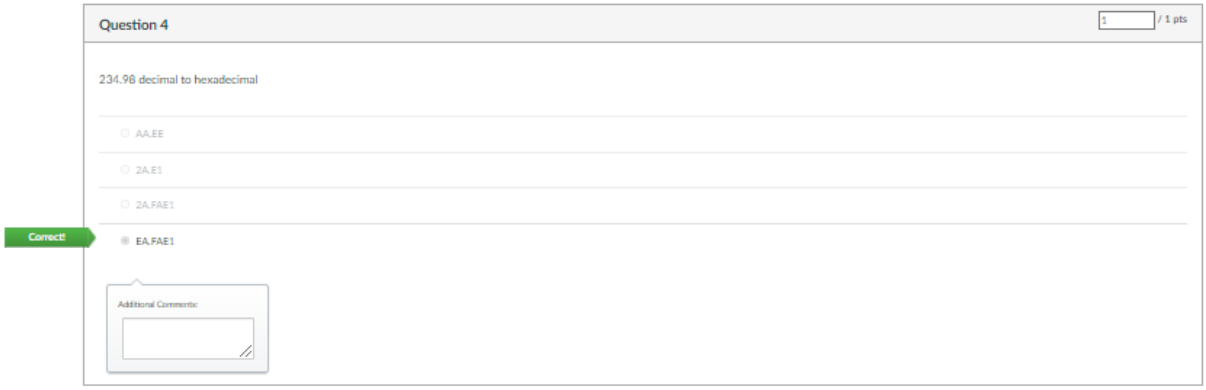
Assignment 2

1. WAP to find minimum of 5 bytes (block) stored in memory 40000H to 40004 H. Store the result immediately after the series.
2. WAP to do the 16 bit multiplication.
3. WAP to put 5 byte of data in memory location 50000H to 50005 H. Find the maximum of it and store it next location.
4. WAP to show the use of logical operation. AND, OR, NOT, EXOR, EXNOR
5. WAP to SORT a series of 10 numbers from 20,000H in ascending order.

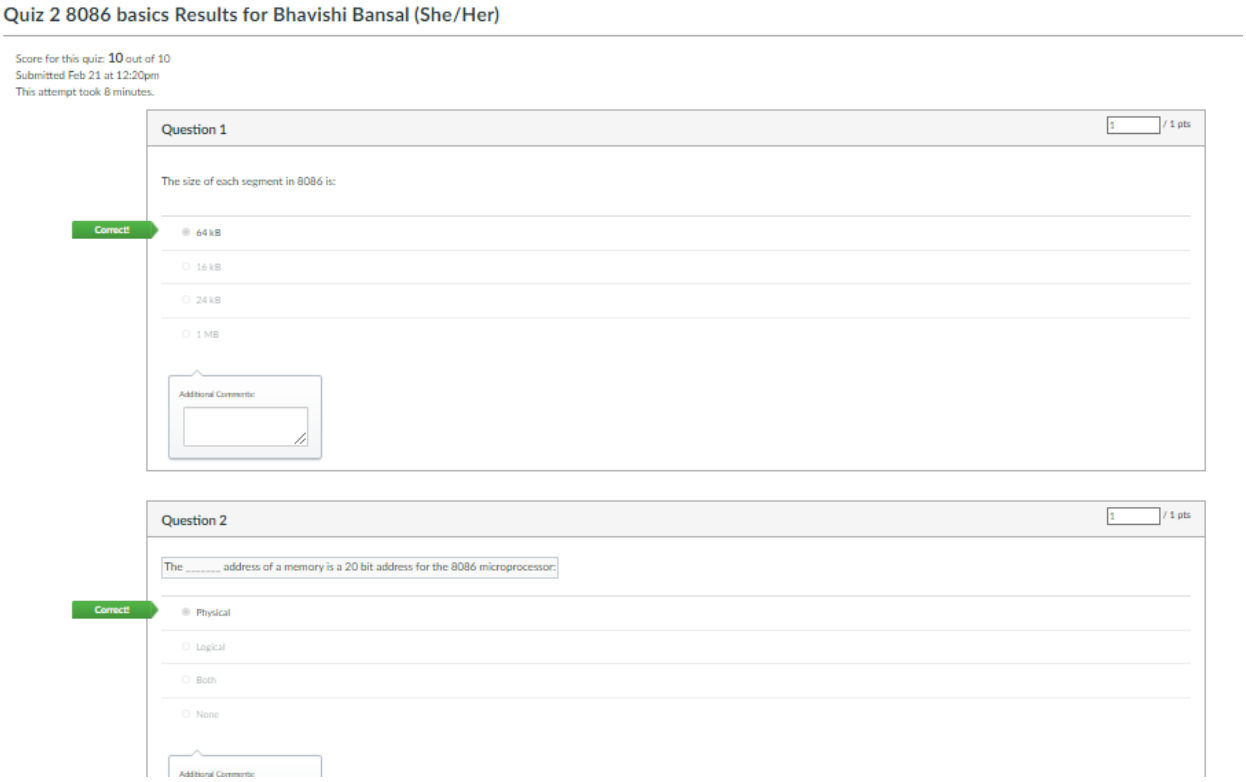
Quiz 1 Number System







Quiz 2 Basics of 8086



Question 3

1 / 1 pts

Which are the part of architecture of 8086:

Correct!

- both b and c
- The execution unit
- The bus interface unit
- None of these

Additional Comments:

Question 4

1 / 1 pts

The instruction, MOV AX, 0005H belongs to the address mode

Correct!

- immediate
- register
- direct
- none

The minimum size of a segment is

Correct!

- 16 Byte
- 16 bit
- 1 MB
- none

Additional Comments:

Question 6

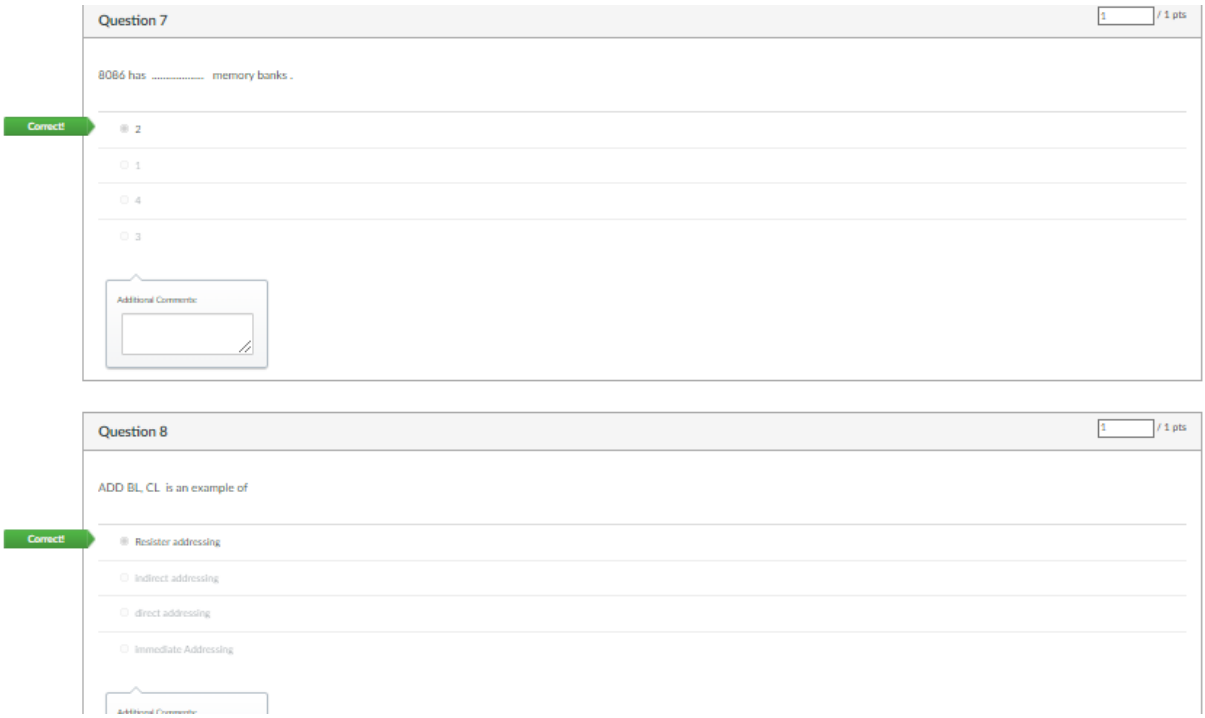
1 / 1 pts

What is the range of 8 bit signed numbers ?

Correct!

- -128.....to +127
- -128 to +128
- 0 to 255
- -127 to +128

Additional Comments:



Quiz 3 Programming

Section B. Write an ALP to find the factorial of a number stored at 20,000H. Store result at 20001H onwards.

Section A Write an ALP to find the sum of 6 bytes stored in memory 50000H to 50005H. Find the sum and stored it at next location.

List of Experiments

SN	Name of Experiment (use Intel 8086 Emulator)
1.	Write an ALP for 8-bit addition. Write an ALP for 16 bit addition.
2.	Write an ALP for 8-bit unsigned subtraction. Write an ALP for 16-bit unsigned subtraction.

3.	Write an ALP for Block transfer (6 byte) using string operation (from location 20000H to 30000H) (also show using MOVSB, MOVSW, CLD and STD mode)
4.	Write an ALP for Block Exchange using string operation (exchange data from location 20000H to 30000H and vice versa)
5.	Write an ALP to multiply two 16-bit numbers. Operands and result in Data Segment. Write an ALP to divide a 16 bit number by an 8 bit number.
6.	Write an ALP to add a series of 10 bytes stored in the memory from locations 20,000H to 20,009H. Store the result immediately after the series.
7.	Write an ALP to find the factorial of a number stored at 24,000H in data segment. Store the result at 24,001H and 24,002H.
8.	Write an ALP to invert a block of 10 bytes from Data Segment to Extra Segment. Write an ALP to get 5 byte of data from the user and store in it memory location 50000H to 50005 H. Find the maximum of it and store it next location.
9.	Write an ALP to SORT a series of 10 numbers from 20,000H in ascending order.
10.	Write an ALP to reverse the string and print the reversed string. Ex Input: String : "Geeks for Geeks" Output: skeeG rof skeeG
11.	Write an ALP to determine how many times “e” exists in “exercise”
12.	Write an ALP to given string is palindrome or not
13.	Write an ALP to Convert a Decimal Number into Hexadecimal. Assume the Decimal Number is stored at 24000H. Store the result at 24001H.