БЕЛОРУССКИЙ ГОСУДАРСТВЕННЫЙ УНИВЕРСИТЕТ

ИНФОРМАТИКИ и РАДИОЭЛЕКТРОНИКИ

Факультет КСиС

Кафедра ЭВМ ФКСиС

Контроль и диагностика средств вычислительной техники

Лабораторная работа № 3

Разработка моделей цифровых устройств на разных уровнях идентификации

Вариант № 3

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Минск

2018

**1. Моделируемая структура**

Моделируемая структура представлена на рисунке 1.1.

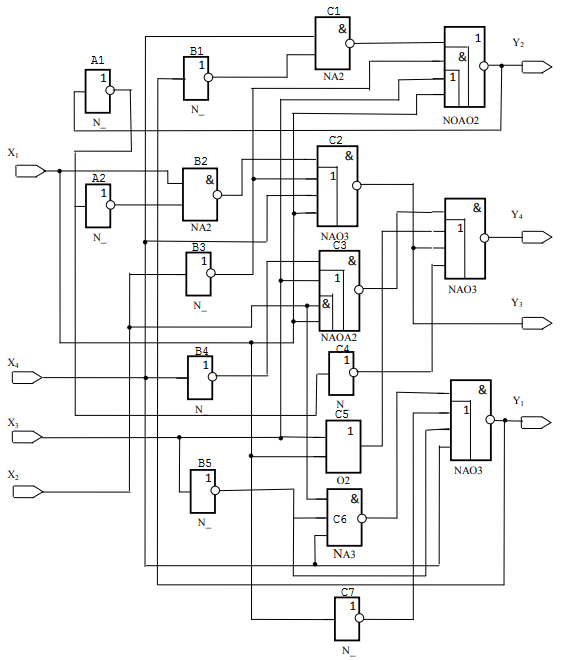


Рис 1.1

Для минимизации функции распишем более подробно выходы каждого блока, рисунок 1.2.

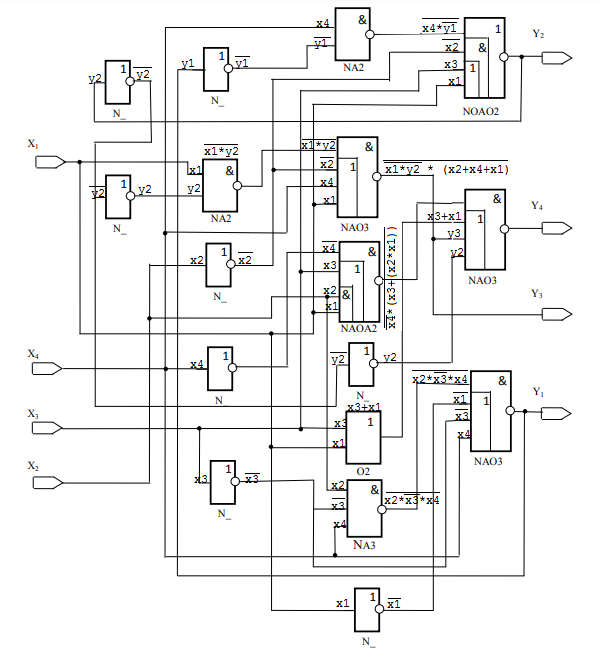
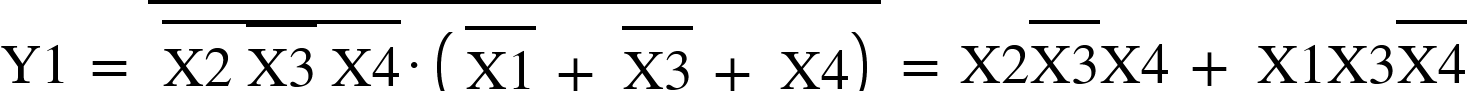
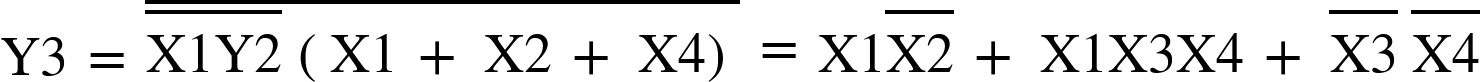


Рис 1.2



<math xmlns="http://www.w3.org/1998/Math/MathML" xmlns:wrs="http://www.wiris.com/xml/mathml-extension"><mpadded voffset="+4px"><mi mathvariant="normal">Y</mi><mn>2</mn><mo>&#xA0;</mo><mo>=</mo></mpadded><mo>&#xA0;</mo><menclose notation="top"><mpadded voffset="+3px"><menclose notation="top"><mpadded voffset="+2px"><mi mathvariant="normal">X</mi><mn>4</mn><menclose notation="top"><mi mathvariant="normal">Y</mi><mn>1</mn></menclose></mpadded></menclose><mo>+</mo><mpadded voffset="+3px"><mfenced><mrow><menclose notation="top"><mi mathvariant="normal">X</mi><mn>2</mn></menclose><mfenced wrs:valign="middle-baseline"><mrow><mi mathvariant="normal">X</mi><mn>3</mn><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><mi mathvariant="normal">X</mi><mn>1</mn></mrow></mfenced></mrow></mfenced></mpadded></mpadded></menclose><mo>&#xA0;</mo><mo>=</mo><mo>&#xA0;</mo><mspace linebreak="newline"/><mpadded voffset="+6px"><mo>=</mo><mo>&#xA0;</mo><menclose notation="top"><mi mathvariant="normal">X</mi><mn>1</mn></menclose><mo>&#xA0;</mo><menclose notation="top"><mi mathvariant="normal">X</mi><mn>2</mn></menclose><mo>&#xA0;</mo><mo>+</mo><menclose notation="top"><mi mathvariant="normal">X</mi><mn>1</mn></menclose><mi mathvariant="normal">X</mi><mn>3</mn><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><menclose notation="top"><mi mathvariant="normal">X</mi><mn>2</mn></menclose><mi mathvariant="normal">X</mi><mn>3</mn><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><menclose notation="top"><mi mathvariant="normal">X</mi><mn>1</mn></menclose><mo>&#xA0;</mo><menclose notation="top"><mi mathvariant="normal">X</mi><mn>4</mn></menclose><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><mi mathvariant="normal">X</mi><mn>1</mn><menclose notation="top"><mi mathvariant="normal">X</mi><mn>2</mn></menclose><mo>&#xA0;</mo><menclose notation="top"><mi mathvariant="normal">X</mi><mn>3</mn></menclose><mo>&#xA0;</mo><mo>+</mo><mi mathvariant="normal">X</mi><mn>1</mn><menclose notation="top"><mi mathvariant="normal">X</mi><mn>2</mn></menclose><mo>&#xA0;</mo><mi mathvariant="normal">X</mi><mn>4</mn><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><mi mathvariant="normal">X</mi><mn>1</mn><mi mathvariant="normal">X</mi><mn>3</mn><mi mathvariant="normal">X</mi><mn>4</mn><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><mi mathvariant="normal">X</mi><mn>1</mn><menclose notation="top"><mi mathvariant="normal">X</mi><mn>3</mn></menclose><mo>&#xA0;</mo><menclose notation="top"><mi mathvariant="normal">X</mi><mn>4</mn></menclose></mpadded></math>



<math xmlns="http://www.w3.org/1998/Math/MathML"><mpadded voffset="+3px"><mi mathvariant="normal">Y</mi><mn>4</mn><mo>&#xA0;</mo><mo>=</mo></mpadded><mo>&#xA0;</mo><menclose notation="top"><mpadded voffset="+2px"><menclose notation="top"><mpadded><mpadded voffset="+2px"><menclose notation="top"><mi mathvariant="normal">X</mi><mn>4</mn></menclose></mpadded><mpadded voffset="+2px"><mfenced><mrow><mi mathvariant="normal">X</mi><mn>3</mn><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><mi mathvariant="normal">X</mi><mn>1</mn><mi mathvariant="normal">X</mi><mn>2</mn></mrow></mfenced></mpadded></mpadded></menclose></mpadded><mpadded voffset="+4px"><mo>&#xA0;</mo><mfenced><mrow><mi mathvariant="normal">X</mi><mn>1</mn><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><mi mathvariant="normal">X</mi><mn>3</mn><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><mi mathvariant="normal">Y</mi><mn>2</mn><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><mi mathvariant="normal">Y</mi><mn>3</mn></mrow></mfenced></mpadded></menclose><mo>&#xA0;</mo><mspace linebreak="newline"/><mpadded voffset="+4px"><mo>=</mo><mo>&#xA0;</mo><mi mathvariant="normal">X</mi><mn>3</mn><menclose notation="top"><mi mathvariant="normal">X</mi><mn>4</mn></menclose><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><mi mathvariant="normal">X</mi><mn>1</mn><mi mathvariant="normal">X</mi><mn>2</mn><menclose notation="top"><mi mathvariant="normal">X</mi><mn>4</mn></menclose><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><mi mathvariant="normal">X</mi><mn>1</mn><mi mathvariant="normal">X</mi><mn>2</mn><menclose notation="top"><mi mathvariant="normal">X</mi><mn>3</mn></menclose><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><mi mathvariant="normal">X</mi><mn>1</mn><menclose notation="top"><mi mathvariant="normal">X</mi><mn>3</mn></menclose><mo>&#xA0;</mo><menclose notation="top"><mi mathvariant="normal">X</mi><mn>4</mn></menclose><mo>&#xA0;</mo><mo>+</mo><mo>&#xA0;</mo><menclose notation="top"><mi mathvariant="normal">X</mi><mn>1</mn></menclose><mi mathvariant="normal">X</mi><mn>2</mn><mi mathvariant="normal">X</mi><mn>3</mn><mi mathvariant="normal">X</mi><mn>4</mn></mpadded></math>

**2. Описание и трансляция в системе VLSI\_SIM**

Описание системы :

circuit KESSO\_L2;

inputs X1(1),X2(1), X3(1),X4(1);

outputs Y1(1),Y2(1),Y3(1),Y4(1);

GATES

A1 'N\_'(1) Y2(1);

A2 'N\_'(1) A1(1);

B1 'N\_'(1) Y1(1);

B2 'NA2'(1) X1(1),A2(1);

B3 'N\_'(1) X2(1);

B4 'N\_'(1) X4(1);

B5 'N\_'(1) X3(1);

C1 'NA2'(1) X4(1),B1(1);

Y3 'NAO3'(1) B2(1),B3(1),X4(1),X1(1);

C3 'NAOA2'(1) B4(1),X3(1),X2(1),X1(1);

C4 'N\_'(1) A1(1);

C5 'O2'(1) X3(1),X1(1);

C6 'NA3'(1) X2(1),B5(1),X4(1);

C7 'N\_'(1) X1(1);

Y2 'NOAO2'(1) C1(1),B3(1),X3(1),X1(1);

Y4 'NAO3'(1) C3(1),C5(1),Y3(1),C4(1);

Y1 'NAO3'(1) C6(1),C7(1),B5(1),X4(1);

ENDGATES

END

**3. Построение теста**

Первая попытка построения теста, рисунки 3.1, 3.2.

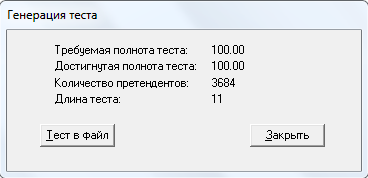


Рис 3.1

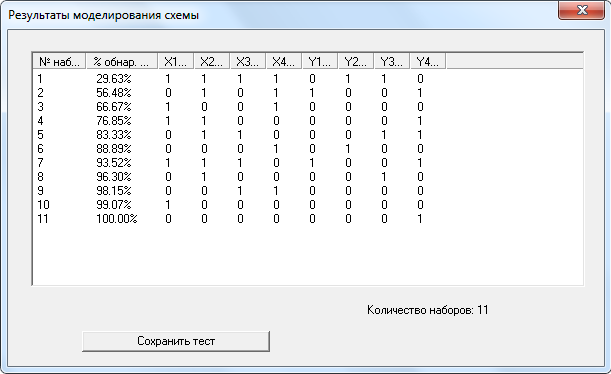


Рис 3.2

Вторая попытка построения теста, рисунки 3.3, 3.4.

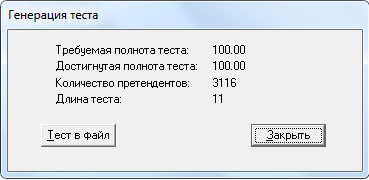


Рис 3.3

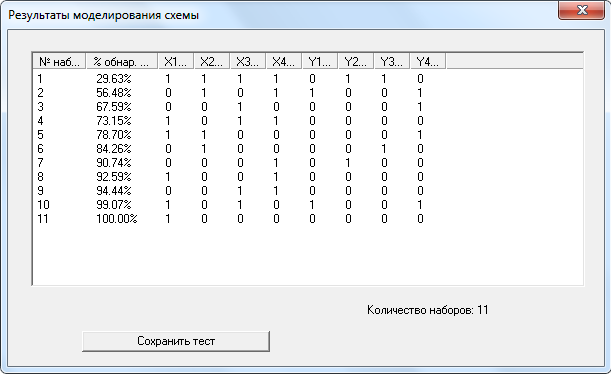


Рис 3.4

Третья попытка построение теста, рисунки 3.5, 3.6.

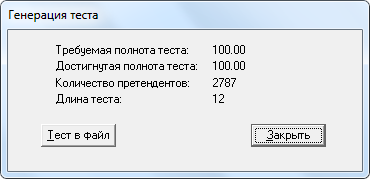


Рис 3.5

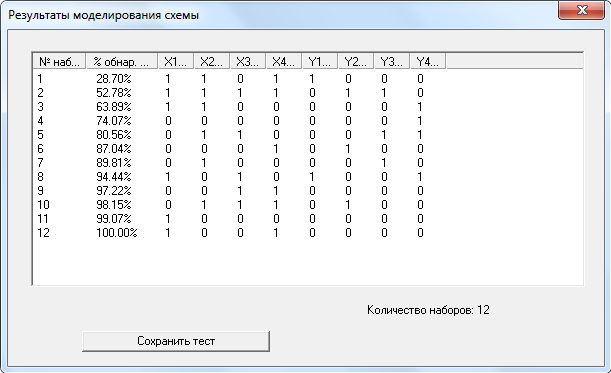


Рис 3.6

Для моделирования системы выберем первый тест.

Тестовый набор : 1111, 0101, 1001, 1100, 0110, 0001, 1110, 0100, 0011, 1000, 0000.

**4. Моделирование на полученном тесте**

Результаты моделирования схемы на случайно сгенерированном тестовом наборе представлены на рисунке 4.1.

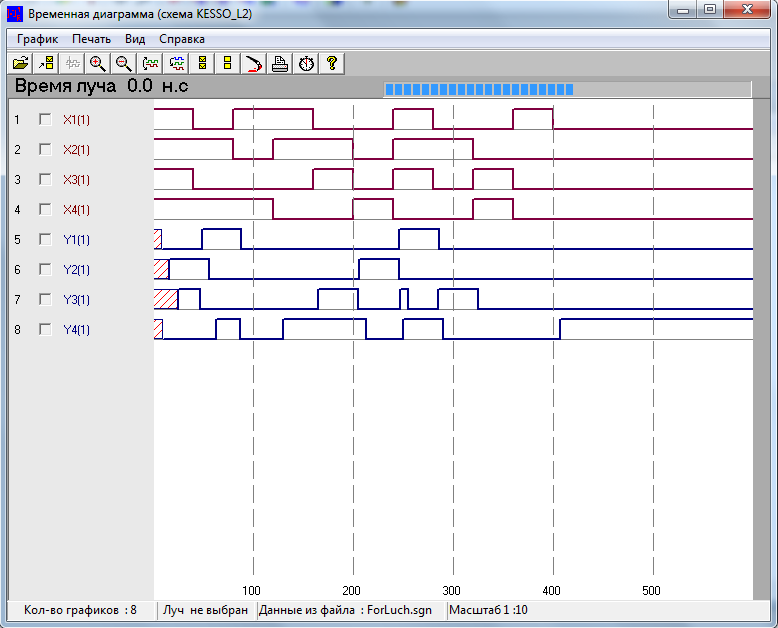


Рис 4.1

**5. Описание устройства в потоковом виде на языке VHDL**

Описание устройства :

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

ENTITY lr IS

PORT (

X1 : in STD\_LOGIC;

X2 : in STD\_LOGIC;

X3 : in STD\_LOGIC;

X4 : in STD\_LOGIC;

Y1 : out STD\_LOGIC;

Y2 : out STD\_LOGIC;

Y3 : out STD\_LOGIC;

Y4 : out STD\_LOGIC

);

END lr;

ARCHITECTURE Behavioral OF lr IS

SIGNAl A1 : STD\_LOGIC;

SIGNAl A2 : STD\_LOGIC;

SIGNAl B1 : STD\_LOGIC;

SIGNAl B2 : STD\_LOGIC;

SIGNAl B3 : STD\_LOGIC;

SIGNAl B4 : STD\_LOGIC;

SIGNAl B5 : STD\_LOGIC;

SIGNAl C1 : STD\_LOGIC;

SIGNAl C2 : STD\_LOGIC;

SIGNAl C3 : STD\_LOGIC;

SIGNAl C4 : STD\_LOGIC;

SIGNAl C5 : STD\_LOGIC;

SIGNAl C6 : STD\_LOGIC;

SIGNAl C7 : STD\_LOGIC;

SIGNAL signal\_Y1 : STD\_LOGIC;

SIGNAL signal\_Y2 : STD\_LOGIC;

SIGNAL signal\_Y3 : STD\_LOGIC;

BEGIN

A1 <= NOT signal\_Y2 AFTER 1 ns;

A2 <= NOT A1 AFTER 1 ns;

B1 <= NOT signal\_Y1 AFTER 1 ns;

B2 <= NOT (X1 AND A2) AFTER 2 ns;

B3 <= NOT X2 AFTER 1 ns;

B4 <= NOT X4 AFTER 1 ns;

B5 <= NOT X3 AFTER 1 ns;

C1 <= NOT (X4 AND B1) AFTER 2 ns;

signal\_Y3 <= NOT (B2 AND (B3 OR X4 OR X1)) AFTER 5 ns;

C3 <= NOT (B4 AND (X3 OR (X2 AND X1))) AFTER 4 ns;

C4 <= NOT A1 AFTER 1 ns;

C5 <= X3 OR X1 AFTER 2 ns;

C6 <= NOT (X2 AND B5 AND X4) AFTER 3 ns;

C7 <= NOT X1 AFTER 1 ns;

signal\_Y2 <= NOT (C1 OR (B3 AND (X3 OR X1))) AFTER 4 ns;

Y4 <= NOT (C3 AND (C5 OR signal\_Y3 OR C4)) AFTER 5 ns;

signal\_Y1 <= NOT (C6 AND (C7 OR B5 OR X4)) AFTER 5 ns;

Y1 <= signal\_Y1;

Y2 <= signal\_Y2;

Y3 <= signal\_Y3;

END Behavioral;

**6. Разработка блока тестирования**

Блок тестирования:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.NUMERIC\_STD.ALL;

use IEEE.std\_logic\_textio.ALL;

library STD;

use std.textio.ALL;

ENTITY lr\_test IS

file test\_file : text;

END lr\_test;

architecture Behavioral of lr\_test is

Component lr

Port (

X1 : in STD\_LOGIC;

X2 : in STD\_LOGIC;

X3 : in STD\_LOGIC;

X4 : in STD\_LOGIC;

Y1 : out STD\_LOGIC;

Y2 : out STD\_LOGIC;

Y3 : out STD\_LOGIC;

Y4 : out STD\_LOGIC);

END Component;

--Input

signal X1 : STD\_LOGIC := '0';

signal X2 : STD\_LOGIC := '0';

signal X3 : STD\_LOGIC := '0';

signal X4 : STD\_LOGIC := '0';

--Output

signal Y1 : STD\_LOGIC;

signal Y2 : STD\_LOGIC;

signal Y3 : STD\_LOGIC;

signal Y4 : STD\_LOGIC;

begin

mapping: lr PORT MAP(

X1 => X1,

X2 => X2,

X3 => X3,

X4 => X4,

Y1 => Y1,

Y2 => Y2,

Y3 => Y3,

Y4 => Y4

);

file\_process :process

variable file\_status : file\_open\_status;

variable inputs : line;

variable SigVect : std\_logic\_vector(3 downto 0);

begin

file\_open(file\_status, test\_file, "sca\_gen\_try\_1.tst", read\_mode);

while not endfile(test\_file) loop

readline(test\_file, inputs);

read(inputs, SigVect);

X1 <= SigVect(3);

X2 <= SigVect(2);

X3 <= SigVect(1);

X4 <= SigVect(0);

wait for 40 ns;

end loop;

end process;

end Behavioral;

**7. Моделирование в системе ModelSim**

Результаты работы тестового блока представлены на рисунке 7.1.

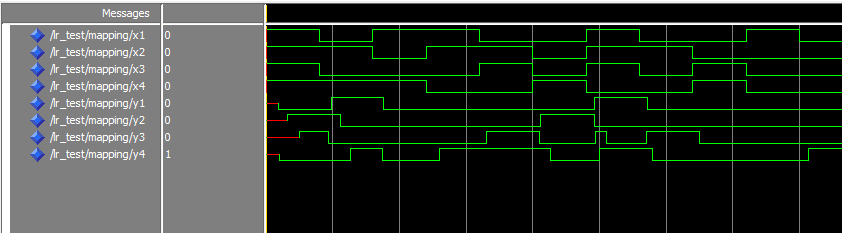


Рис 7.1

**8. Анализ полученных результатов**

Сравнение результатов моделирований представленно на рисунке 8.1.

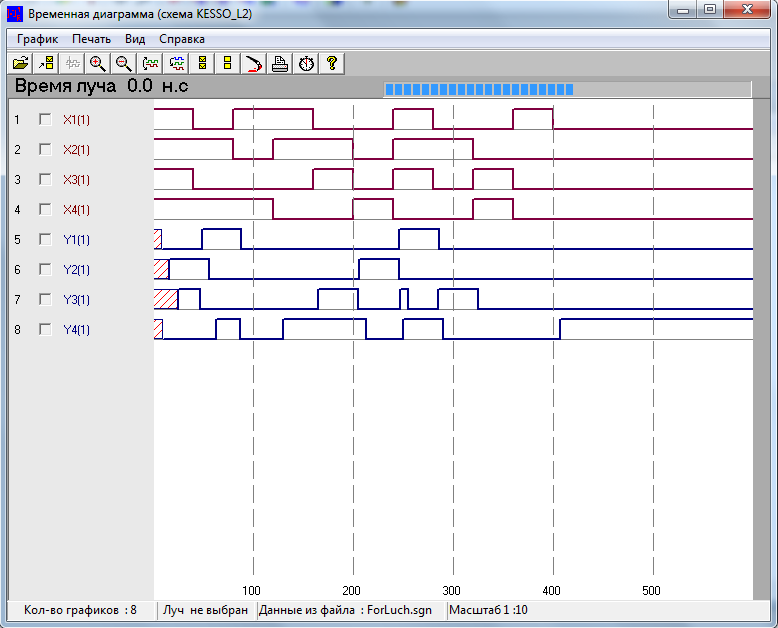
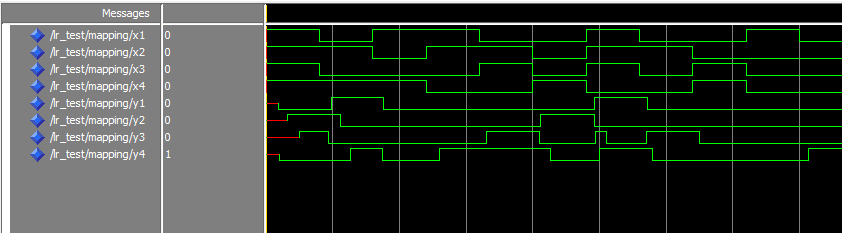


Рис 8.1

Временные диаграммы полученные в ходе моделирования схемы полностью совпали. Исходя из этого можно сделать вывод, что описание схемы корректно в обоих случаях.

**9. Структурное описание схемы на языке VHDL**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

ENTITY lr\_stract IS

PORT (

X1 : in STD\_LOGIC;

X2 : in STD\_LOGIC;

X3 : in STD\_LOGIC;

X4 : in STD\_LOGIC;

Y1 : out STD\_LOGIC;

Y2 : out STD\_LOGIC;

Y3 : out STD\_LOGIC;

Y4 : out STD\_LOGIC

);

END lr\_stract;

ARCHITECTURE Arch OF lr\_stract IS

component n

Port ( X : in STD\_LOGIC;

Y : out STD\_LOGIC);

end component;

component o2

Port ( X1 : in STD\_LOGIC;

X2 : in STD\_LOGIC;

Y : out STD\_LOGIC);

end component;

component na2

Port ( X1 : in STD\_LOGIC;

X2 : in STD\_LOGIC;

Y : out STD\_LOGIC);

end component;

component na3

Port ( X1 : in STD\_LOGIC;

X2 : in STD\_LOGIC;

X3 : in STD\_LOGIC;

Y : out STD\_LOGIC);

end component;

component nao3

Port ( X1 : in STD\_LOGIC;

X2 : in STD\_LOGIC;

X3 : in STD\_LOGIC;

X4 : in STD\_LOGIC;

Y : out STD\_LOGIC);

end component;

component naoa2

Port ( X1 : in STD\_LOGIC;

X2 : in STD\_LOGIC;

X3 : in STD\_LOGIC;

X4 : in STD\_LOGIC;

Y : out STD\_LOGIC);

end component;

component noao2

Port ( X1 : in STD\_LOGIC;

X2 : in STD\_LOGIC;

X3 : in STD\_LOGIC;

X4 : in STD\_LOGIC;

Y : out STD\_LOGIC);

end component;

SIGNAl A1 : STD\_LOGIC;

SIGNAl A2 : STD\_LOGIC;

SIGNAl B1 : STD\_LOGIC;

SIGNAl B2 : STD\_LOGIC;

SIGNAl B3 : STD\_LOGIC;

SIGNAl B4 : STD\_LOGIC;

SIGNAl B5 : STD\_LOGIC;

SIGNAl C1 : STD\_LOGIC;

SIGNAl C2 : STD\_LOGIC;

SIGNAl C3 : STD\_LOGIC;

SIGNAl C4 : STD\_LOGIC;

SIGNAl C5 : STD\_LOGIC;

SIGNAl C6 : STD\_LOGIC;

SIGNAl C7 : STD\_LOGIC;

SIGNAL signal\_Y1 : STD\_LOGIC;

SIGNAL signal\_Y2 : STD\_LOGIC;

SIGNAL signal\_Y3 : STD\_LOGIC;

BEGIN

a\_1: n port map(signal\_Y2, A1);

a\_2: n port map(A1, A2);

b\_1: n port map(signal\_Y1, B1);

b\_2: na2 port map(X1, A2, B2);

b\_3: n port map(X2, B3);

b\_4: n port map(X4, B4);

b\_5: n port map(X3, B5);

c\_1: na2 port map(X4, B1, C1);

c\_2: nao3 port map(B2, B3, X4, X1, signal\_Y3);

c\_3: naoa2 port map(B4, X3, X2, X1, C3);

c\_4: n port map(A1, C4);

c\_5: o2 port map(X3, X1, C5);

c\_6: na3 port map(X2, B5, X4, C6);

c\_7: n port map(X1, C7);

e\_1: noao2 port map(C1, B3, X3, X1, signal\_Y2);

e\_2: nao3 port map(C3, C5, signal\_Y3, C4, Y4);

e\_3: nao3 port map(C6, C7, B5, X4, signal\_Y1);

Y1 <= signal\_Y1;

Y2 <= signal\_Y2;

Y3 <= signal\_Y3;

END Arch;

**10. Разработка блока тестирования**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.NUMERIC\_STD.ALL;

use IEEE.std\_logic\_textio.ALL;

library STD;

use std.textio.ALL;

ENTITY lr\_stract\_tb IS

file test\_file : text;

END lr\_stract\_tb;

architecture Behavioral of lr\_stract\_tb is

Component lr\_stract

Port (

X1 : in STD\_LOGIC;

X2 : in STD\_LOGIC;

X3 : in STD\_LOGIC;

X4 : in STD\_LOGIC;

Y1 : out STD\_LOGIC;

Y2 : out STD\_LOGIC;

Y3 : out STD\_LOGIC;

Y4 : out STD\_LOGIC);

END Component;

--Input

signal X1 : STD\_LOGIC := '0';

signal X2 : STD\_LOGIC := '0';

signal X3 : STD\_LOGIC := '0';

signal X4 : STD\_LOGIC := '0';

--Output

signal Y1 : STD\_LOGIC;

signal Y2 : STD\_LOGIC;

signal Y3 : STD\_LOGIC;

signal Y4 : STD\_LOGIC;

begin

mapping: lr\_stract PORT MAP(

X1 => X1,

X2 => X2,

X3 => X3,

X4 => X4,

Y1 => Y1,

Y2 => Y2,

Y3 => Y3,

Y4 => Y4

);

file\_process :process

variable file\_status : file\_open\_status;

variable inputs : line;

variable SigVect : std\_logic\_vector(3 downto 0);

begin

file\_open(file\_status, test\_file, "sca\_gen\_try\_1.tst", read\_mode);

while not endfile(test\_file) loop

readline(test\_file, inputs);

read(inputs, SigVect);

X1 <= SigVect(3);

X2 <= SigVect(2);

X3 <= SigVect(1);

X4 <= SigVect(0);

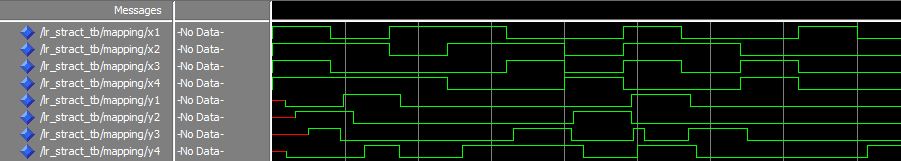
wait for 40 ns;

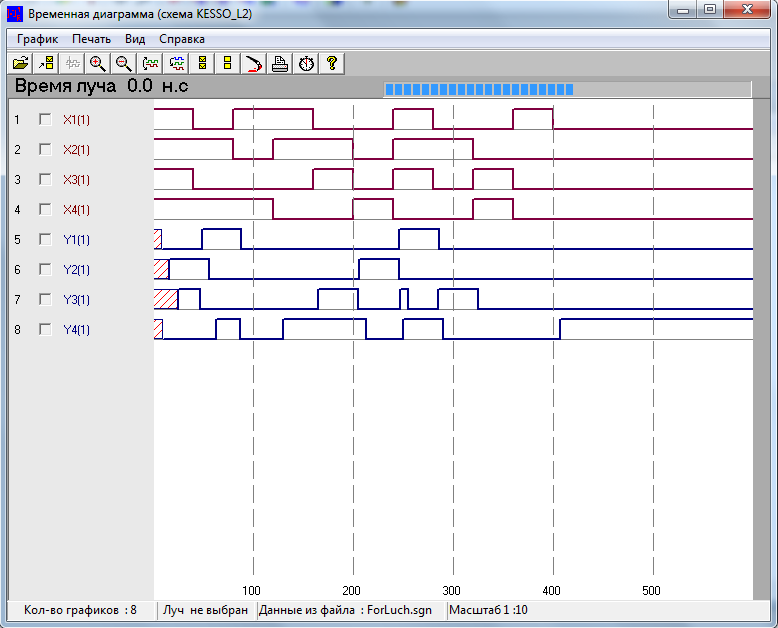
end loop;

end process;

end Behavioral;

**11. Анализ полученных результатов**





**12. Поведенческое описание схемы на языке VHDL**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

ENTITY lr\_pov IS

PORT (

X1 : in STD\_LOGIC;

X2 : in STD\_LOGIC;

X3 : in STD\_LOGIC;

X4 : in STD\_LOGIC;

Y1 : out STD\_LOGIC;

Y2 : out STD\_LOGIC;

Y3 : out STD\_LOGIC;

Y4 : out STD\_LOGIC

);

END lr\_pov;

ARCHITECTURE Arch OF lr\_pov IS

BEGIN

Y1 <= (X2 AND (NOT X3) AND X4) OR (X1 AND X3 AND(NOT X4));

Y2 <= ((NOT X1) AND (NOT X2) AND (NOT X3) AND X4) OR (X2 AND X3 AND X4);

Y3 <= ((NOT X1) AND X2 AND (NOT X4)) OR (X1 AND X2 AND X3 AND X4);

Y4 <= (X3 AND (NOT X4)) OR (X1 AND X2 AND (NOT X4)) OR ((NOT X1) AND (NOT X2) AND (NOT X4)) OR ((NOT X1) AND X2 AND (NOT X3) AND X4);

END Arch;

**13. Разработка блока тестирования**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.NUMERIC\_STD.ALL;

use IEEE.std\_logic\_textio.ALL;

library STD;

use std.textio.ALL;

ENTITY lr\_pov\_tb IS

file test\_file : text;

END lr\_pov\_tb;

architecture Behavioral of lr\_pov\_tb is

Component lr\_pov

Port (

X1 : in STD\_LOGIC;

X2 : in STD\_LOGIC;

X3 : in STD\_LOGIC;

X4 : in STD\_LOGIC;

Y1 : out STD\_LOGIC;

Y2 : out STD\_LOGIC;

Y3 : out STD\_LOGIC;

Y4 : out STD\_LOGIC);

END Component;

--Input

signal X1 : STD\_LOGIC := '0';

signal X2 : STD\_LOGIC := '0';

signal X3 : STD\_LOGIC := '0';

signal X4 : STD\_LOGIC := '0';

--Output

signal Y1 : STD\_LOGIC;

signal Y2 : STD\_LOGIC;

signal Y3 : STD\_LOGIC;

signal Y4 : STD\_LOGIC;

begin

mapping: lr\_pov PORT MAP(

X1 => X1,

X2 => X2,

X3 => X3,

X4 => X4,

Y1 => Y1,

Y2 => Y2,

Y3 => Y3,

Y4 => Y4

);

file\_process :process

variable file\_status : file\_open\_status;

variable inputs : line;

variable SigVect : std\_logic\_vector(3 downto 0);

begin

file\_open(file\_status, test\_file, "sca\_gen\_try\_1.tst", read\_mode);

while not endfile(test\_file) loop

readline(test\_file, inputs);

read(inputs, SigVect);

X1 <= SigVect(3);

X2 <= SigVect(2);

X3 <= SigVect(1);

X4 <= SigVect(0);

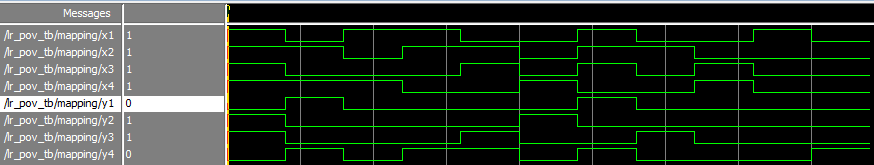
wait for 40 ns;

end loop;

end process;

end Behavioral;

**14. Анализ полученных результатов**

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