KIA Data Sheet

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- 8-Bit Wishbone Slave Interface
- 16-Byte FIFO Queue
- Queue Full and Empty Status Flags
- Software Explicit Dequeue
- Perfect for Processors With or Without Interrupts
- Registered Interface Provides One Cycle Latency

1 Introduction

The Keyboard Interface Adapter, or KIA, provides a very easy to use PS/2 keyboard interface. It features a 16-byte first-in, first-out (FIFO) queue to hold incoming data long enough for busy software to respond to the keyboard without requiring an interrupt subsystem. A dedicated signal indicating when the queue is empty is exposed, in support for those processors which prefer interrupts for such events. The software-driven explicit dequeue feature allows the keyboard driver software to avoid the use of "shadow registers" in ordinary RAM. Combined, these features makes the KIA ideal for use in small, deep-embedded applications where RAM may be at a premium.

2 Internal Architecture

Figure 1 illustrates the block diagram of the KIA.

2.1 Shift Register and Frame Detection

The D_I and C_I signals couple to the serial-in, parallel-out shift register. Additionally, feedback from the shift register, coupled with the C_I input, helps the frame detection logic decide when a full PS/2 frame of data has been received. Upon detection of a byte, it pushes it into the queue.

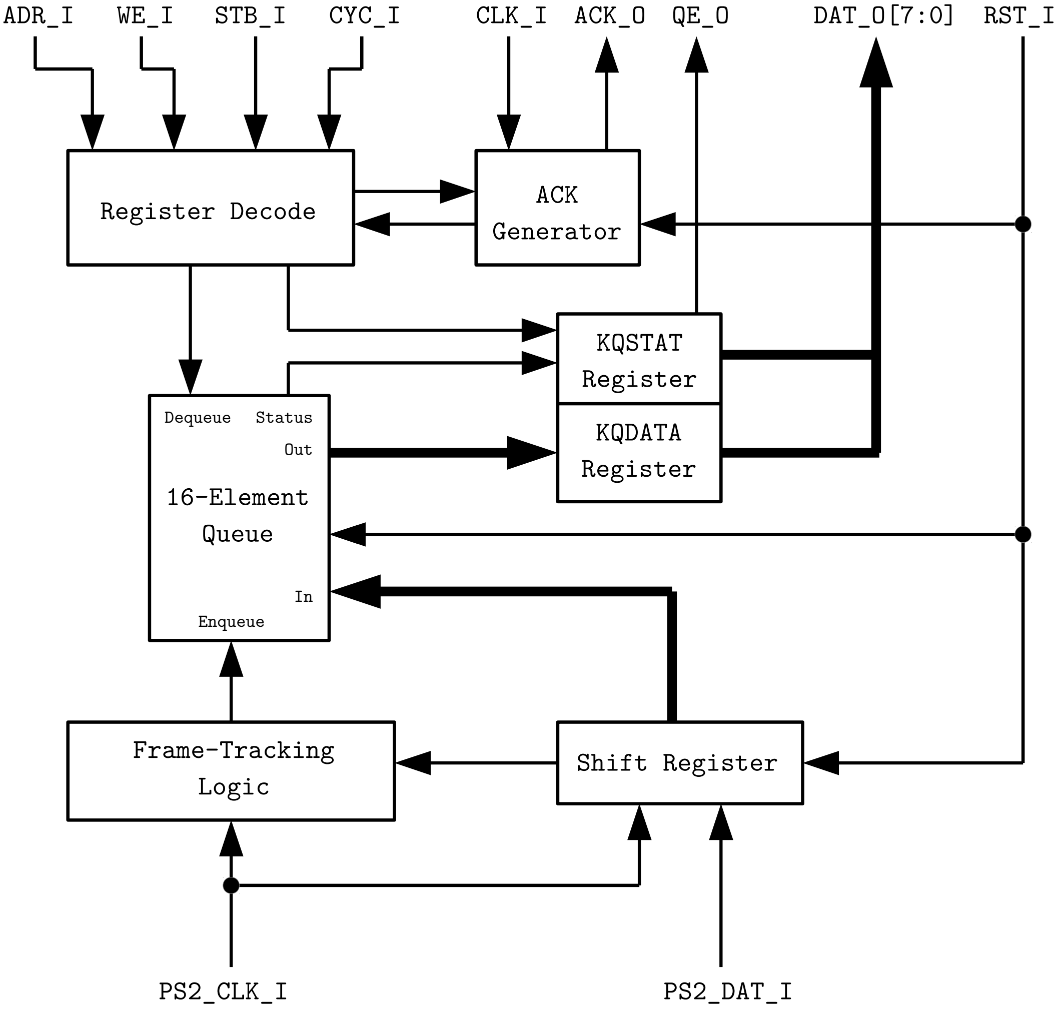


Figure 1: Block Diagram of the Keyboard Interface Adapter.

REG#	R/W	Reg Name	7	6	5	4	3	2	1	0
0	R/O	KQSTAT	-	-	-	-	-	-	QF	QE
1	R/O	KQDATA	D7	D6	D5	D4	D3	D2	D1	D0

REG#	R/W	Reg Name	7	6	5	4	3	2	1	0
0	W/O	n/a	-	-	-	-	-	-	-	-
1	W/O	KQPOP	-	-	-	-	-	-	-	-

Figure 2: KIA Register Map.

2.2 Operation of the FIFO Queue

The queue contains 16 bytes of storage space. Of this space, up to 15 bytes may hold pending data before the QF bit asserts, and no further data will be accepted. Internally, a 4-bit *read_pointer* and a *write_pointer* register exists, both reset to zero when the KIA is reset. The *write_pointer* register increments for each successful data byte received. The queue is considered full when the *write_pointer* approaches the *read_pointer* from behind, threatening to overwrite unread data.

Likewise, when data is read from the KIA, the *read_pointer* register increments. The queue becomes empty when the *read_pointer* equals the *write_pointer* register.

2.3 The Register Map

The register map appears in figure 2.

KQSTAT. This read-only register contains the queue status bits. Two bits exist: QE (bit 0) indicates when the queue contains no further data for reading, while QF (bit 1) indicates whether the queue is so full that it cannot accept any additional data. Bits 7 through 2 officially are undefined, and software must ignore their values.

KQDATA. This read-only register provides visibility into the head of the queue. Reading this register does not automatically pop the queue. After software has completed working with the current byte, it must dequeue that byte by writing to the KQDATA/KQPOP register.

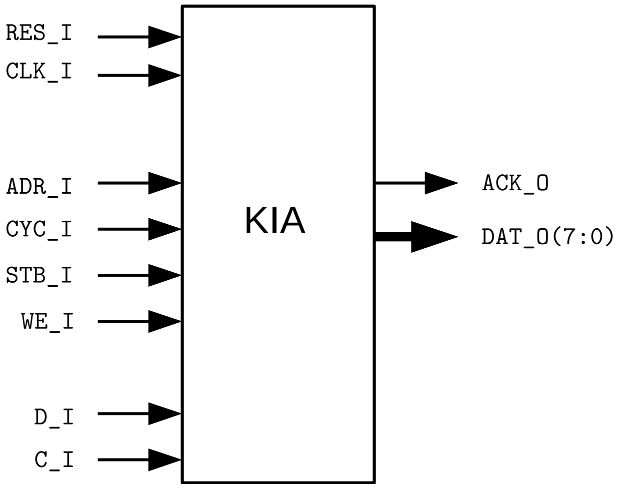


Figure 3: KIA Logic Symbol.

KQPOP. This write-only register stores no value; however, the act of writing to this register causes the FIFO to dequeue the current head byte, thus revealing (if present) the next byte to read. If the queue becomes exhausted, the QE bit of KQSTAT asserts. Writes to KQPOP with QE asserted do nothing.

3 Hardware Interface

3.1 Logic Symbol

The logic symbol for the KIA appears in figure 3.

3.2 Signal Descriptions

The KIA complies with Wishbone B3 bus slave standards with an 8-bit port size and 8-bit granularity.

3.2.1 SYSCON Signals

CLK_I. Provides the standard time-base for the peripheral. All bus state transitions occur on the rising edge of this signal.

RES_I. When asserted during the rising edge of CLK_I, the KIA resets to its power-on default state, empties its queue, and discards any PS/2 data frame in progress.

3.2.2 SLAVE Signals

ACK_O. The KIA generates its own acknowledgement for a single-beat Wishbone bus transaction.

ADR_I. This 1-bit input selects the I/O register to read from, or to write to if supported.

CYC_I. This signal serves as a flag to external bus arbitration logic that a bus master wishes to use the bus, asserting it when it has data to transfer, and negating it otherwise. As such, CYC_I qualifies *all* other bus signals except for RES_I and CLK_I.

DAT_O(7:0). The KIA places the contents of the addressed register during a read cycle; during a write cycle, however, this bus remains undefined.

QE_O. If asserted, the queue lacks any data bytes to read. When at least one byte exists to be read by the host processor, the KIA will negate QE_O, and keep it negated until all bytes have been read. This signal may be used to generate external interrupts to a host microprocessor.

STB_I. This signal qualifies a single bus transfer specifically to the KIA. The current bus master (typically a microprocessor) and its associated address decoding logic collaborate to assert this signal when the master addresses the KIA and is ready for the data.

WE_I. If asserted, the current bus transaction is a write cycle, used to dequeue the FIFO. In this case, DAT_O(7:0) will remain undefined. If negated, the master will expect the addressed register's contents on the DAT_O(7:0) bus. Note that the KIA lacks a corresponding data input bus, so any data written to the KIA will be ignored.

3.2.3 PS/2 Signals

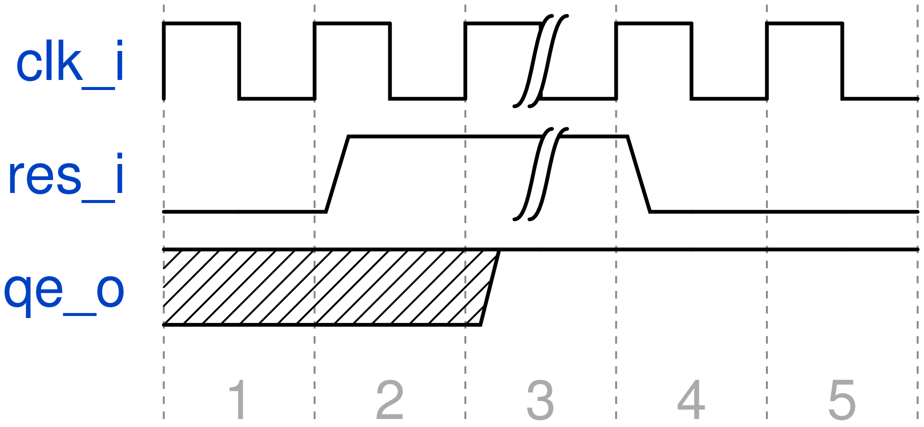
C_I. The clock signal generated by the attached PS/2 peripheral.

D_I. The data signal generated by the attached PS/2 peripheral. The peripheral synchronizes the bits of data on this pin against C_I.

3.3 Timing Diagrams

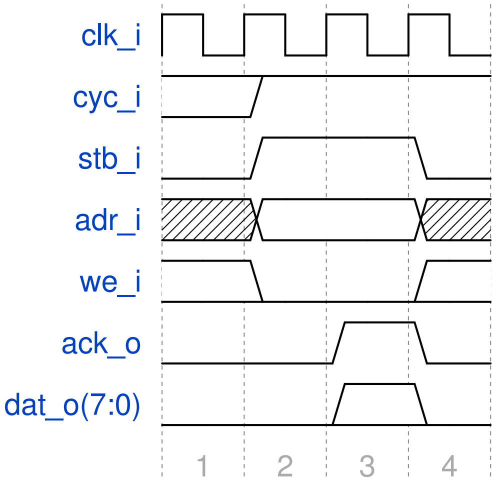
3.3.1 Reset Timing

Reset timing follows standard Wishbone B3 recommendations. For any rising clock edge, the KIA will reset immediately if RES_I becomes asserted, and will continue to reset for as long as RES_I remains asserted.



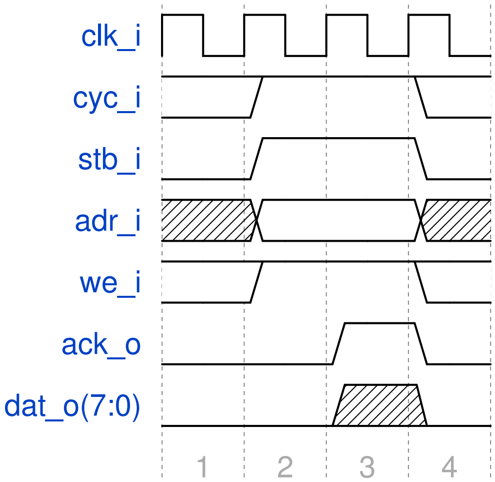
3.3.2 Register Read

Read timing follows standard Wishbone B3 recommendations. The KIA incurs a one-cycle latency for read operations due to its fully synchronous design. To prevent internal glitching, the KIA and the addressing bus master should run from the same clock. Directly crossing clock domains may result in undesirable behavior.

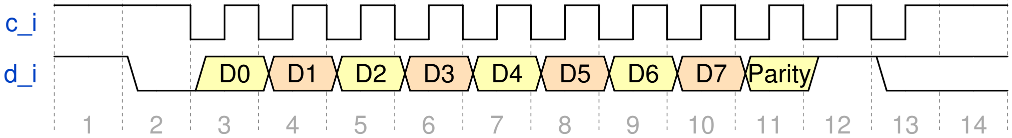


3.3.3 Register Write

Write timing follows standard Wishbone B3 recommendations. The KIA incurs a one-cycle latency for write operations due to its fully synchronous design. To prevent internal glitching, the KIA and the addressing bus master should run from the same clock. Directly crossing clock domains may result in undesirable behavior.



3.3.4 PS/2 Data Frame Reception


c_i
d_i
D0
D1
D2
D3
D4
D5
D6
D7
Parity
1
2
3
4
5
6
7
8
9
10
11
12
13
14