

VLSI Design Assignment-1

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Q1) Design a minimum size CMOS inverter (minimum possible equal rise and fall time) with fixed NMOS and PMOS channel length of $0.15\mu\text{m}$ (this is the minimum channel length). The minimum channel width for NMOS is fixed to $0.42\mu\text{m}$ (restriction from the PDK) and the width of PMOS is to be obtained by design. The input should be a rail-to-rail square wave with rise/fall times of 20 PS, and the inverter will be loaded by another minimum size inverter.

Simulate and report the following in the tabular fashion shown below:

Inverter Design Parameter	Value
PMOS Width (W_P) (μm)	
PMOS Length (L_P) (μm)	
NMOS Width (W_N) (μm)	
NMOS Length (L_N) (μm)	

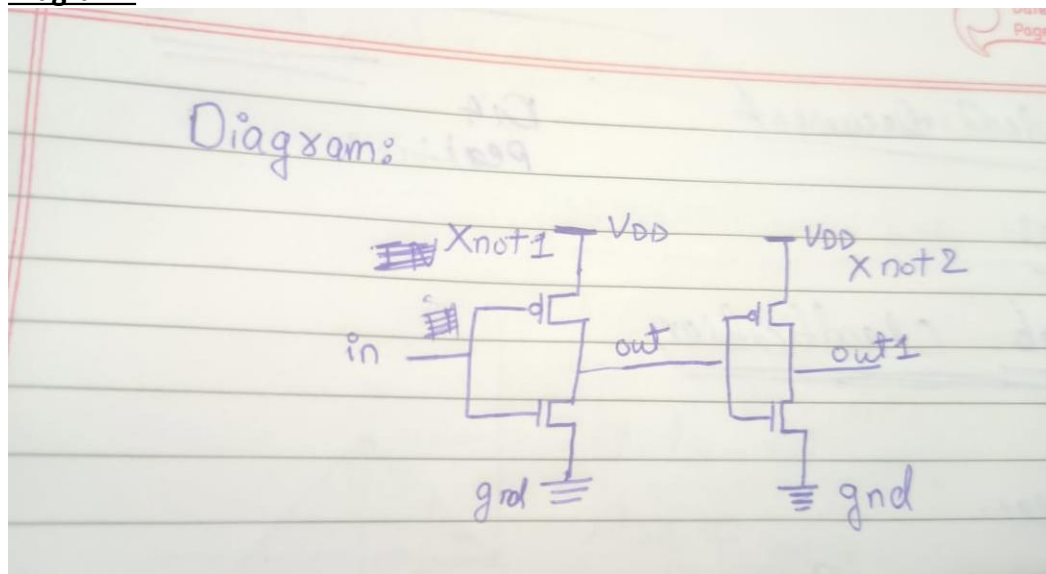
Inverter Dynamic Characteristic	Value
Rise time, t_r (ps)	
Fall time, t_f (ps)	
Propagation delay, t_p (ps)	

Once designed, plot (in the submission) the static transfer characteristics of this inverter by using a DC sweep on the input from 0 to VDD and report the following in the tabular fashion below:

Inverter Static Characteristic	Value
V_{IH} (V)	
V_{IL} (V)	
NM_H (V)	
NM_L (V)	
Switching Voltage, V_M (V)	

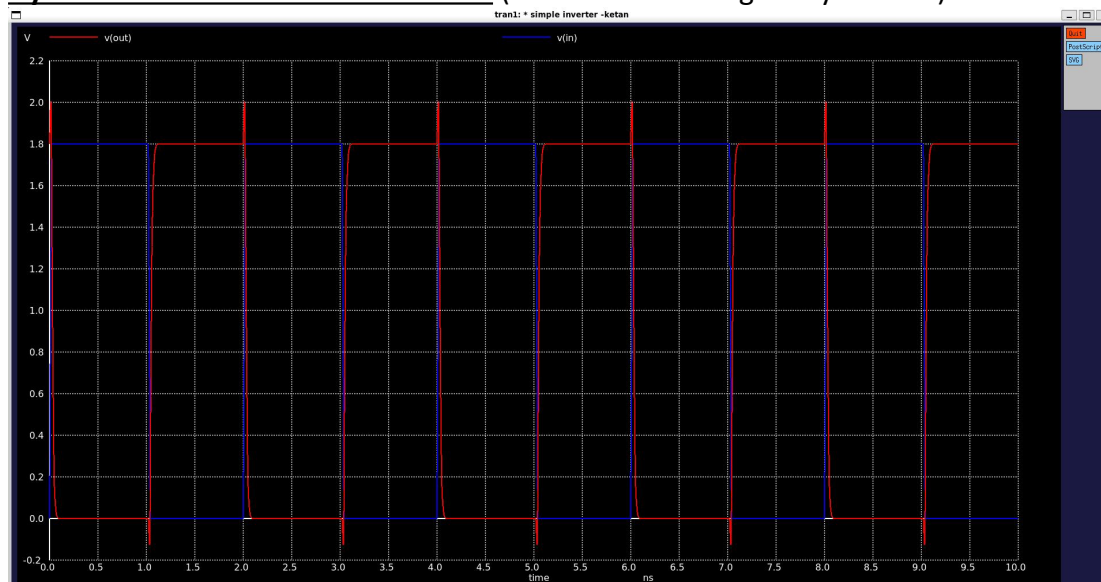
Solution:

Diagram:



Inverter Design Parameter (For INVX1)	Value
PMOS Width (W_P) (μ_m)	1.26 ($\sim 3 \times W_N$)
PMOS Length (L_P) (μ_m)	0.15
NMOS Width (W_N) (μ_m)	0.42
NMOS Length (L_N) (μ_m)	0.15

Dynamic Characteristics of Inverter:- (Plot is from Timing Analysis code)



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Circuit: * simple inverter -ketan

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

Initial Transient Solution
-----
Node                Voltage
-----
vdd                  1.8
in                   0
out                  1.8
out1                 1.12952e-07
v1#branch            0
vdd#branch           -6.21766e-11

Reference value : 9.13250e-09
No. of Data Rows : 10065

Measurements for Transient Analysis

rise_time           = 1.852437e-11 targ= 1.061191e-09 trig= 1.042667e-09
fall_time           = 1.851907e-11 targ= 4.307560e-11 trig= 2.455652e-11
error_time          = 5.30087e-15
error_percent       = 2.86156e-02
p_delay_tphl        = 2.280225e-11 targ= 3.280225e-11 trig= 1.000000e-11
p_delay_tplh        = 1.975849e-11 targ= 1.049758e-09 trig= 1.030000e-09
p_delay_avg         = 2.12804e-11

```

(parameters from Timing analysis code)

Inverter Dynamic Characteristic	Value
Rise time, tr (ps) (20% to 80%)	18.52
Fall time, tf (ps) (80% to 20%)	18.51
Propagation delay, tp (ps)	21.28

Below is the code for reference:- (Code for Timing Analysis)

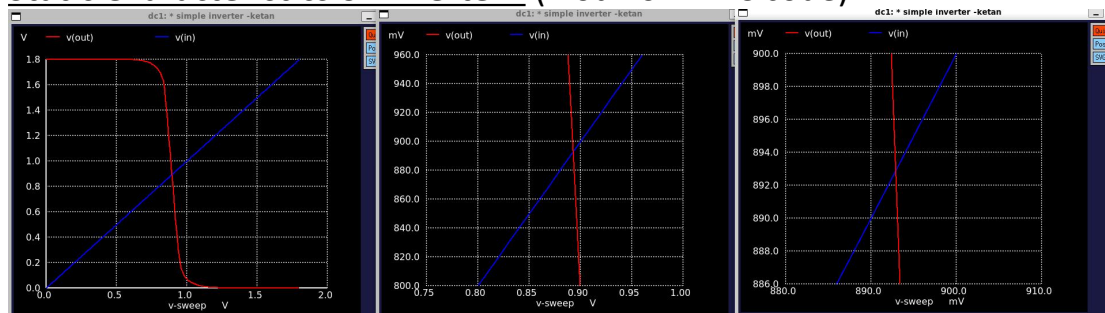
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File Edit Selection View Go Run Terminal Help
ngspice_simulations

TimingAnalysis-INVX1.cir X TimingAnalysis-INVX1.cir
Inverter-simulation > TimingAnalysis-INVX1.cir
1 * simple inverter -ketan
2 .lib /usr/local/share/pdk/sky130A/libs.tech/ngspice/sky130.lib.spice tt
3
4 .param asn = 0.42*2*0.15
5 .param pdn = 2*(0.42 + 2*0.15)
6 .param wp = 0.84 + 0.42
7 .param asp = wp*2*0.15
8 .param pdp = 2*(wp + 2*0.15)
9 *.param rise_time = 0
10 *.param fall_time = 0
11
12 *the voltage sources:
13 vdd vdd gnd dc 1.8
14 v1 in gnd pulse(0 1.8 0p 20p 20p 1n 2n)
15
16
17 Xnot1 in vdd gnd out not1 ; Inverter of single drive strength
18 Xnot2 out vdd gnd out1 not1
19
20 .subckt not1 a vdd vss z ; subcircuit for inverter of single drive strength
21 xnm1 z a vdd vdd sky130 fd_pr_pfet_01v8 l=0.15 w=wp as=asp ad=asp ps=pdp pd=pdp
22 xnm2 z a vss vss sky130 fd_pr_nfet_01v8 l=0.15 w=0.42 as=asn ad=asn ps=pdn pd=pdn
23 .ends
24
25 * simulation command for Time analysis:
26 .tran 1ps 10ns 0 1p
27 .measure tran rise_time TRIG v(out) VAL=0.36 RISE=1 TARG v(out) VAL=1.44 RISE=1 ; measure rise and fall times
28 .measure tran fall_time TRIG v(out) VAL=1.44 FALL=1 TARG v(out) VAL=0.36 FALL=1
29 .measure tran error_time PARAM="abs(rise_time - fall_time)" ; measure error time between rise and fall times
30 .measure tran error_percent PARAM="error_time*100/rise_time" ; measure error percentage between rise and fall times
31 .measure tran P_delay_tphl TRIG v(in) VAL= 0.9 RISE=1 TARG v(out) VAL=0.9 FALL=1 ; measure propagation delay from input to output for high to low
32 .measure tran P_delay_tplh TRIG v(in) VAL= 0.9 FALL=1 TARG v(out) VAL=0.9 RISE=1 ; measure propagation delay from input to output for low to high
33 .measure tran P_delay_avg PARAM="(P_delay_tphl + P_delay_tplh)/2" ; measure average propagation delay
34
35 .control
36 run
37 plot v(out) v(in)
38 .endc

```

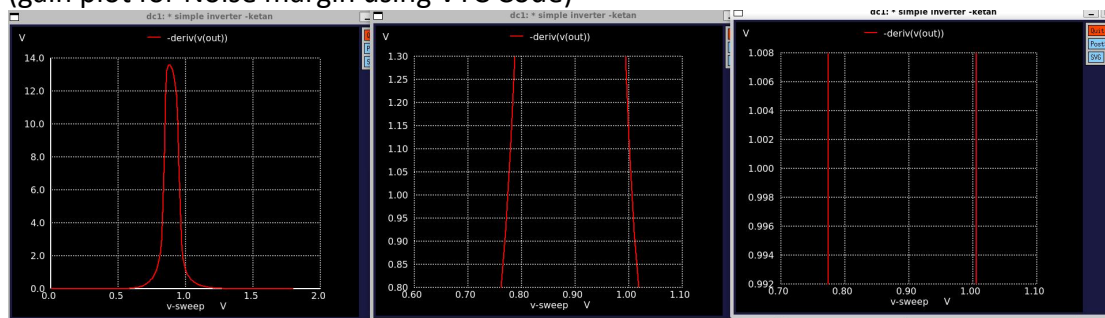
Static Characteristics of Inverter:- (Plot from VTC code)



$V_m = V_{in} = v_{out}$

$x_0 = 0.892905, y_0 = 0.892842$

(gain plot for Noise margin using VTC Code)



V_{IL}
(using gain plot)

V_{IH}

$x_0 = 0.774775, y_0 = 0.99996$

$x_0 = 1.00631, y_0 = 0.99988$

$x_0 = 0.774459, y_0 = 1.74562$ ← V_{OH} for equivalent V_{il}
(Using VTC plot)

$x_0 = 1.0059, y_0 = 0.06525$ ← V_{OL} for equivalent V_{IH}

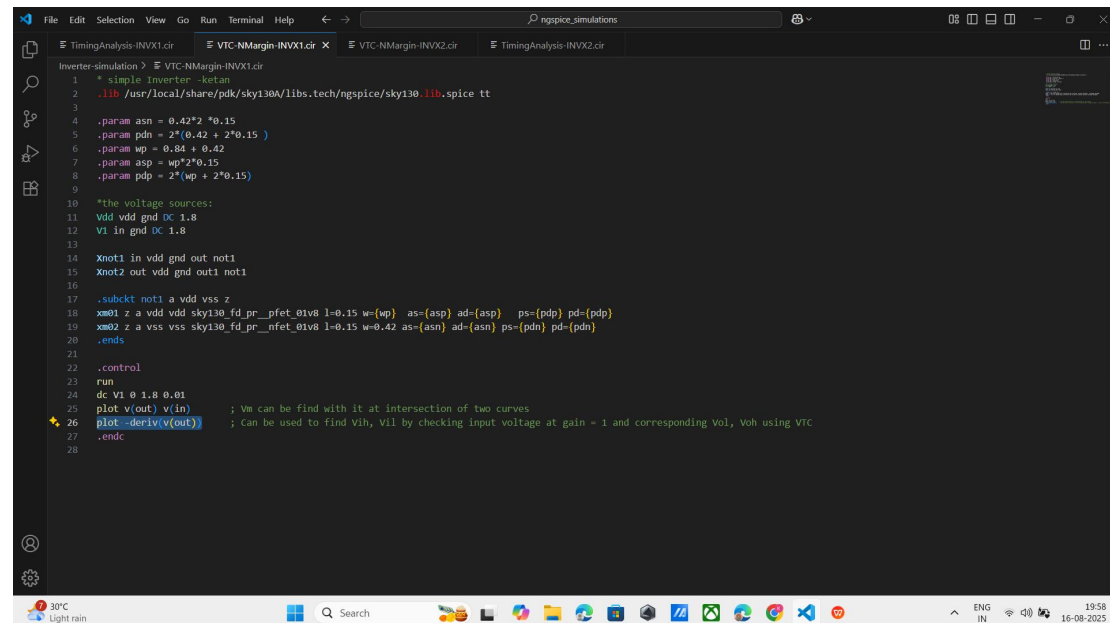
Calculations:

Noise margin High NM_H (V) = $V_{OH} - V_{IH} = 1.745 - 1.006 = 0.739V$

Noise margin Low NM_L (V) = $V_{IL} - V_{OL} = 0.774 - 0.065 = 0.709V$

Inverter Static Characteristic	Value
V_{IH} (V)	1.006
V_{IL} (V)	0.775
NM_H (V)	0.739
NM_L (V)	0.709
Switching Voltage, V_M (V)	0.893

Below is the code for reference:



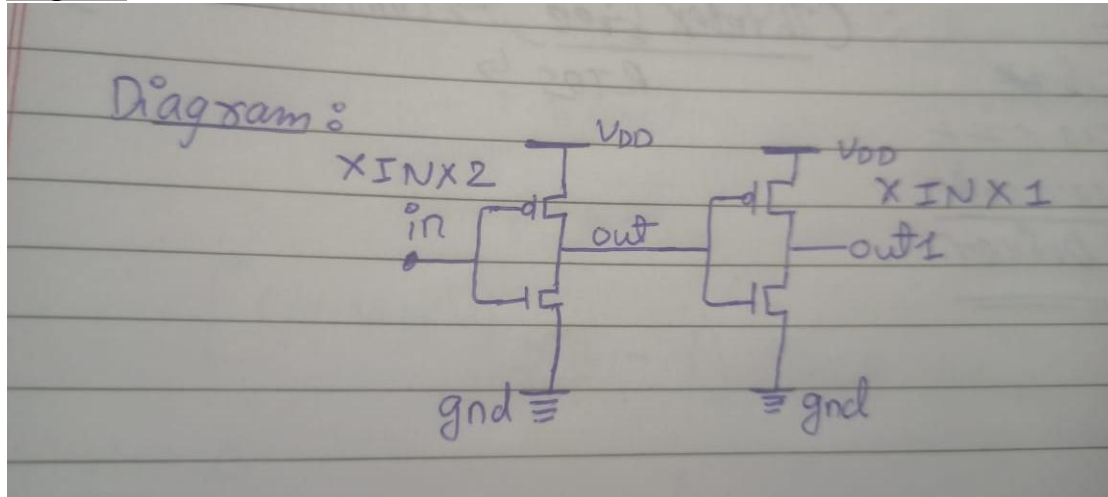
```
1 * simple Inverter -ketan
2 .lib /usr/local/share/pdk/sky130A/libs.tech/ngspice/sky130.lib.spice tt
3
4 .param asn = 0.42*2 *0.15
5 .param pdn = 2*(0.42 + 2*0.15 )
6 .param wp = 0.84 + 0.42
7 .param asp = wp*2*0.15
8 .param pdp = 2*(wp + 2*0.15)
9
10 *the voltage sources:
11 Vdd vdd gnd DC 1.8
12 Vi in gnd DC 1.8
13
14 Xnot1 in vdd gnd out not1
15 Xnot2 out vdd gnd out1 not1
16
17 .subckt not1 a vdd vss z
18 xm01 z a vdd vdd sky130_fd_pr__pfet_01v8 l=0.15 w={wp} as={asp} ad={asp} ps={pdp} pd={pdp}
19 xm02 z a vss vss sky130_fd_pr__nfet_01v8 l=0.15 w={0.42} as={asn} ad={asn} ps={pdn} pd={pdn}
20 .ends
21
22 .control
23 run
24 dc Vi 0 1.8 0.01
25 plot v(out) v(in) ; Vm can be find with it at intersection of two curves
26 plot -deriv v(out) ; Can be used to find Vih, Vil by checking input voltage at gain = 1 and corresponding Vol, Voh using VTC
27 .endc
28
```

Comment: By doing trial and error method for the given NMOS width of $0.42\ \mu\text{m}$ the PMOS width has been tuned to $1.26\ \mu\text{m}$ so that symmetric inverter has been achieved whose rise and fall time are approximately equal with error of 0.028% (or 0.0053 ps) .

Q2) Let's call the inverter in Q1 as INVX1 (strength-1 inverter). Design a strength-2 inverter (INVX2) and report all the tabular parameters above when the INVX2 is loaded with INVX1. Comment on the results obtained.

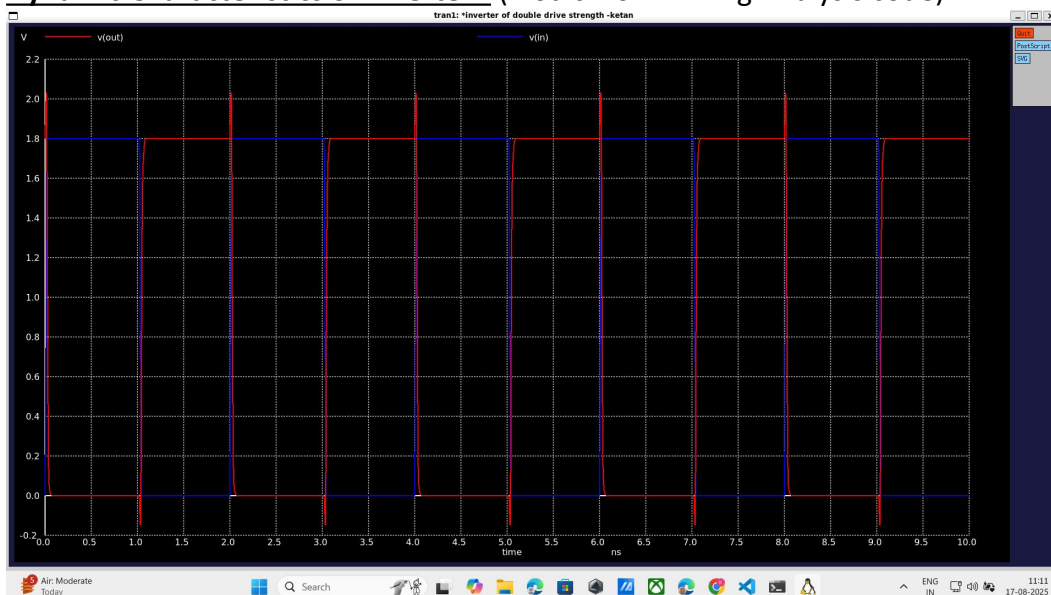
Solution:

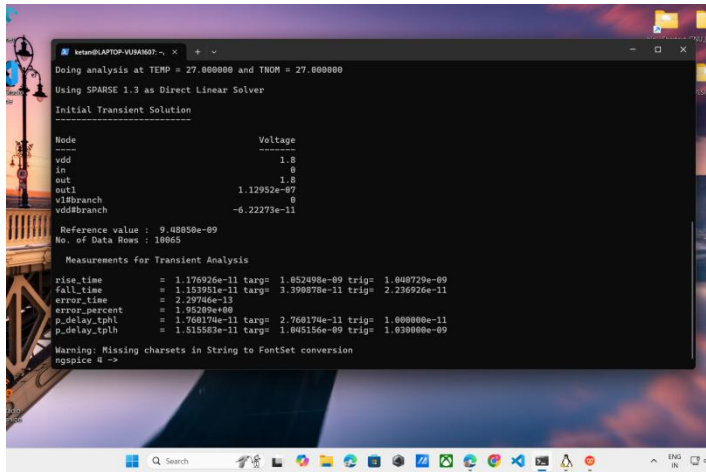
Diagram:



Inverter Design Parameter (For INVX2)	Value
PMOS Width (W_P) (μ_m)	2.52
PMOS Length (L_P) (μ_m)	0.15
NMOS Width (W_N) (μ_m)	0.84
NMOS Length (L_N) (μ_m)	0.15

Dynamic Characteristics of Inverter:- (Plot is from Timing Analysis code)





(Param is from TimingAnalysis code)

Inverter Dynamic Characteristic	Value
Rise time, tr (ps) (20% to 80%)	11.77
Fall time, tf (ps) (80% to 20%)	11.54
Propagation delay, tp (ps)	16.38

By doing trial and error method for the given NMOS width of $0.84 \mu\text{m}$ the PMOS width has been tuned to $2.52 \mu\text{m}$ so that symmetric inverter has been achieved whose rise and fall time are approximately equal with error of 1.952%

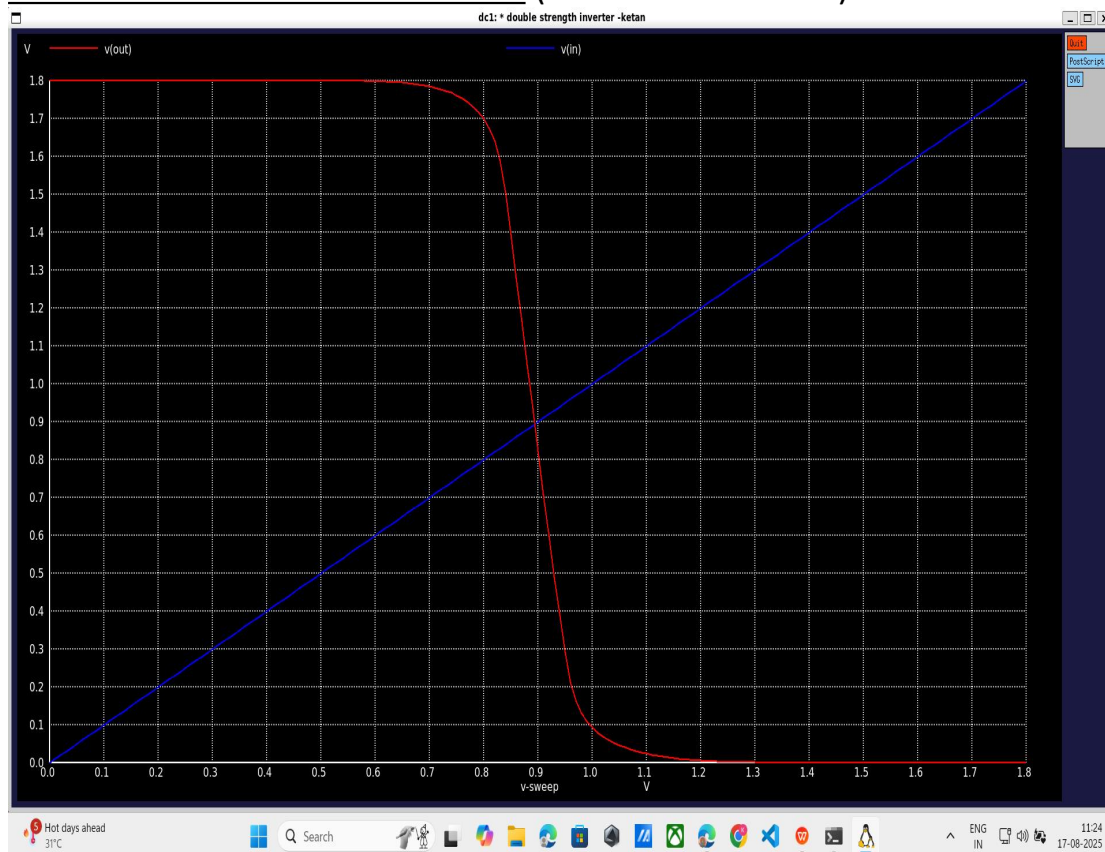
Below is the code for reference:- (Code for Timing Analysis)

```

File Edit Selection View Go Run Terminal Help ngspice_simulations
TimingAnalysis-INVX1.cir VIC-NMargin-INVX1.cir TimingAnalysis-INVX2.cir VIC-NMargin-INVX2.cir
Inverter simulation > TimingAnalysis-INVX2.cir
1 *Inverter of Double drive Strength
2 .lib /usr/local/share/pdk/sky130/130nm.tech/ngspice/sky130.lib.spice tt
3
4 .param asn = 0.42*2*0.15 ; parameter of nmos
5 .param pdn = 2*(0.42*2*0.15)
6 .param wp = 0.84 + 0.42 ; parameter of pmos
7 .param asp = wp*2*0.15
8 .param pdp = 2*(wp*2*0.15)
9 .param wp2 = 2*wp
10 .param pdp2 = 2*(2*0.42)*(2*0.15)
11 .param pdp2 = 2*(wp2) + (2*0.15)
12
13 *the voltage sources:
14 Vdd vdd gnd DC 1.8
15 Vi in gnd pulse(0 1.8 0p 20p 20p in 2n)
16
17 XINVX2 in vdd gnd out not2 ; Inverter of double drive Strength
18 XINVX1 out vdd gnd out1 not1 ; Inverter of single drive Strength
19
20 .subckt not1 a vdd vss z ; subcircuit for reference inverter
21 xnm1 z a vdd vdd sky130_fd_pr__pfet_01v0 l=0.15 w=(wp) as=(asp) ad=(asp) ps=(pdp) pd=(pdp)
22 xnm2 z a vss vss sky130_fd_pr__nfet_01v0 l=0.15 w=0.42 as=(asn) ad=(asn) ps=(pdn) pd=(pdn)
23 .ends
24
25 .subckt not2 a vdd vss z ; subcircuit for inverter of double drive Strength
26 *nm1 z a vdd vdd sky130_fd_pr__pfet_01v0 l=0.15 w=(wp2) as=2*(asp) ad=2*(asp) ps=(pdp2) pd=(pdp2) ; this format gives error for double Strength in ngspice
27 *nm2 z a vss vss sky130_fd_pr__nfet_01v0 l=0.15 w=2*0.42 as=2*(asn) ad=2*(asn) ps=(pdp2) pd=(pdp2)
28 xnm1 z a vdd vdd sky130_fd_pr__pfet_01v0 l=0.15 w=2.52 as=0.756 ad=0.756 ps=5.64 pd=5.64 ; This values are hard coded as substitute of above format
29 xnm2 z a vss vss sky130_fd_pr__nfet_01v0 l=0.15 w=0.84 as=0.252 ad=0.252 ps=2.28 pd=2.28
30 .ends
31
32 * simulation command for Time analysis:
33 .tran 1ps 10ns 0 1p
34 .measure tran rise_time TRIG v(out) VAL=0.36 RISE=1 TARG v(out) VAL=1.44 RISE=1 ; measure rise and fall times
35 .measure tran fall_time TRIG v(out) VAL=1.44 FALL=1 TARG v(out) VAL=0.36 FALL=1
36 .measure tran error_time PARAM="abs(rise_time - fall_time)" ; measure error time between rise and fall times
37 .measure tran error_percent PARAM="error_time/rise_time" ; measure error percentage
38 .measure tran P_delay_tphl TRIG v(in) VAL= 0.9 RISE=1 TARG v(out) VAL=0.9 FALL=1 ; measure propagation delay from input to output for high to low
39 .measure tran P_delay_tplh TRIG v(in) VAL= 0.9 FALL=1 TARG v(out) VAL=0.9 RISE=1 ; measure propagation delay from input to output for low to high
40
41 .control
42 run
43 plot v(out) v(in)
44 .ends

```

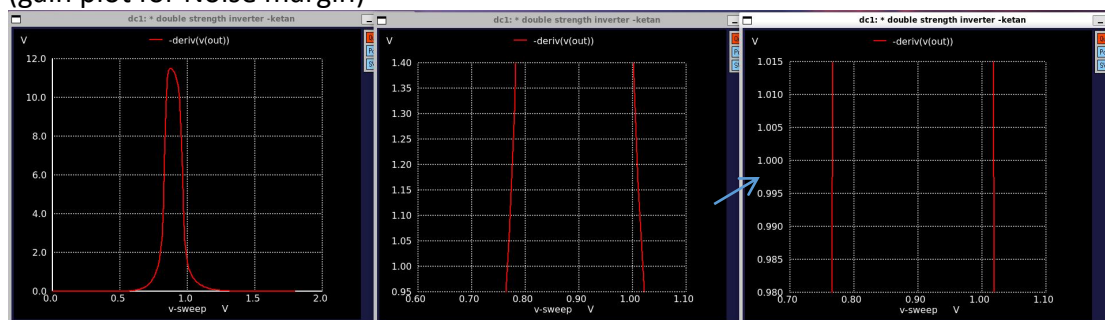

Static Characteristics of Inverter:- (Plot from VTC code)



$$V_m = V_{in} = v_{out}$$

$$x_0 = 0.893649, y_0 = 0.89352$$

(gain plot for Noise margin)



$$V_{IL} \quad x_0 = 0.766667, y_0 = 0.999773$$

$$V_{IH} \quad x_0 = 1.01892, y_0 = 0.999886$$

$$x_0 = 0.767027, y_0 = 1.7464 \quad \leftarrow V_{OH} \text{ for equivalent } V_{IL} \text{ (Using VTC plot)}$$

$$x_0 = 1.01891, y_0 = 0.0708333 \leftarrow V_{OL} \text{ for equivalent } V_{IH}$$

Calculations:

Noise margin High = $V_{OH} - V_{IH} = 1.746 - 1.019 = 0.727V$

Noise margin Low = $V_{IL} - V_{OL} = 0.767 - 0.071 = 0.696V$

Inverter Static Characteristic	Value
V_{IH} (V)	1.019
V_{IL} (V)	0.767
NM_H (V)	0.727
NM_L (V)	0.696
Switching Voltage, V_M (V)	0.8935

Below is the code for reference:

```

1  * Double strength Inverter -ketan
2
3  .lib /usr/local/share/pdk/sky130A/libraries/ngspice/sky130.lib.spice tt
4
5  .param asn = 0.42*2*0.15 ; parameter of nmos
6  .param pdn = 2*(0.42*2*0.15)
7  .param wp = 0.84 + 0.42 ; parameter of pmos
8  .param asp = wp*2*0.15
9  .param pdp = 2*(wp* 2*0.15)
10 .param wp2 = 2*wp ; double drive strength
11 .param pdn2 = 2*((2*0.42)+(2*0.15))
12 .param pdp2 = 2*((wp2) + (2*0.15))
13
14
15 *the voltage sources:
16 Vdd vdd gnd DC 1.8
17 Vi in gnd DC 1.8
18
19 XIMAX2 in vdd gnd out not2 ; Inverter of double drive strength
20 XINX1 out vdd gnd out1 not1 ; Inverter of single drive strength
21
22 .subckt not1 a vdd vss z
23 xm01 z a vdd vdd sky130_fd_pr__pfet_01v8 l=0.15 w={wp} as={asp} ad={asp} ps={pdp} pd={pdp}
24 xm02 z a vss vss sky130_fd_pr__nfet_01v8 l=0.15 w=0.42 as={asn} ad={asn} ps={pdn} pd={pdn}
25 .ends
26 .subckt not2 a vdd vss z
27 *xm01 z a vdd vdd sky130_fd_pr__pfet_01v8 l=0.15 w={wp2} as=2*(asp) ad=2*(asp) ps={pdp2} pd={pdp2} ; this format gives error for double strength in ngspice
28 *xm02 z a vss vss sky130_fd_pr__nfet_01v8 l=0.15 w=2*0.42 as=2*(asn) ad=2*(asn) ps={pdp2} pd={pdp2}
29 xm01 z a vdd vdd sky130_fd_pr__pfet_01v8 l=0.15 w=2.52 as=0.756 ad=0.756 ps=5.64 pd=5.64 ; This values are hard coded as substitute of above format
30 xm02 z a vss vss sky130_fd_pr__nfet_01v8 l=0.15 w=0.84 as=0.252 ad=0.252 ps=2.28 pd=2.28
31 .ends
32
33 .control
34 run
35 dc Vi 0 1.8 0.01
36 plot v(out) v(in) ; Vm can be find with it at intersection of two curves
37 plot -deriv(v(out)) ; can be used to find Vih, Vil by checking input voltage at gain = 1 and corresponding Vol, Voh using VTC
38 .endc
  
```

Observations:-

- As, rise time and fall time is directly proportional to R_{ON} of MOSFETs and inversely proportional to the width of the MOSFET as we increase the width (i.e, strength-2) the rise time and fall time decreased so same is observed in Q2 as compared with Q1 (around 37%).
- Propagation delay for the strength-2 inverter is shorter compared to that of strength-1 inverter. So, we can say that strength-2 inverter has faster switching speed (around 23%).
- Switching Voltage of the Strength-2 inverter is slightly shifted towards right as compared with the Switching Voltage of the Strength-1 inverter (since PMOS strength dominates over NMOS in strength-2 inverter) and also as compared with Strength-1 inverter the Strength-2 inverter switching voltage goes nearer to half of source voltage (i.e, $V_{dd}/2$) (shifted by 0.0006V).