VLSI Design Assignment-1

Name:- Ketan Agarwal
Roll No:- 25M1174

Q1) Design a minimum size CMOS inverter (minimum possible equal rise and fall time) with fixed NMOS and PMOS channel length of 0.15µm (this is the minimum channel length). The minimum channel width for NMOS is fixed to 0.42µm (restriction from the PDK) and the width of PMOS is to be obtained by design. The input should be a rail-to-rail square wave with rise/fall times of 20 PS, and the inverter will be loaded by another minimum size inverter.
Simulate and report the following in the tabular fashion shown below:

Inverter Design Parameter	Value
PMOS Width (W_P) (μ_m)	
PMOS Length (L_P) (μ_m)	
NMOS Width (W_N) (μ_m)	
NMOS Length (L_N) (μ_m)	

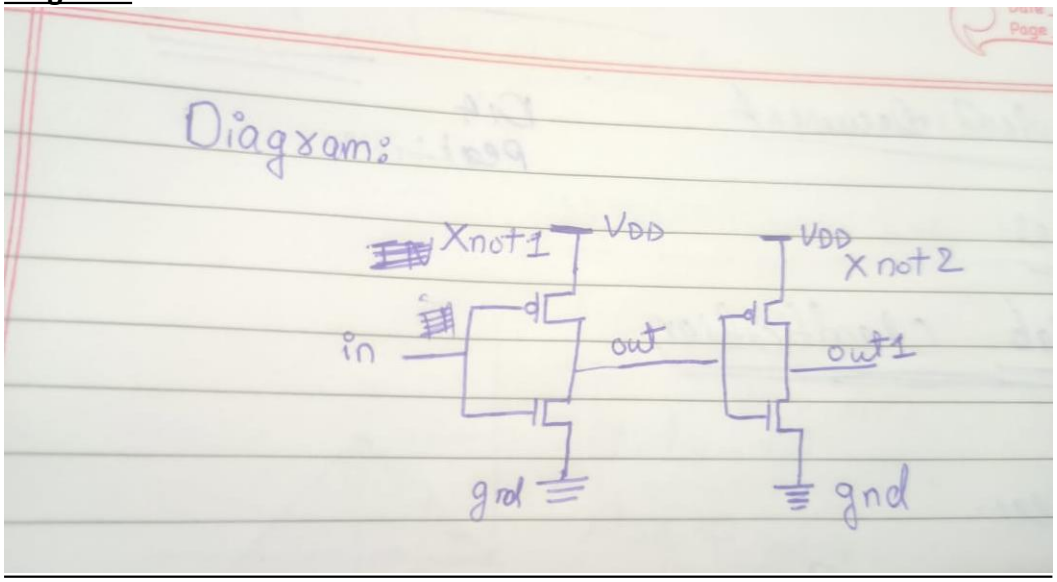
Inverter Dynamic Characteristic	Value
Rise time, tr (ps)	
Fall time, tf (ps)	
Propagation delay, tp (ps)	

Once designed, plot (in the submission) the static transfer characteristics of this inverter by using a DC sweep on the input from 0 to VDD and report the following in the tabular fashion below:

Inverter Static Characteristic	Value
V_{IH} (V)	
V_{IL} (V)	
NM_H (V)	
NM_L (V)	
Switching Voltage, V_M (V)	

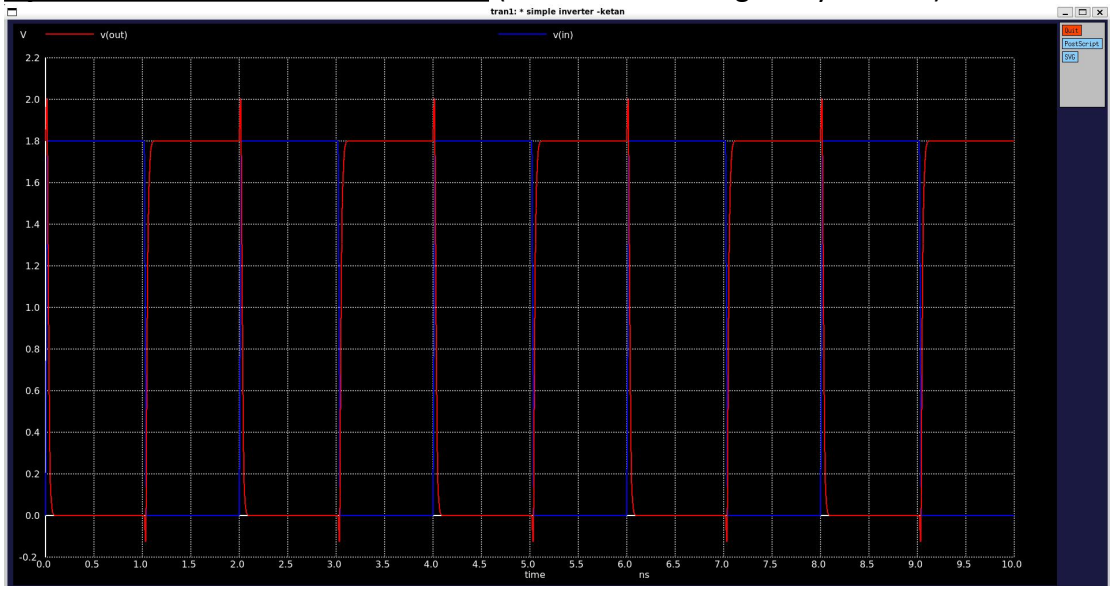
Solution:

Diagram:



Inverter Design Parameter (For INVX1)	Value
PMOS Width (W_P) (μ_m)	1.26 (~3x W_N)
PMOS Length (L_P) (μ_m)	0.15
NMOS Width (W_N) (μ_m)	0.42
NMOS Length (L_N) (μ_m)	0.15

Dynamic Characteristics of Inverter:- (Plot is from Timing Analysis code)

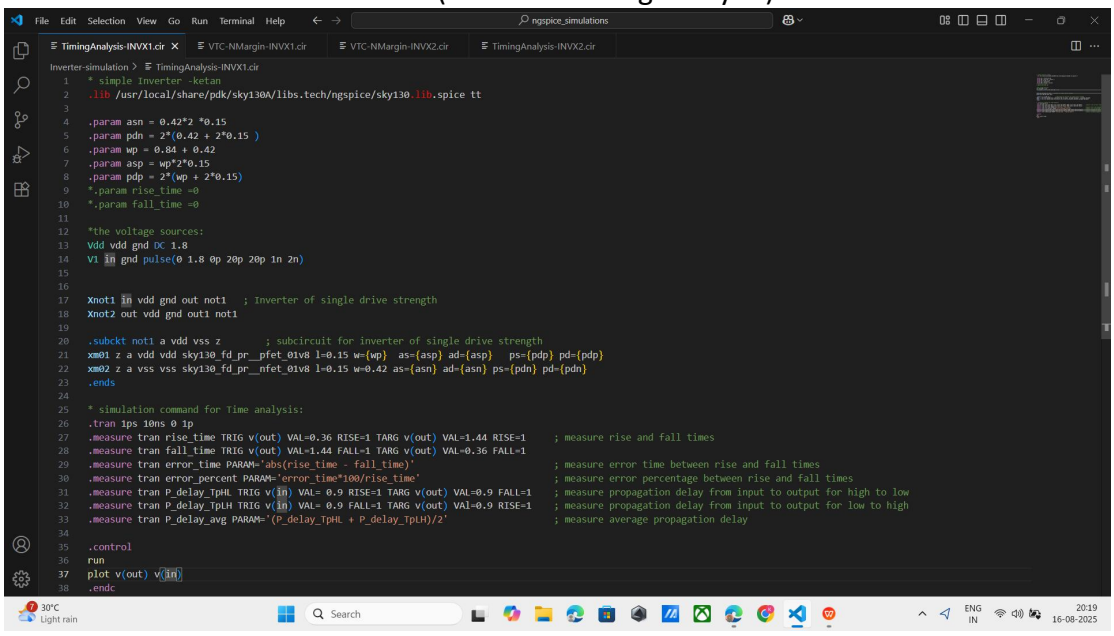


```
Circuit: * simple inverter -ketan

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vdd                                        1.8
in                                           0
out                                        1.8
out1                                 1.12952e-07
v1#branch                                    0
vdd#branch                          -6.21766e-11

 Reference value :  9.13250e-09
No. of Data Rows : 10065

  Measurements for Transient Analysis

rise_time            =  1.852437e-11 targ=  1.061191e-09 trig=  1.042667e-09
fall_time            =  1.851907e-11 targ=  4.307560e-11 trig=  2.455652e-11
error_time           =  5.30087e-15
error_percent        =  2.86156e-02
p_delay_tphl         =  2.280225e-11 targ=  3.280225e-11 trig=  1.000000e-11
p_delay_tplh         =  1.975849e-11 targ=  1.049758e-09 trig=  1.030000e-09
p_delay_avg          =  2.12804e-11
```

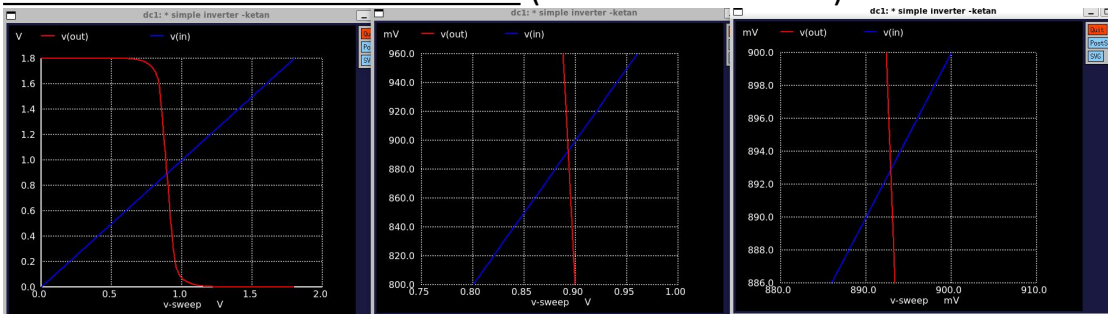
(parameters from Timing analysis code)

Inverter Dynamic Characteristic	Value
Rise time, tr (ps) (20% to 80%)	18.52
Fall time, tf (ps) (80% to 20%)	18.51
Propagation delay, tp (ps)	21.28

Below is the code for reference:- (Code for Timing Analysis)

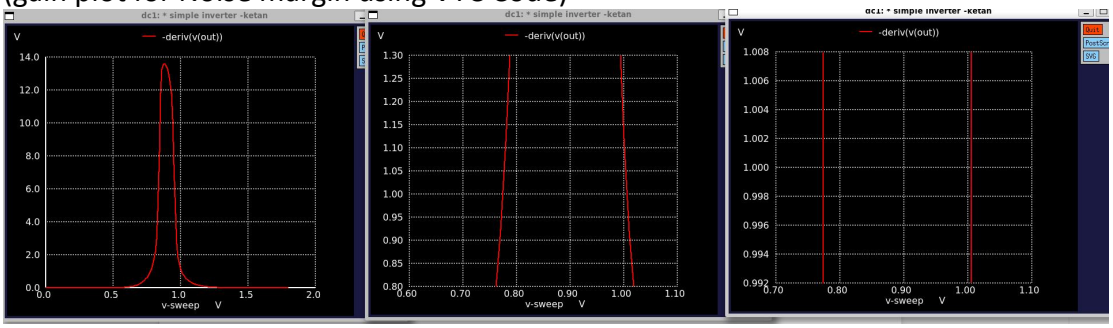


Static Characteristics of Inverter:- (Plot from VTC code)

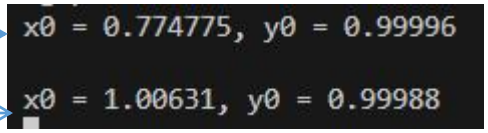


Vm = Vin = vout

(gain plot for Noise margin using VTC Code)



V_{IL} (using gain plot)



V_{IH}

V_{OH} for equivalent V_{il} (Using VTC plot)

V_{OL} for equivalent V_{IH}

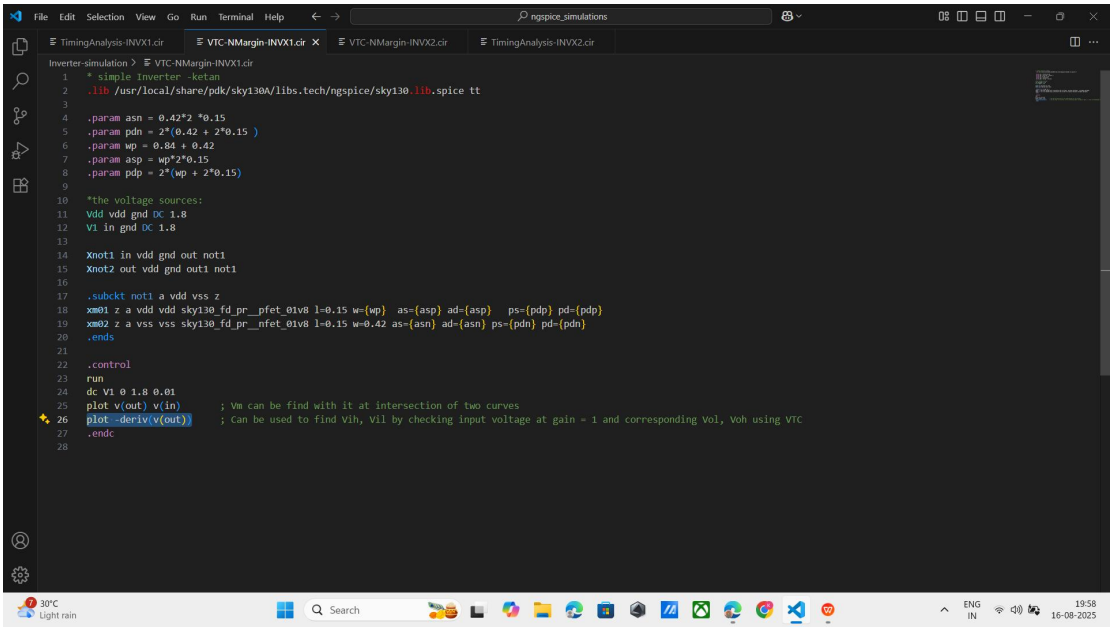
Calculations:

Noise margin High NM_H (V) = V_{OH} - V_{IH} = 1.745 - 1.006 = 0.739V

Noise margin Low NM_L (V) = V_{IL} - V_{OL} = 0.774 - 0.065 = 0.709V

Inverter Static Characteristic	Value
V_{IH} (V)	1.006
V_{IL} (V)	0.775
NM_H (V)	0.739
NM_L (V)	0.709
Switching Voltage, V_M (V)	0.893

Below is the code for reference:

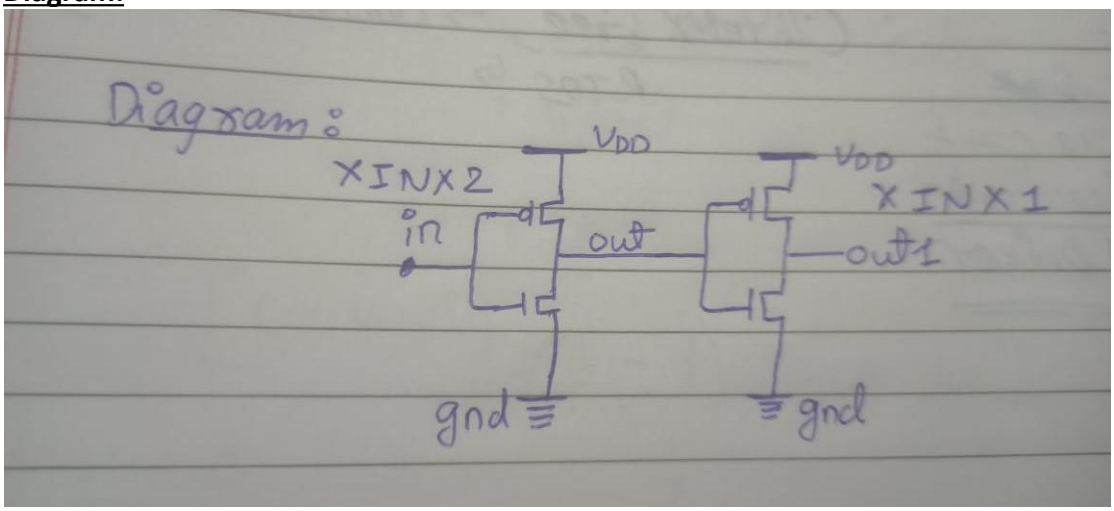


Comment: By doing trial and error method for the given NMOS width of 0.42 µm the PMOS width has been tuned to 1.26 µm so that symmetric inverter has been achieved whose rise and fall time are approximately equal with error of 0.028% (or 0.0053 ps) .

Q2) Let's call the inverter in Q1 as INVX1 (strength-1 inverter). Design a strength-2 inverter (INVX2) and report all the tabular parameters above when the INVX2 is loaded with INVX1. Comment on the results obtained.

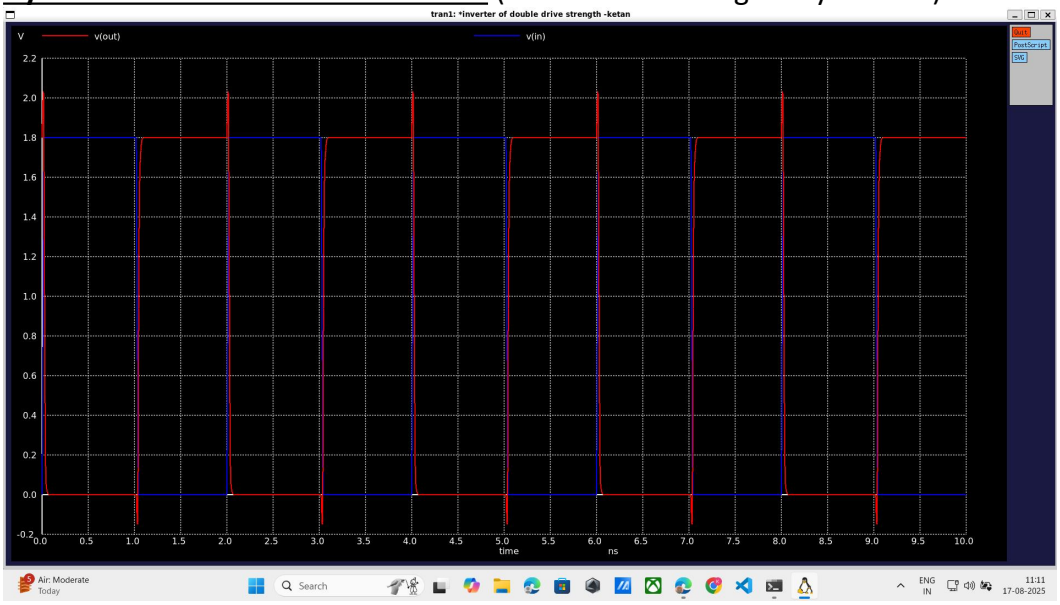
Solution:

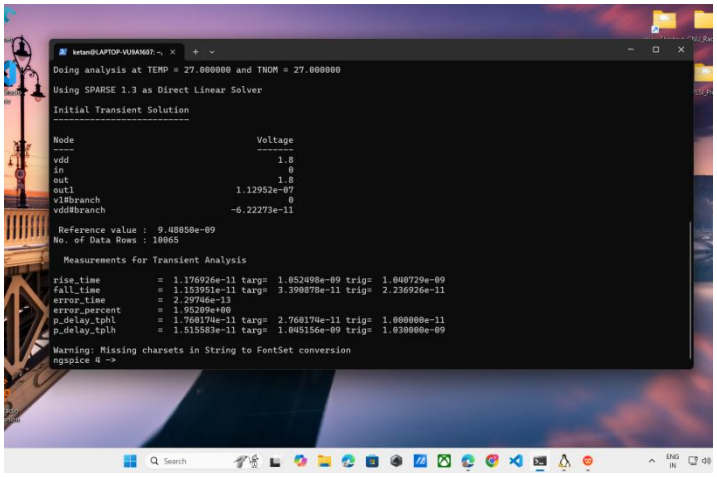
Diagram:



Inverter Design Parameter (For INVX2)	Value
PMOS Width (W_P) (μ_m)	2.52
PMOS Length (L_P) (μ_m)	0.15
NMOS Width (W_N) (μ_m)	0.84
NMOS Length (L_N) (μ_m)	0.15

Dynamic Characteristics of Inverter:- (Plot is from Timing Analysis code)



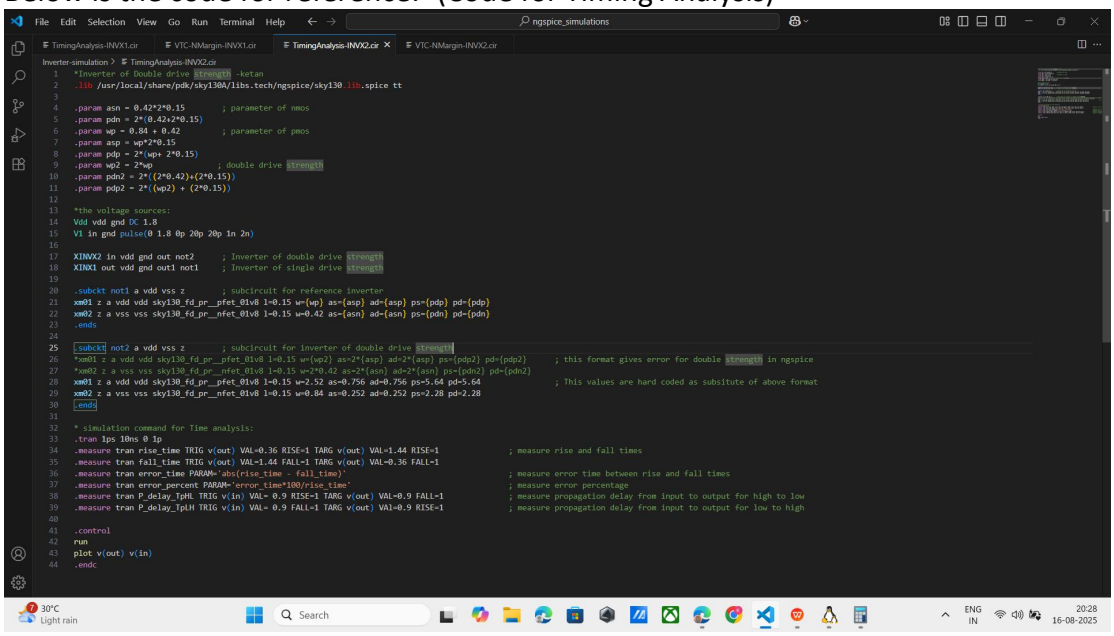


(Param is from TimingAnalysis code)

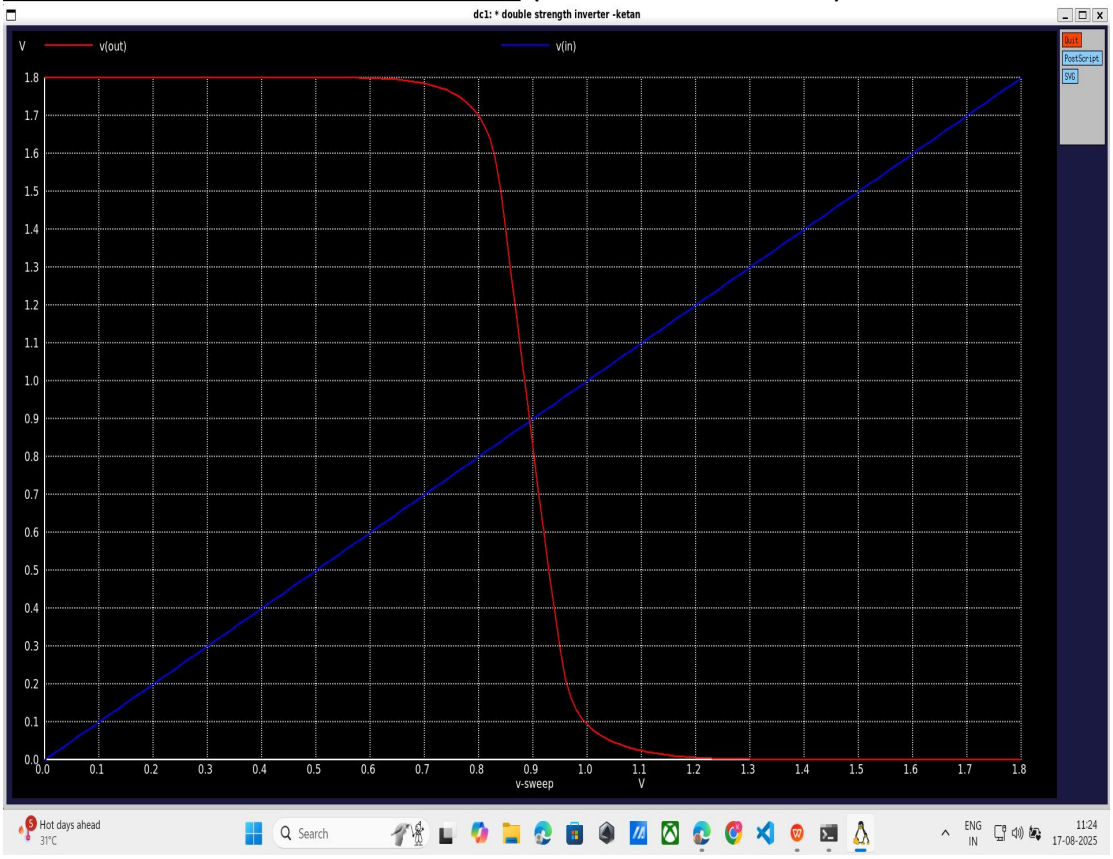
Inverter Dynamic Characteristic	Value
Rise time, tr (ps) (20% to 80%)	11.77
Fall time, tf (ps) (80% to 20%)	11.54
Propagation delay, tp (ps)	16.38

By doing trial and error method for the given NMOS width of 0.84 µm the PMOS width has been tuned to 2.52 μ_m so that symmetric inverter has been achieved whose rise and fall time are approximately equal with error of 1.952%

Below is the code for reference:- (Code for Timing Analysis)



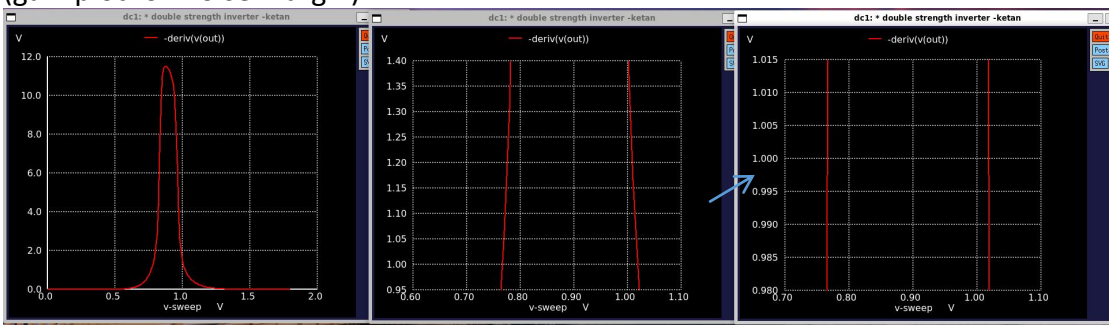
Static Characteristics of Inverter:- (Plot from VTC code)



Vm = Vin = vout

```
x0 = 0.893649, y0 = 0.89352
```

(gain plot for Noise margin)



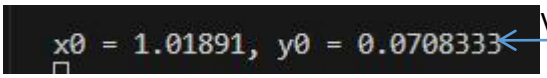
V_{IL} (using gain plot)

V_{IH}

```
x0 = 0.766667, y0 = 0.999773

x0 = 1.01892, y0 = 0.999886
```

```
x0 = 0.767027, y0 = 1.7464
```

V_{OH} for equivalent V_{il} (Using VTC plot)



V_{OL} for equivalent V_{IH}

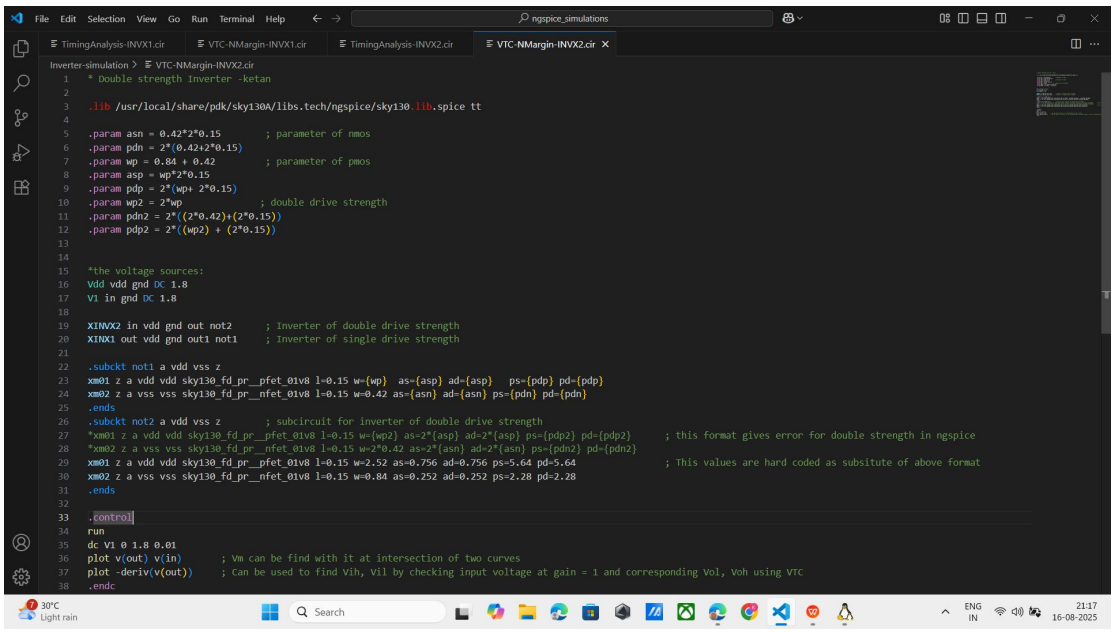
Calculations:

Noise margin High = V_{OH} - V_{IH} = 1.746 - 1.019 = 0.727V

Noise margin Low = V_{IL} - V_{OL} = 0.767 - 0.071 = 0.696V

Inverter Static Characteristic	Value
V_{IH} (V)	1.019
V_{IL} (V)	0.767
NM_H (V)	0.727
NM_L (V)	0.696
Switching Voltage, V_M (V)	0.8935

Below is the code for reference:



Observations:-

- As, rise time and fall time is directly proportional to RON of MOSFETs and inversely proportional to the width of the MOSFET as we increase the width (i.e, strength-2) the rise time and fall time decreased so same is observed in Q2 as compared with Q1 (around 37%).
- Propagation delay for the strength-2 inverter is shorter compared to that of strength-1 inverter. So, we can say that strength-2 inverter has faster switching speed (around 23%).
- Switching Voltage of the Strength-2 inverter is slightly shifted towards right as compared with the Switching Voltage of the Strength-1 inverter (since PMOS strength dominates over NMOS in strength-2 inverter) and also as compared with Strength-1 inverter the Strength-2 inverter switching voltage goes nearer to half of source voltage (i.e, Vdd/2) (shifted by 0.0006V).