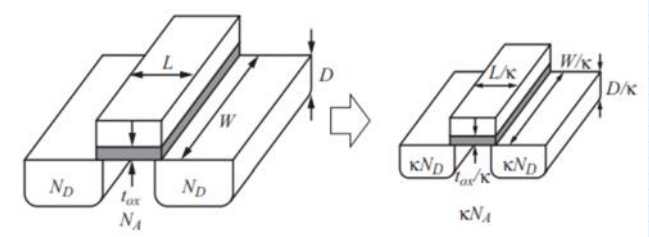
Lecture - 2



Scaling of FETs in CMOS process :-

1) The No of MOSFETs on a chip $\alpha \frac{1}{WL}$ $\Rightarrow$ Scales as $K \times K = \boxed{K^2}$

No of MOS $\uparrow K^2$.

2) The speed of MOSFETs $\alpha \frac{1}{L}$ $\Rightarrow$ Scales as $\boxed{K}$

Speed $\uparrow K$

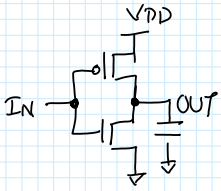
3) Gate-oxide capacitance, $C = \frac{\epsilon A}{d} = \frac{\epsilon WL}{t_{ox}}$

$\Rightarrow \alpha \frac{1/K \times 1/K}{1/K}$ $\Rightarrow$ scales as $\boxed{1/K}$

Gate cap $\downarrow K$

4) Energy :-

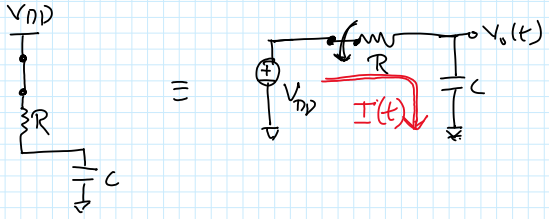
* Consider a switching circuit using CMOS



a) when IN = Logic-0, PMOS → ON & NMOS OFF.

Acting like switches

Any 'ON' switch has a finite resistance & the equivalent model.



The energy supplied by the source is computed by integrating source power

i.e $E_{source} = \int_0^\infty V_{DD} \cdot I(t)\, dt$

For a switching RC circuit, $I(t) = \frac{V_{DD}}{R}\left[e^{-t/RC}\right]$

[Assuming zero charge on C initially i.e cap was discharged previously]

$\therefore E_{source} = V_{DD} \cdot \frac{V_{DD}}{R} \int_0^\infty \left(e^{-t/RC}\right) dt$

$= \frac{V_{DD}^2}{R} e^{-t/RC} \Big|_0^\infty (-RC) = \boxed{V_{DD}^2 C}$

Energy from source

$$= \frac{V_{DD}^2}{R} \; e^{-t/RC} \Big|_0^{\infty} (-RC) = \boxed{V_{DD}^2 C}$$

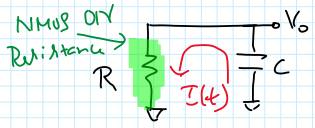
Energy from source

The energy stored on a capacitor is $\boxed{\frac{1}{2}CV^2}$

Energy on cap

$\Rightarrow \frac{1}{2}CV^2$ is lost on the resistor (dissipated as heat)

* Now consider the case when input is logic high and the cap was previously charged to V_{DD} by the PMOS switch. The equivalent model is:-



At the end of this, the total charge on the capacitor is zero (i.e, V_o is 0, & the cap is fully discharged, i.e logic-low output)

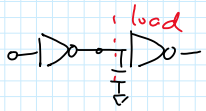
Since all the charges on the capacitor are lost, the energy of cap ($\frac{1}{2}CV^2$) must be dissipated on the resistor.

$\therefore$ $\frac{1}{2}CV^2$ is lost on the resistor, this time on the NMOS side !! (dissipated as heat)

* At the end of the operation, a total of CV^2 ($\frac{1}{2}CV^2$ on PMOS side & $\frac{1}{2}CV^2$ on NMOS) energy is lost/dissipated in the circuit [this energy is provided by the supply V_{DD}]

$\therefore$ Energy dissipation $\rightarrow \propto CV^2$.

* Usually in a digital circuit every gate sees another gate as a load



$\therefore$ C is approximately same as the gate capacitance we computed and scales as $1/K$.

* As we scale technology, the same Electric field can be maintained for the same performance as previous technology node

$$\text{Electric field (to crack channel)} = \frac{V_{DD}}{t_{ox}}$$

Since $t_{ox} \downarrow K$, V_{DD} can also be $\downarrow K$

Inherent assumption that V_{TH} of MOSFETs also scale down (not proportionally) with technology.

with technology.

* We go back to discussion on energy.

Energy dissipated is CV^2, $C \propto 1/k$ and $V \propto 1/k$

$\Rightarrow$ Energy dissipated $\propto \boxed{1/k^3}$

Energy dissipated $\downarrow k^3$

5) Power = $\frac{\text{Energy}}{\text{Time}}$

* Assuming that the NMOS & PMOS (in our circuit above) are periodically switching with period T (or frequency f),

Power dissipated = $\frac{CV^2}{T} = CV^2 f$.

* In a digital circuit there are plenty of gates/flip-flops etc which are NOT all switching at the same time. We define an average switching factor called, activity factor (α alpha) to compute average power consumption

$\therefore P_{diss} = \alpha C V^2 f$

$\therefore$ Power dissipated $\propto$ (proportional) $C \; V_{DD}^2 \; f$

$C \propto 1/k$, $V_{DD}^2 \propto 1/k^2$, $f \propto k$

$\Rightarrow \boxed{P_{dissipated} \propto 1/k^2}$

Power dissipation $\downarrow k^2$ with scaling

i.e For same functionality on chip, the power dissipation/heating of a digital IC $\downarrow k^2$ with technology scaling

6) Power density.

with scaling, power dissipation $\downarrow k^2$ & $\boxed{\text{No of transistors} \uparrow k^2}$ (More functionality on a chip)

$\Rightarrow$ Power density = $1/k^2 \times k^2 = \boxed{1}$.

Implying with scaling, the functionality can be increased on a chip with no additional power/heat dissipation !!!

* while these are true for traditional CMOS technology, below 65nm node,

(a) The V_{DD} does NOT scale down as k

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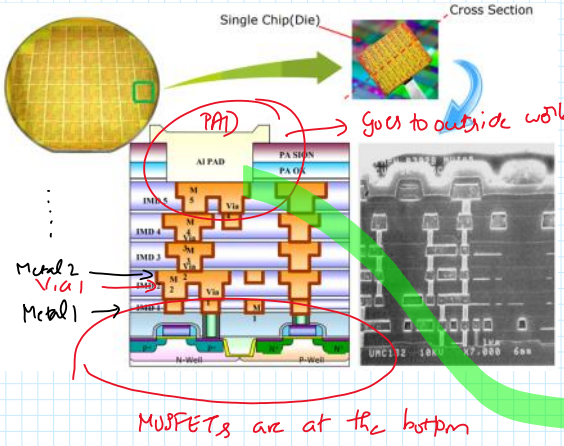
(b) Due to reduced control over the channel with scaling, the leakage current ↑ and adds more power dissipation.

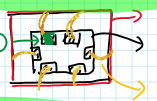
To tackle this new devices like FinFET's, RibbonFET's are replacing traditional CMOS

More info on this is provided via video links on Moodle.

We stick with CMOS in this course (specifically 130nm process)

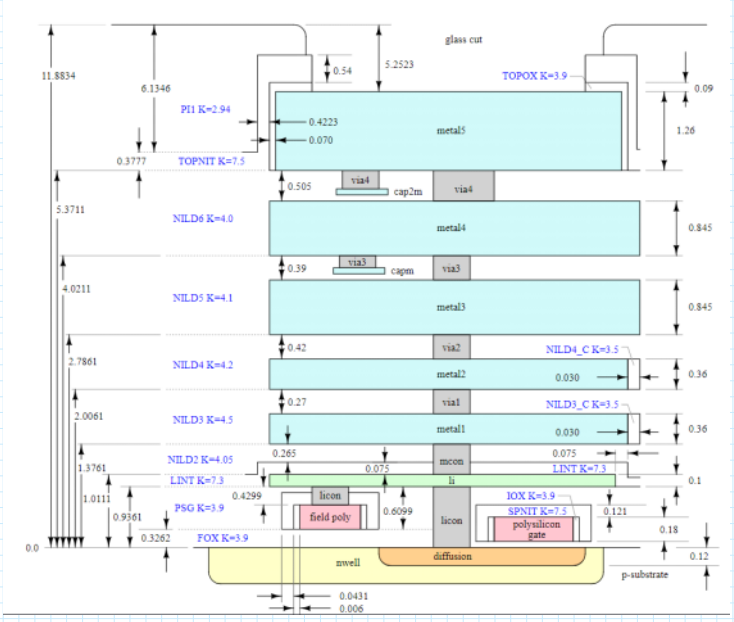


* A chip is like building a tall structure in 3D with MOS on bottom & Metals at top
* Metals (used as wires) are used for signal & supply connections
* Every layer of metal is connected to another metal layer using a "Via" (Similar to a 4-layer PCB or higher but nano scale)



PAD talks to outside world

* The 130nm Skywater process stack is shown below:-



Z-Direction (Stack)

* The thickness of metal or any other layer is fixed for a process & not a design variable.
* Observe that metal thickness increases with higher metals (Metal 5 > 4 > 3...)

This is because the metals have finite routing (or wire) resistance

* The current will be highest at higher metals (since the PAD is connected to highest metal and it has to distribute current to MOSFETs at lowest metal)

∴ To reduce IR power dissipation due to metal wires, Metal thickness are not the same for all layers ($R = \rho l/A$)

Each process technology has a specific set of design rules to be strictly adhered to

This is due to what can be & cannot be fabricated in the foundry for a given technology

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Table 3 Table 2 - Minimum CDs in Design or on Wafer, required by Technology

Layer Name	Feature Size	Space Size
Metal 1	0.14	0.14
Metal 1 - Cu	0.14	0.14
Via	0.15	0.17
Via - Cu	0.18	0.13
Capacitor MiM	2	0.84
Metal 2	0.14	0.14
Metal 2 - Cu	0.14	0.14
Via 2-TNV	0.28	0.28

→ Example design rule specification for CMOS 130nm Skywater.

→ Spacing between 2 metal-1 layers (space bit routed)

→ Minimum width of metal-1 layer (wire width can be higher than this but not lower)

→ Spacing between 2 via-1's (via1 connects metal 1 to metal 2)

→ Minimum size of via-1

⋮ etc for other layers

← Checks all the design rules like these are not violated

* Before chip fabrication a DRC (Design Rule Check) is performed before submitting the final design files to the foundry for fabrication