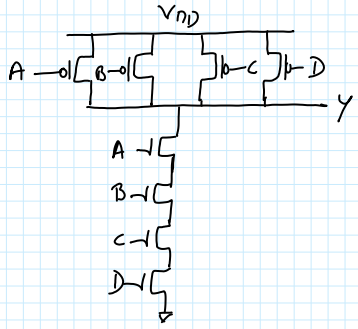
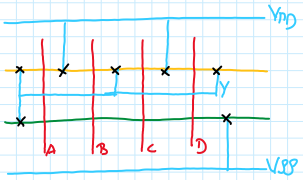
Lecture - 9

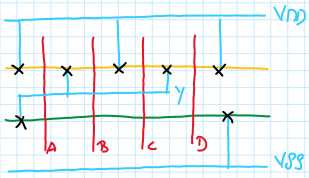
We continue our discussion on stick diagram.

* 4 input NAND gate

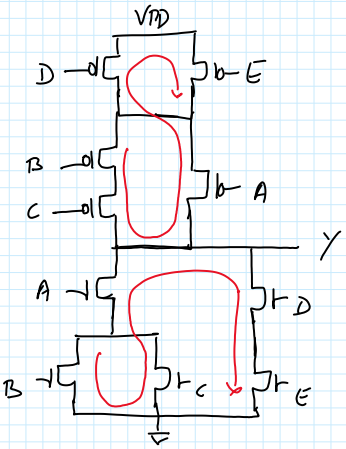




OR

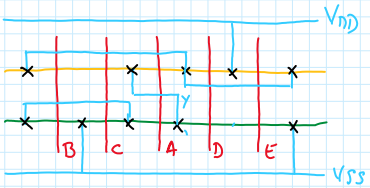


* Now consider the logic $Y = \overline{A(B+C) + D \cdot E}$



* To determine the ordering of gates (or poly), form a common Euler path on the PMOS and NMOS side
  ↳ A Euler path dictates a traversal through all nodes exactly once

Eg: The path DBCAE → No path on NMOS side
DEBAC → No path on PMOS side
CBADE → No path on PMOS side
BCADE → ✓



* So far we have looked at following cells in the standard cell library

→ INVERTER
→ 2NAND
→ 3NAND
→ 4NAND
→ 2NOR
→ 3NOR
→ 4NOR
↓
different inputs

} X1, X2, X4 etc → different strengths

* Other useful combinational logic cells are 2to1 multiplexer, XOR gate, AOI (AND-OR-INVERT), OAI (OR-AND-INVERT) etc
* We will look at XOR gates later. Now consider the 2 to 1 multiplexer
* Remember:

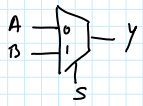
```
if (s)
begin
.
end
```

This Verilog code will be synthesized as a 2-to-1 multiplexer with 's' as select

```
begin
  .
end
else
begin
  :
end
```

This Verilog code will be synthesized as a 2-to-1 multiplexer with 's' as select

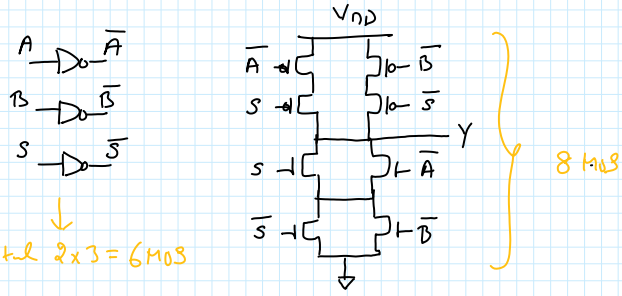
* For a 2to1 MUX, $Y = A\bar{S} + BS$



To implement the static CMOS logic,

$$Y = \overline{A\bar{S} + BS} = \overline{(A\bar{S})(BS)}$$

$$= \overline{(\bar{A}+S)\cdot(\bar{B}+\bar{S})}$$

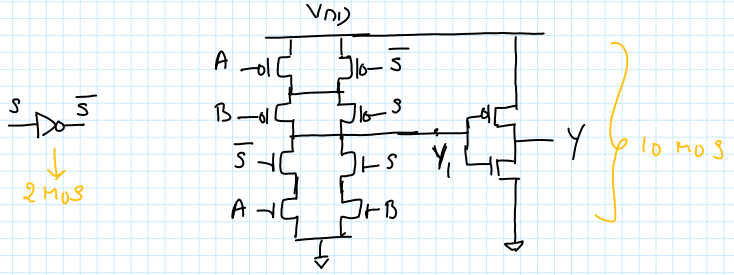


. Total of 14 MOS to implement a 2-to-1 MUX.

* Now consider another implementation.

$Y = A\bar{S} + BS$, $Y_1 = \bar{Y} = \overline{A\bar{S} + BS}$ → First implement this CMOS

& $Y = \bar{Y_1}$ → & invert the output.



. Total of 12 MOS only to implement a 2-to-1 MUX !!!

* Homework :- Figure out the sizing and the stick diagram for MUX.

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* Consider an AOI22 gate. 22 implies 2 inputs each (total 4 inputs) to AND gate.

. $Y = \overline{(AB) + (CD)}$

* An OAI22 gate will have

$Y = \overline{(A+B)(C+D)}$

* An OAI22 gate will have

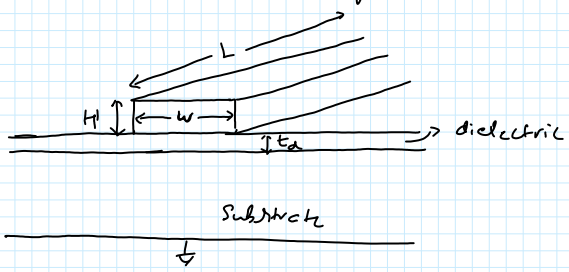
$$Y = \overline{(A+B)(C+D)}$$

* Homework - work out the MOS schematic and stick diagram for these gates

— x — x —

* From a full chip perspective, interconnects are an important aspects. They are usually metal lines that connect different points on a chip
* A modern chip (eg 10mm x 10mm) has total interconnect lengths upto few Kms to 10's of Kms
  (mm) (Km) COMPLEX ROUTING!!!
* While modern tools handle the complex routing, it is important to have understanding of the impact of an interconnect on a chip

* Consider a metal shown below, on a substrate. Usually there is an oxide (typically SiO_2) around the metal acting as insulator between adjacent metals.



- The resistance of the wire is given by $R = \rho \frac{L}{A}$ Usually Aluminium is used as metal (today there are also copper being introduced due to lower ρ)

$$R = \frac{\rho . L}{W \times H}$$

$$= \left(\frac{\rho}{H}\right) \frac{L}{W}$$

→ Constant for a given process/technology

$$R = \left(\rho_{\square}\right) \frac{L}{W}$$

, $\rho_{\square}$ → Sheet resistance and the number is provided by the fabrication foundry for poly, and different metals.
→ Using this number we can compute R, by simply multiplying by our designed (L/W)

- The capacitance (bit metal & substrate) is

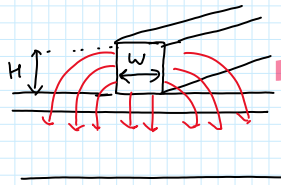
$$C = \frac{\epsilon_0 \epsilon_r A}{d} = \frac{\epsilon_0 \epsilon_d (L.W)}{t_d}$$, $\epsilon_d = 3.9$ for SiO_2

$$C = \left(\frac{\epsilon_0 \epsilon_d}{t_d}\right)(L\,W)$$

→ Constant for given technology.

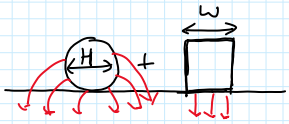
- In modern chips, with scaling "W" has to decrease to increase the routing density

o In modern chips, with scaling "W" has to decrease to increase the routing density (i.e for the same area, No of transistors ↑ ⇒ routing ↑)



Fringe fields are dominant (i.e fringe capacitance)

* Can be modeled as a cylindrical conductor (for fringe cap) in combination with plate conductor

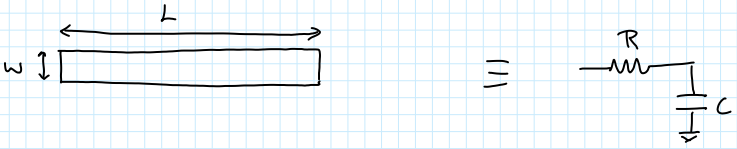


* For intuition, we will stick with zero fringe fields and see the impact of interconnect on the delay

* We can compute the time constant, τ as a measure of the delay due to interconnect

* There are 2 approaches (a) Lumped RC model
(b) Distributed RC model

(a) Lumped RC model

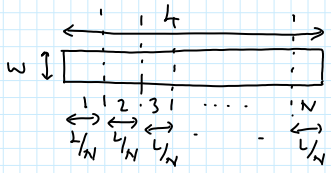


$$\tau = RC = \rho_{\square} \frac{L}{W} \times \left(\frac{\epsilon_0 \epsilon_d}{t_d}\right) L.W$$

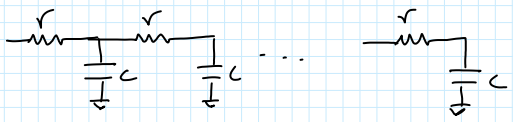
$$\tau = \left(\frac{\rho_{\square} \epsilon_0 \epsilon_d}{t_d}\right) L^2$$

* Doubling the interconnect length L → quadruples the delay !!!

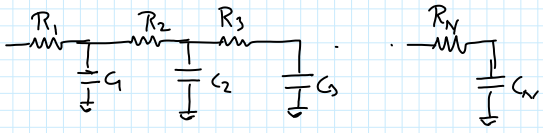
(b) Distributed RC model



* Divide line into "N" segments of length L/N



Consider the network -



* From Elmore's delay, we can compute τ upto a first order as

$$\tau = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3) C_3 + \ldots (R_1 + R_2 + \ldots R_N) C_N$$

in our case, $R_1 = R_2 = \ldots R_N = r$

$\tau = r_1 c_1 + (r_1 + r_2) c_2 + (r_1 + r_2 + r_3) c_3 + \ldots + (r_1 + r_2 + \ldots + r_N) c_N$

in our case, $R_1 = R_2 = \ldots R_N = r$

$C_1 = C_2 = \ldots C_N = c$

$\therefore \tau = rc\left[1 + 2 + 3 + \ldots N\right] = rc\,\frac{N(N+1)}{2}$

Also, $r = \rho_\square \left(\frac{L}{N}\right)\frac{1}{W}$ and $C = \left(\frac{\epsilon_0 \epsilon_d}{t_d}\right)\left(\frac{L}{N}\right) \cdot W$

$\therefore \tau = \rho_\square \left(\frac{L}{N}\right)\frac{1}{W} \times \frac{\epsilon_0 \epsilon_d}{t_d}\left(\frac{L}{N}\right) W \cdot \frac{N(N+1)}{2}$

$\tau = \left(\frac{\rho_\square \epsilon_0 \epsilon_d}{t_d}\right) L^2 \cdot \frac{N(N+1)}{2N^2}$

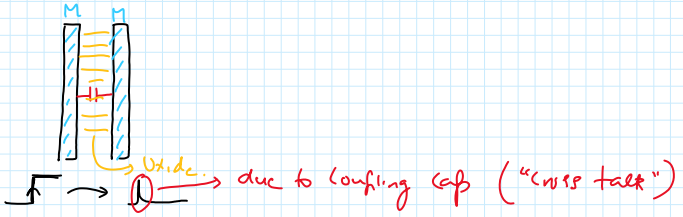
* For very fine segments $N \to \infty$ and $N(N+1) \to N^2$

$\therefore \tau = \left(\frac{\rho_\square \epsilon_0 \epsilon_d}{t_d}\right)\frac{L^2}{2}$

* The lumped RC model is a pessimistic delay model for an interconnect!!!

— x —

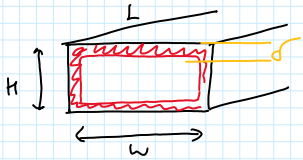
* There are also coupling capacitance b/t adjacent metal traces.



* Those are complex design challenges that cannot be solved (for digital design) using pen-paper and we have to use design tools
* While the tool does all the internal delay computation during routing, a model called as "wireline model" is to be fed as input to the tool. This "wireline model" data comes from the fabrication foundry and has details on the R, C and L of the different interconnects (Metal 1, Metal 2, ... etc)

— x —

* A few things to notice
  * we have ignored "L" effect. However, a wire with high frequency excitation (eg:- clock line) behaves like a high impedance line!
  * At high frequencies :- effect of "skin depth" comes into play. and the "skin depth" $\propto 1/\sqrt{f}$



Intuitively, the cross-section area will reduce (WH vs $2(W+H)\delta$) and R ↑ ($\because R \propto 1/A$)

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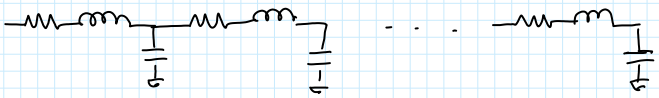
* Further, the RC delay line model will have to be replaced by an equivalent RLC model.



Now we deal with transmission lines (Reflection, standing waves etc) which is outside the scope of this course