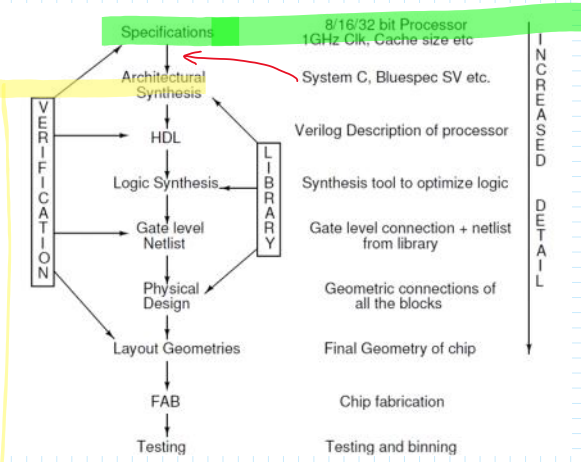
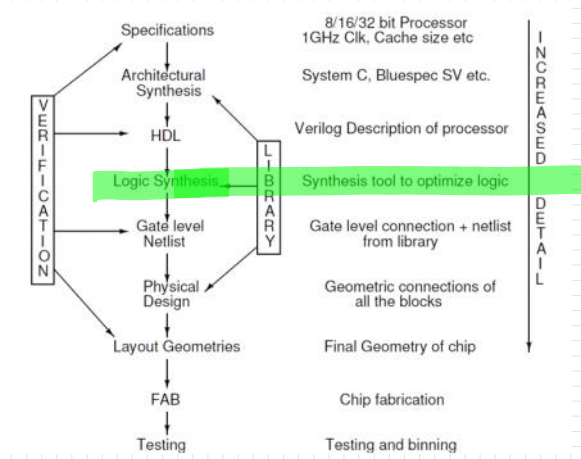
Lecture- 3



If the design is complicated, it makes sense to start describing the hardware at a higher level of abstraction (i.e System Verilog (SV) or Bluespec System verilog etc instead of HDL)

The "design architect" comes up with an architecture of the design. For example "A 6-stage pipelined processor with RISC-ISA with 32-bit registers" The architect will explore all possible combinations of design to optimize based on the specifications (Ex: Fast processor (clk rate) or low-power processor)

* Architectural Synthesis converts SV code to HDL codes.
  * Benifit :- Faster design time & verification @ SV level means bugs are caught up-front
  * Disadvantage - The synthesis tool might introduce additional hardware while converting to HDL
    => optimizations might be limited.
* Design can be directly started @ HDL level of abstraction (always the case for smaller fully optimized designs)



* Logic Synthesis converts HDL code to gate level circuit or RTL (Register transfer level). This design will only be built using GATES, FLIP FLOPS, ADDERS, MULTIPLIERS, MEMORY etc
* Logic synthesis is performed using a synthesis tool. This tool must be aware of what basic cells are available to build a gate level circuit from the HDL code. These basic cells are placed in an "IP Library"
* These IP libraries will have GATES, FLIP FLOPS, ADDERS, MULTIPLIERS, MEMORY etc
* The Synthesis tool will insert these basic cells to output an RTL built using Library
* ∴ A library needs to be developed before we start the chip design process.
* A Netlist is a textual representation of a circuit/design.

A Simple Example:-

HDL Code (in Verilog)

```
module myckt(
    input A, B, CLK,
    output Y,
);
wire C,
```

```
    output Y,
),
wire C,

assign C = A & B,

always @ (posedge CLK)
begin
    Y <= C,
end
endmodule
```

will be mapped to an "AND gate"

will be mapped to a "D flip-flop"

Synthesis Software / tool

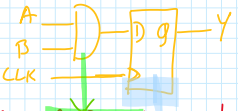
```
module myckt (
    input A, B, CLK,
    output Y,
),

AND  A1 (.A(A), .B(B), .C(C));
DFF  D1 (.D(C), .Q(Y), .CLK(CLK)),

endmodule
```

RTL Netlist or Gate level Netlist

This Netlist is a "textual representation" of

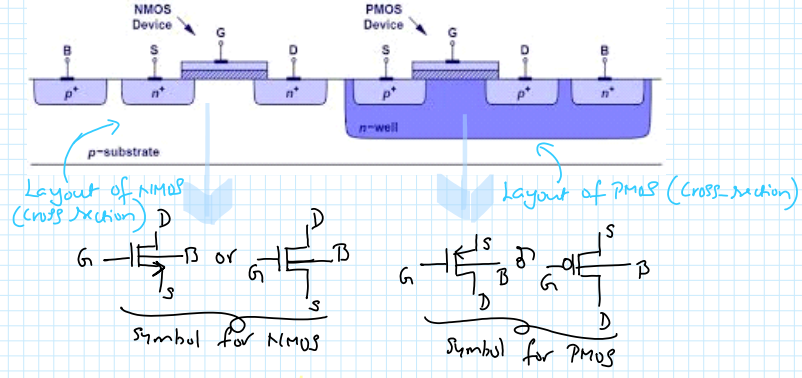


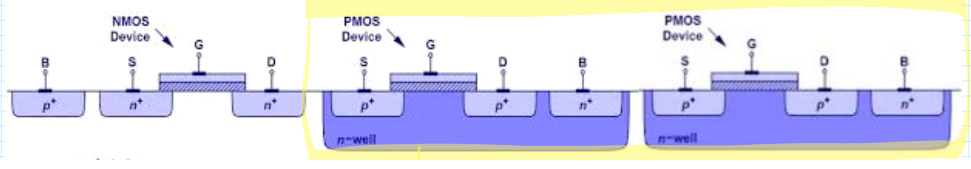
This AND gate was picked from "Library"

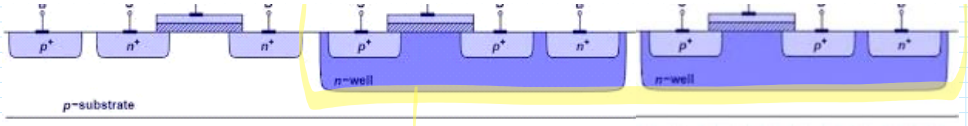
This D-FF was picked from "Library"

* The first half of the course will deal with developing an "IP library" to be used in the Digital Design flow.
* To do this, we must start with the basic CMOS gate → An inverter.
* To understand an inverter, we need to understand MOS operation at a "digital designer's" level (not at a device engineer level)

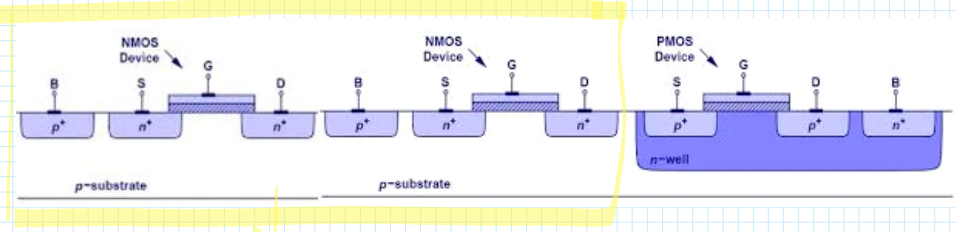
An NMOS & PMOS in bulk technology







* Notice that the two PMOS devices have different "BULK (B)" connection.



* Notice that the "BULK (B)" connection is common/shared/same for all NMOS devices and cannot be different due to a shared p-substrate. This is true in a "BULK technology".

* To have separate access to NMOS bulk we need to have "TRIPLE WELL PROCESS"

  i.e A "N-well" (well 1) on a p-substrate → A P-well (well 2) inside this N-well → Another N-well (well 3) inside this P-well

  Total 3 wells (∴ TRIPLE WELL)

* With "TRIPLE WELL PROCESS" every NMOS bulk is separately controllable. However this process is not supported in all Bulk CMOS technology & might cost more.

* In an FD-SOI technology, this is automatically taken care (please check the video on Moodle)

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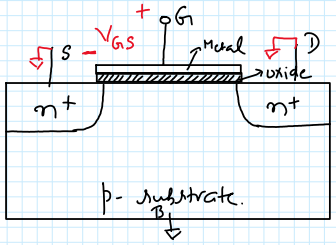
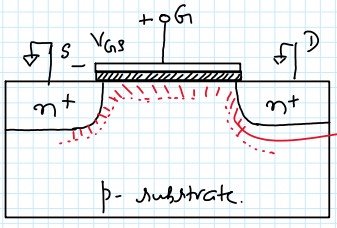


* Gate Voltage (w.r.t Source) V_{GS}
  Drain Voltage (w.r.t Source) V_{DS}

With $V_{DS}=0$, we start increasing the gate voltage

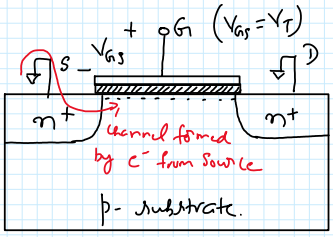
→ As V_G ↑, holes are repelled from under the gate, due to this repulsion, a depletion region is created (i.e region depleted of all charges)



→ Region depleted of all charges due to finite V_G (i.e holes are repelled)

→ when the V_{GS} voltage V_T (threshold voltage) of the MOSFET, the

→ When the V_{GS} voltage V_T (threshold voltage) of the MOSFET, the surface charge $\phi_S = 2\phi_F$ (Fermi potential, ϕ_F), all holes are depleted off and a small incremental V_{GS} will suck-in electrons from the source-side to form a thin layer of channel [Source is n^+ doped & connected to ground, a rich source of electrons]



∴ $V_{GS} < V_T$, the NMOSFET is OFF &
$V_{GS} = V_T$, the MOSFET just turns ON.

* Since $V_{DS} = 0$, no current. But, channel is formed.

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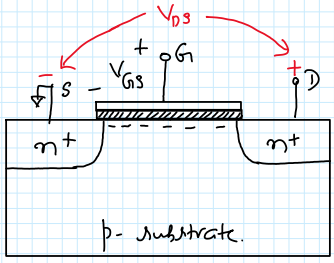
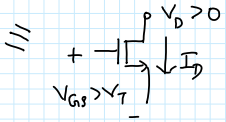
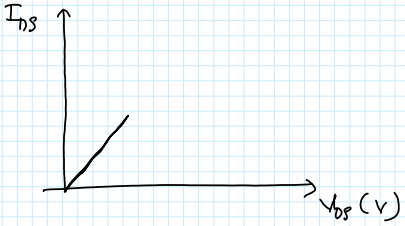
* Now with $V_{GS} > V_T$, we start increasing V_{DS}.



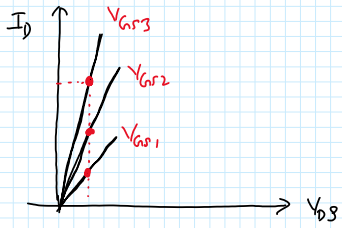
Potential difference across V_{DS} & with the channel formed already $(V_{GS}-V_T)$, e^- will flow from S to D
∴ a I_D (drain current from D to S)



* As V_{DS} ↑, the current also increases linearly (ohm's law), once $V_{GS} > V_T$
At the surface of channel (along the channel), all voltages are @ $V_{GS}-V_T$.



* Now, if we repeat the experiment with a higher $V_{GS}-V_T$ (i.e V_{GS} ↑ further) more channel charges are formed an channel can handle higher current (lower resistance)



$V_{GS3} > V_{GS2} > V_{GS1} > V_T$

∴ For $V_{GS} > V_T$, depending on the value of V_{GS}, the MOS acts like a resistor. and the drain current is given by

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

μ_n: Mobility; C_{ox}: Oxide capacitance per area; $\frac{W}{L}$: width & length of MOS. Design parameters.

$\left[\left(V_{GS} - V_T\right) V_{DS} - \frac{V_{DS}^2}{2} \right]$

Mobility — width & length of MOS: Design parameters

Remember designers don't have control in the thickness/depth but W & L are design parameters.

For small V_{DS}, $V_{DS}^2 \approx 0$ & $I_D \approx \mu_n C_{ox} \frac{W}{L} \left[\left(V_{GS} - V_T\right) V_{DS}\right]$

$\therefore I_D = \frac{V_{DS}}{R}$ } Linear I_D, V_D : Linear Region

& $R = \frac{1}{\mu_n C_{ox} \frac{W}{L} \left[V_{GS} - V_T\right]}$

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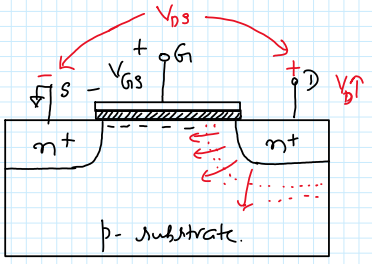
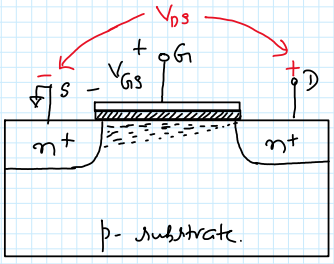
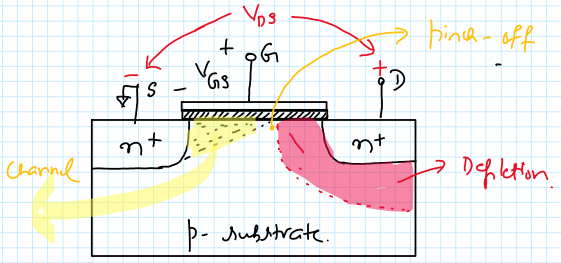


* As V_{DS} is increased further, the reverse-biased p-n junction (Drain-Bulk) depletion region width increases.
* Near the drain, the field is more controlled by Drain Voltage V_D

* The channel surface is at $V_{GS} - V_T$ and when $V_{DS} = V_{GS} - V_T$, the junction of gate & drain are just enough to keep the channel near the drain. At the junction, the channel just pinches-off



$V_{DS} = V_{GS} - V_T$

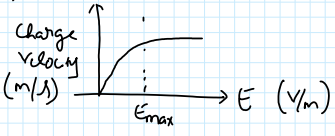


$V_{DS} > V_{GS} - V_T$

* As V_{DS} ↑ further, pinch-off shifts left. In this phase, there is no more dependance of I_D on V_{DS}. The current is limited by the Electric field in the depletion region. (∵ of Velocity saturation of charges)

* Electric field, $E = \frac{V}{d}$,

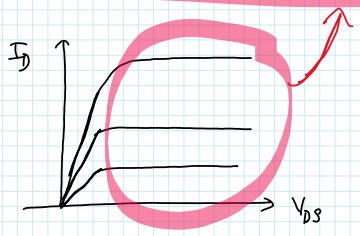
As E ↑ Velocity of charge ↑ For $E > E_{max}$ the velocity does not increase further.



∴ Current, I_D in saturation region = $\frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left[V_{GS} - V_T\right]^2$

∴ Current, I_D in saturation region = $\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[V_{GS}-V_T\right]^2$

i.e I_D is independant of V_{DS}



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In summary: For an NMOS

a) $V_{GS} < V_T$: OFF (acts like an OFF switch)

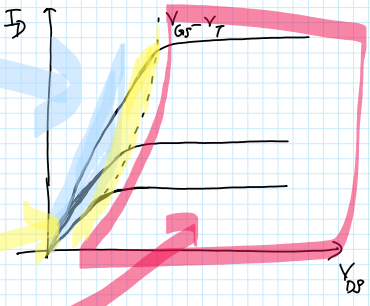
b) $V_{GS} \geq V_T$

↳ (i) $V_{DS} < V_{GS}-V_T$:

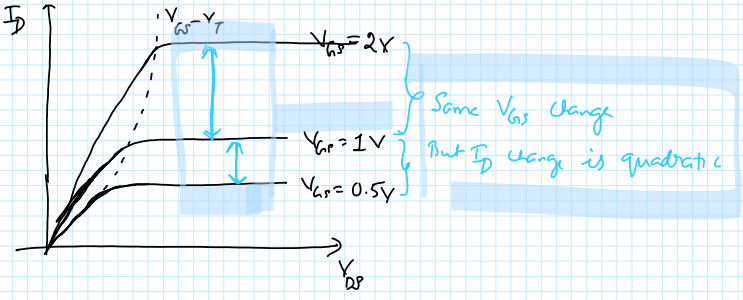
$$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

(ii) $V_{DS} \geq V_{GS}-V_T$

$$I_D = \mu C_{ox}\frac{W}{L}\left[V_{GS}-V_T\right]^2$$



* Point to note :- $I_D \propto (V_{GS}-V_T)^2$ ⇒ In the I_D-V_{DS} curve the change in current is quadratic (not linear) wrt V_{GS}.



* Another point to be noted:

I_D in saturation, $I_D \propto \frac{W}{L}$

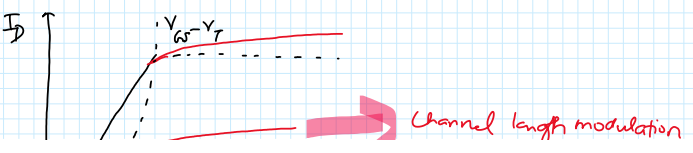
with pinch-off, effectively the 'L' ↓. Pinch-off point is a function of V_{DS}

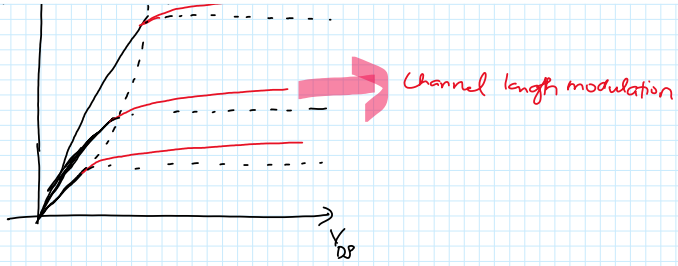
∴ L is a function of V_{DS}. (i.e as V_{DS}↑, L↓ ⇒ I_D↑)

∴ There is an increase in current, as V_{DS}↑ [Channel-length Modulation]

. we fit an empirical model to capture this

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[V_{GS}-V_T\right]^2\left[1+\lambda V_{DS}\right]$$ → fitting for





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* At lower technology nodes, 'L' is significantly lower.

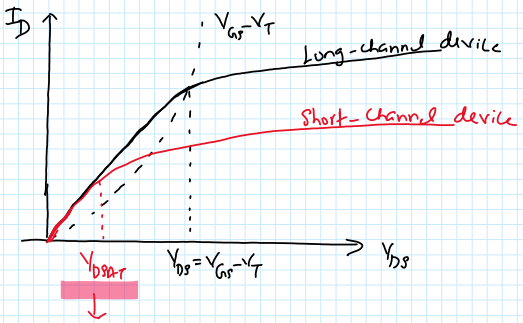
. The horizontal Electric field (from Drain – Source direction)

$E = V/L$ → L is very small for lower technology nodes

⇒ E ↑↑↑

∴ At lower nodes, $E > E_{max}$ for a smaller V, compared to another process with higher technology node (large minimum L)

∴ For short channel MOSFETs, the current is limited by Velocity saturation, much before pinch off (i.e for $V_{DS} < V_{GS} - V_T$, Velocity saturation occurs since L is small)



Velocity saturation occurs much b4 $V_{GS}-V_T$ in short-channel device.