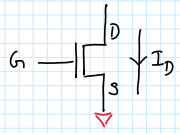
Lecture - 4

* An NMOS device has a threshold voltage $+V_{TN}$ and V_{GS} must be $> V_T$ to turn ON the MOS.
  ∴ V_{GS} must be +ve & hence "Source terminal" of NMOS is always tied to the lowest potential (i.e GND/VSS in this case)

* A PMOS device has a threshold voltage $-V_{TP}$ and $V_{GS} < -V_{TP}$ to turn ON the MOS.
  ∴ V_{GS} must be -ve However, there are only $+V_{DD}$ & V_{SS} available on chip (No negative voltage). ∴ To counter this we tie the "Source terminal" of PMOS is always tied to the higher potential (i.e V_{DD} in this case) to ensure V_{GS} is negative (i.e $V_G - V_{DD}$)

*

NMOS



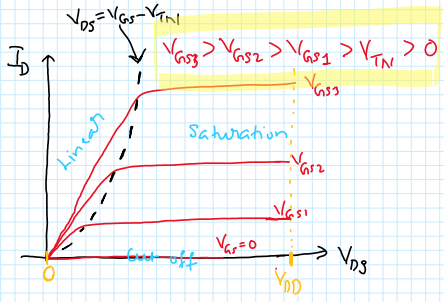
Threshold Voltage. V_{TN}

MOS OFF : $V_{GS} < V_{TN}$

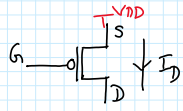
MOS ON : $V_{GS} > V_{TN}$

(i) $V_{DS} < V_{GS} - V_{TN}$: linear

(ii) $V_{DS} \geq V_{GS} - V_{TN}$: Saturation



PMOS



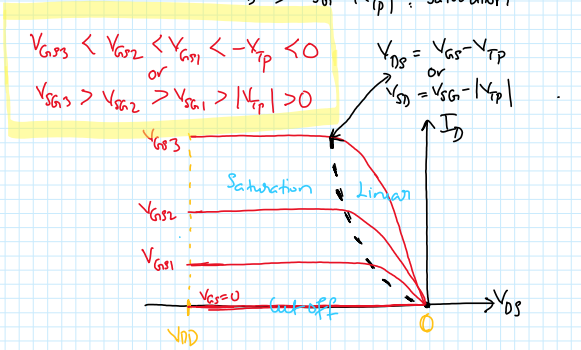
Threshold voltage : $-V_{TP}$

MOS OFF : $V_{GS} > -V_{TP}$ or $V_{SG} < |V_{TP}|$

MOS ON : $V_{GS} < -V_{TP}$ or $V_{SG} > |V_{TP}|$

(i) $V_{SD} < V_{SG} - |V_{TP}|$: linear

(ii) $V_{SD} \geq V_{SG} - |V_{TP}|$: Saturation



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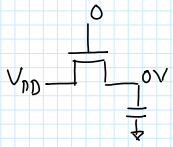
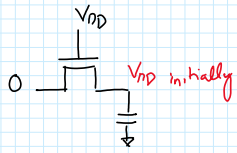
* Consider the cases for NMOS below

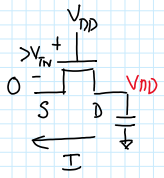
(a)



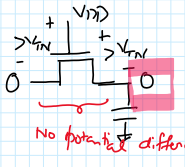
: Switch is OFF so no change in condition.

(b)

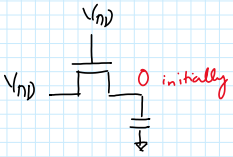


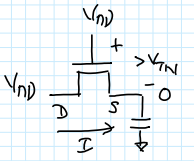


Finally ⇒

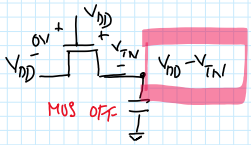


(c)



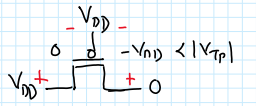


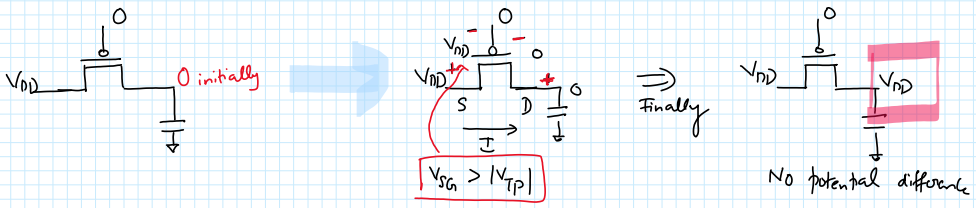
Finally ⇒

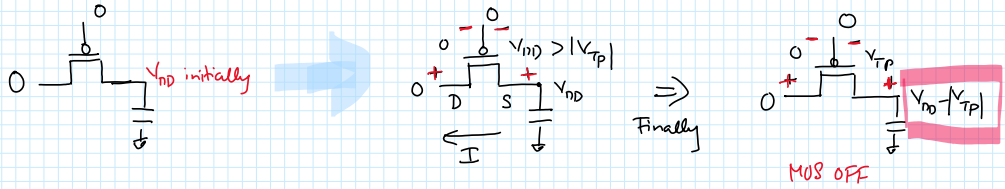


For NMOS, $V_o = \min(V_{IN}, V_{DD} - V_{TN})$

* Consider the cases for PMOS below

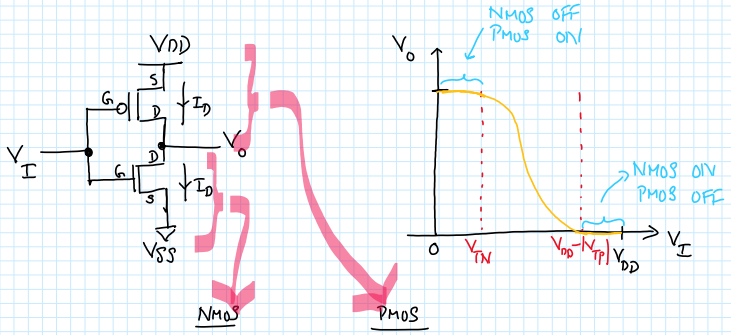
(a) 

(b) 

(c) 

* Observations:
  a) NMOS passes strong logic-0 & weak logic-1 (i.e o/p is not V_{DD})
  b) PMOS passes strong logic-1 & weak logic-0 (i.e o/p is not 0)

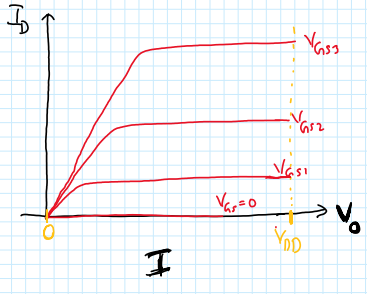
* To get a strong logic-0 & logic-1, we can use a combination of NMOS & PMOS

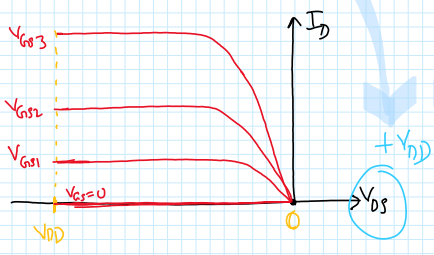


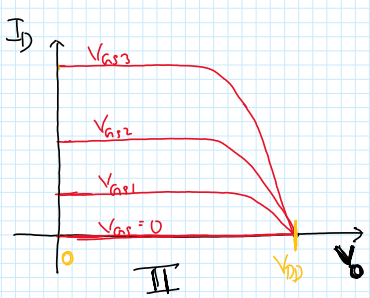
$V_{DS,NMOS} = V_o$ $\quad$ $V_{DS,PMOS} = V_o - V_{DD}$

* To bring both V_{DS} to same co-ordinate system (w.r.t V_o):

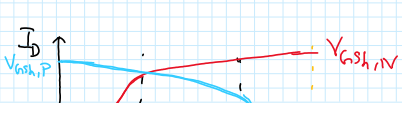
(I) $V_{DS,NMOS} = V_o$ $\quad$ (II) $V_o = V_{DD} + V_{DS,PMOS}$

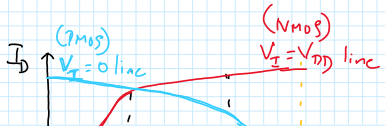


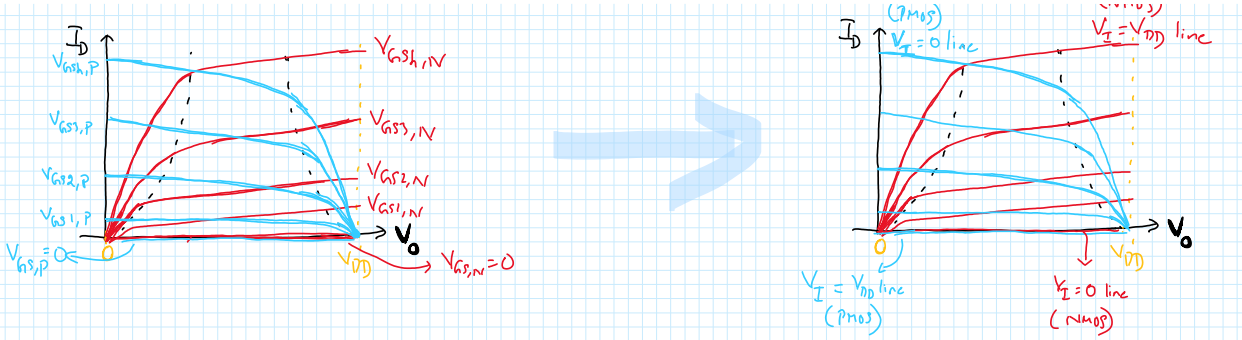




* To get the operating point (load line) of the inverter, we overlap plot I (for NMOS) & plot II (for PMOS)






I_D
$V_{GSh,P}$
$V_{GS3,P}$
$V_{GS2,P}$
$V_{GS1,P}$
$V_{GS,P}=0$
0
$V_{GSh,N}$
$V_{GS3,N}$
$V_{GS2,N}$
$V_{GS1,N}$
V_{DD}
$V_{GS,N}=0$
V_o
(PMOS)
$V_I=0$ line
$V_I=V_{DD}$ line
$V_I=V_{DD}$ line
(PMOS)
$V_I=0$ line
(NMOS)