EE 618 (ZELE) CMOS Analog VLSI Design Quiz-1

Date: 28th August 2023

Duration: 1 Hour

Max. Marks: 25

ACADEMIC HONESTY POLICY—IIT BOMBAY (https://www.litb.ac.in/newacadhome/rules.isp)
Copying in exams has serious consequences.

Do not communicate with other students during exams

Do not carry unauthorized material during exams

Do not make changes in valued answer books

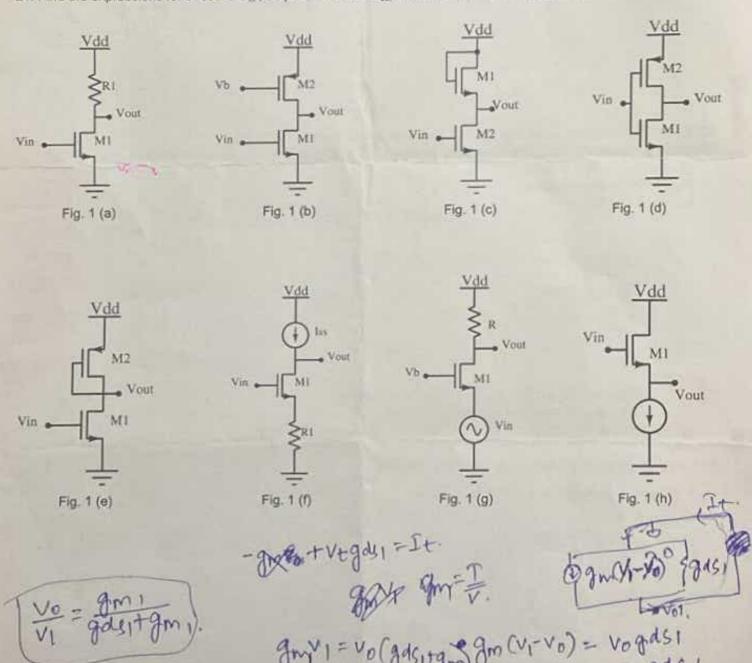
Do not communicate with others during toilet breaks during exams

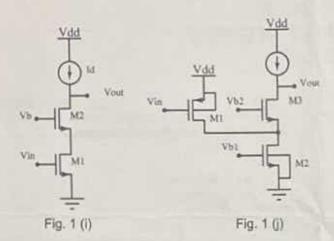
State your assumptions clearly, if any.

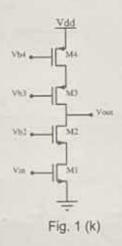
Ignore body effect ($\gamma=0$) unless it is explicitly mentioned or shown in the circuits below.

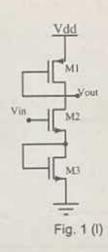
Q1. Find the expressions for effective $G_{\rm in}$, output resistance $R_{\rm out}$ and small signal voltage gain $A_{\rm v}$.

[12 Marks]









Q2. For the circuit shown in Fig. 2,

- (a) Draw the small signal model with proper polarity and labels. [1.5 Marks]
- (b) Derive an expression for small signal voltage gain A, using KVL and KCL. [1.5 Marks]

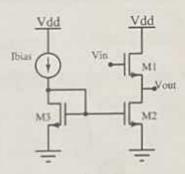


Fig. 2

Q3. For the circuits given in Fig. 3(a) and Fig. 3(b), Evaluate the expression for the following in terms of V_{DS} , V_{DSAT} and V_{TN} of each transistor:

- (a) Minimum output voltage
- (b) Maximum output voltage
- (c) Output voltage swing

[5 Marks]

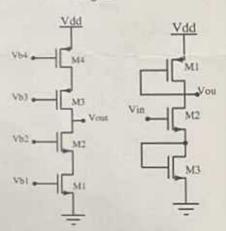


Fig. 3(a)

Fig. 3(b)

Q4. As V_x varies from 0 V to 1.5 V, for the circuit shown in Fig.4

- (a) Find the region of operation of transistor M1
- (b) Plot I, vs V,

[5 Marks]

Use the technology parameters given below (as required):-

$$t_{ox} = 9nm, \; \mu_n = 350 \; \frac{cm^2}{V-s}, \; \mu_p = 100 \; \frac{cm^2}{V-s}, \; C_{ox} = 3.38 \; \frac{fF}{(\mu m)^2}, \; \lambda_p = 0.2V^{-1}, \; \lambda_n = 0.1V^{-1}$$
 and $V_{TNO} = 0.5V$

Fig. 4