EE671: VLSI Design
Autumn 2024-25
Course Modalities

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Course Rules & Grading

- Audit not allowed
- Course interaction & updates: Moodle
- Additional reading materials: Moodle
- All submission deadlines are hard: no extensions (refer to course plan)
- Copy cases (assignments, quiz, mid-sem,end-sem,projects): will be awarded zero marks and referred to institute/dept. for disciplinary action
- Attendance mandatory

- Grading:

Assignments (x4)	10%
Quiz (x2)	10%
Mid-Semester Exam	20%
End-Semester Exam	20%
Course Project (x2)	40%

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COURSE MODALITIES

- Pre-requisites (must be strictly adhered):
  - HDL (Verilog or VHDL) basics
  - CMOS basics (PMOS and NMOS operation)
  - Digital Circuits (undergrad)

- References:
  - Rabaey, Chandrakasan, Nikolic "Digital Integrated Circuits – A Design perspective," Pearson 2nd Edition
  - OpenLane Documentation
  - SkyWater SKY130 PDK Documentation
  - Efabless Caravel SoC Documentation

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