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EE-671 VLSI Design 2024/2025
Mid-Semester Examination

Name: **Roll. No:**

Note: MCQ's carry a penalty of –0.5 marks for wrong answers. Total Marks: 40

1) When the clock frequency of a CMOS chip is doubled, and the supply voltage is halved simultaneously, the power consumption: (assume no static and short-circuit current) **[1 Mark]**

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(a) Remains same (b) Halves (c) Doubles (d) Can't say

2) For the circuit shown, V_{in} is the input, V_{out} is the output, V_{DD} = 1.8 V and V_{TN} = 0.5 V. Assuming that the two NMOS transistors are perfectly symmetric (they have exactly same parameters) and ignoring all second order effects, answer the following. **[2 Marks]**

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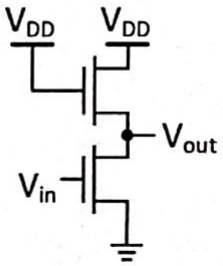

a) When V_{In} = 0 V, V_{out} = -0.5 V

b) When V_{In} = V_{DD}, V_{out} = 0 V

3) A symmetric inverter was designed with Noise margins NM_H and NM_L. Now, the PMOS transistor width is increased and NMOS is unchanged. The new respective NM_H and NM_L: **[1 Mark]**

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(a) Increase,Increase (b) Increase,Decrease (c) Decrease,Decrease (d) Decrease,Increase

4) Consider the following statements regarding standard cell library:

(i) The .lef file has physical coordinates of the layout pins or ports

(ii) The .lib file has timing information of all standard cells

(iii) The .lib file has power consumption information of all standard cells

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Which of the above statements are true? **[1 Mark]**

(a) (iii) only (b) (ii) and (iii) only (c) (i), (ii) and (iii) (d) (i) and (ii) only

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5) A 16-bit adder is implemented using the following different ways: **[10 Marks]**

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(Case a:) A complete 16-bit ripple carry adder (using only FA)
(Case b:) A carry-bypass adder with 4-bit ripple carry adder (using only FA)
(Case c:) A carry-save adder with 4-bit ripple carry adder (using only FA)
(Case d:) A Brent-Kungg tree adder
(Case e:) A Kogge-Stone tree adder

Assume FA carry generation takes 2-unit time, the FA sum generation from carry takes 2-unit time, multiplexer has a delay of 1-unit time, P and G generation takes 1-unit time, carry generation from P and G takes 1-unit time and sum generation from carry and P takes 1-unit time. List the approximate critical path delays for each of the adder (in units of unit-time)

Case a: 32 units, **Case b:** 22 units, **Case c:** 15 units, **Case d:** 8 units,
Case e: 5 units.

7) A static CMOS logic with output $Y = \overline{(A+B+C)\cdot D}$ is to be implemented. The ratio of mobilities in the chosen CMOS technology is, u_n/u_p is 3. Answer the following:

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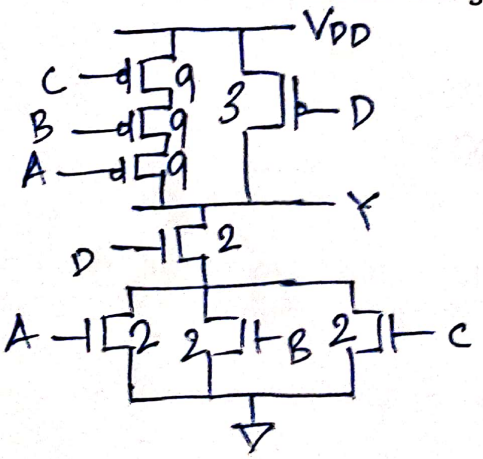
a) Draw the static CMOS circuit and annotate the strength of MOSFETs **[2 Marks]**



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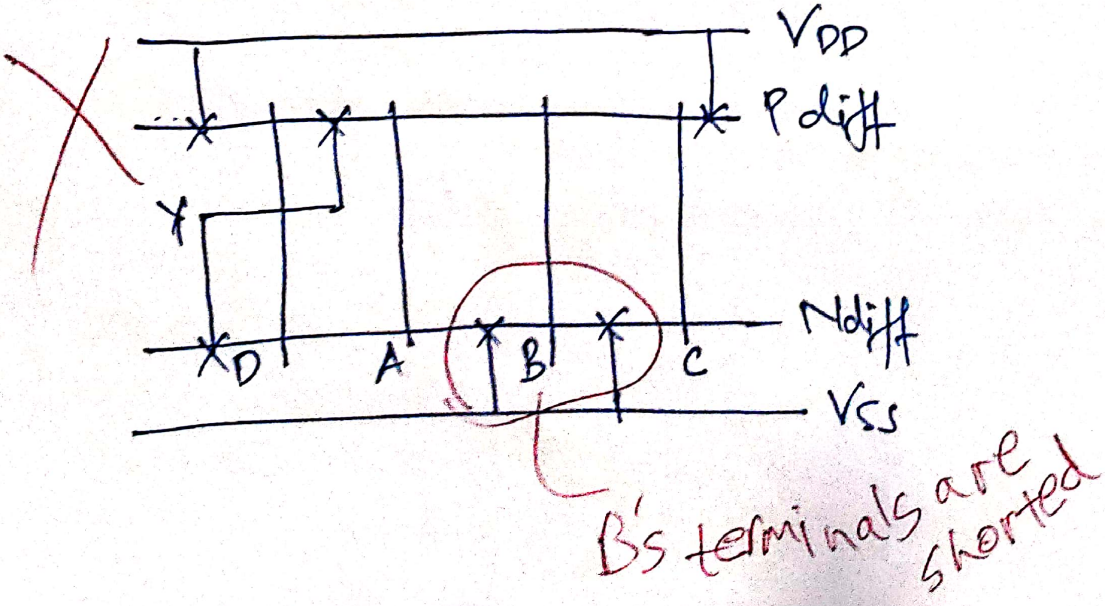
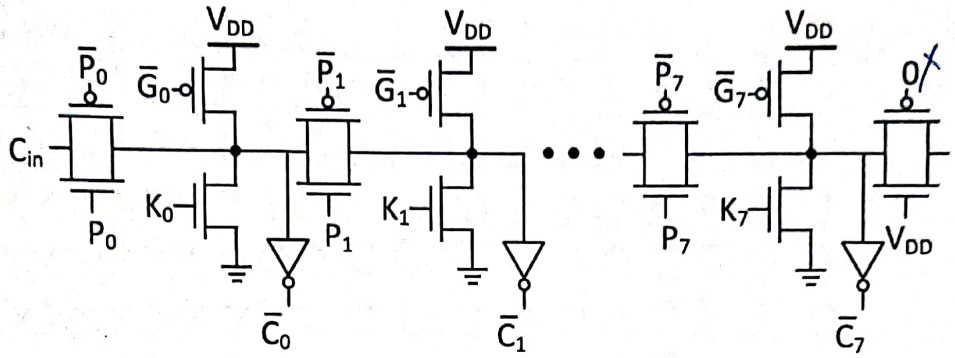
b) Draw the stick diagram for the above circuit. **[3 Marks]**



8) An 8-bit Manchester carry chain adder is implemented using transmission gates (TG) as shown below. The TG, PMOS and NMOS devices have a mean ON resistance of 1 kΩ. The TG offers a symmetric capacitance of 2 fF on either side. The inverter has an input capacitance of 3 fF. Ignore all other parasitic resistances, capacitances and the delay of the final stage vertical inverters. Answer the following:

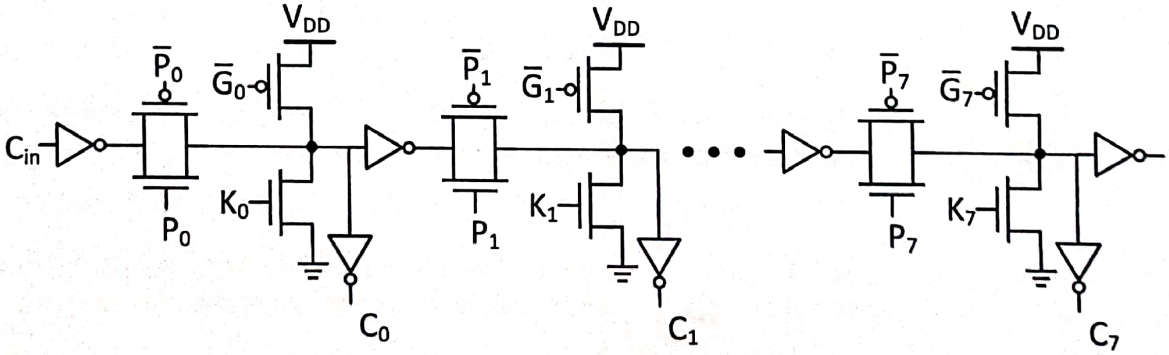


a) The condition (in terms of logic states of P_i and/or G_i and/or K_i) for worst case delay is: $\Pi P_i = 1 \Rightarrow P_0 \cdot P_1 \cdot P_2 \ldots P_7 = 1$ **[1 Mark]**

b) Assuming all P_i, G_i and K_i signals (and their complements) are available, the worst-case carry propagation delay is 21 ps **(rounded off to nearest integer).** **[4 Marks]**

c) The circuit is modified and implemented as shown below. Ignore all other parasitic resistances, capacitances and the delay of only the final stage vertical inverters. The new worst-case carry propagation delay is 59 ps **(rounded off to nearest integer).**

[Hint: propagation delays of successive stages can be simply added to compute overall propagation delay]. **[5 Marks]**



9) A modified Booth-2 encoding is used to multiply two 12-bit binary numbers A and B. For the case when A = 011010011100 and B = 111001101010, write down the partial products generated (up to 24-bits) with the corresponding left shifts denoted by X. Use the "B" input for the Booth-2 encoding. **[7 Marks]**

PP1 = 1 1 1 1 1 1 1 1 1 1 1 0 0 1 0 1 1 0 0 1 0 0 0

PP2 = 1 1 1 1 1 1 1 1 1 1 1 0 0 1 0 1 1 0 0 1 0 0 X X

PP3 = 1 1 1 1 1 1 1 1 1 1 1 0 0 1 0 1 1 0 0 1 0 0 X X X X

PP4 = 0 0 0 0 0 0 1 1 0 1 0 0 1 1 1 0 0 0 X X X X X X

PP5 = 1 1 1 1 0 0 1 0 1 1 0 0 1 0 0 0 X X X X X X X X

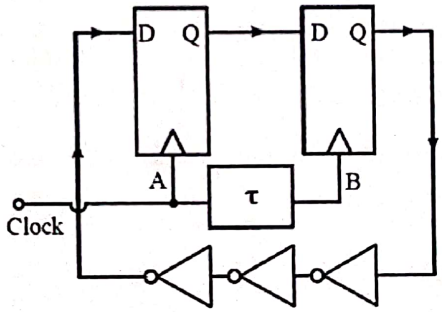
PP6 = 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 X X X X X X X X X X

PP7 = 0 1 1 0 1 0 0 1 1 1 0 0 X X X X X X X X X X X X

PP8 = 0 0 0 0 0 0 0 0 0 0 0 0 X X X X X X X X X X X X

PP9 = 0 0 0 0 0 0 0 0 X X X X X X X X X X X X X X X X

10) For the sequential circuit shown, the D FFs have a set-up and hold time of 4 ns, Clk-to-Q delay of 8 ns. The inverters have a propagation delay of 1 ns each. τ is the delay in the clock between the two flops and $\tau \geq 0$.



a) For $\tau = 0$, the maximum clock frequency of the circuit without any timing violation is 67 MHz **(rounded off to nearest integer).** **[1 Mark]**

b) The minimum positive value of τ for which the circuit stops working correctly (irrespective of the clock frequency) is 1 ns **(rounded off to nearest integer).** **[2 Marks]**