EE671: VLSI Design
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Laxmeesha Somappa

Department of Electrical Engineering

IIT Bombay

laxmeesha@ee.iitb.ac.in

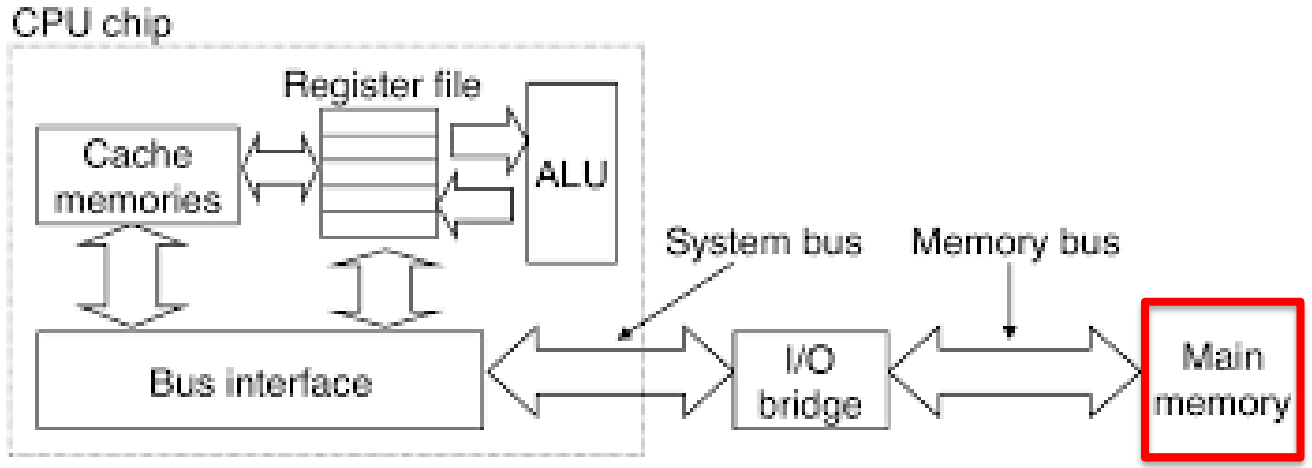
LECTURE – 36
DRAM & OTHER MEMORIES

laxmeesha@ee.iitb.ac.in

Memory

- SRAM: Digital (binary data) memory
- Is there an analog memory?
  - How about inductors and capacitors?
- Can we use capacitor as a memory?
  - DRAM: Dynamic RAM
  - What is dynamic?
- SRAM: Static RAM (volatile)
  - Unless you turn-off power, data is retained
- DRAM: Dynamic RAM (also volatile)
  - During power-on, if you do not do read/write operation, data is lost
  - Has to be dynamically refreshed!

Memory Hierarchy in Processors



	Capacity	Latency	Cost/GB
Register	1000s of bits	20 ps	$$$$
SRAM	~10 KB-10 MB	1-10 ns	~$1000
DRAM	~10 GB	80 ns	~$10
Flash*	~100 GB	100 us	~$1
Hard disk*	~1 TB	10 ms	~$0.10

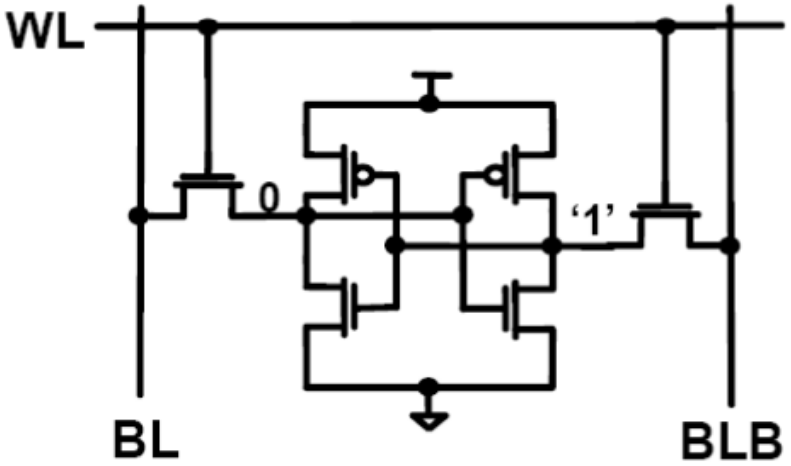
Processor Datapath

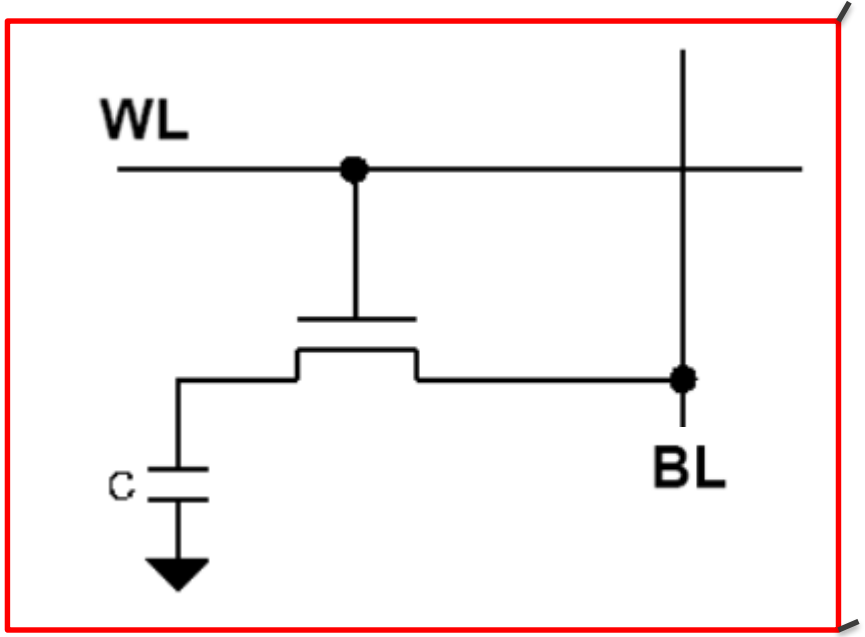
Memory Hierarchy

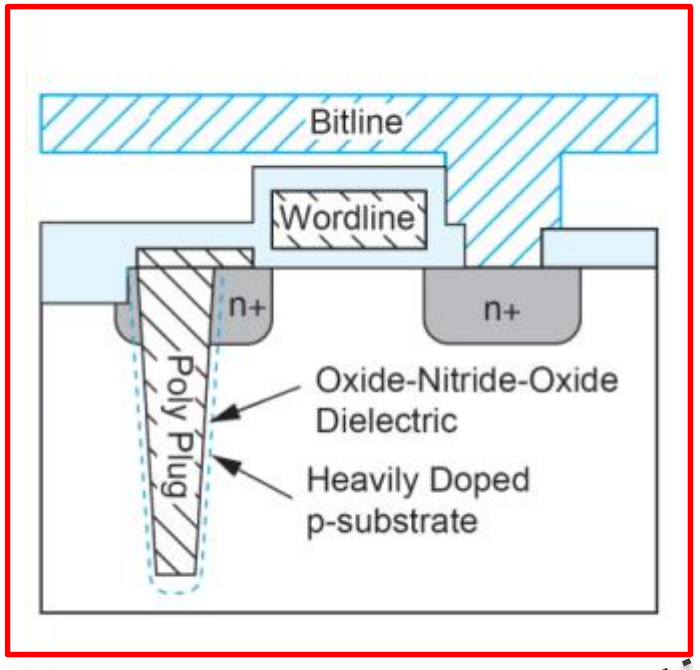
I/O subsystem

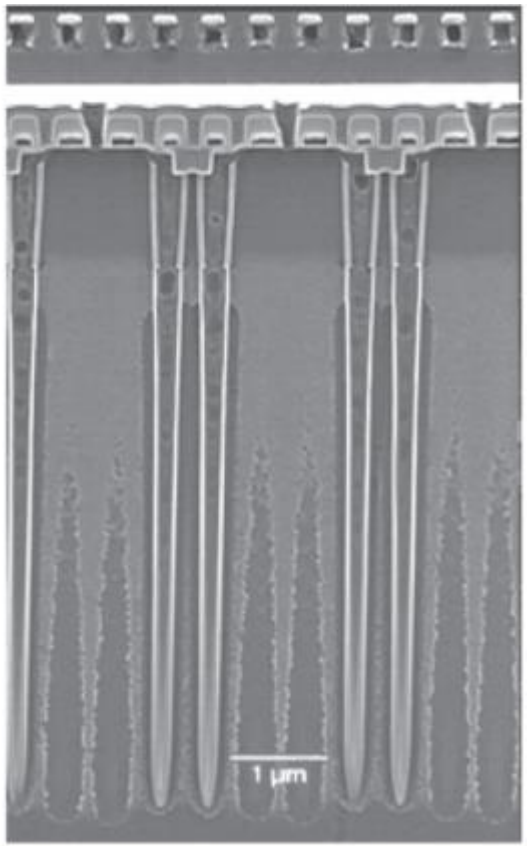
* non-volatile (retains contents when powered off)

SRAM vs DRAM


WL
0
'1'
BL
BLB

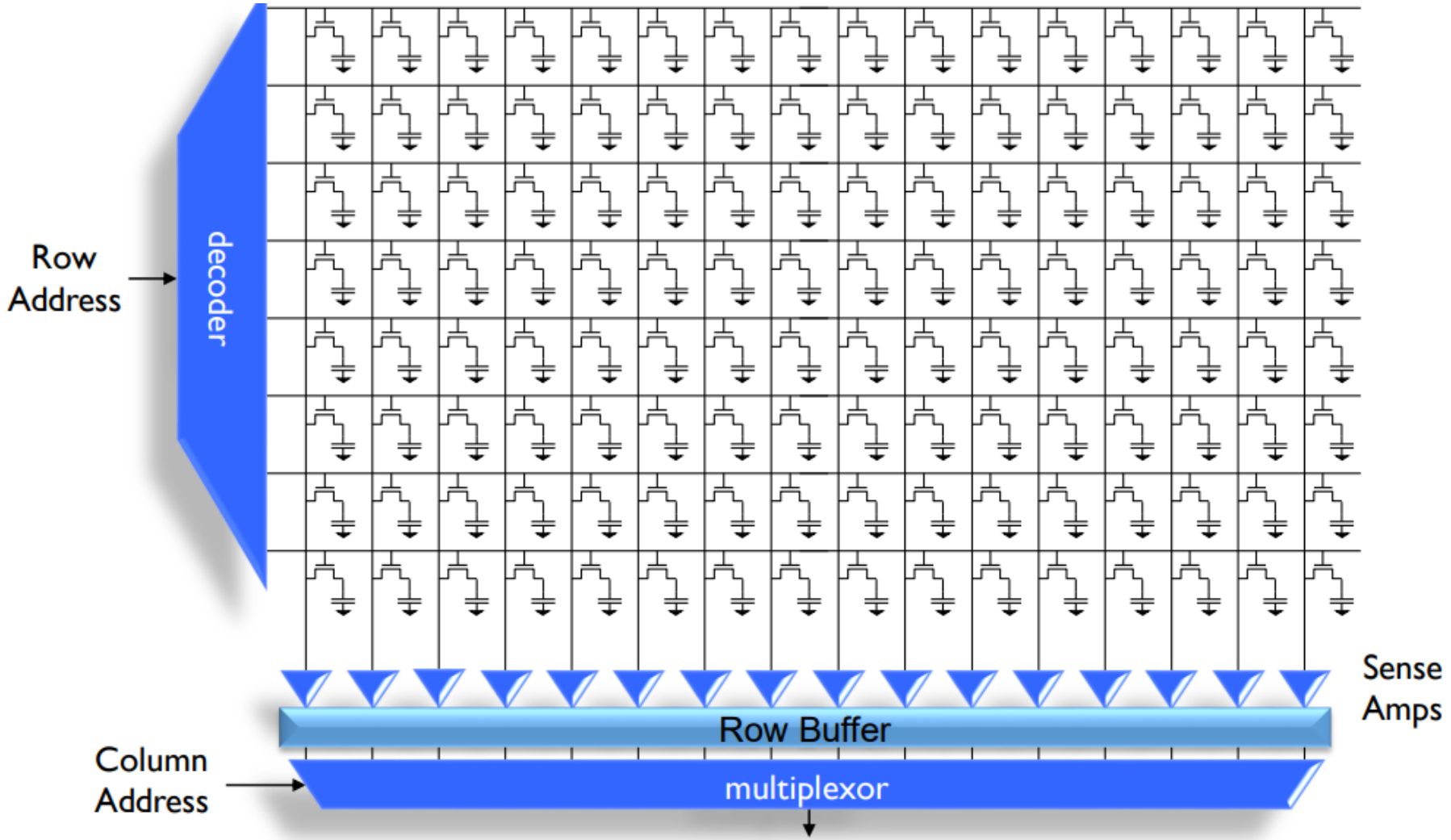

WL
C
BL


Bitline
Wordline
n+
n+
Poly Plug
Oxide-Nitride-Oxide
Dielectric
Heavily Doped
p-substrate


1 μm

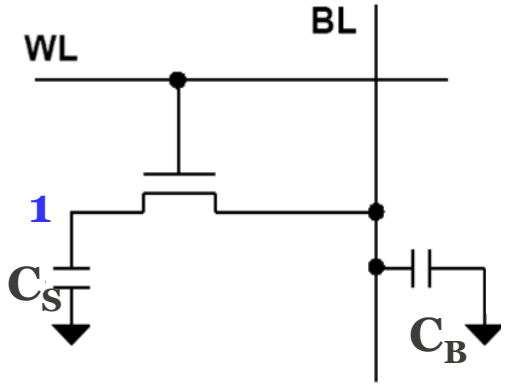
DRAM

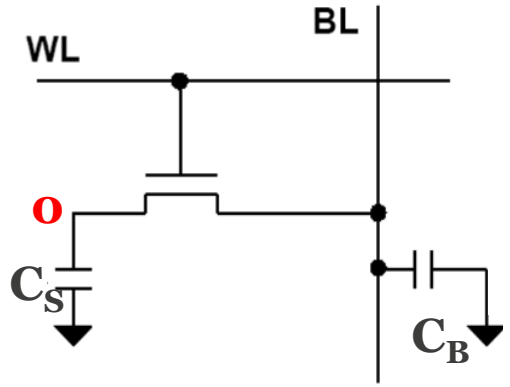
- One NMOS, One trench capacitor → highly dense !
- Trench capacitor is in itself an area of research

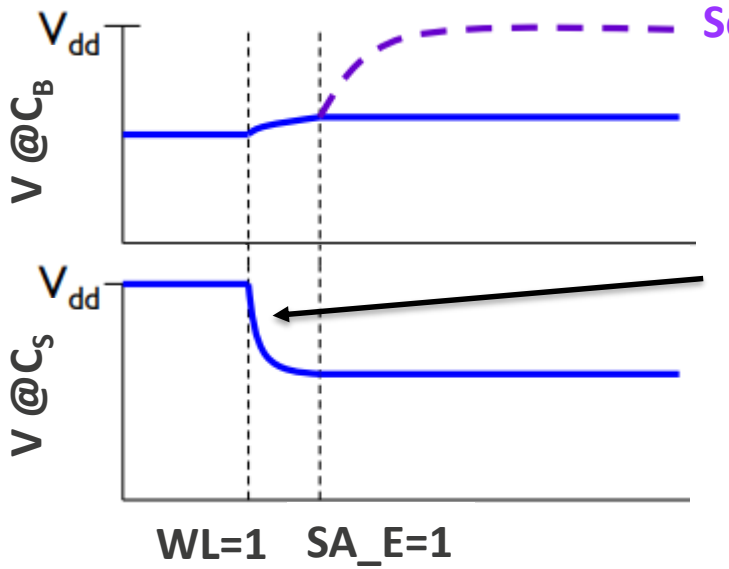


DRAM Read Operation

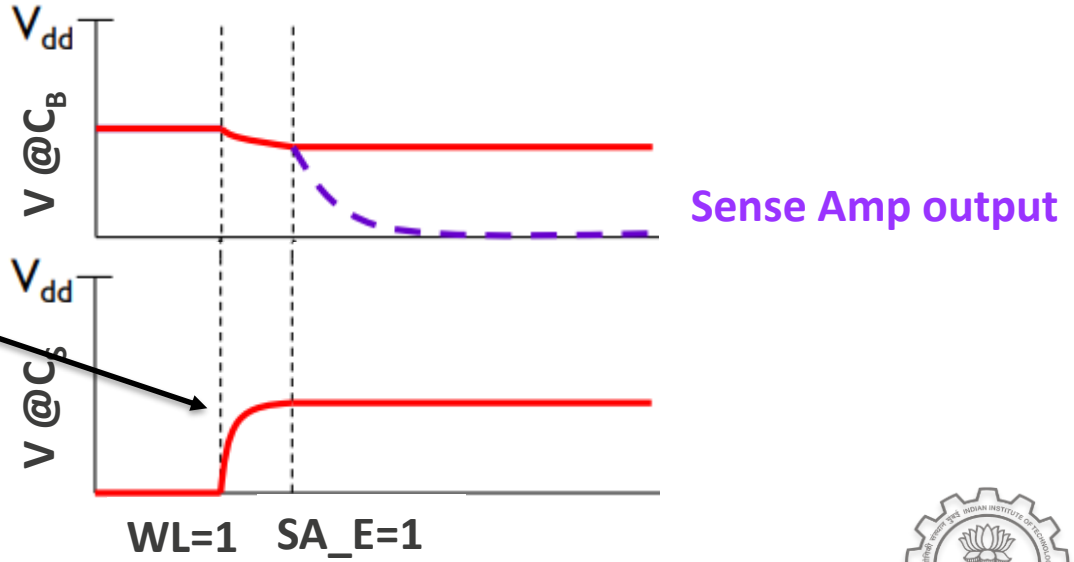
- Say storage cap: C_S and bit line capacitance: C_B
- Pre-charge bit line to $V_{DD}/2$ (or V_{DD} → both designs exist, power saving in half-V_{DD})







Charge sharing takes when word-line is fired → reads are destructive (analog memory)

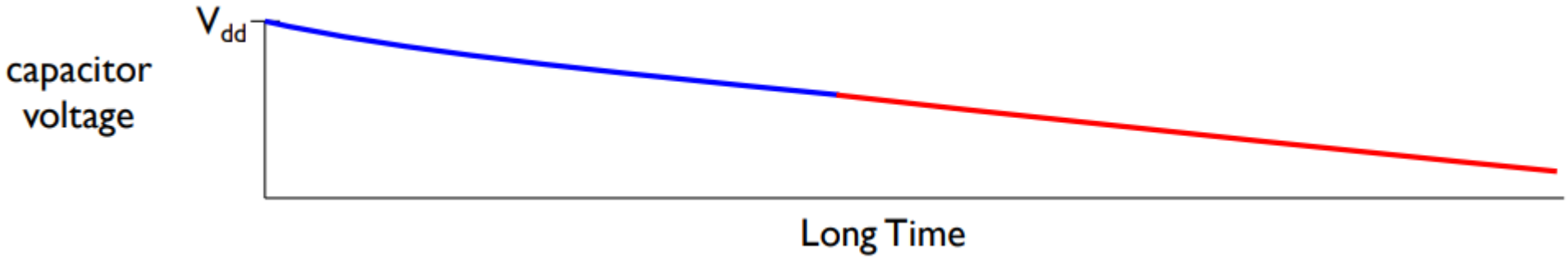


DRAM Read

- Read is destructive: write back after a read from a buffer (Sense Amp output after read)
- After every read, mandatory write of the read data back to the row (before next read operation)

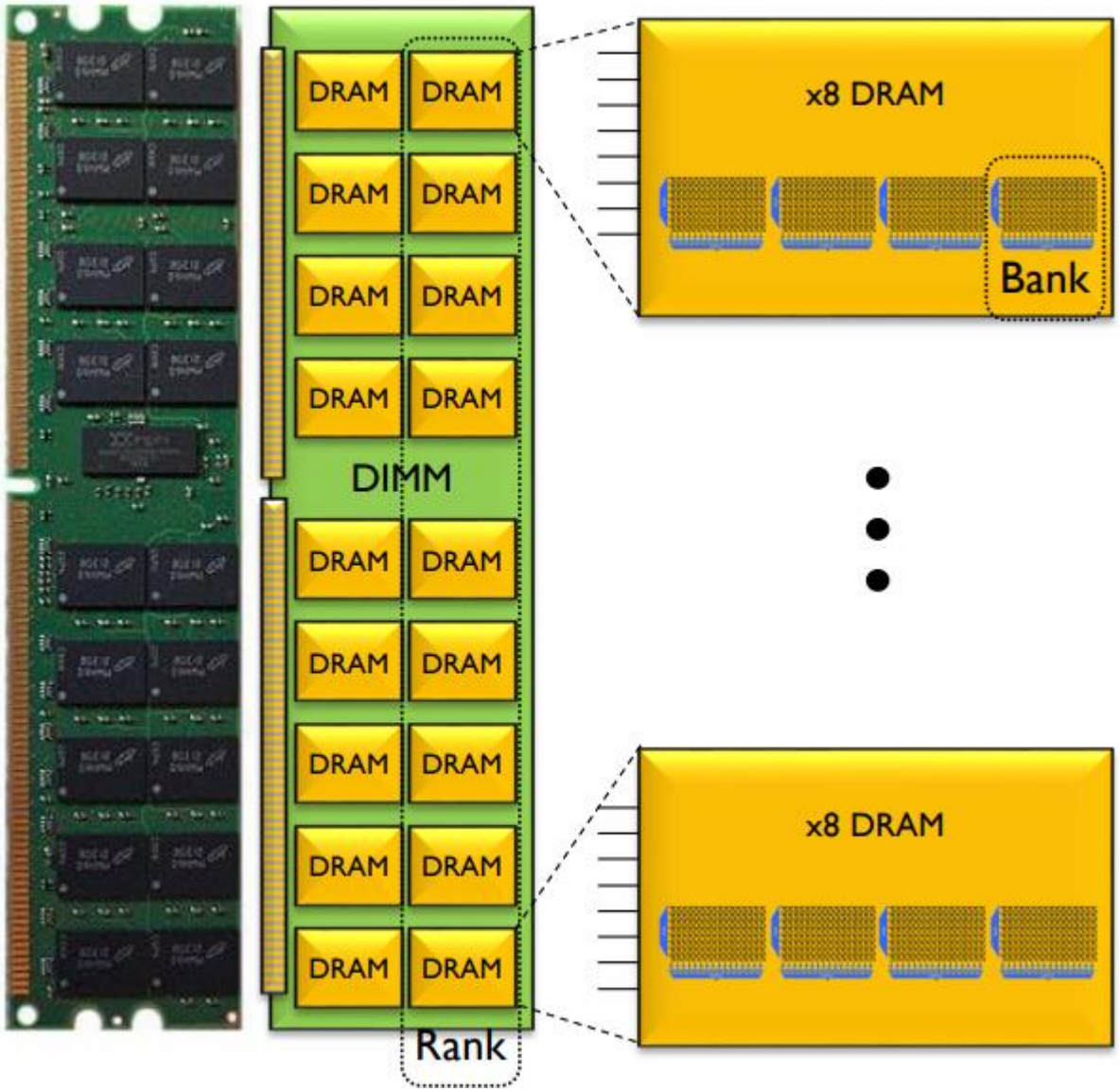
DRAM Refresh

- If DRAM is not accessed: capacitor loses its content (leaky analog memory!)



- Therefore, DRAM must be regularly read/written
  - That is periodically perform a refresh
- DRAM refresh policies (to be handled by the memory controller):
  - Burst: stop all read/write access and refresh all content
  - Distributed: refresh one row at a time in a time-division-multiplexing

Typical DRAM Organization



- Each DRAM: Multiple banks (for high bandwidth)
- Each DRAM: has 8-bits
- Each Rank: has 8-DRAM chips (64-bits)
- One additional DRAM for 8-bit ECC (error correction code)

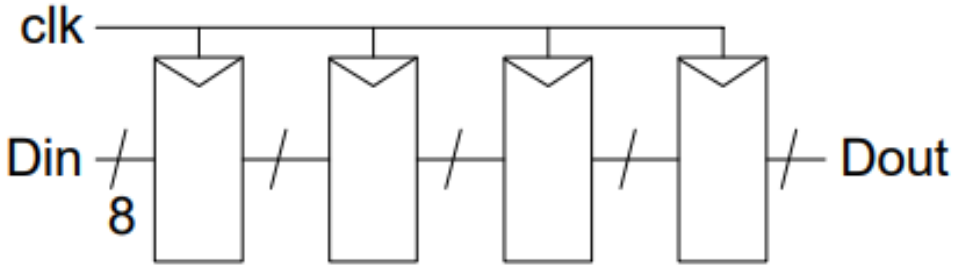
- Read up on using banks in DRAM for high bandwidth using interleaved address map

Serial Memory

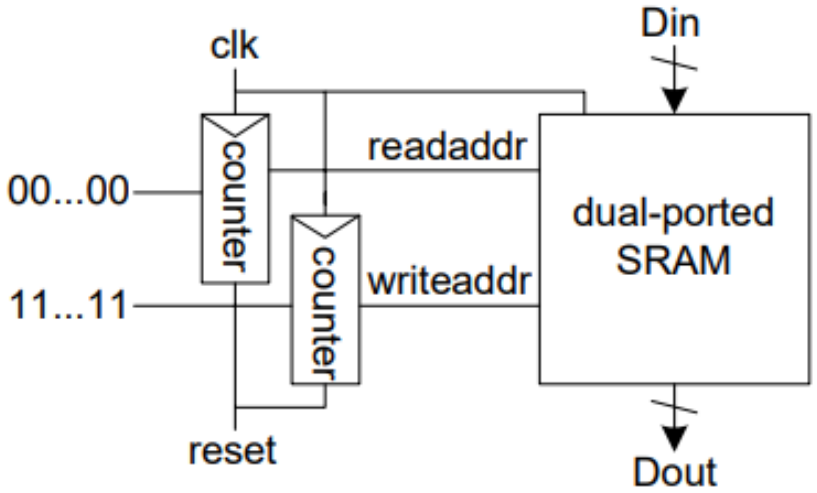
- Serial access memory: do not use addressing (example: 1-bit DFF)
- Following types:
  - Shift registers
  - SIPO: Serial-In Parallel-Out
  - PISO: Parallel-In Serial-Out
  - Queues (FIFO, LIFO etc).

SHIFT REGISTERS

- Delay in data storage (example Z^{-1} realization in DSP)
- Beware of hold violations !!!

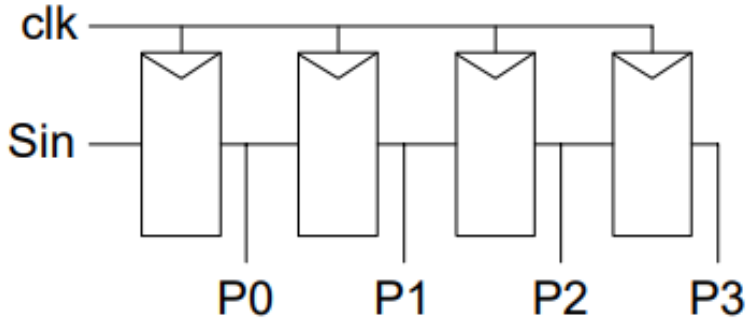


- DFF: not area efficient
- For higher density, use SRAMs
  - Move the pointers to read and write address

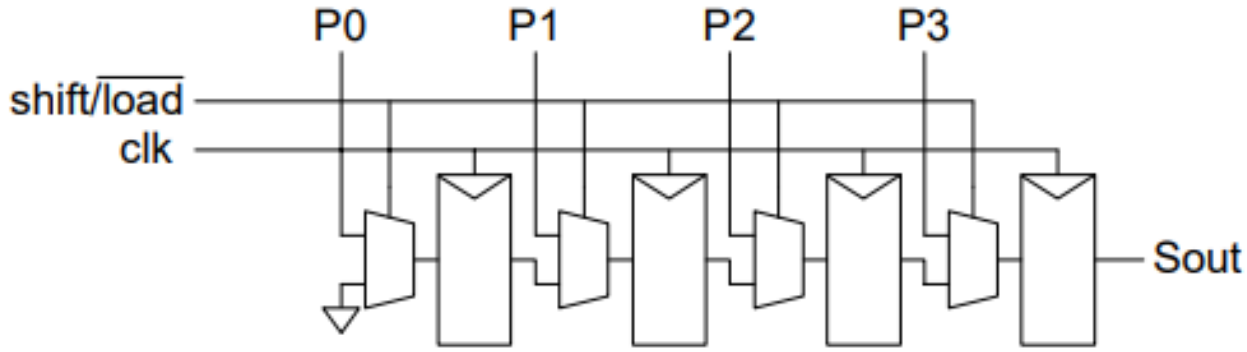


SIPO AND PISO

- SIPO: 1-bit shift register → after N cycles → N bits parallel output



- PISO: Load N bit parallel data when shift = 0, then shift one bit per clk



QUEUES

- FIFO/LIFO: built using SRAMs and counters
- Two counters: Read & Write pointer (RP, WP)
- FIFO:
  - Initialize RP = WP (Queue is empty)
  - Increment WP counter after every write
  - Increment RP counter after every read
  - Generate FULL signal based on WP and RP
- LIFO:
  - Typically called “Stack”
  - A single pointer (P) for read and write
  - Depending on ascending/descending stack → increment decrement address after write/read