EE 618 (ZELE)
CMOS Analog VLSI Design
MIDSEM

Date : 23th September 2023 **Duration**: 2 Hours **Max. Marks** : 43

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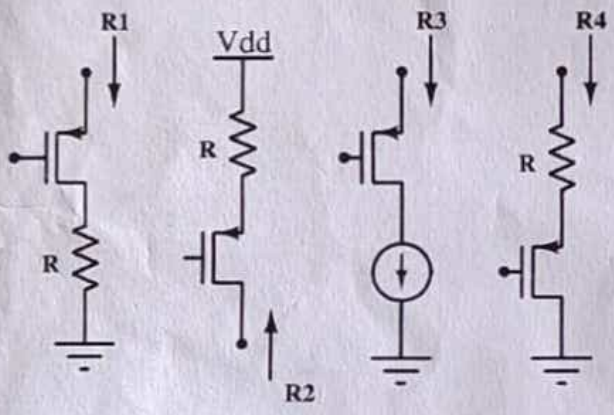
Copying in exams has serious consequences.
Do not communicate with other students during exams. Do not carry unauthorized material during exams
Do not make changes in valued answer books. Do not communicate with others during toilet breaks during exams

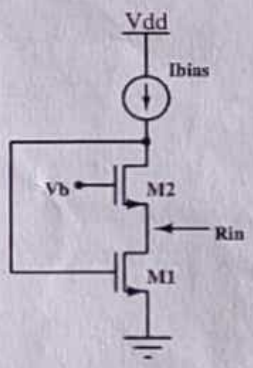
State your assumptions clearly, if any.

Ignore body effect ($\gamma = 0$) unless it is explicitly specified.

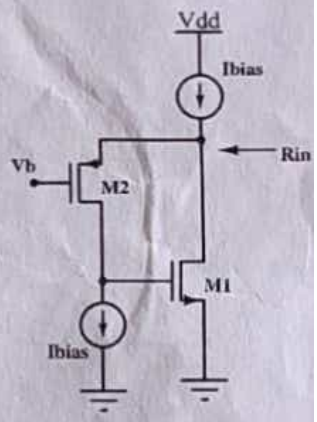
Q1. For the circuit shown in Q.1, all the transistors have identical g_m, r_o. Assume $g_m r_o >> 1$. [3 Marks]
(a) Find R_1, R_2, R_3 and R_4. (No need to show small signal analysis) [2]
(b) Arrange R_1, R_2, R_3 and R_4 in order of increasing resistance. **ex: R1 > R2 > R3 > R4** [1]



Q.1



Q.2(a)



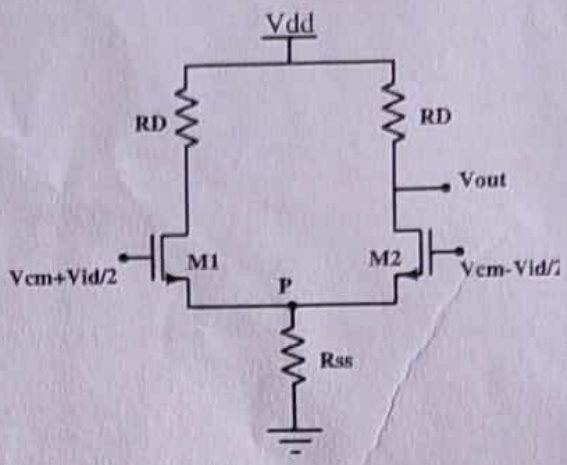
Q.2(b)

Q2. Using small signal analysis, [5 Marks]
(a) Find R_{in}. (in terms of g_{m1}, r_{o1}, g_{m2}, r_{o2}) [2]
(b) Find R_{in}. (in terms of g_{m1}, r_{o1}, g_{m2}, r_{o2}) [3]

Q3. Draw schematic diagram. Label every detail. [10 Marks]
(a) Telescopic cascode OTA with **pmos input** differential pair. [2]
(b) Regulated cascode current mirror. [2]
(c) Two stage OTA with **pmos input** differential pair. Use RC compensation where zero is tracks the non-dominant pole. Show correct biasing. [6]

Q4. Assume all transistors have same g_m and r_o. [4 Marks]
Find (in terms of g_m, r_o, R_D and R_{SS})

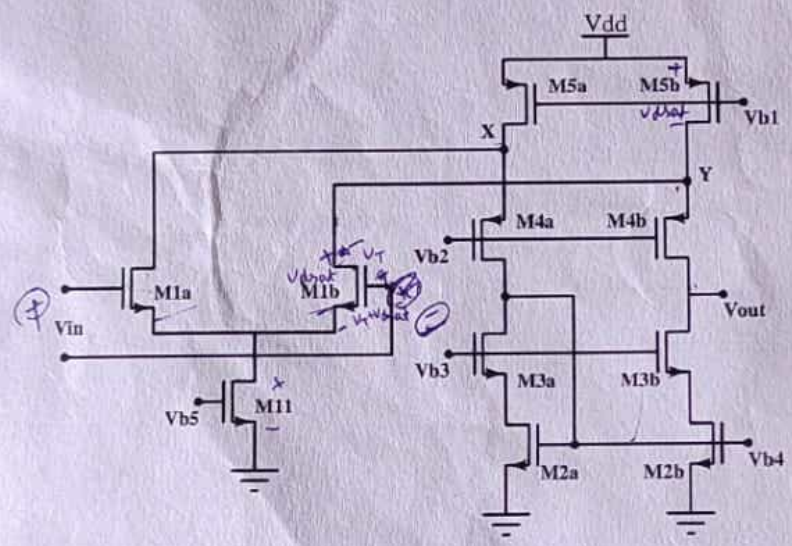
(a) Differential gain A_{DM}. [1.5]
(b) Common mode gain A_{CM}. [1.5]
(c) Common mode rejection ratio **CMRR**. [1]



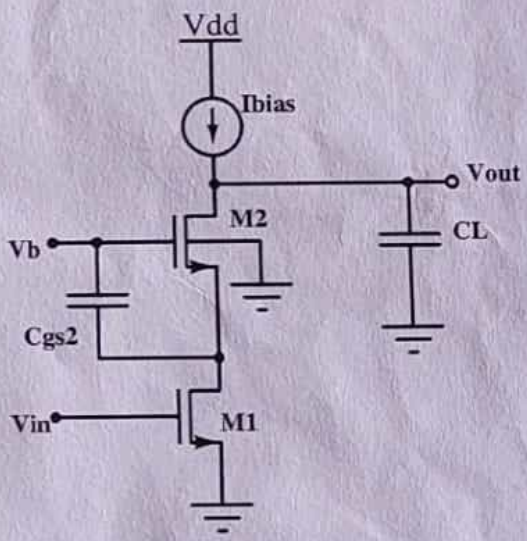
Q.4

Q5. M_{1a} and M_{1b} match with g_{m1}, r_{o1} parameters.
Other transistors pairs are matched and follow **similar pattern**. Find [7 Marks]

(a) Small signal **Gm**. [2]
(b) Small signal **Rout**. [2]
(c) Voltage gain **Av**. [1]
(d) Input common mode range maximum ($V_{CMdc(max)}$) and minimum ($V_{CMdc(min)}$). [2]



Q.5



Q.6

Q6. Derive the transfer function of cascode amplifier.[4] Ignore all the device capacitance except C_{gs2}. Use dominant pole approximations to figure out pole-zero locations.[2] Draw the bode plots clearly annotating gain, phase, all axes, pole-zero locations.[3] [9 Marks]

Q7. (a) Draw the low-voltage high-swing cascode current mirror with self biasing resistor **R**. [2 Marks]
(b) Find the expression for maximum and minimum limit of **R** in terms of V_{TH} and V_{DSAT} of devices. [2 Marks]

Q8. List 2 **concrete** suggestions to improve second half of **EE618** course. [1 Mark]