EE671: VLSI Design
Spring 2024/25

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LECTURE – 22
PHYSICAL DESIGN

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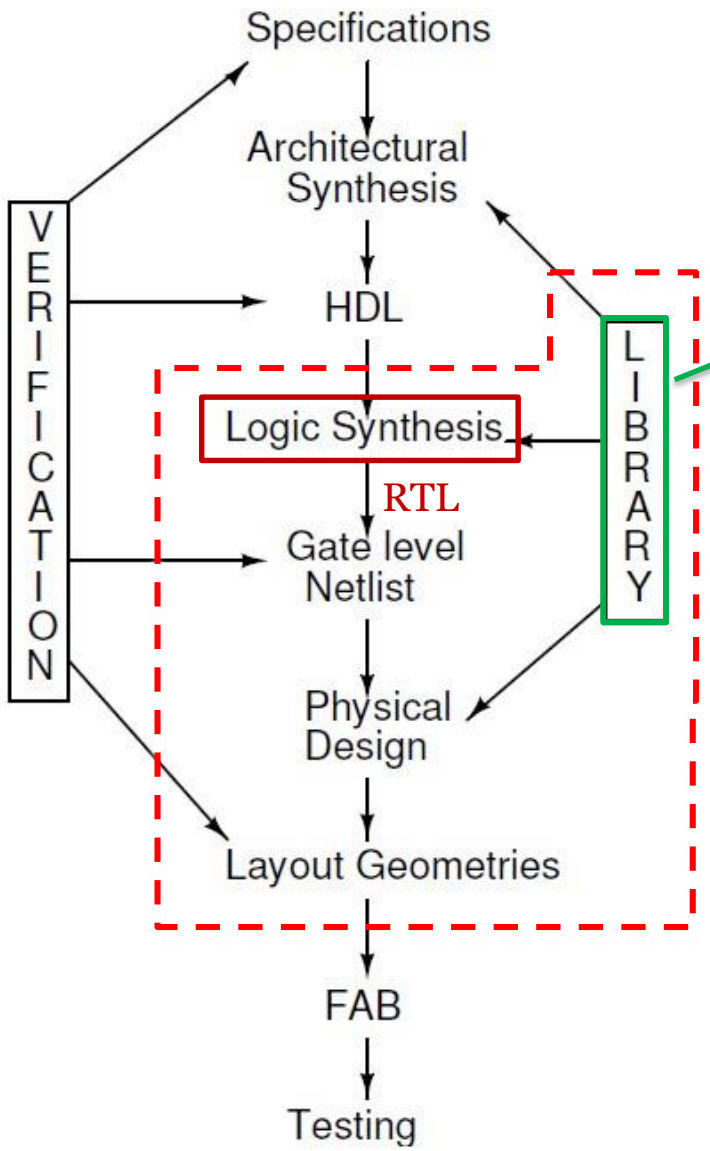
LOGIC SYNTHESIS

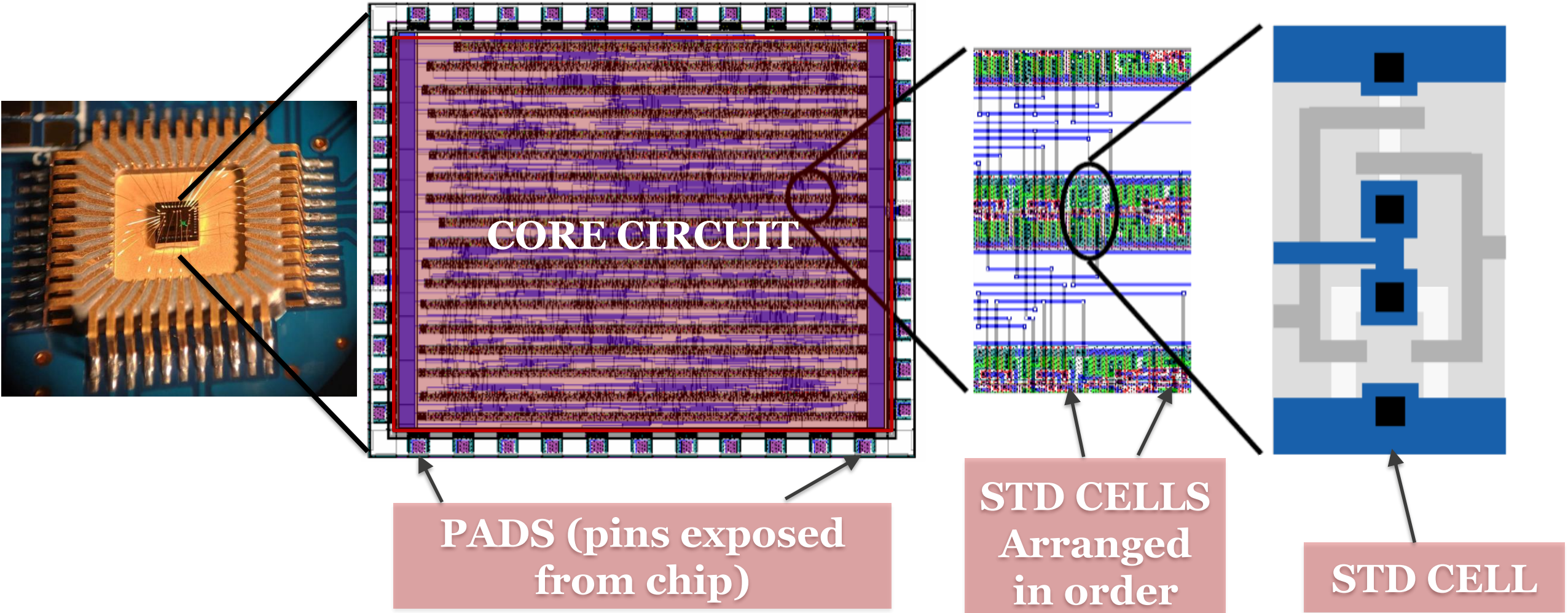


STANDARD CELL LIBRARY:
.V, .LEF. LIB, .SP, .GDSII/.MAG

LOGIC SYNTHESIS:

- INPUT: HDL (VERILOG – BEHAVIORAL/STRUCTURAL CODE)
- OUTPUT: RTL (REGISTER TRANSFER LEVEL VERILOG)
- RTL: COULD BE OR COULD NOT BE MAPPED TO A TECHNOLOGY (STD. CELL LIBRARY)

MOTIVATION



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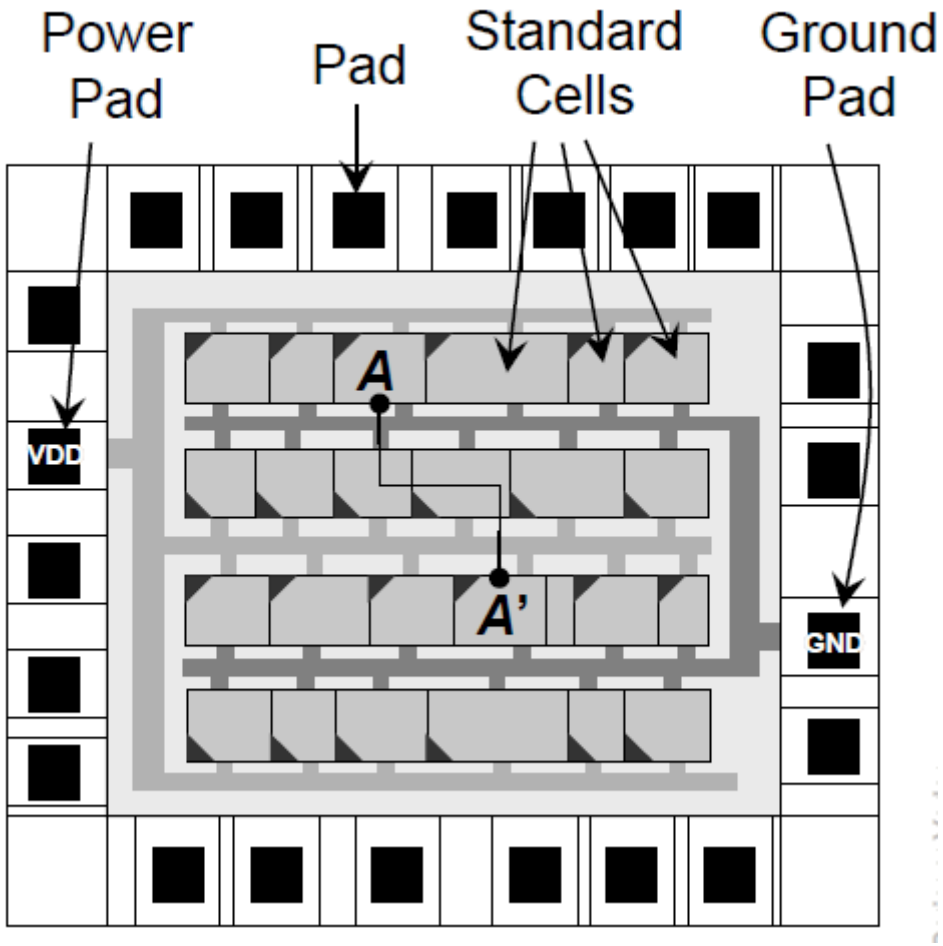
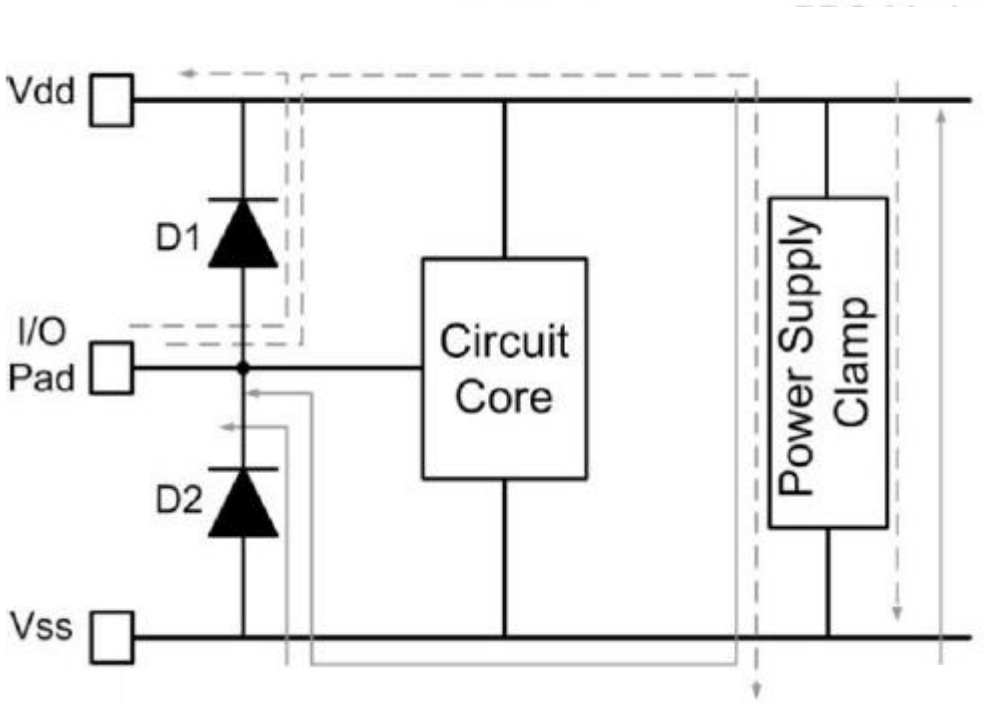
MOTIVATION

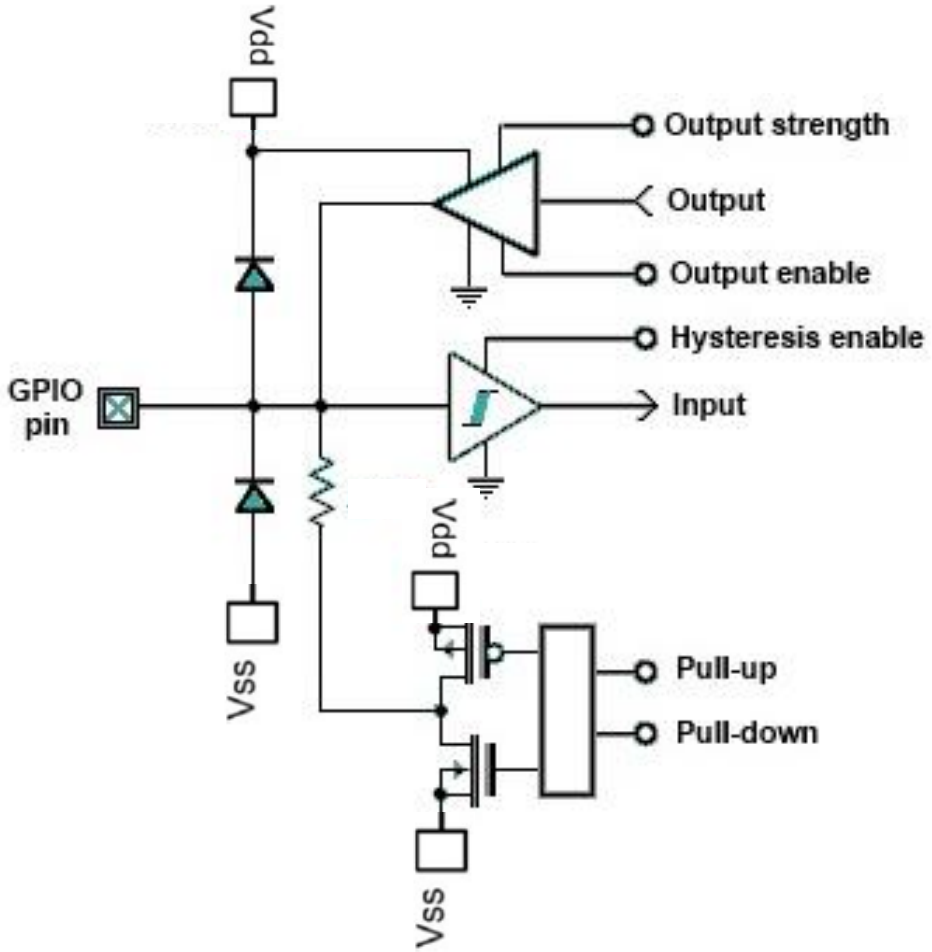


- Standard cell library:
  - comprises of all standard cells – combinational & sequential elements
- IO Library:
  - Comprises of IO pads – VDD pads, VSS pads, analog pads, digital input/output pads
  - ESD protection part of the IO pad (usually circuit under pad)

TYPICAL ESD PROTECTION CIRCUIT



Typical Analog I/O PAD



Typical bi-directional, programmable digital I/O PAD

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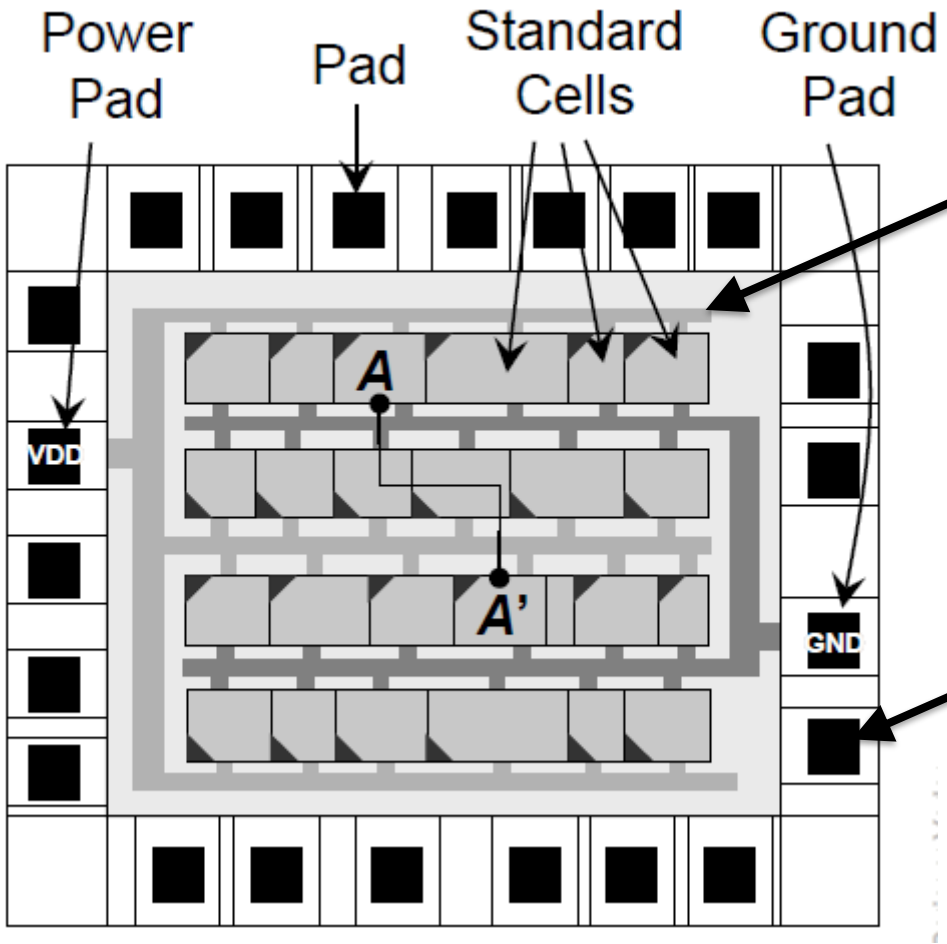
FULL CHIP PICTURE

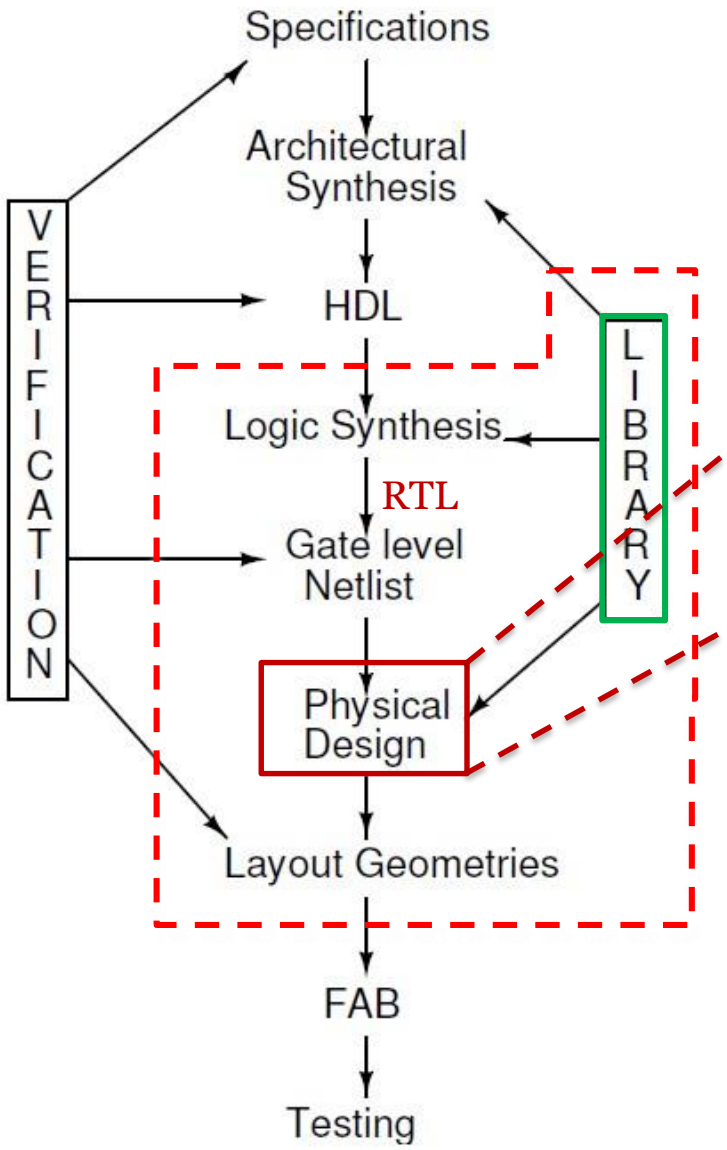


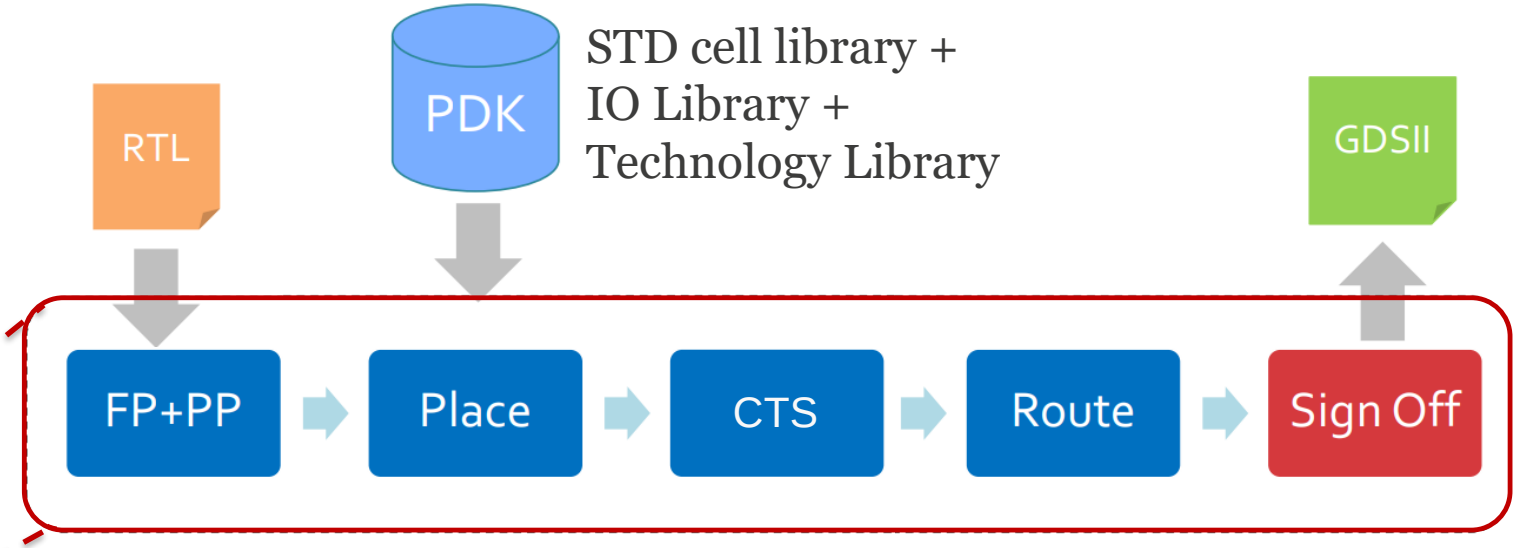
Core circuit area made of standard cells.

Analog or digital IO pads depending on the nature of the signal. The circuit is sitting under the metal pad (black shade) outside the core area.

The metal pad will be wire-bonded to the package

PHYSICAL DESIGN





1. FP + PP: Floor planning + Power planning
2. Place: Placement
3. CTS: Clock tree synthesis
4. Route: Routing (Global and local)
5. Sign-off: final checks before gdsII submission
   a) DRC: Design rule check
   b) LVS: layout – vs - schematic
   c) STA: Static Timing Analysis

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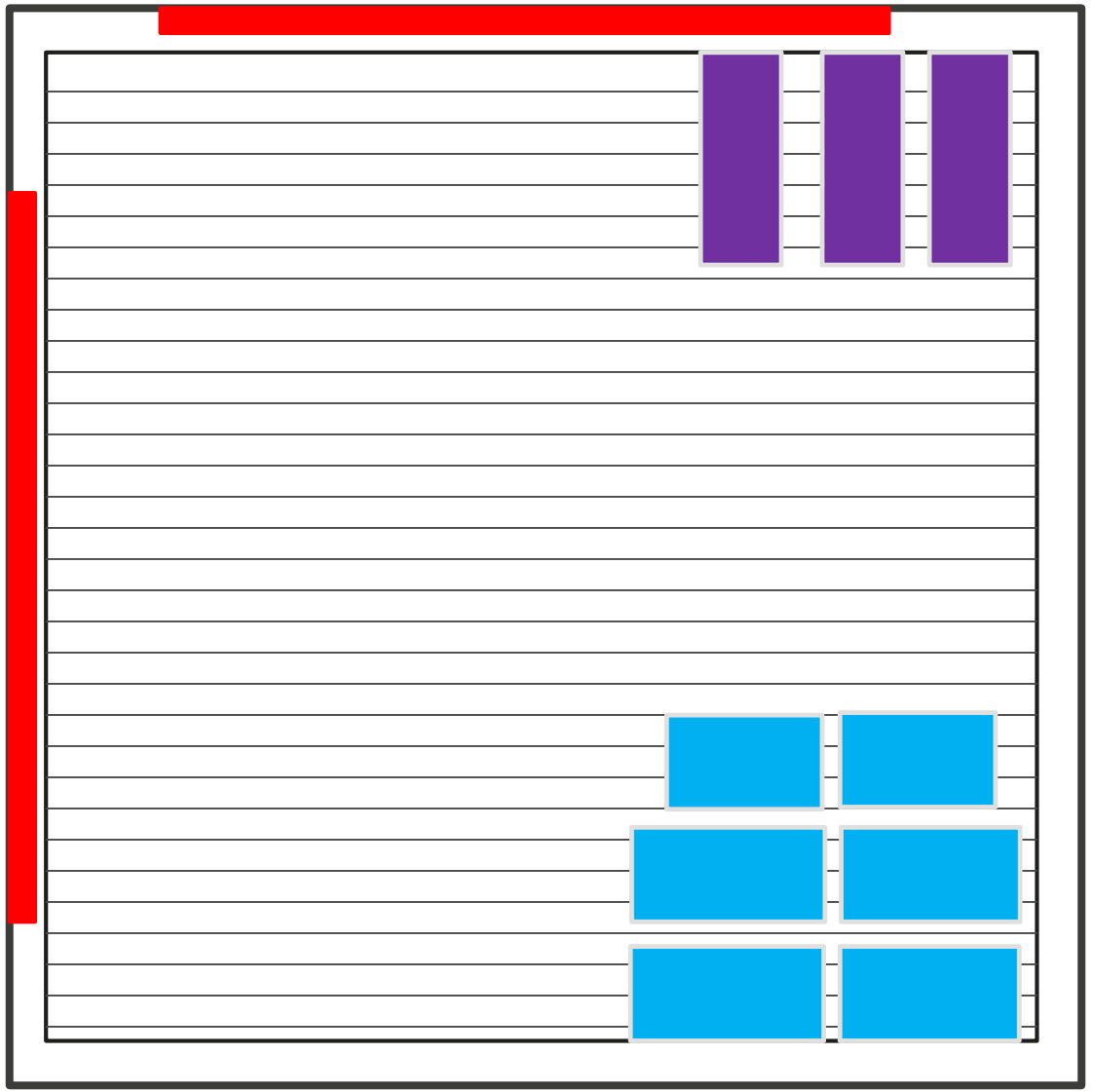
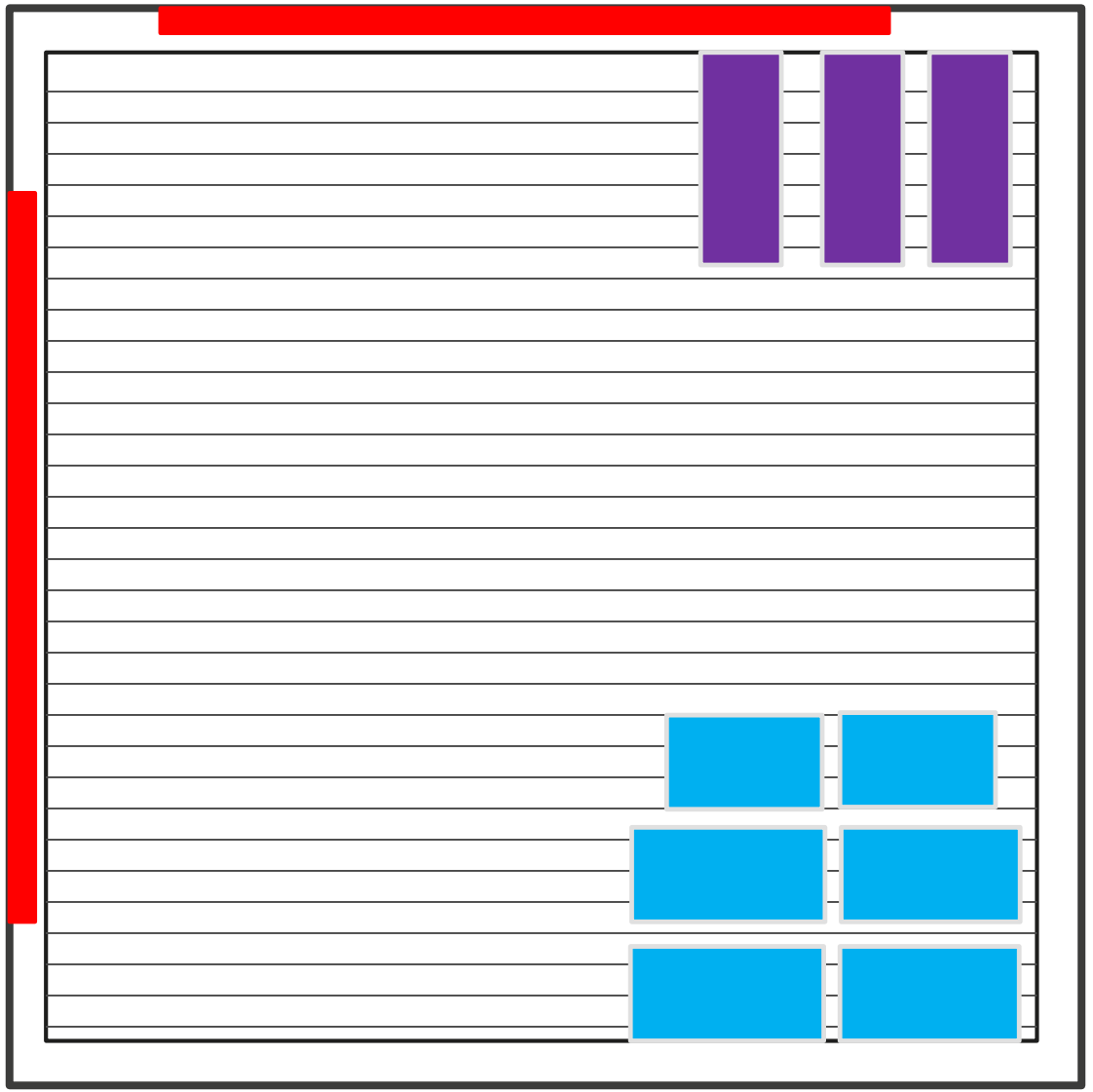
PHYSICAL DESIGN: FLOORPLAN

- Floor planning:
- Define core area size (Area: Width & Height)
- Create cell rows (std cell height)
- IO placement:
  - Define what kind of IO (analog/digital/VDD/VSS) should reside where
- Macro cell placement:
  - Macros are modules for which you already have a layout (Ex: third part memory, ARM core etc.)



PHYSICAL DESIGN: FLOORPLAN

- Macro Placement:
- Make smart choices:
  - Timing: be aware of what block talk to what so that you can place them closer (for minimal routing)
  - Macro pins oriented towards nearest standard cells
  - Distance of memory macro from standard cells
  - Plan to avoid routing congestion (number of connections from macro)



PHYSICAL DESIGN: FLOORPLAN

- Macro Placement:
  - Example congestion planning

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PHYSICAL DESIGN: FLOORPLAN

- Macro Placement:
  - Example congestion planning
  - Move macros away from IO if the macro does not have any connections to IO
  - Place memory cells to avoid routing congestion

Floorplan Height

Floorplan Width

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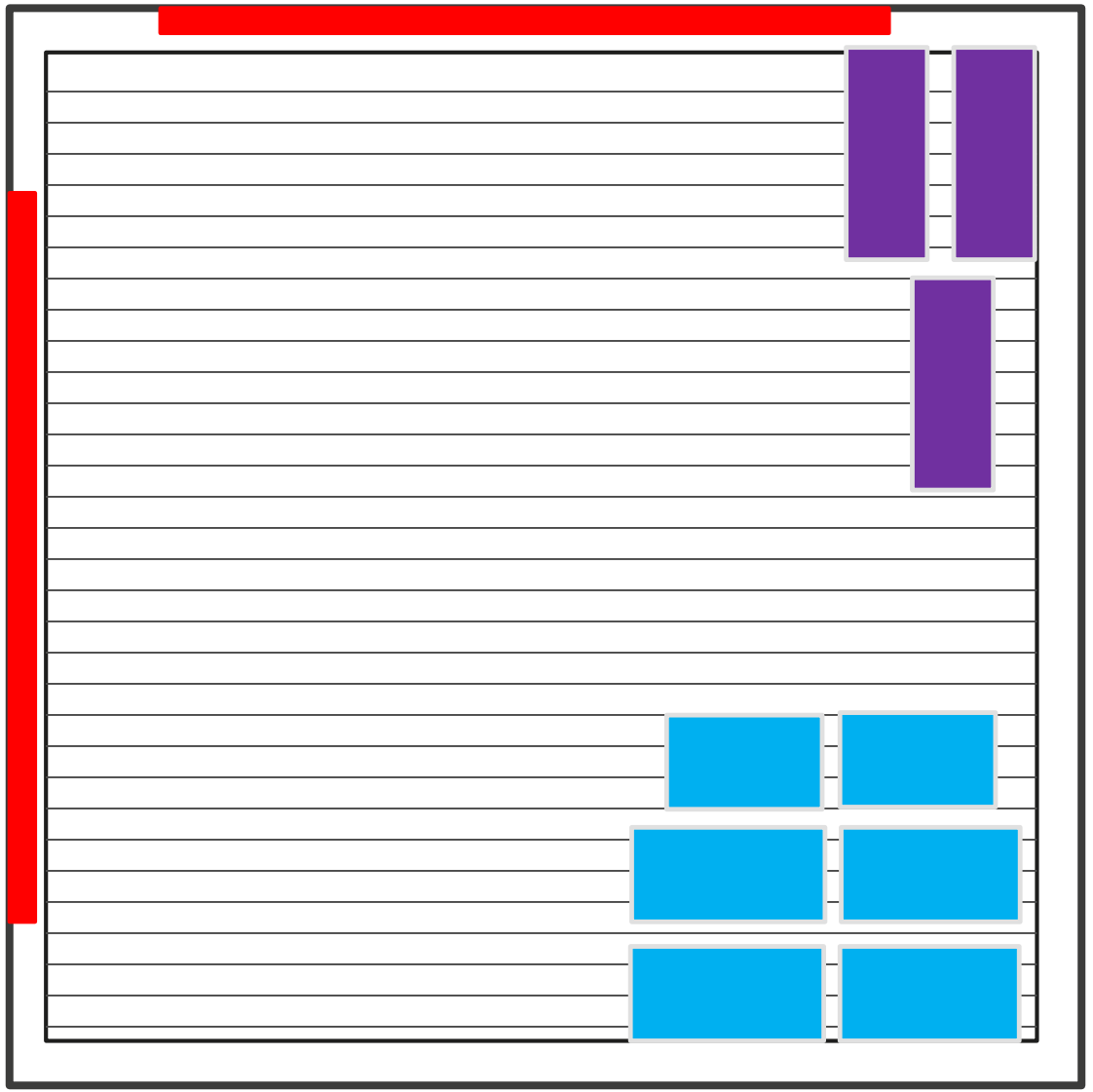

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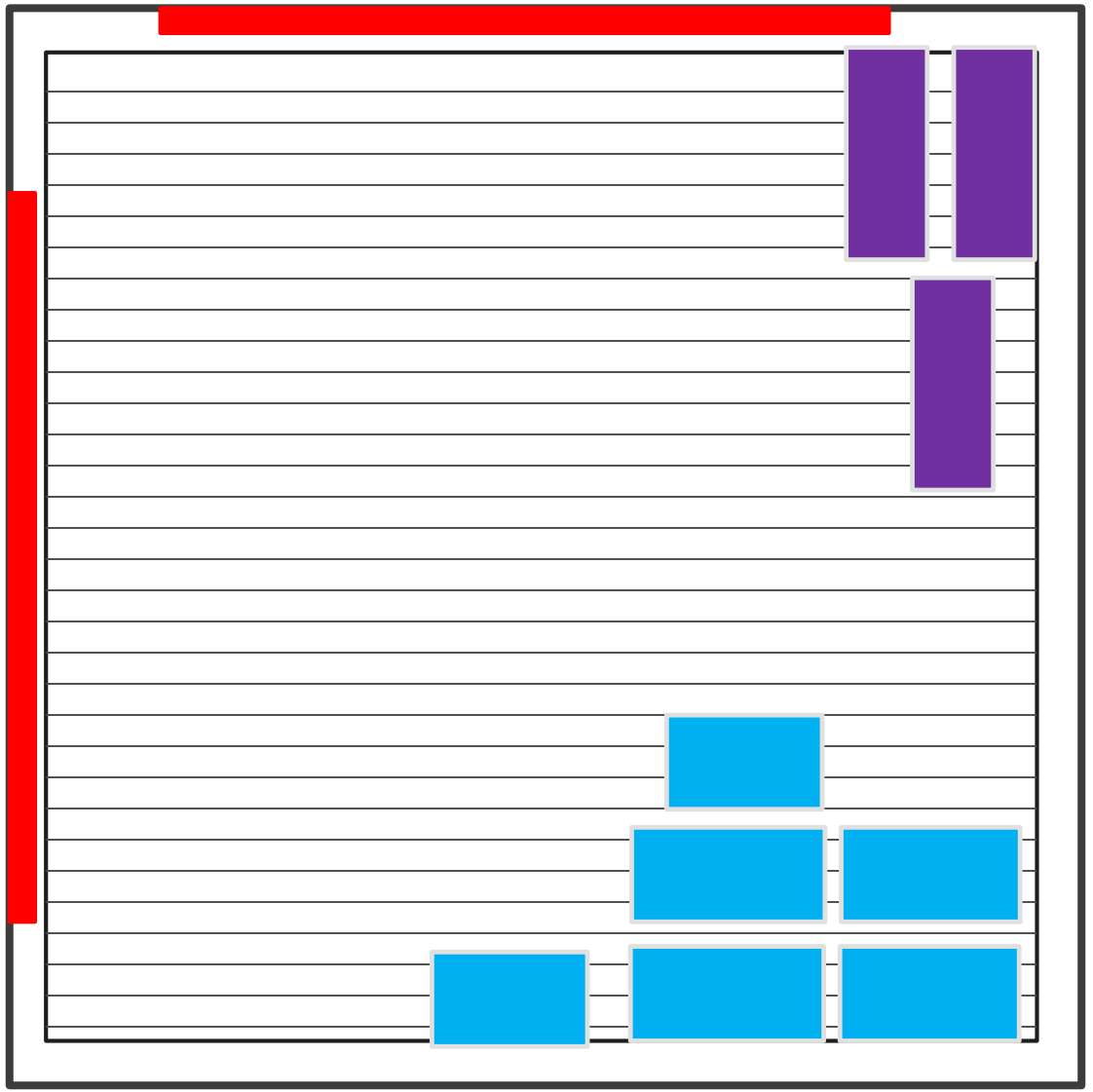

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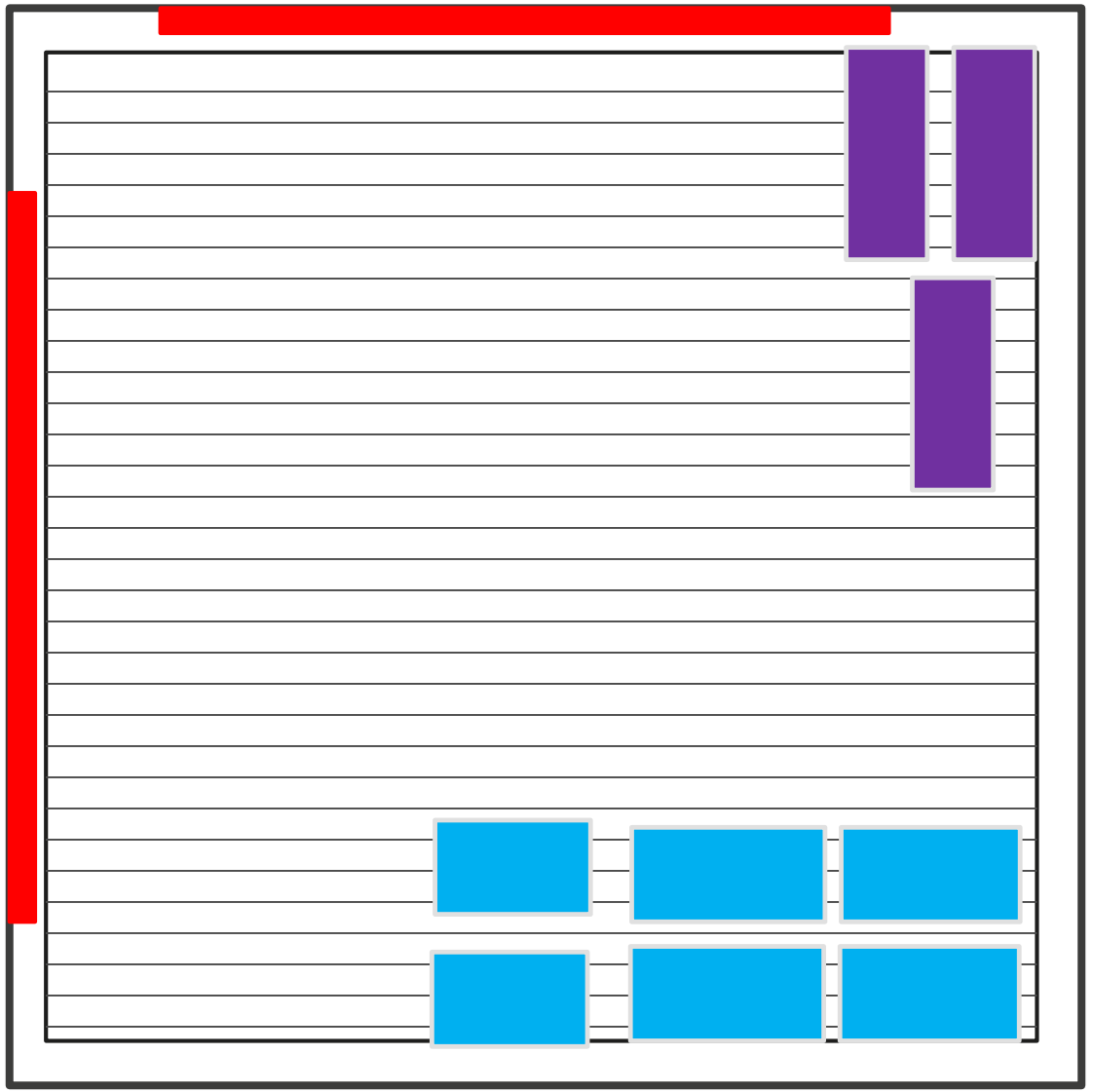

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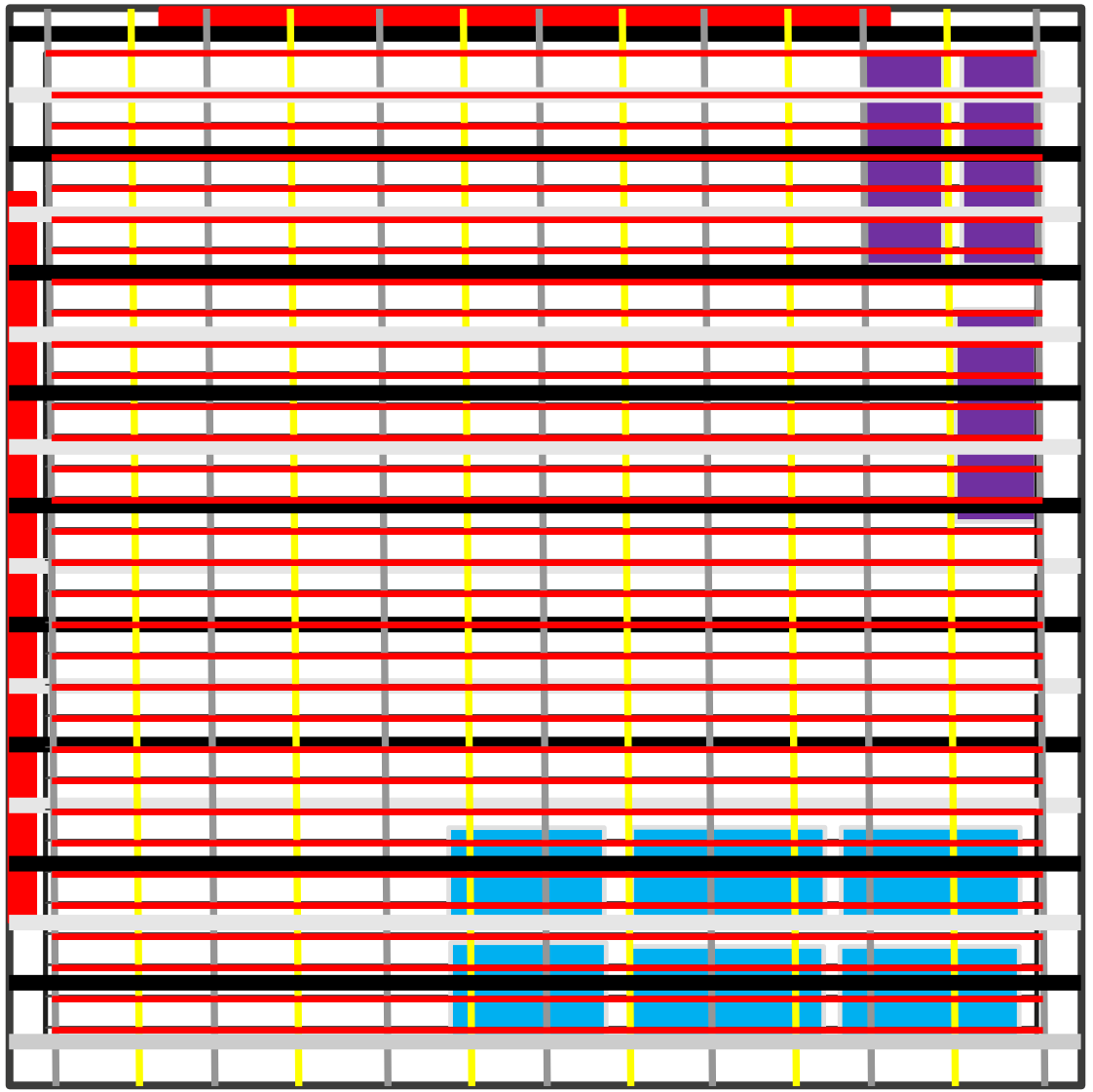
PHYSICAL DESIGN: FLOORPLAN

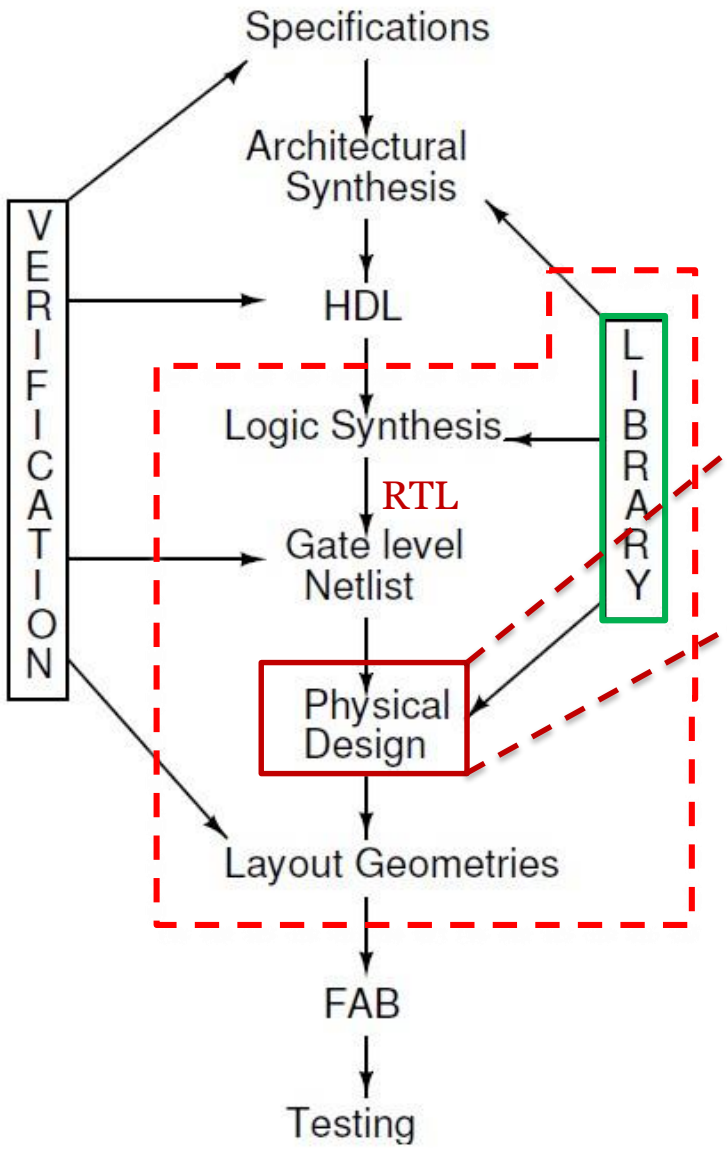
- Power Planning:
- Supply VDD/VSS to standard cells and Macros
- Complex designs:
  - Be aware of the power consumption of blocks – IR drop on the power rail/grid – degrades circuit performance

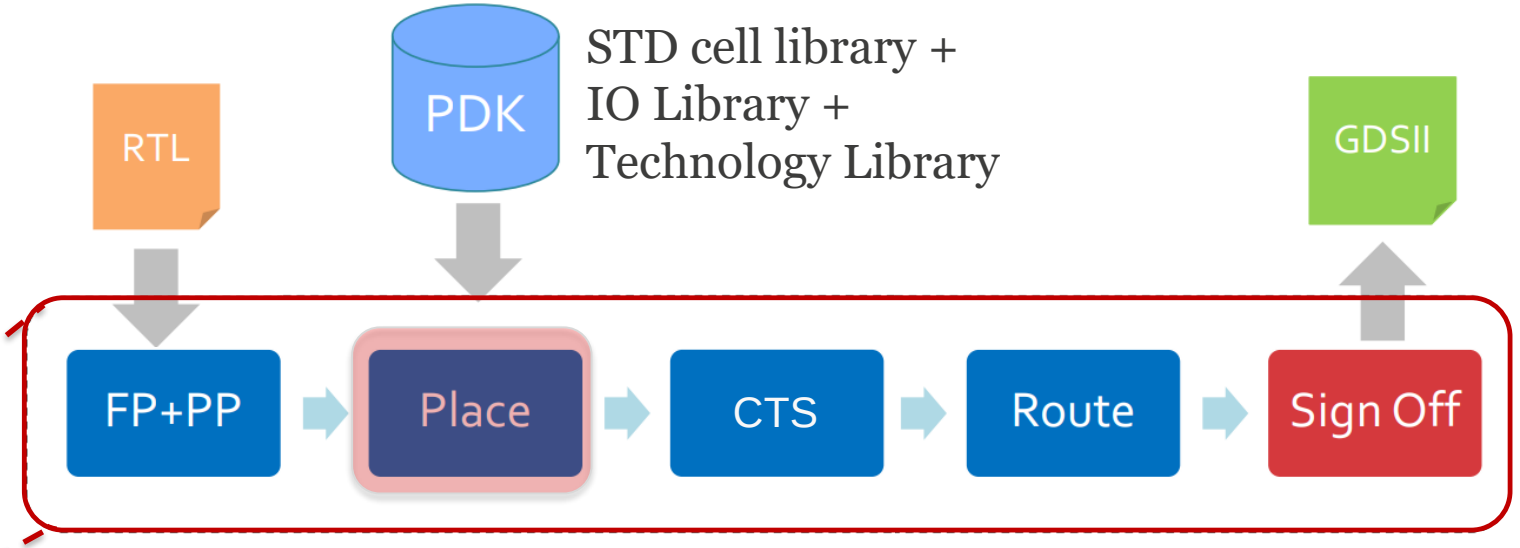


Floorplan Height

Floorplan Width

PHYSICAL DESIGN





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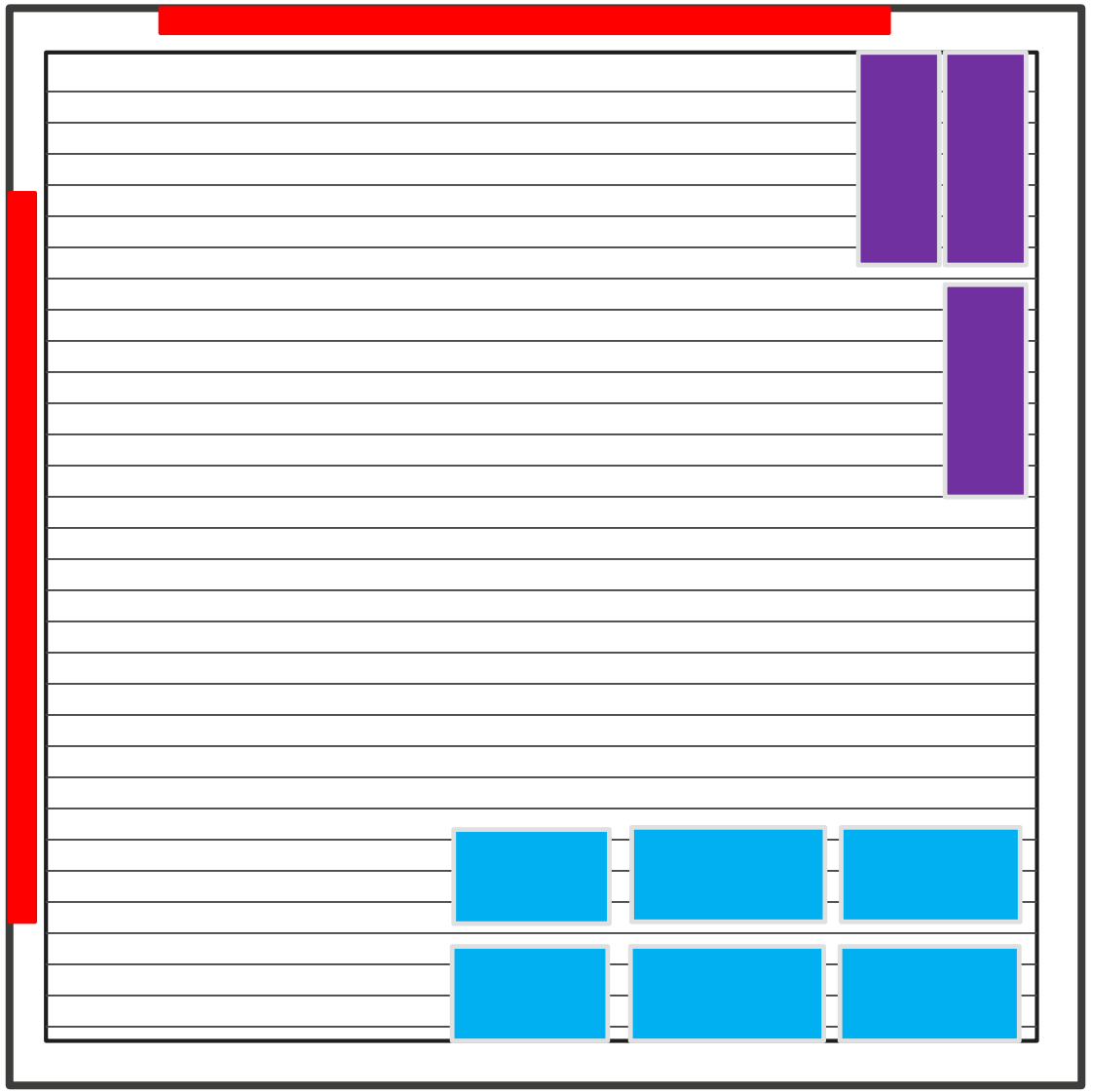
PHYSICAL DESIGN: PLACEMENT

- Placement: mainly placement of std cells. Following steps:
  - Placement optimization
  - Timing optimization
  - Parasitic estimation based on global route (wire line model discussed earlier)
  - Congestion removal
  - Standard cell legalization



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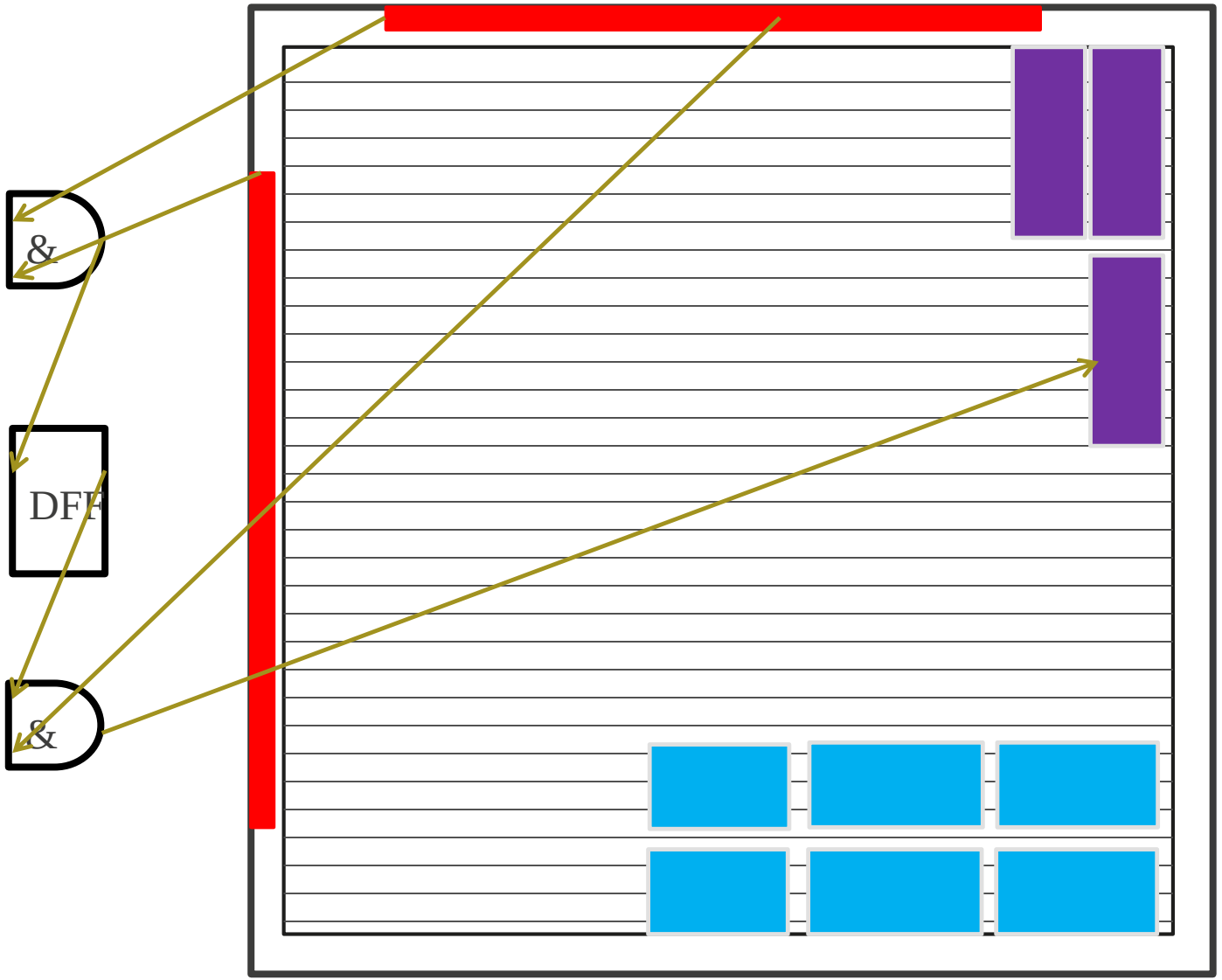

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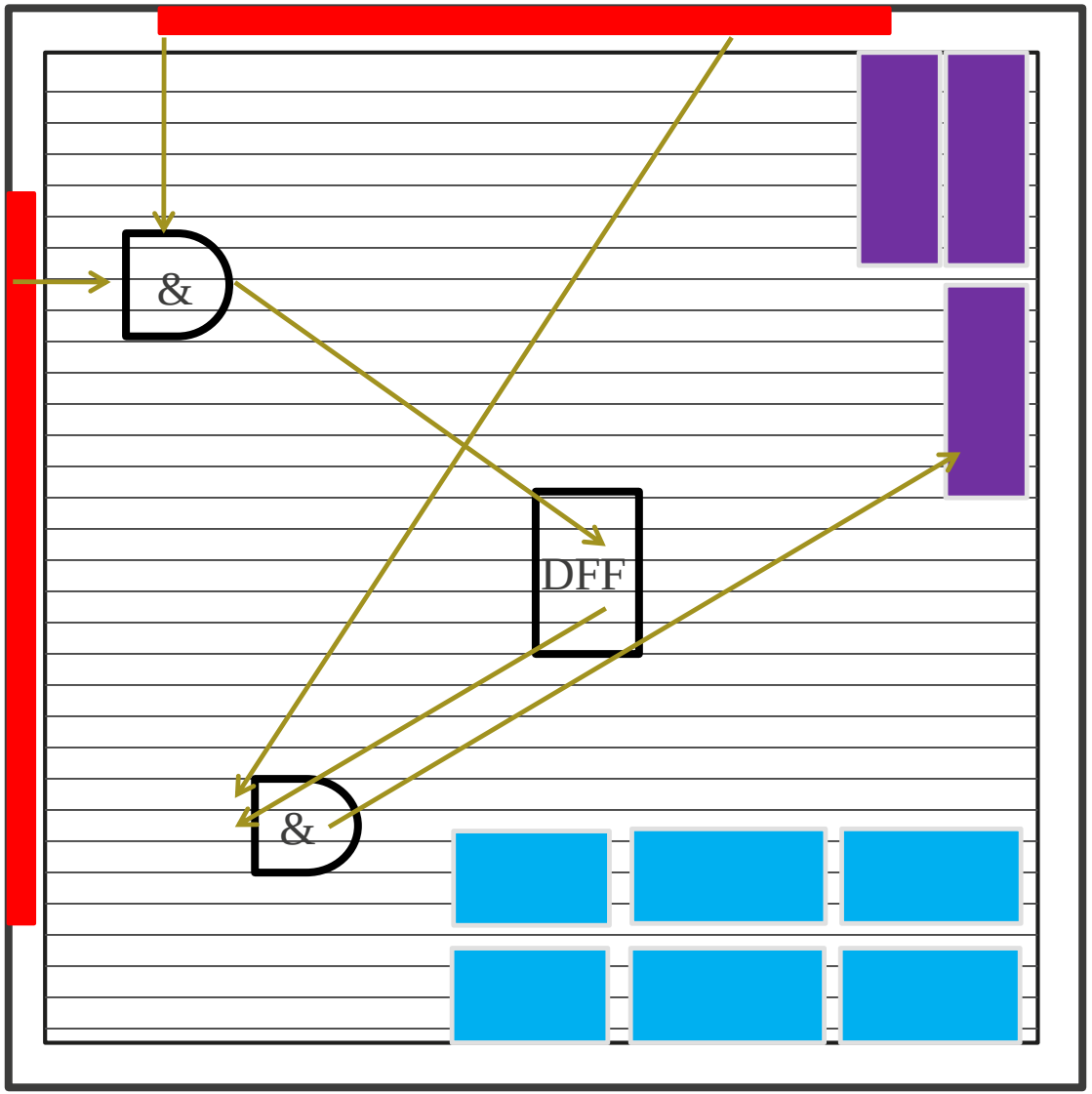

Floorplan Height

Floorplan Width

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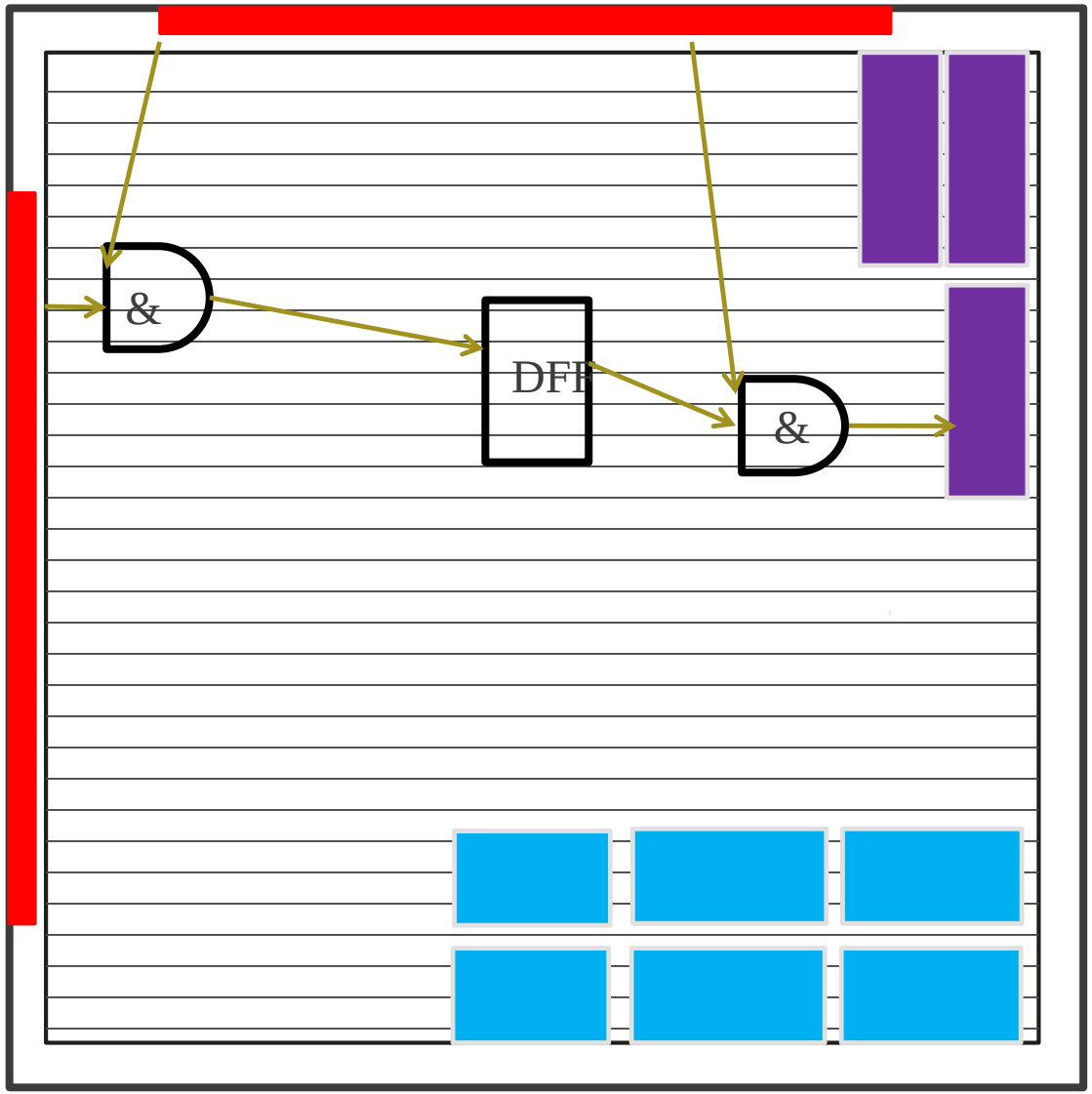
PHYSICAL DESIGN: PLACEMENT

- Placement optimization
  - Placing cells in the vicinity
- Timing optimization
  - Size cells (x1, x2, x4 ..)
  - Buffer insertion
  - Based on wire delay and input capacitance



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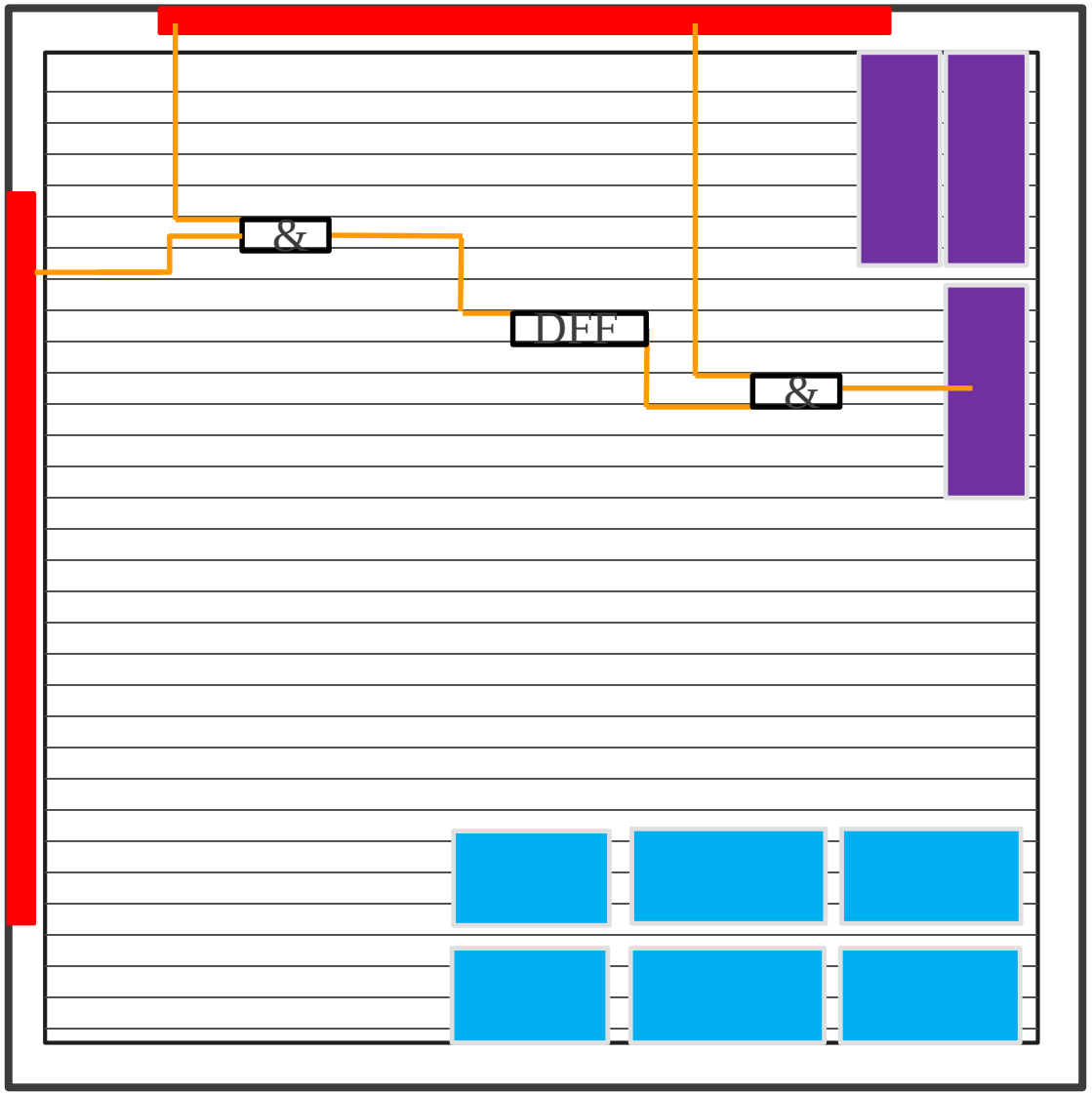

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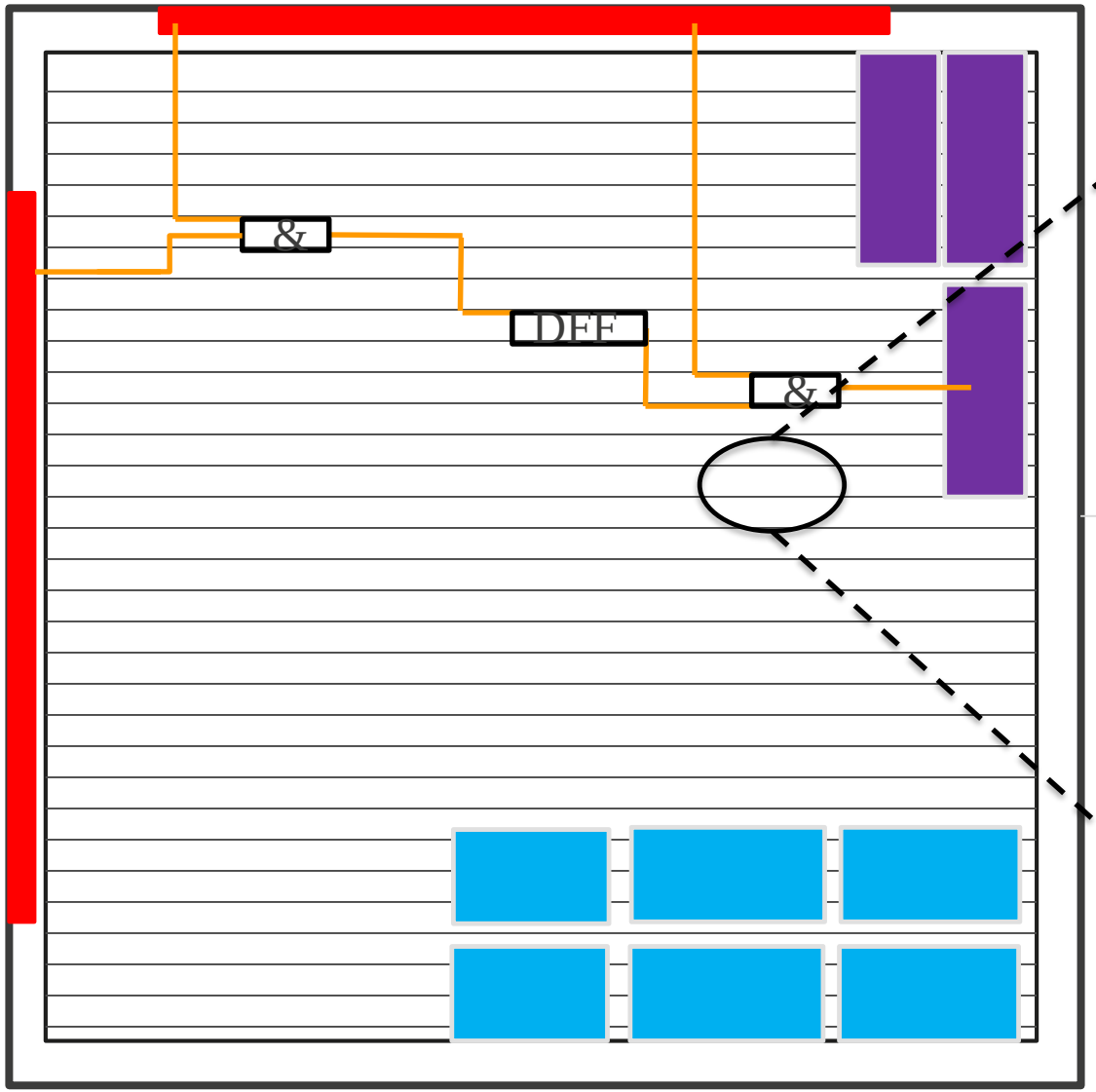
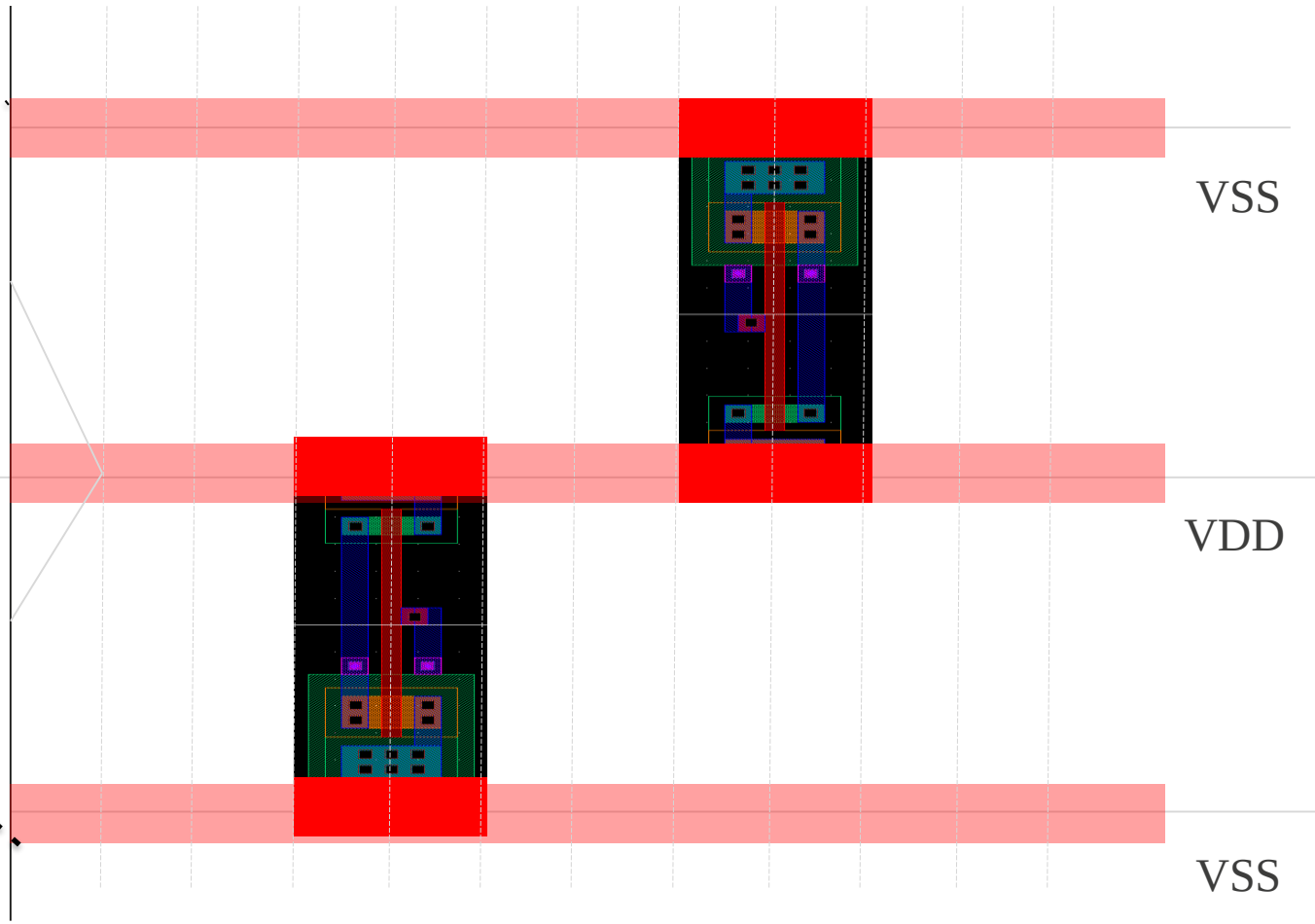
PHYSICAL DESIGN: PLACEMENT LEGALIZATION





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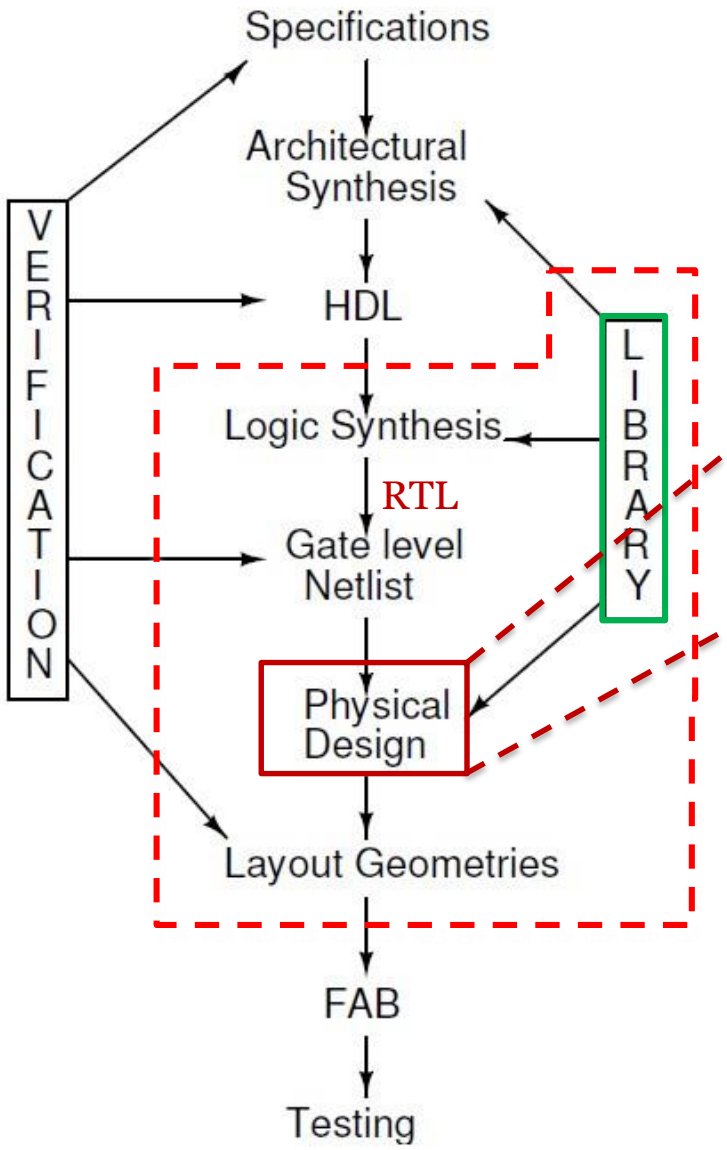

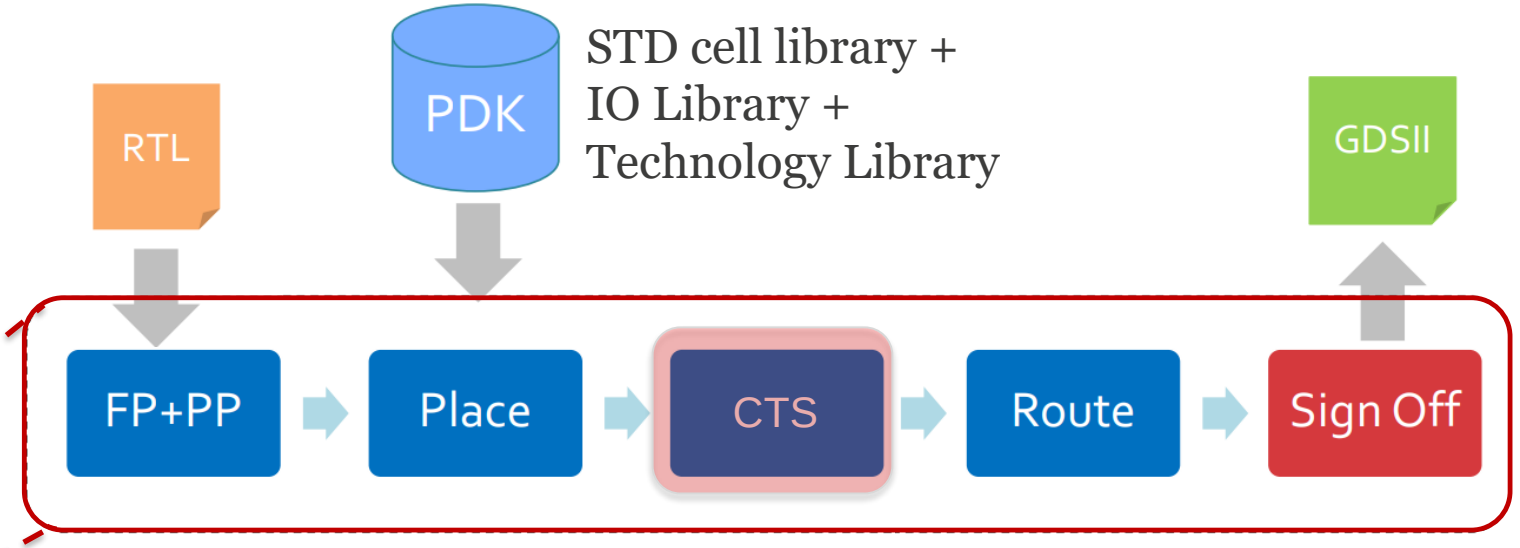

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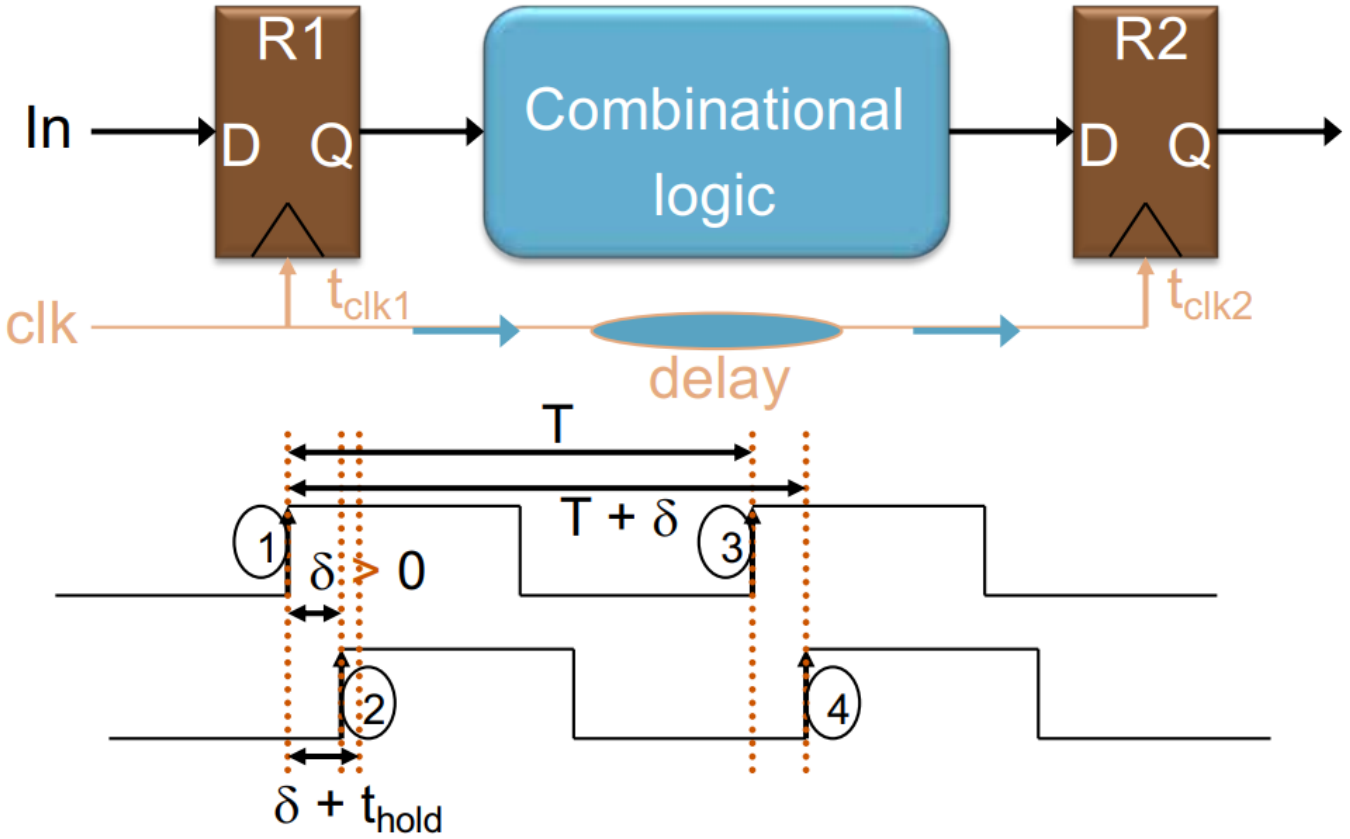
PHYSICAL DESIGN: CTS MOTIVATION

- Clock Skew: delay in clock edges between sequential elements



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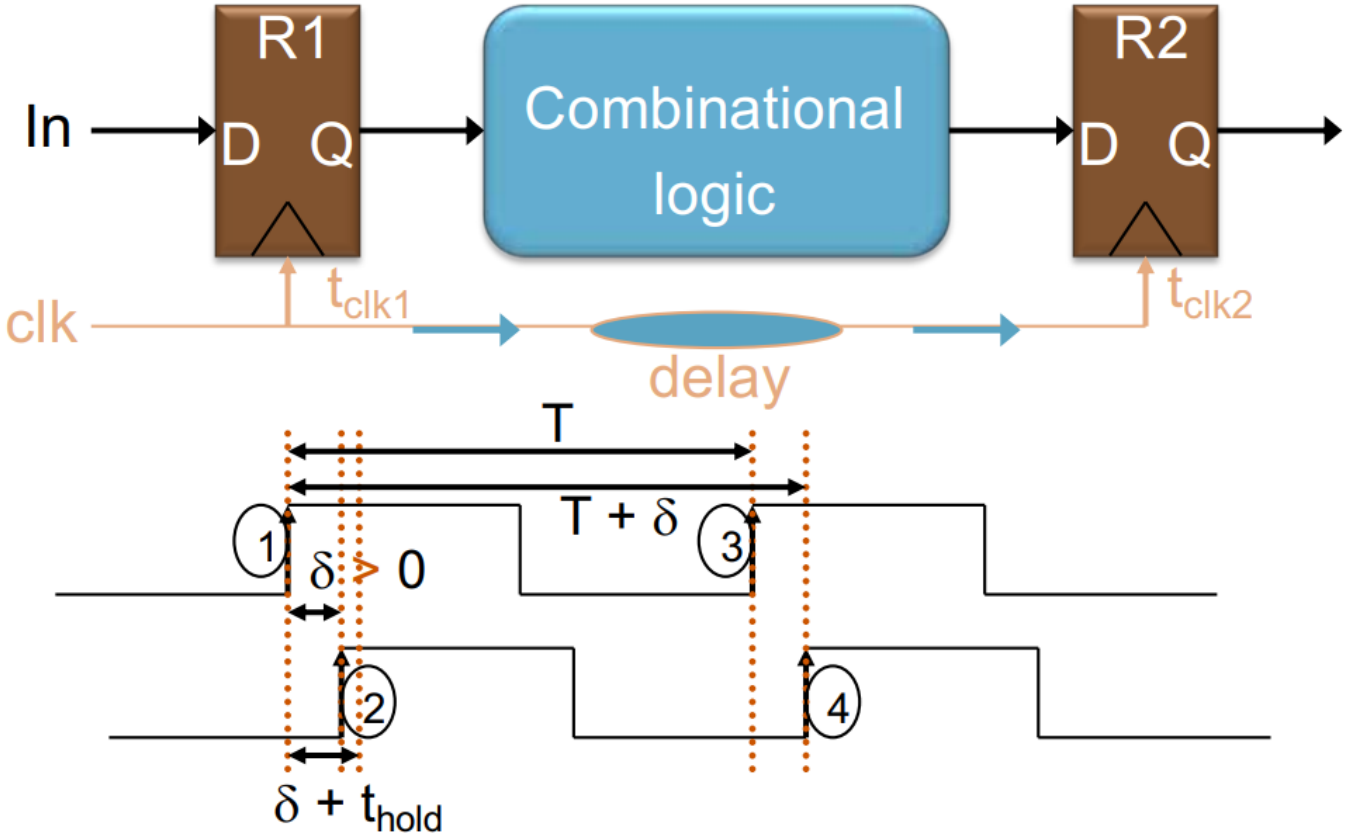
PHYSICAL DESIGN: CTS MOTIVATION

- Positive clock skew: $\delta > 0$

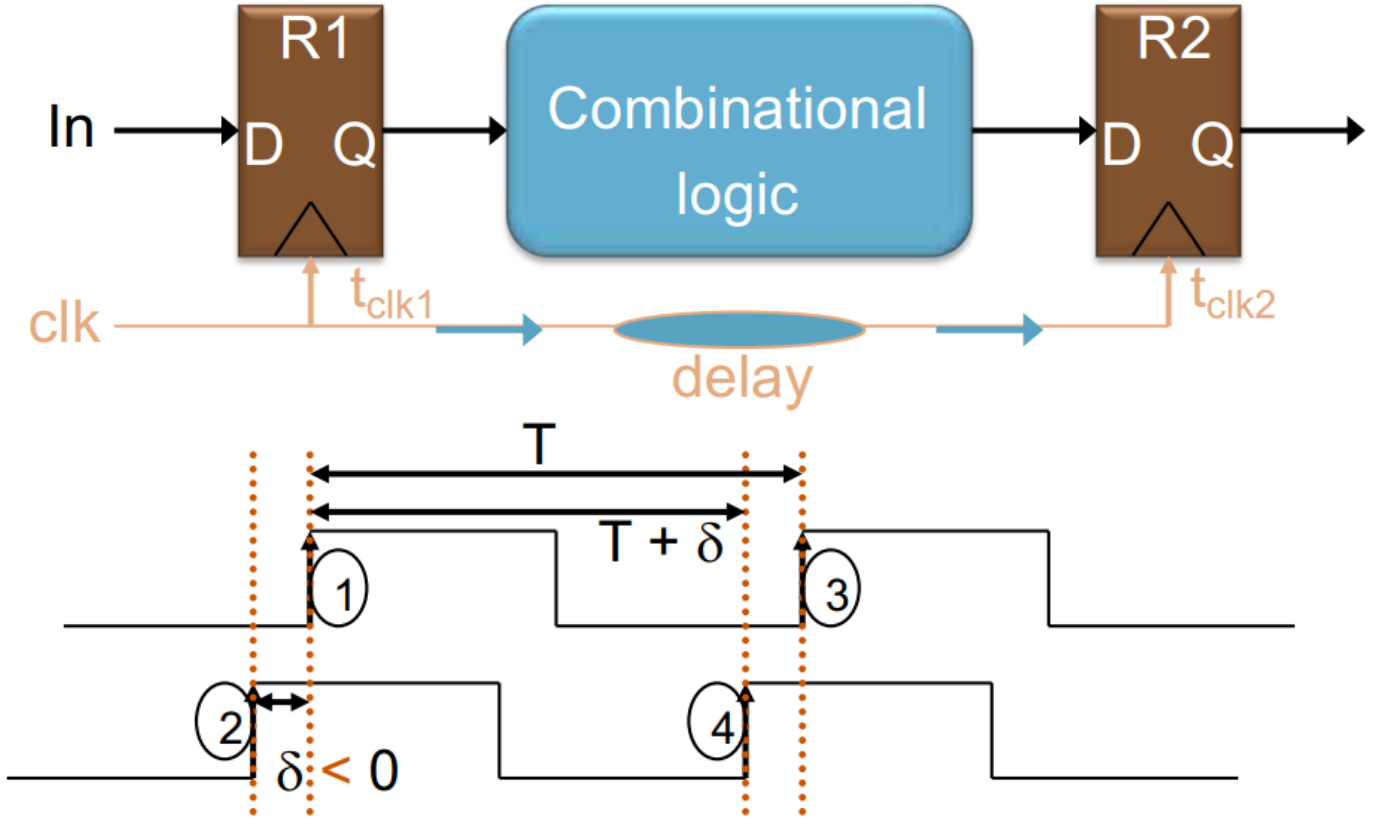


$$T + \delta \geq t_{clk\text{-}Q} + t_{p\text{-}logic(max)} + t_s \rightarrow T \geq t_{clk\text{-}Q} + t_{p\text{-}logic(max)} + t_s - \delta$$ 😀

$$t_h + \delta \leq t_{clk\text{-}Q} + t_{p\text{-}logic(min)} \rightarrow t_h \leq t_{clk\text{-}Q} + t_{p\text{-}logic(min)} - \delta$$ ☹

PHYSICAL DESIGN: CTS MOTIVATION

- Negative clock skew: $\delta < 0$



$$T - |\delta| \geq t_{clk\text{-}Q} + t_{p\text{-}logic(max)} + t_s \rightarrow T \geq t_{clk\text{-}Q} + t_{p\text{-}logic(max)} + t_s + |\delta| \quad ☹$$

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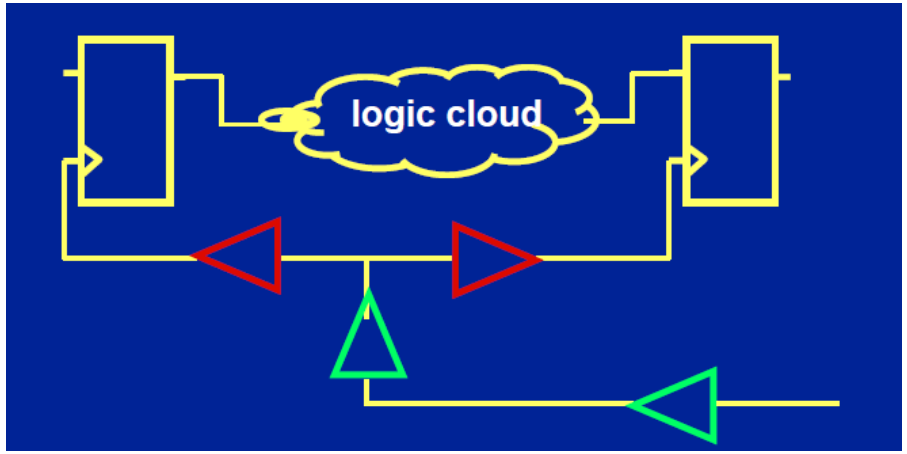
PHYSICAL DESIGN: CTS

- Need clock to reach all points ideally at the same time – to avoid timing violations (setup/hold) due to clock skew

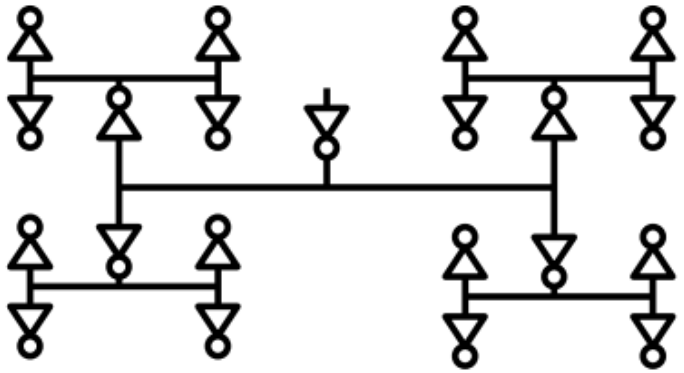


- Create a clock distribution network
  - Three broad categories:
    - Clock tree
    - Clock mesh
    - Clock spine

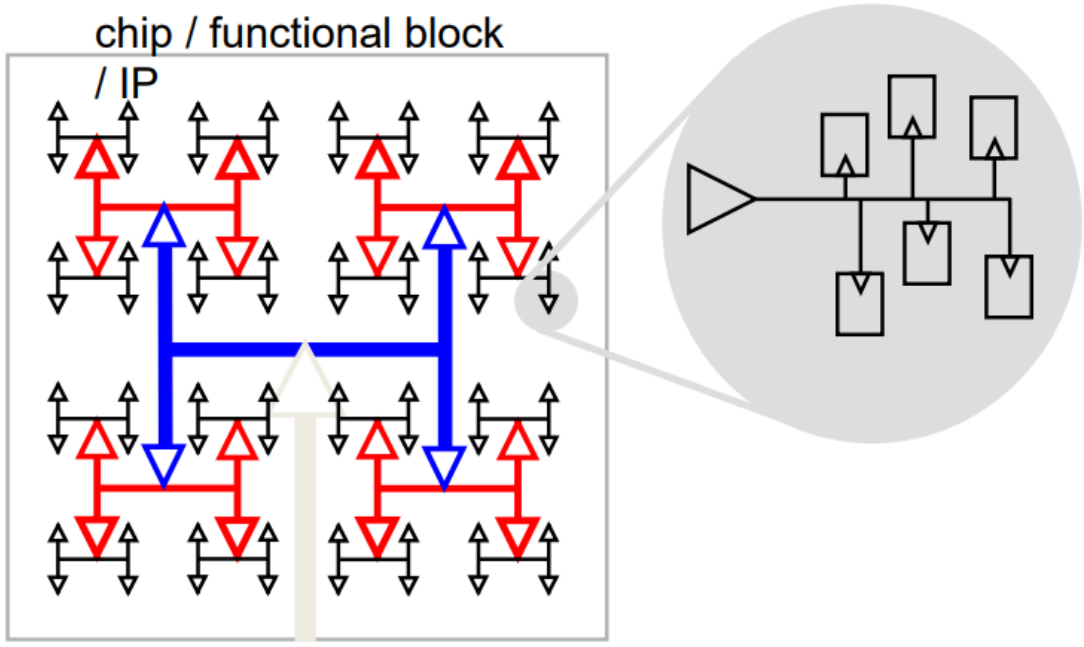
} Will not be covered in this course

PHYSICAL DESIGN: CTS

- Clock tree: popularly used version is H-tree



- Recursively build H-style structure to match wire length
- Inserting a buffer at branching point
- More realistic: tapered H-tree



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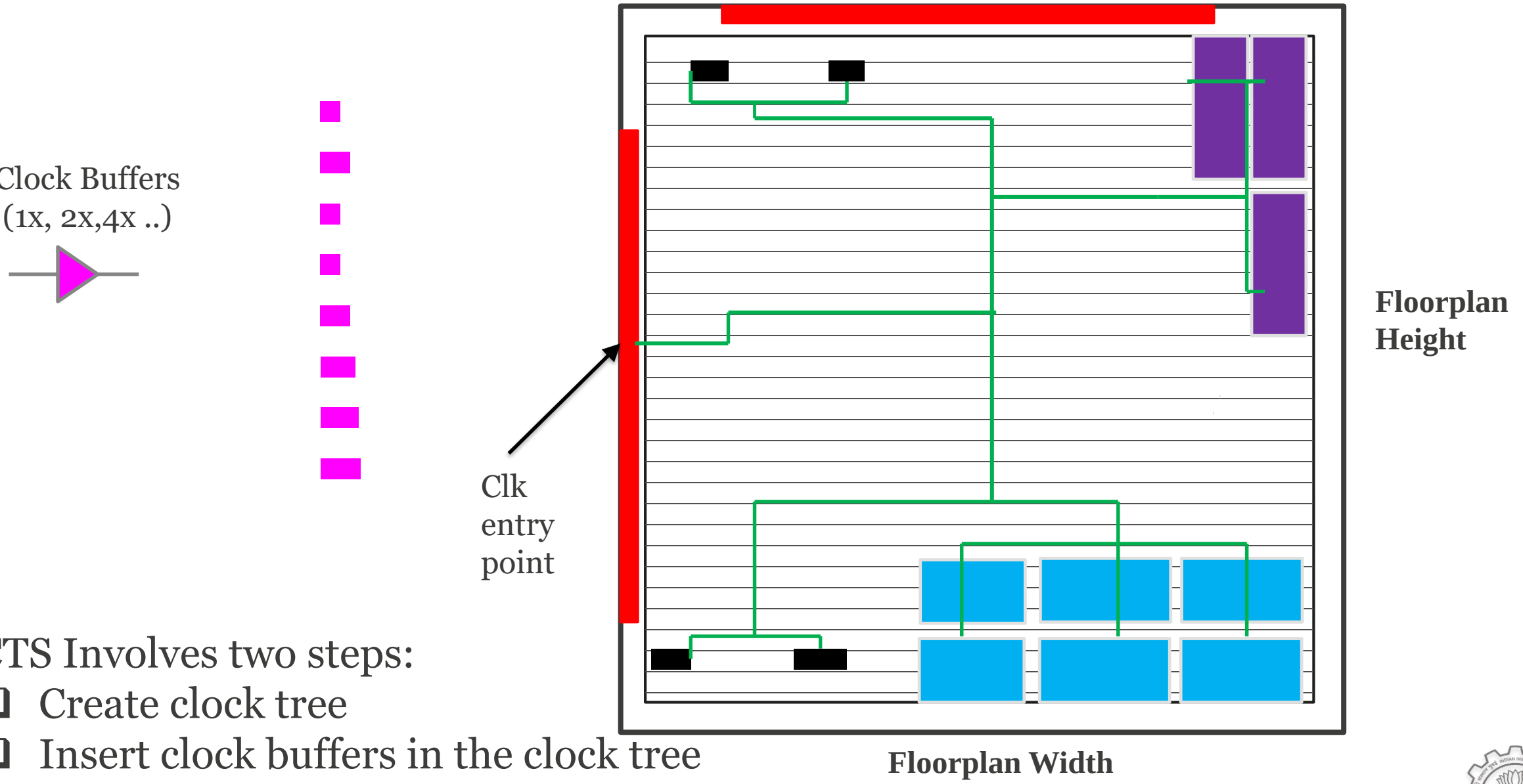
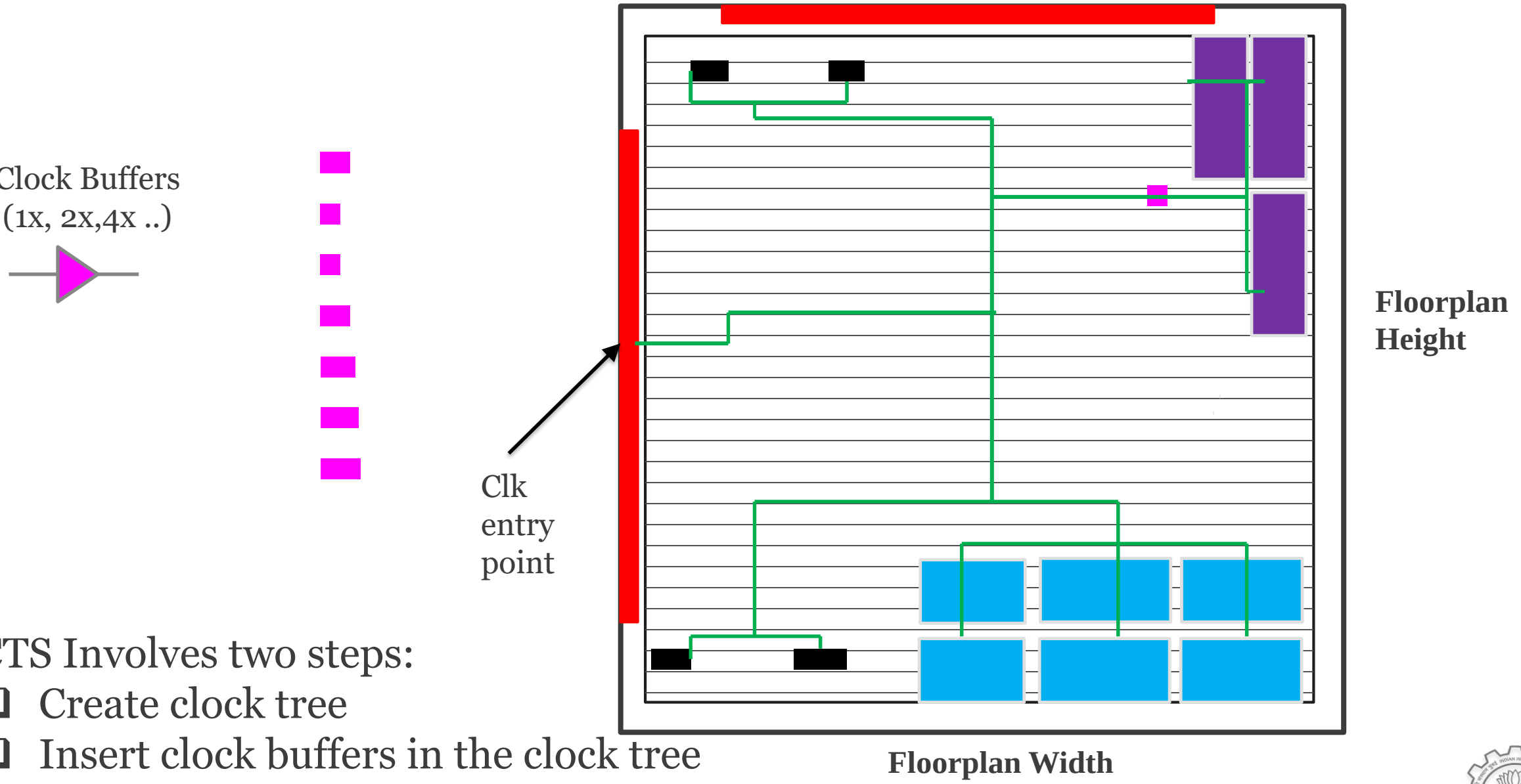
PHYSICAL DESIGN: CTS



- CTS Involves two steps:
  - Create clock tree
  - Insert clock buffers in the clock tree

PHYSICAL DESIGN: CTS



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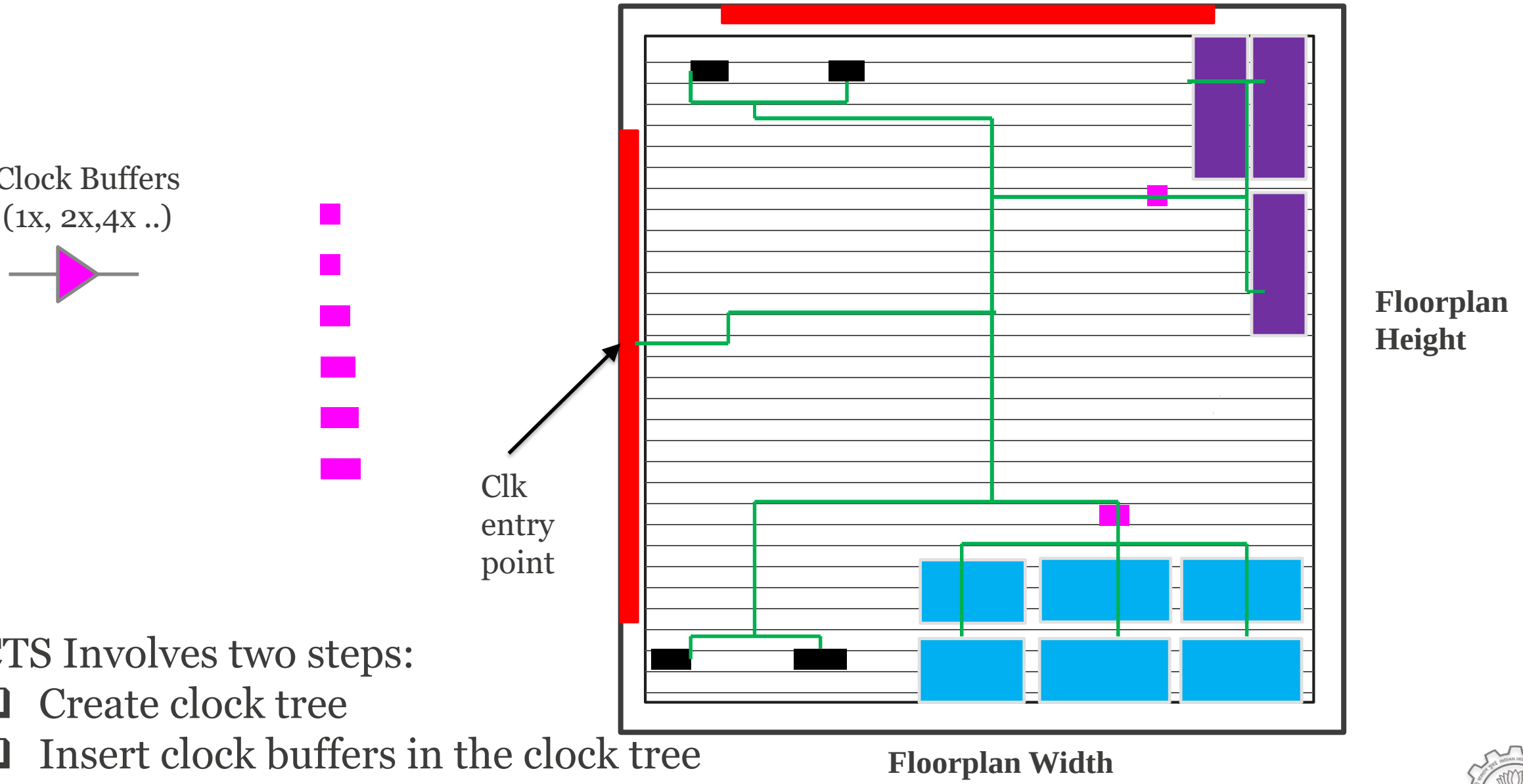

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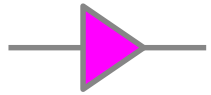
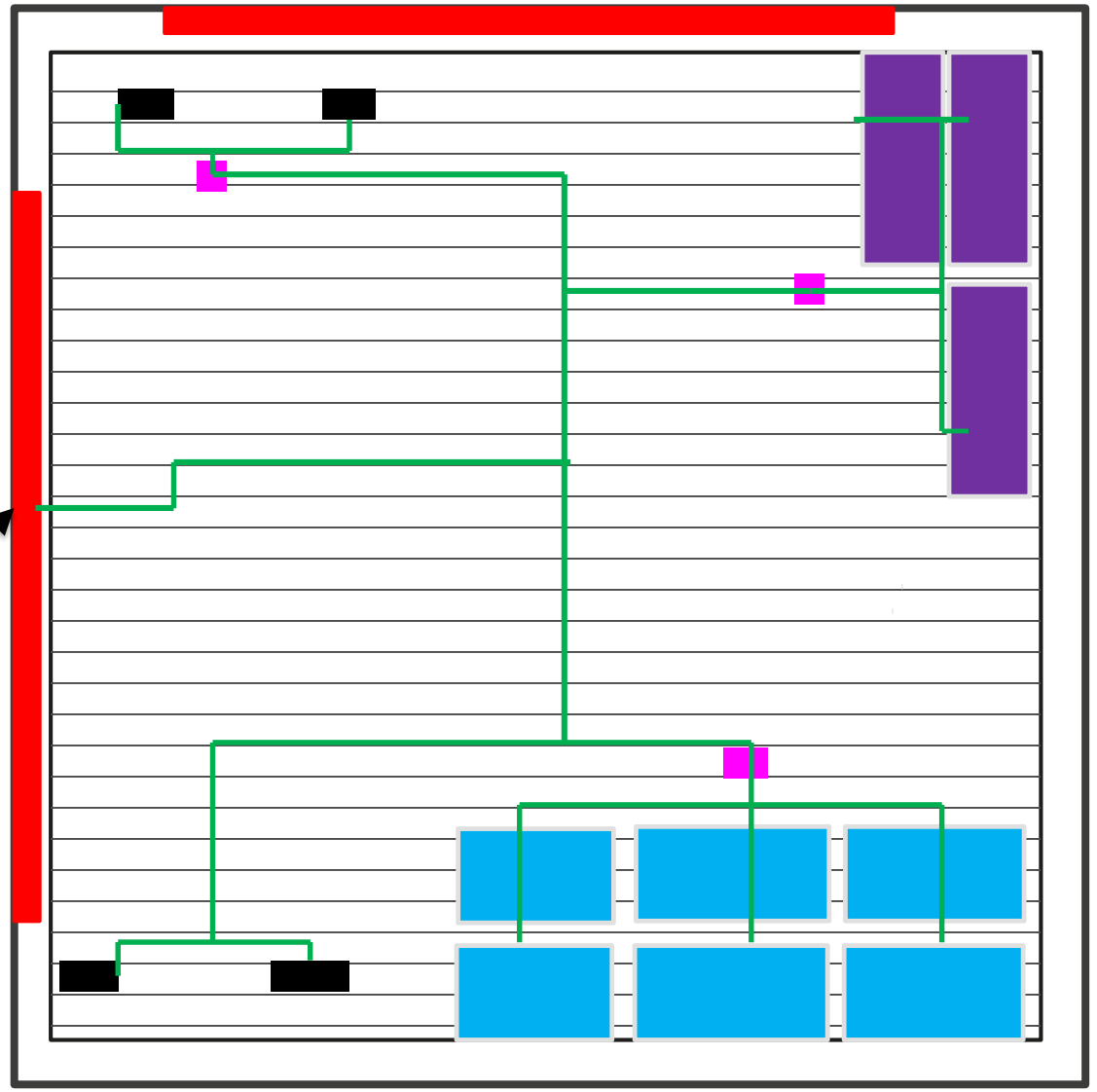
PHYSICAL DESIGN: CTS

Clock Buffers
(1x, 2x,4x ..)





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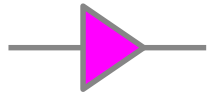

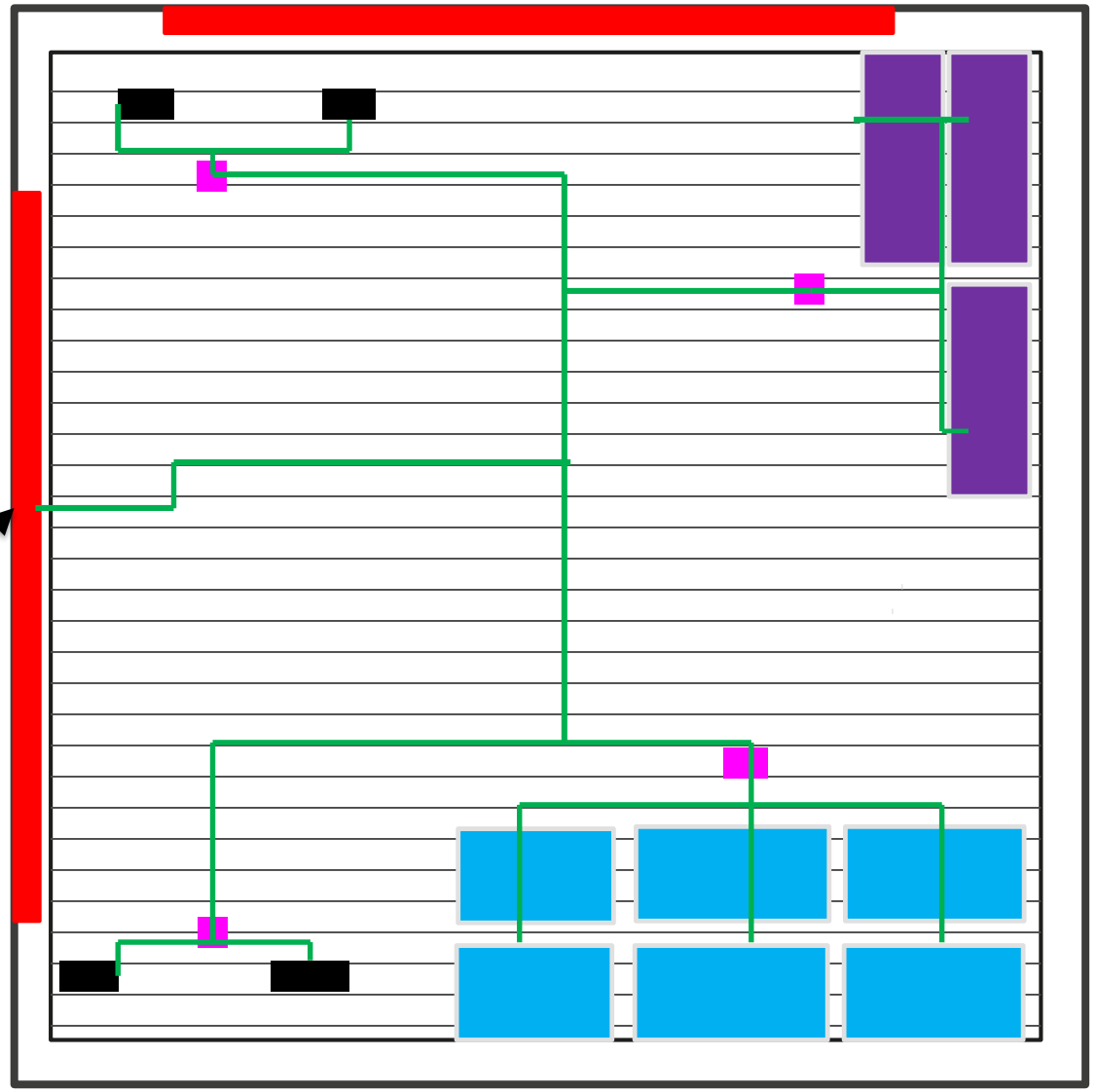

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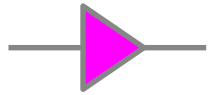

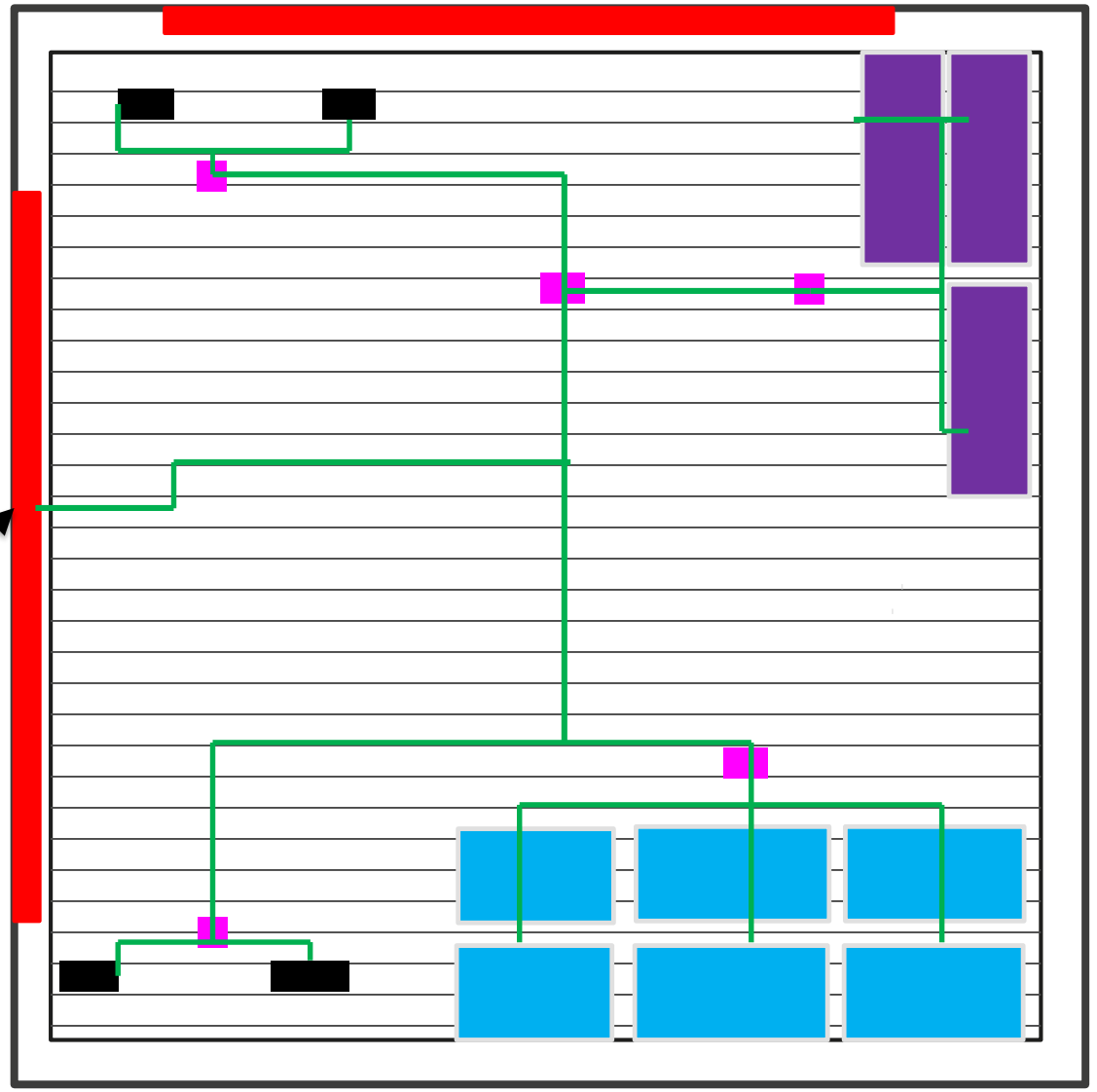

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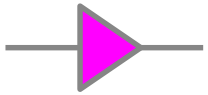
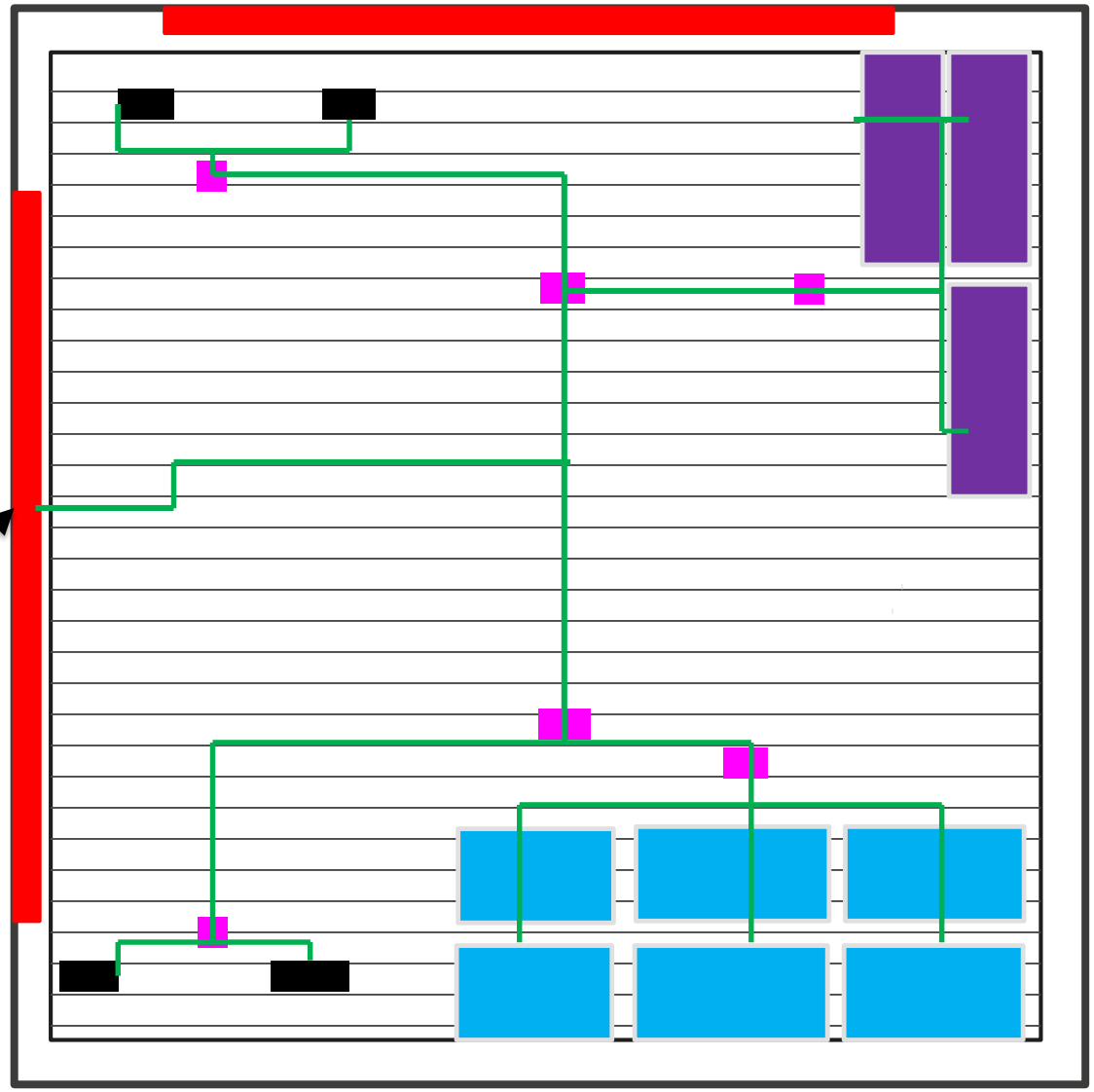


Clk
entry
point



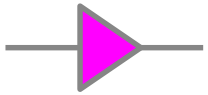
Floorplan Height

Floorplan Width

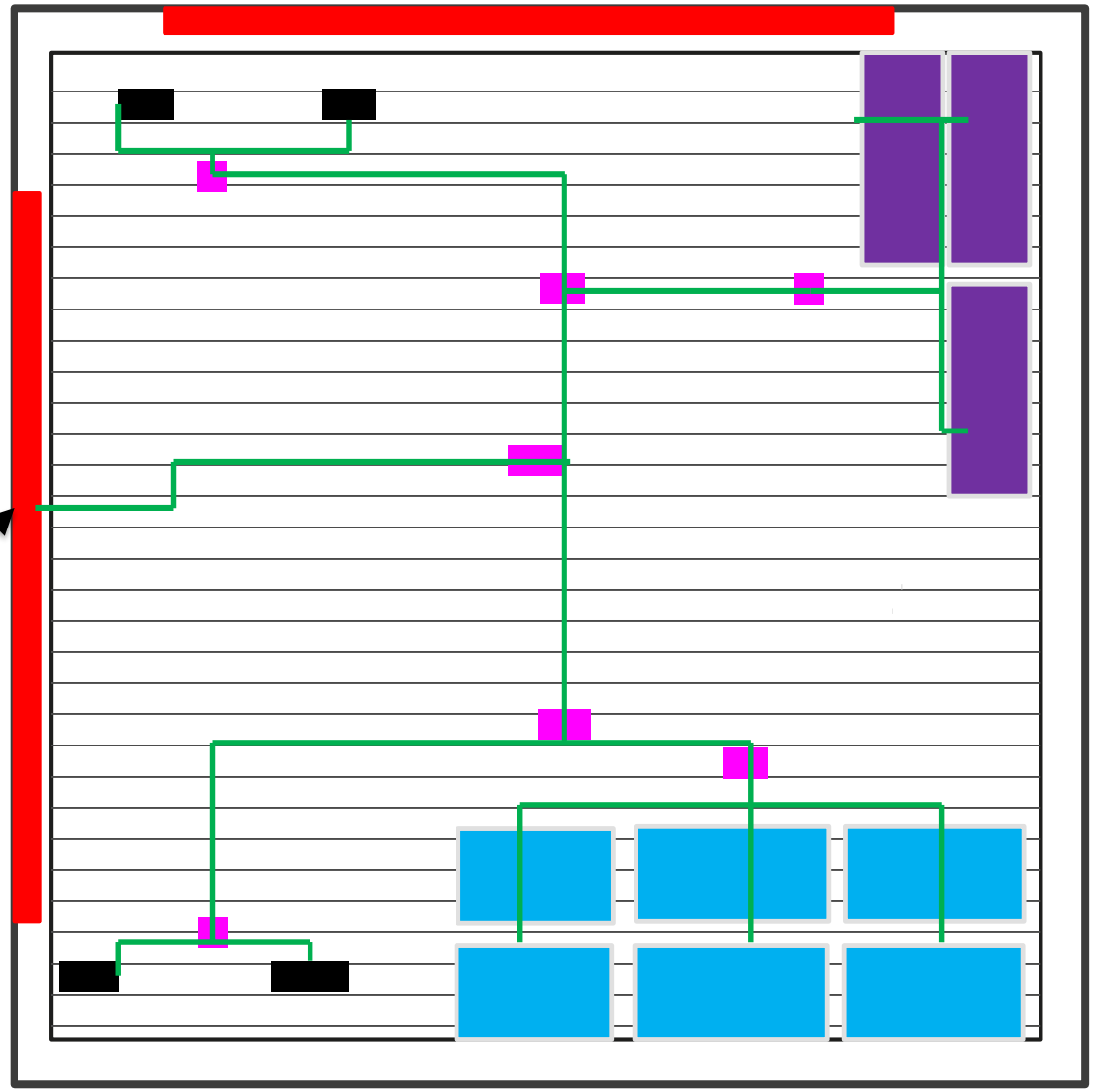
- CTS Involves two steps:
  - Create clock tree
  - Insert clock buffers in the clock tree

PHYSICAL DESIGN: CTS

Clock Buffers
(1x, 2x,4x ..)



Clk
entry
point



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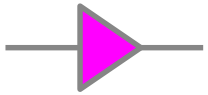

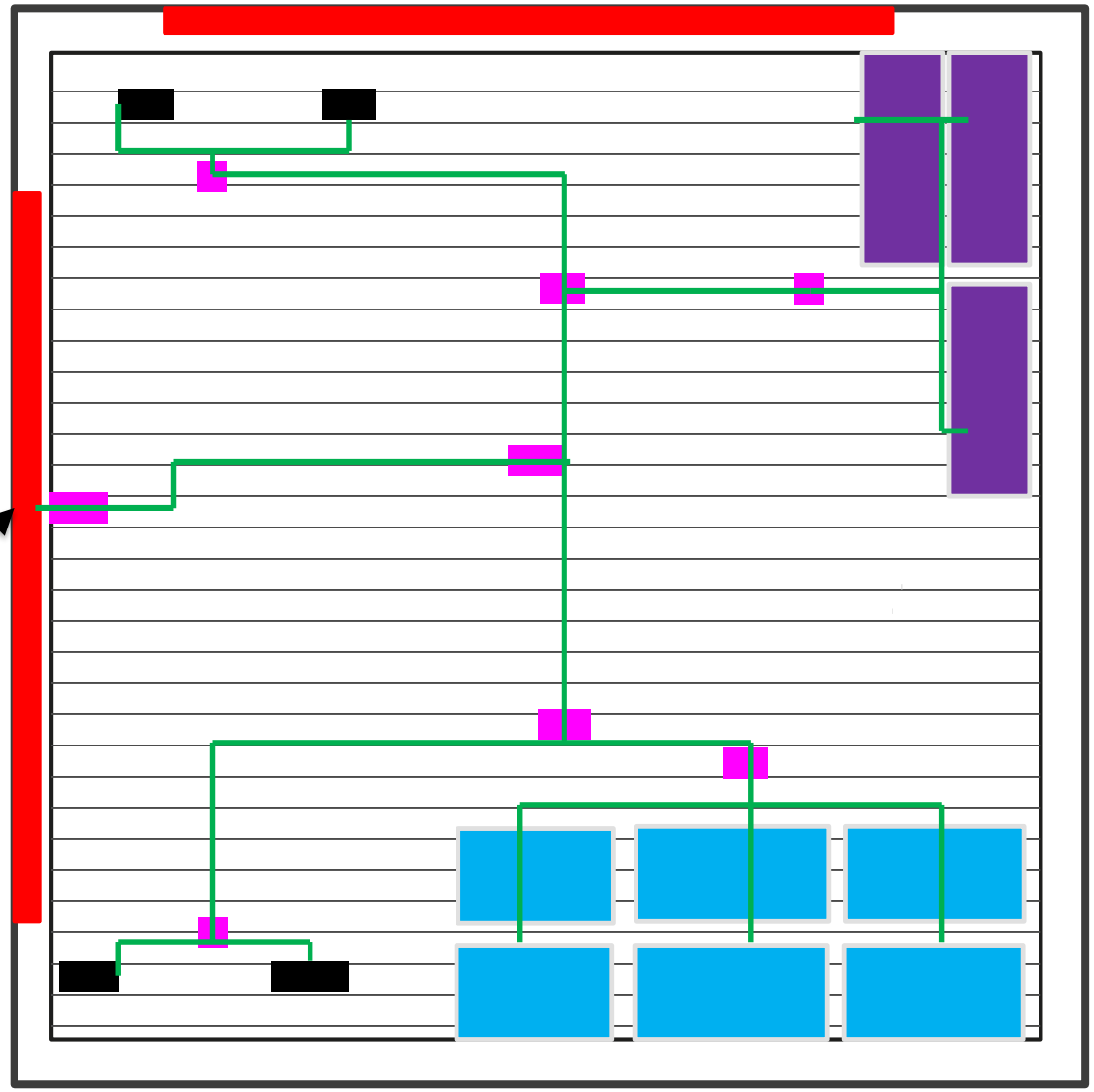

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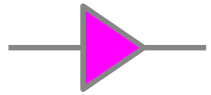
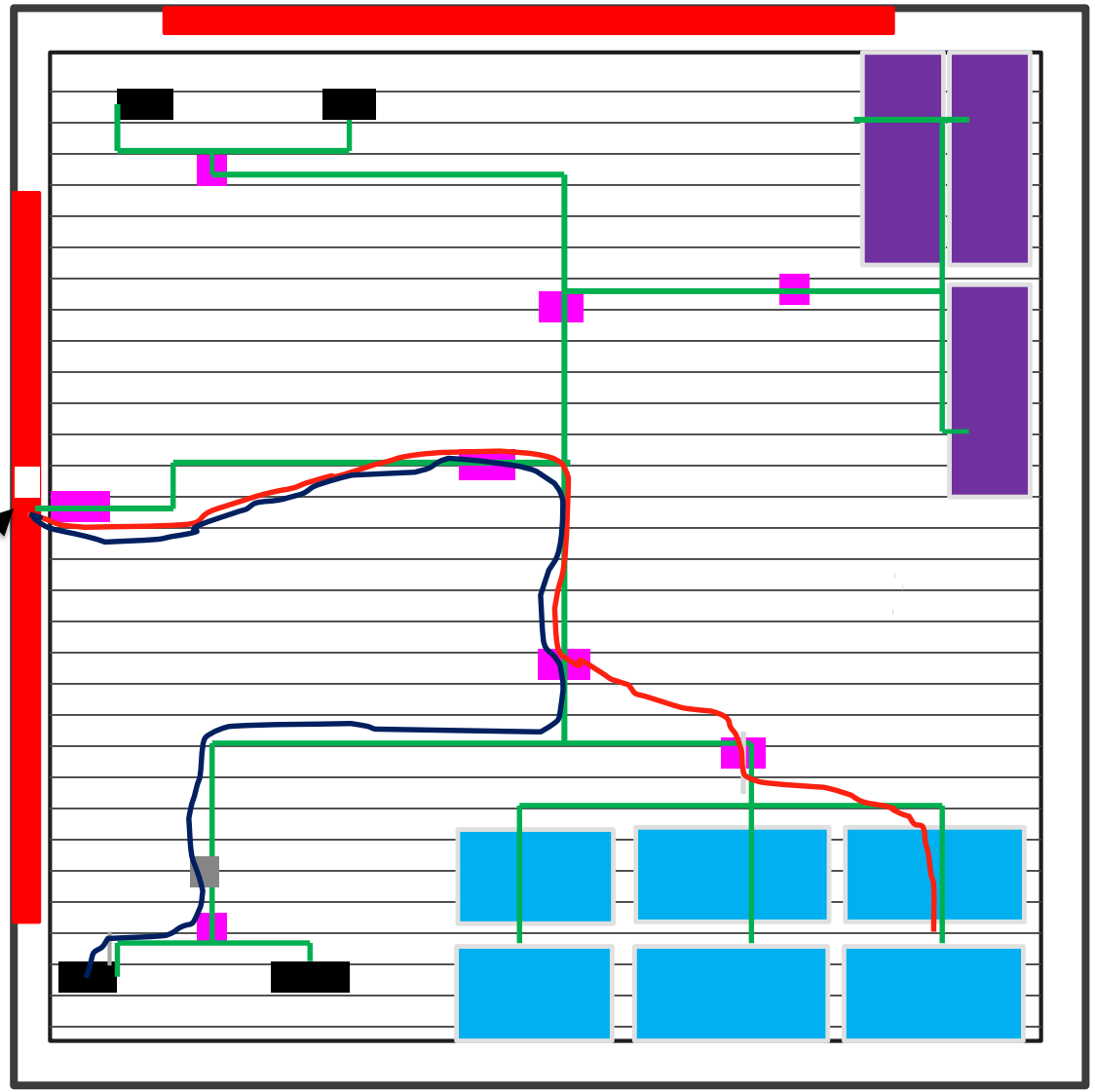
PHYSICAL DESIGN: CTS

Clock Buffers
(1x, 2x,4x ..)





Insertion Delay
Time taken by clock tree to transfer the clock signal to the sink

Skew

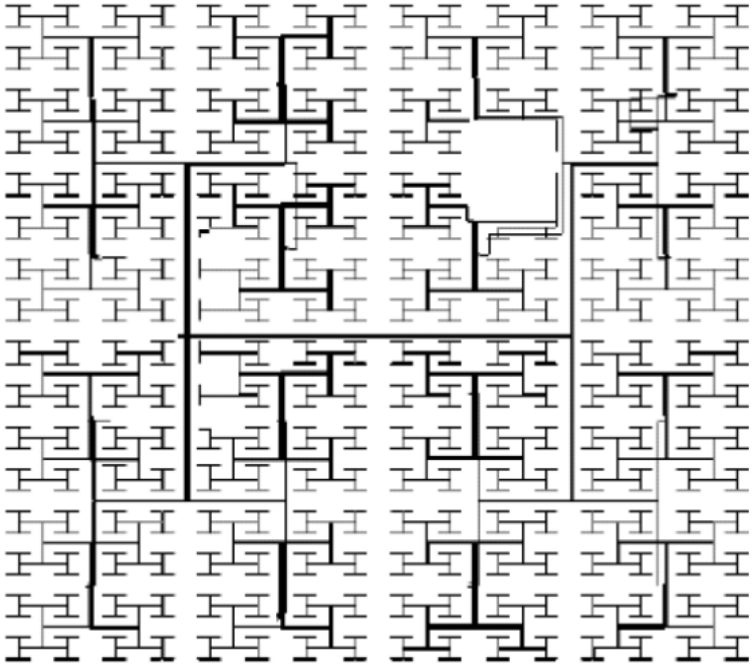
Difference between the insertion delays

Clock tree balancing
Achieve Identical insertion delay for all sinks
i.e. zero skew

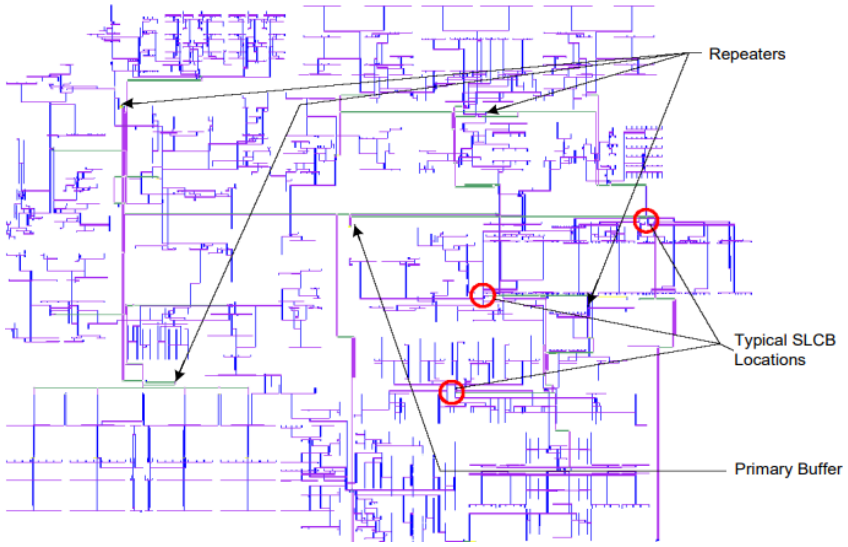
PHYSICAL DESIGN: CTS

- Note that the dynamic power is $\alpha\ CV^2 f$. For clock, $\alpha = 1$.
  - Insertion of clock tree → additional dynamic power!

- In order to reduce skew → we are burning area and power and insertion delay!
- Modern tools do better → Clock concurrent optimization (CCopt) → advanced topic



IBM power PC 2002: H tree



Intel Itanium 2005: H tree