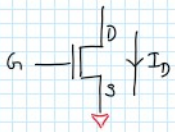
* An NMOS device has a threshold voltage $+V_{TN}$ and V_{GS} must be $> V_T$ to turn ON the MOS.
  ∴ V_{GS} must be +ve & hence "source terminal" of NMOS is always tied to the lowest potential (i.e GND/VSS in this case)

* A PMOS device has a threshold voltage $-V_{TP}$ and $V_{GS} < -V_{TP}$ to turn ON the MOS.
  ∴ V_{GS} must be -ve. However, there are only $+V_{DD}$ & V_{SS} available on chip (No negative voltage). ∴ To counter this we tie the "source terminal" of PMOS is always tied to the highest potential (i.e V_{DD} in this case) to ensure V_{GS} is negative (i.e $V_G - V_{DD}$)

*

NMOS



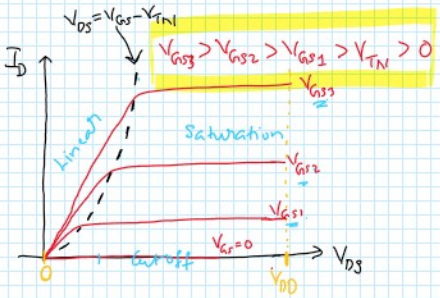
Threshold Voltage : V_{TN}

MOS OFF : $V_{GS} < V_{TN}$

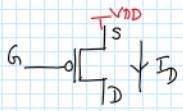
MOS ON : $V_{GS} \geq V_{TN}$

(i) $V_{DS} < V_{GS} - V_{TN}$: linear

(ii) $V_{DS} \geq V_{GS} - V_{TN}$: Saturation



PMOS



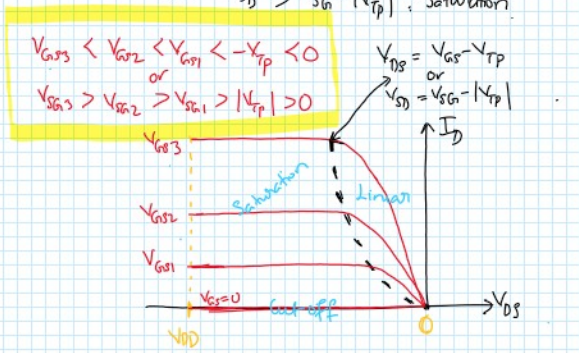
Threshold voltage : $-V_{TP}$

MOS OFF : $V_{GS} > -V_{TP}$ or $V_{SG} < |V_{TP}|$

MOS ON : $V_{GS} \leq -V_{TP}$ or $V_{SG} \geq |V_{TP}|$

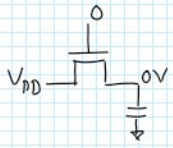
(i) $V_{SD} < V_{SG} - |V_{TP}|$: linear

(ii) $V_{SD} \geq V_{SG} - |V_{TP}|$: Saturation



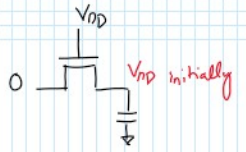
* Consider the cases for NMOS below

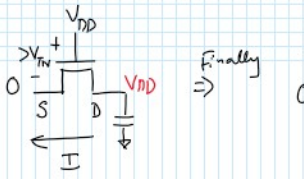
(a)



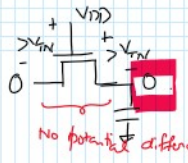
: Switch is OFF so no change in condition.

(b)

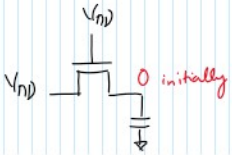


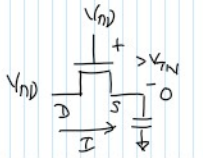


Finally ⇒

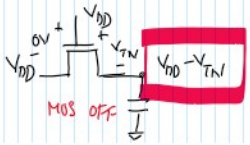


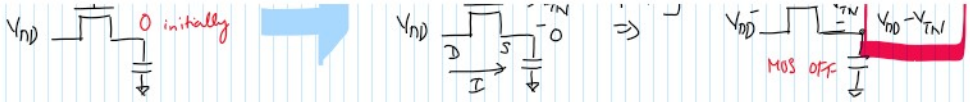
(c)





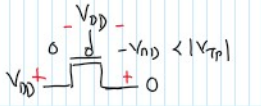
Finally ⇒

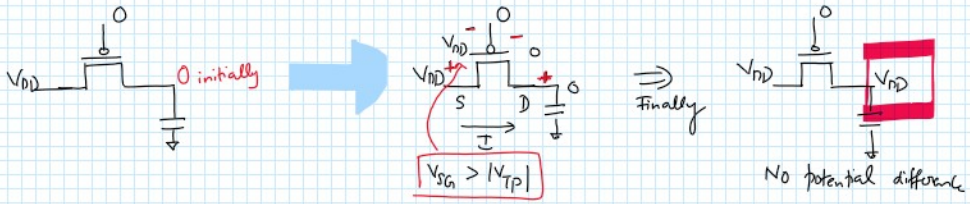


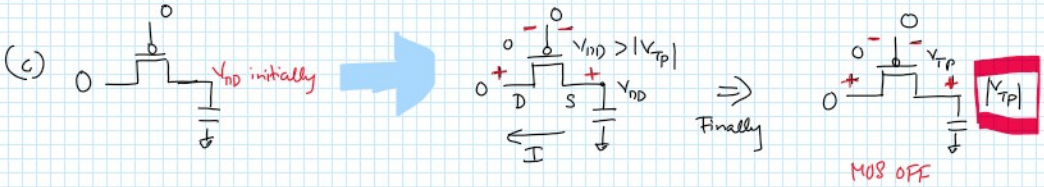


For NMOS, $V_o = \min(V_{IN}, V_{DD} - V_{TN})$

* Consider the cases for PMOS below

(a) 

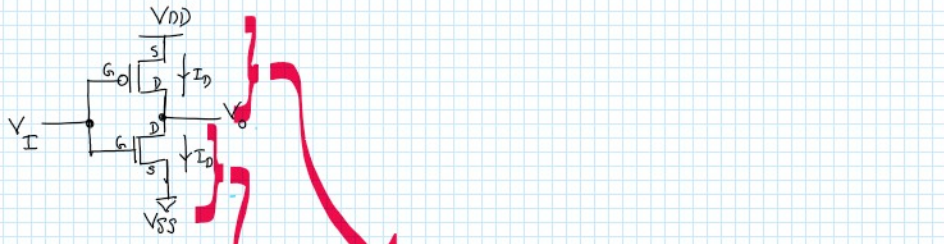
(b) 

(c) 

* Observations:

a) NMOS passes strong logic-0 & weak logic-1 (i.e o/p is not V_{DD})

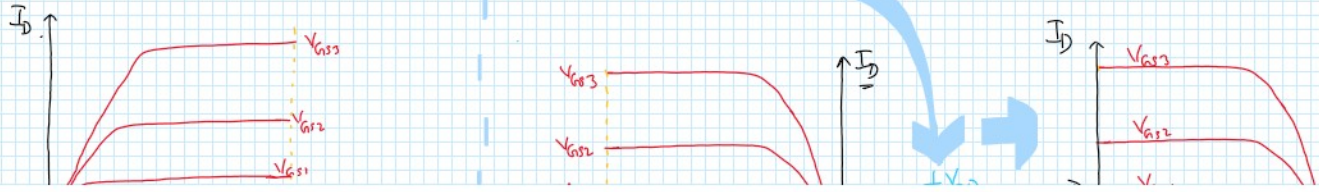
b) PMOS passes strong logic-1 & weak logic-0 (i.e o/p is not 0)

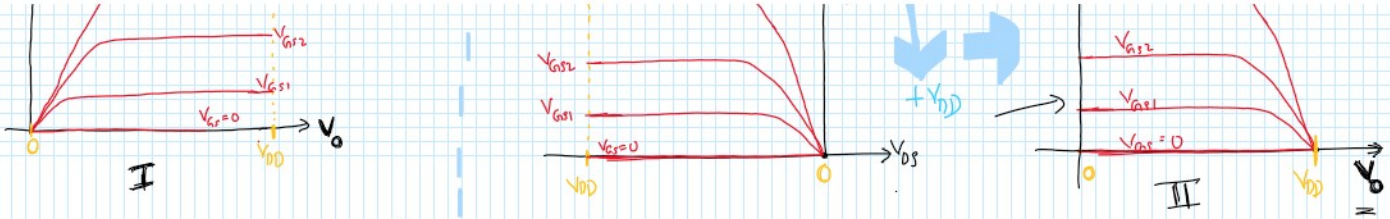


* To bring both V_{DS} to same co-ordinate system (w.r.t V_o):

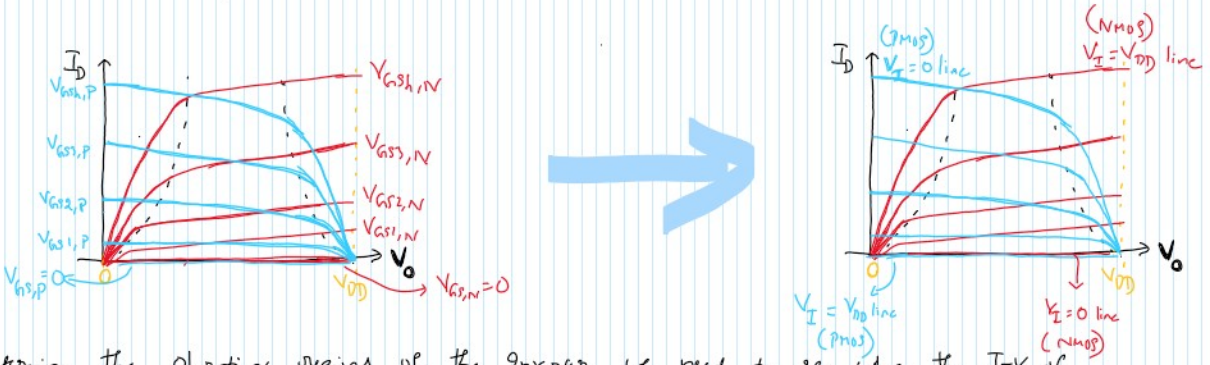
(i) $V_{DS,NMOS} = V_o$

(ii) $V_o = V_{DD} + V_{DS,PMOS}$



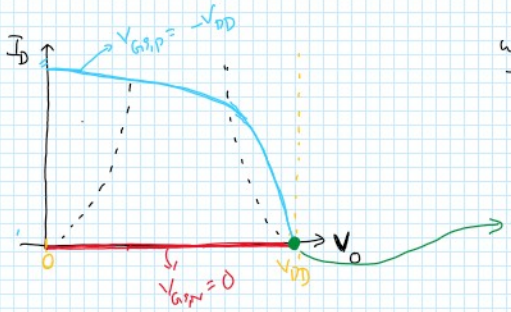


* To get the operating point (load line) of the inverter, we overlap plot I (for NMOS) & plot II (for PMOS)



* To determine the operating regions of the inverter, we need to see when the I-V of the PMOS & NMOS intersect (i.e finding solution for $f_1(x) = f_2(x)$)

Case I: $V_I = 0$



When $V_I = 0$:-

$V_{GS_N} = 0$ & $V_{SG,P} = V_{DD}$

(Cut-off) NMOS

(ON & maximum V_{SG}) PMOS

* The intersection of these two curves & hence the solution.

$\Rightarrow$ The solution is $V_o = V_{DD}$

* From this I-V curve, we also notice that NMOS is in cut off and PMOS is in linear region.

* We can also prove this from the conditions

NMOS

$V_{GS,N} = 0 < V_{TN}$

$\therefore$ NMOS in cut-off

PMOS

$V_{SG,P} = V_{DD} > |V_{TP}|$ $\therefore$ ON

$\hookrightarrow$ $V_{SD,P} \geq V_{SG,P} - |V_{TP}|$ for saturation

$V_S - V_D \geq V_S - V_G - |V_{TP}|$

$V_D \leq V_G + |V_{TP}|$

$V_{DD} \leq 0 + |V_{TP}|$ $\rightarrow$ Not true

$\therefore$ PMOS is in linear region.

Case II: $V_I = V_{DD}$

When $V_I = V_{DD}$:-

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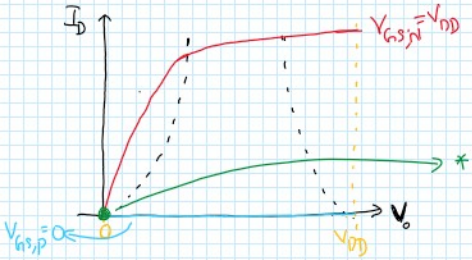
When $V_I = V_{DD}$:-



$V_{GS,N} = V_{DD}$ (ON & maximum V_{GS}) — NMOS

$V_{SG,P} = V_{DD} - V_{DD} = 0$ (OFF) — PMOS

* The intersection of these two curves & hence the solution.

=) The solution is $V_o = 0$ V

* From this I-V curve, we also notice that PMOS is in cut off and NMOS is in linear region.
* We can also prove this from the conditions

NMOS

$V_{GS,N} = V_{DD} > V_{TN}$ (ON)

↳ $V_{DS,N} \geq V_{GS,N} - V_{TN}$ for saturation

$0 \geq V_{DD} - V_{TN}$ → Not true

∴ NMOS is in linear region.

PMOS

$V_{SG,P} = 0 < |V_{TP}|$

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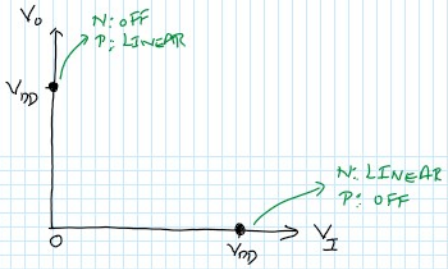
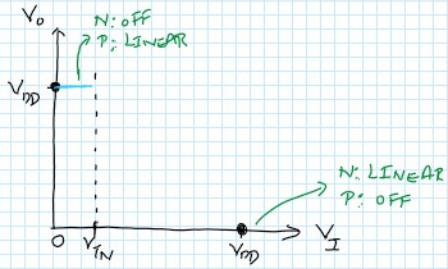
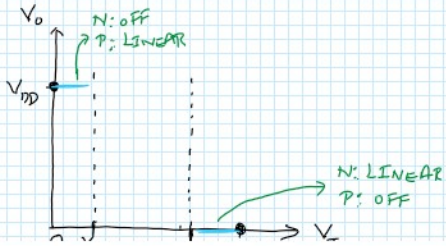
* Based on case-I & case-II ; we can draw the inverter transfer curve (V_I Vs V_o)

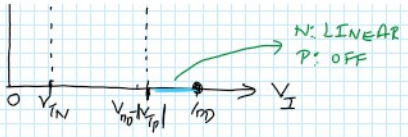


* As we increase V_I till V_{TN}, the NMOS will stay in cut-off & PMOS in linear (similar to case - I)

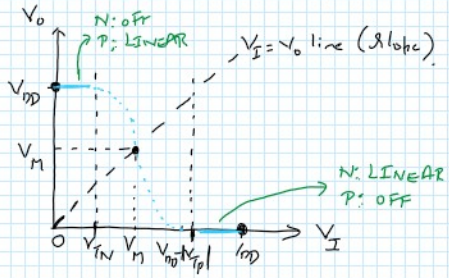


* Symmetrically, as V_I is reduced from V_{DD} to $V_{DD} - |V_{TP}|$, the PMOS will stay in cut-off & NMOS will be in linear region (similar to case II)



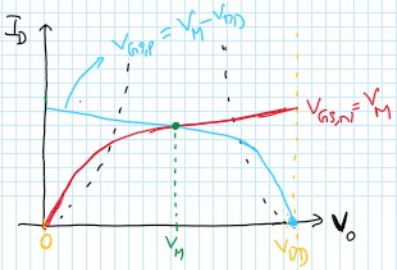


* The transfer curve will go from $V_o = V_{DD}$ to 0 as V_I goes from 0 to V_{DD}. In the process, it will intersect a line $V_I = V_o$ (i.e straight line with slope = 1)



* At the intersection point, $V_I = V_o = V_M$. Lets consider this as case III

Case III :- $V_I = V_o = V_M$



When $V_I = V_o = V_M$:-

* Both PMOS & NMOS are ON & the two MOSFETs are in saturation (as shown in the left figure)
* The intersection point and the solution is $V_o = V_M$

NMOS

$V_{DS} \geq V_{GS} - V_{TN}$ for saturation.

$V_M - 0 \geq V_M - 0 - V_{TN}$

$V_M \geq V_M - V_{TN}$ (True)

∴ NMOS is in saturation.

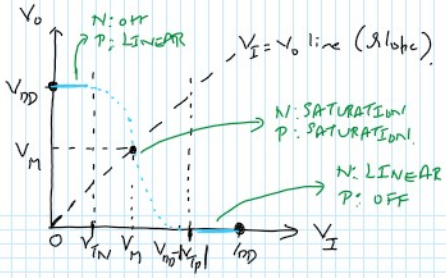
PMOS

$V_{SD} \geq V_{SG} - |V_{Tp}|$ for saturation

$V_{DD} - V_M \geq V_{DD} - V_M - |V_{Tp}|$

$V_M \leq V_M + |V_{Tp}|$ (True)

∴ PMOS is in saturation.



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