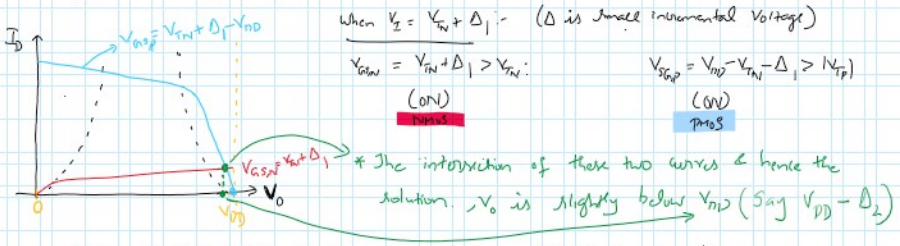
Case IV: $V_I > V_{TN}$ & $V_I < V_M$

When $V_I = V_{TN} + \Delta_1$:- (Δ is small incremental voltage)

$V_{GS,N} = V_{TN} + \Delta_1 > V_{TN}$: (ON) NMOS

$V_{SG,P} = V_{DD} - V_{TN} - \Delta_1 > |V_{TP}|$ (ON) PMOS



* The intersection of these two curves & hence the solution, V_o is slightly below V_{DD} (Say $V_{DD} - \Delta_2$)

* From the I-V curve, NMOS is in Saturation & PMOS is in linear region.

NMOS

$V_{DS} \geq V_{GS} - V_{TN}$ for saturation.

$V_o \geq V_I - V_{TN}$

$V_{DD} - \Delta_2 \geq V_{TN} + \Delta_1 - V_{TN}$

$V_{DD} \geq \Delta_1 + \Delta_2$ (true)

$\therefore$ NMOS is in saturation

PMOS

$V_{SD} \geq V_{SG} - |V_{TP}|$ for saturation

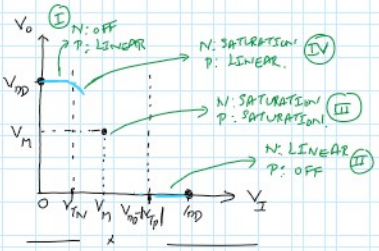
$V_{DD} - V_o \geq V_{DD} - V_I - |V_{TP}|$

$V_o \leq V_I + |V_{TP}|$

$V_{DD} - \Delta_2 \leq V_{TN} + \Delta_1 + |V_{TP}|$

$V_{DD} \leq \Delta_1 + \Delta_2 + |V_{TP}| + V_{TN}$ (False)

$\therefore$ PMOS is in linear region.



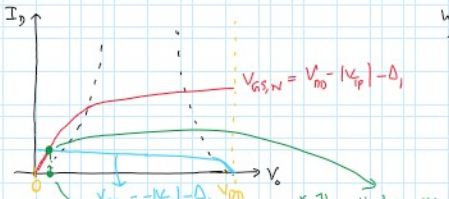
Case V: $V_I < V_{DD} - |V_{TP}| - \Delta_1$ & $V_I > V_M$

When $V_I = V_{DD} - |V_{TP}| - \Delta_1$: (Small incremental Voltage)

$V_{GS,N} = V_{DD} - |V_{TP}| - \Delta_1 > V_{TN}$ (ON) NMOS

$V_{SG,P} = V_{DD} - (V_{DD} - |V_{TP}| - \Delta_1)$

$= |V_{TP}| + \Delta_1 > |V_{TP}|$ (ON) PMOS.



* The intersection of these two curves & hence the solution, V_o is slightly above 0. (Say Δ_2)

* From the I-V curve, NMOS is in linear & PMOS is in saturation region.

NMOS

$V_{DS} \geq V_{GS} - V_{TN}$ for saturation.

$V_o \geq V_I - V_{TN}$

$\Delta_2 \geq V_{DD} - |V_{TP}| - \Delta_1 - V_{TN}$

$\Delta_2 \geq V_{DD} - (V_{TN} + |V_{TP}|) - \Delta_1$ (FALSE)

$\therefore$ NMOS is in Linear Region

PMOS

$V_{SD} \geq V_{SG} - |V_{TP}|$ for saturation

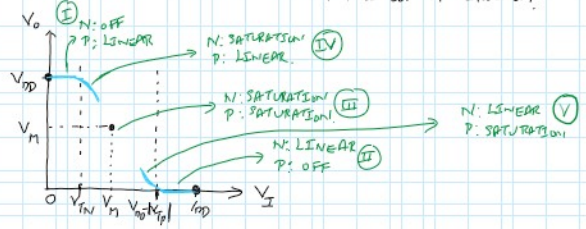
$V_{DD} - V_o \geq V_{DD} - V_I - |V_{TP}|$

$V_o \leq V_I + |V_{TP}|$

$\Delta_2 \leq V_{DD} - |V_{TP}| - \Delta_1 + |V_{TP}|$

$\Delta_2 \leq V_{DD} - \Delta_1$ (true)

$\therefore$ PMOS is in Saturation



* Final transfer curve of an Inverter is:-

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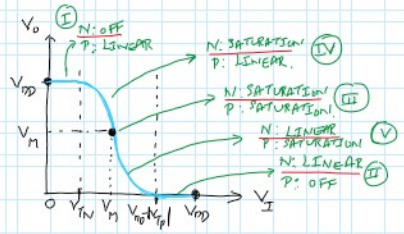
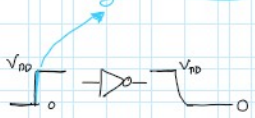


* As V_I changes from 0 to V_{DD} } NMOS transitions from OFF → SATURATION → LINEAR
PMOS transitions from LINEAR → SATURATION → OFF



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* Let's try to evaluate V_M (i.e the voltage @ which $V_I = V_O$)

* Recall that in case III ($V_I = V_O = V_M$), both NMOS & PMOS are in saturation

$$\therefore I_{D,NMOS,SAT} = I_{D,PMOS,SAT} \quad \text{(ignoring channel length modulation)}$$

$$\frac{1}{2}\underbrace{\mu_n C_{ox}\left(\frac{W}{L}\right)_N}_{K_N}(V_{GS}-V_{TN})^2 = \frac{1}{2}\underbrace{\mu_p C_{ox}\left(\frac{W}{L}\right)_p}_{K_p}(V_{SG}-|V_{Tp}|)^2$$

$$\therefore K_N\left[V_M - V_{TN}\right]^2 = K_p\left[V_{DD} - V_M - |V_{Tp}|\right]^2$$

$$V_M - V_{TN} = \sqrt{\frac{K_p}{K_N}}\left[V_{DD} - V_M - |V_{Tp}|\right]$$

Define $\beta = \sqrt{\frac{K_p}{K_N}}$

$$V_M - V_{TN} = \beta\left[V_{DD} - V_M - |V_{Tp}|\right]$$

$$V_M\left[1+\beta\right] = \beta\left[V_{DD} - |V_{Tp}|\right] + V_{TN}$$

$$\therefore V_M = \frac{V_{TN} + \beta\left[V_{DD} - |V_{Tp}|\right]}{1+\beta}$$

* V_M (also called "Switching Voltage" or "Trip-point voltage" of an Inverter) is a function of $V_{TN}, |V_{Tp}|, \mu_n, \mu_p, \left(\frac{W}{L}\right)_N$ & $\left(\frac{W}{L}\right)_p$.

* The only design parameters (available for designers) is $\left(\frac{W}{L}\right)_N$ & $\left(\frac{W}{L}\right)_p$.

* Consider the special case where $V_{TN} = |V_{Tp}|$ and $\beta = 1$

$$V_M = \frac{V_{TN} + V_{DD} - V_{TN}}{2} = V_{DD}/2$$

i.e for a exactly symmetric inverter (switching voltage $V_m = V_{DD}/2$) $\beta = 1$ AND $V_{TN} = |V_{Tp}|$.

$\beta = 1 \Rightarrow K_n = K_p \Rightarrow \mu_n (W/L)_n = \mu_p (W/L)_p$.

$$\therefore \frac{(W/L)_p}{(W/L)_N} = \frac{\mu_n}{\mu_p}$$

* For same PMOS & NMOS channel length [usually L_{min}],

$$\frac{W_p}{W_N} = \frac{\mu_n}{\mu_p}$$

i.e the ratio of PMOS to NMOS width = ratio of electron to hole mobilities.

* Typically $\mu_n = f \cdot \mu_p$ & $f = 2$ or 2.5 or 3.

* Note that if $V_{TN} \neq |V_{Tp}|$ (which is usually the case), $W_p/W_N \neq \frac{\mu_n}{\mu_p}$ for $V_M = V_{DD}/2$

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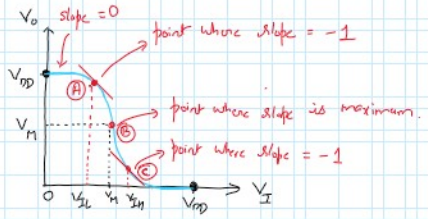
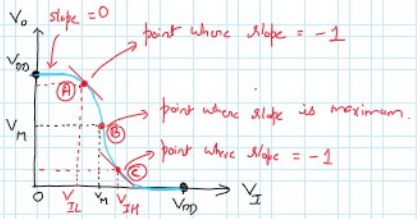
* Let's go back to the transfer curve of the inverter.



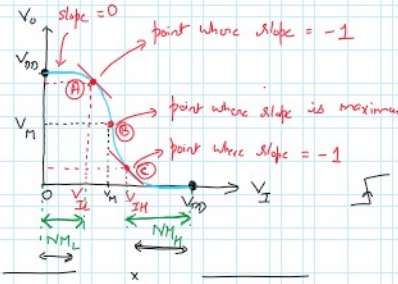
* The inverter's function is to operate as a digital switching logic without amplifying noise. Amplifying noise can change the logic level at the output.

* For faithful operation, we need to define Noise margins of the inverter (max & min inputs)
* Before Point (A) on the transfer curve, the magnitude of the slope is either 0 or < 1
  ⇒ No amplification happens (∵ slope corresponds to gain)
* After Point (C) on the transfer curve, the magnitude of the slope is either 0 or < 1
  ⇒ No amplification happens (∵ slope corresponds to gain)

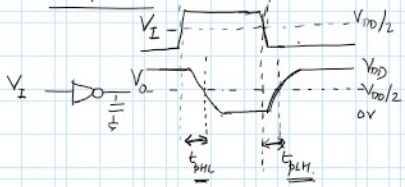


* V_I below V_{IL} are not amplified, V_I above V_{IH} are not amplified.
* In region (B) the inverter is acting as an amplifier with maximum gain.
  [both PMOS & NMOS in the saturation Region] → for analog designers.
* We define Noise margin High (NM_H) & Noise Margin Low (NM_L)

$$NM_H = V_{DD} - V_{IH} \quad \& \quad NM_L = V_{IL}.$$

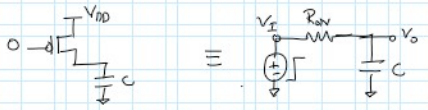


Transient characteristics of the inverter :-



* Let's define propagation delay as the time taken for the output to reach 50% of the maximum input
  ↳ $t_{p,HL}$ → propagation delay when o/p goes from high to low
  $t_{p,LH}$ → propagation delay when o/p goes from low to high

* When $V_I = 0$, PMOS is ON & the equivalent circuit is



$$V_o = V_I\left(1 - e^{-t/RC}\right)$$

For $t = t_{p,LH}$, $\quad 0.5V_I = V_I\left(1 - e^{-t_{PLH}/RC}\right)$

$$\Rightarrow \quad t_{p,LH} = 0.69 R_{ON,P} C.$$

* Recall that the PMOS goes OFF → SATURATION → LINEAR region. Assuming the time spent in saturation region is very small (for first-hand pen-paper calculations),

$$R_{ON,P} = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_P\left(V_{DD} - |V_{TP}|\right)}$$

* Similarly for NMOS; $\quad t_{p,HL} = 0.69 R_{ON,N} C$

$$R_{ON,N} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_N\left(V_{DD} - V_{TN}\right)}$$

* For Symmetric Inverter, $t_{p,LH} = t_{p,HL}$.

$$\therefore \quad 0.69 R_{ON,P} C = 0.69 R_{ON,N} C$$

$$\Rightarrow \quad \underbrace{\mu_p C_{ox}\left(\frac{W}{L}\right)_P}_{K_P}\left[V_{DD} - |V_{TP}|\right] = \underbrace{\mu_n C_{ox}\left(\frac{W}{L}\right)_N}_{K_N}\left[V_{DD} - V_{TN}\right]$$

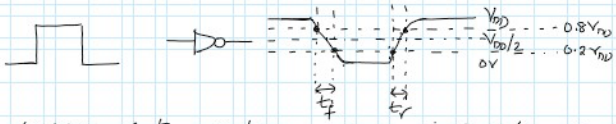
$$\left(\frac{K_P}{K_N}\right)\left[V_{DD} - |V_{TP}|\right] = V_{DD} - V_{TN}.$$

$$\gamma^2\left[V_{DD} - |V_{TP}|\right] = V_{DD} - V_{TN}. \quad \text{—(i)}$$

* Condition (i) above is true provided $V_{TN} = |V_{TP}|$ & $\gamma = 1$

This is the same condition we got for $V_M = V_{DD}/2$!!!

* We define rise-time (t_r) & fall-time (t_f) as 20% to 80% V_{DD} time & vice versa.



* Under the same concept, if $t_{p,LH}$ & $t_{p,HL}$ are symmetric t_f & t_r will also be symmetric!!

∴ Provided $V_{TN} = |V_{TP}|$, if by design $\gamma = 1$ (i.e. $\frac{W_p}{W_N} = \frac{\mu_n}{\mu_p}$), we get

(i) $V_M = V_{DD}/2$
(ii) $t_{p,HL} = t_{p,LH}$
(iii) $t_r = t_f$

} Symmetric Inverter

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* For an Inverter, we can define the following

(a) Static characteristics:
  (i) V_M (Switching voltage)
  (ii) V_{IH}, V_{OH} & $N_{M,H}$, $N_{M,L}$ (Noise Margins)

(b) Dynamic characteristics.
  (i) $t_{p,LH}$ & $t_{p,HL}$ (Low to High & High-to-low propagation time)
  (ii) $t_p = \frac{t_{p,LH} + t_{p,HL}}{2}$ (total propagation time)

(ii) $t_p = \frac{t_{p,LH} + t_{p,HL}}{2}$ (total propagation time)

(iii) t_r & t_f (Rise & fall time)

* To design a symmetric inverter, i.e $\begin{bmatrix} V_M = V_{DD}/2 \\ t_{p,LH} = t_{p,HL} \\ t_r = t_f \end{bmatrix}$,

if $V_{TN} = |V_{TP}|$, for a given minimum length (L_{min}), $\frac{W_p}{W_N} = \frac{\mu_N}{\mu_p}$.

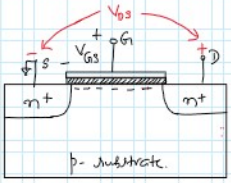
→ This will be the starting point for your simulations.

→ In a practical Process Design Kit (PDK), $V_{TN} \neq |V_{TP}|$

⇒ To achieve symmetric conditions W_p, W_N must be tuned.

Capacitance of MOSFET:

a) Due to channel :-



* When the MOSFET is ON (linear or saturation), there exists a capacitance between gate & source (C_{GS})

i.e top-plate of cap → Gate Metal

dielectric → Gate oxide

& bottom-plate of cap → Channel connected to source

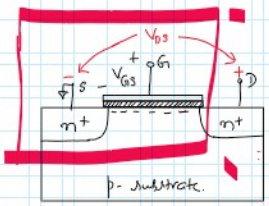
* When the MOSFET is in linear region, there also exists a capacitance b/t Gate & Drain (C_{GD})

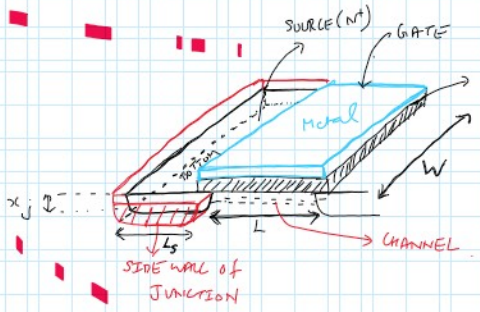
(Remember, in saturation, the channel does not extend to the drain because of depletion, hence no capacitance b/t gate & drain)

∴ Effectively :-

when MOS is in linear region.

b) Due to junctions (P-N) :-





* There is a P-N junction on the bottom side of the source (and corresponding top surface of substrate)

* There is a P-N junction on the bottom side of the source (and corresponding top surface of substrate)
  If C_j is the junction cap / unit-area, $C_{bottom} = C_j \times W \times L_s$.

* There are P-N junctions on three sides of the source (except for the fourth side towards the Gate)
  The depth x_j is fixed for a given process. If C_{sw} is the side-wall cap / unit area,
  If C_{jsw} is the side-wall capacitance,

$$C_{jsw} = C_{sw} \times \left[\underbrace{(x_j \times L_s)}_{\text{sidewall 1 area}} + \underbrace{(x_j \times L_s)}_{\text{sidewall 2 area}} + \underbrace{(x_j \times W)}_{\text{sidewall 3 area}} \right]$$

$$= \underbrace{C_{sw} x_j}_{C'_{jsw}} [2L_s + W]$$

C'_{jsw} → Depends on the technology.

$$\therefore C_{jsw} = C'_{jsw} [2L_s + W]$$

- ∴ Capacitance due to junctions, also called diffusion capacitance is

$$C_{diff} = C_{bottom} + C_{jsw}$$

$$= C_j \times AREA + C_{sw} \times PERIMETER$$

$$C_{diff} = C_j L_s W + C_{sw} [2L_s + W]$$

* Look out for "as, ad, ps, pd" spice parameters in your assignment-1.

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