Lecture - 8

Review →
- Till now looked at NMOS, PMOS characteristics (plots and equations)
- Built a CMOS inverter, analyzed and characterized (static & dynamic) using simulations, equations and intuition.
- With INVx1, other logic gates like NANDX1, NORX1, NANDX2, etc. can be designed.
- Given any new "device" (other than an NMOS or PMOS), the same set of steps can be used to design, analyze and characterize logic gates in a given technology

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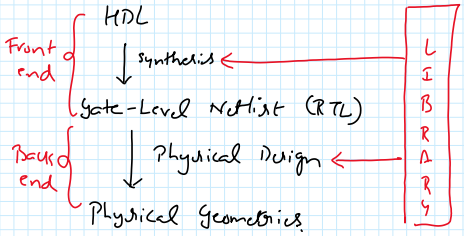
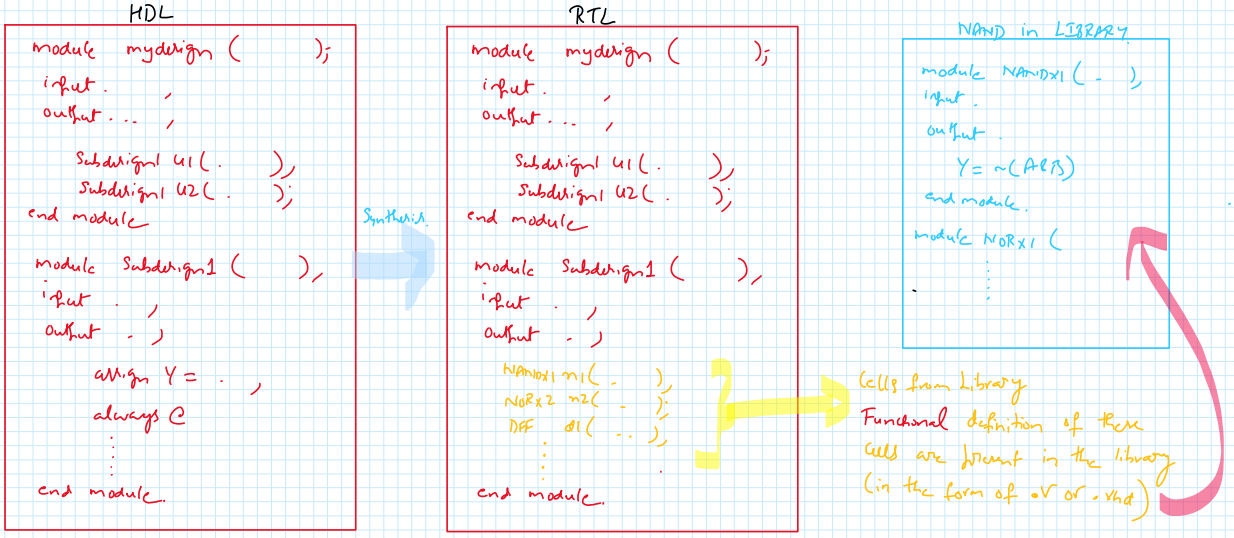


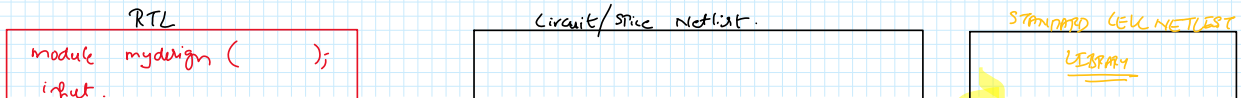
Eg

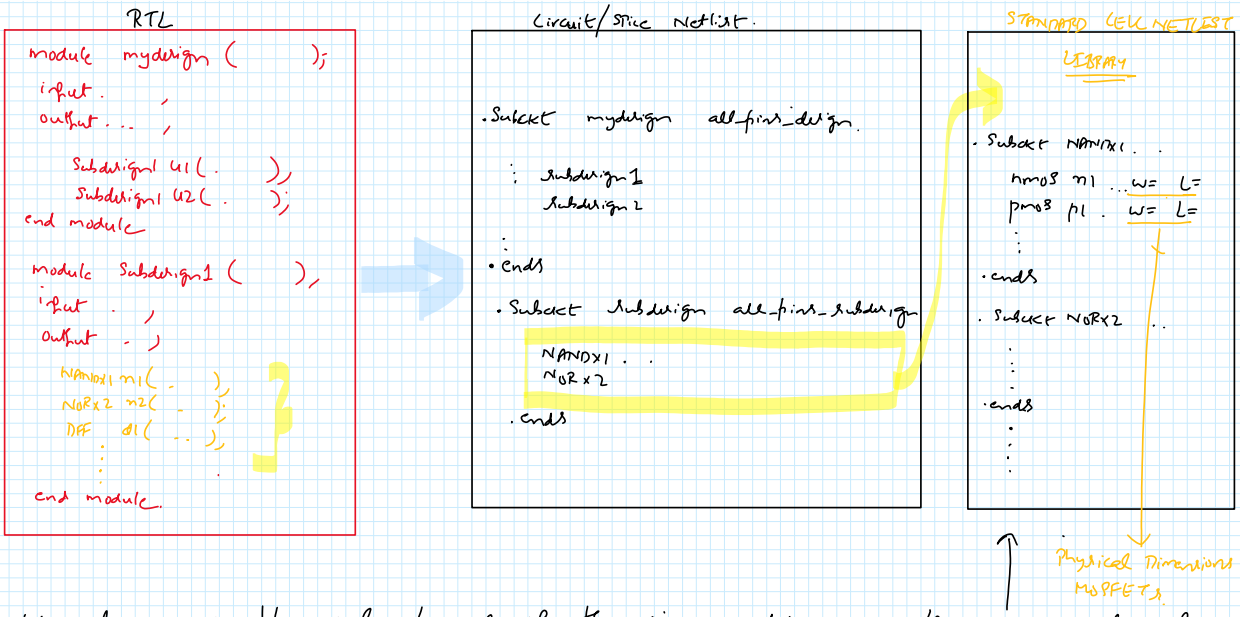


∴ Library [also called standard cell library] will contain functional definition (.v or .vhd) of all the logic gates (also called standard cells)
- The .v/.vhd views of the standard cells provide functional definition for simulation at the higher abstraction level (compared to MOSFET level simulation)
  - This enables faster debugging (we don't have to fix bugs at the MOSFET level ~10 billion MOSFETS)
  - This enables faster simulation (MOSFET level spice simulation for billion gates is VERY VERY VERY VERY VERY.... VERY SLOW)

* However, remember that for final fabrication, we need the physical MOSFET and interconnect geometries. This detail is incorporated in the spice netlist and layout.
* The transformation from RTL to physical geometry is performed by the "Physical Design" tool. The tool needs access to individual spice netlist & layout of the logic gates (standard cells).

Eg.





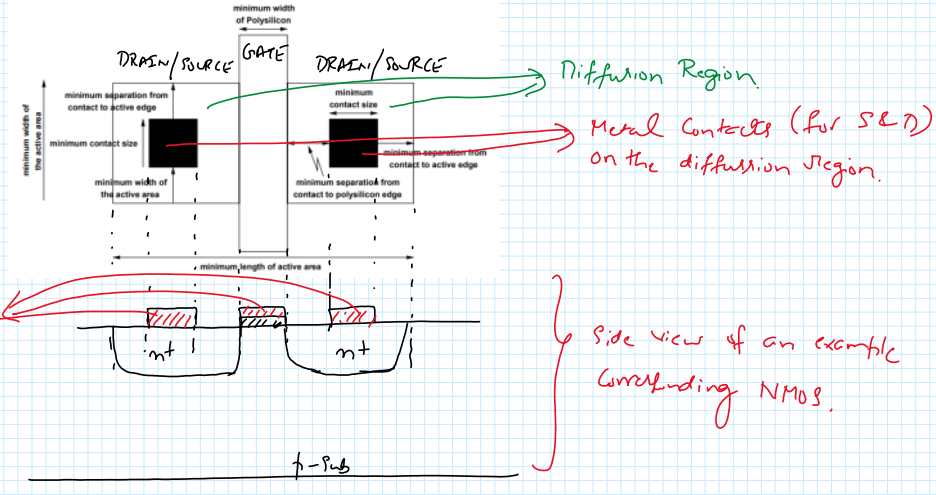
* We also need physical layout of the circuit defined in the netlist for fabrication. This layout is saved in .gdsII format

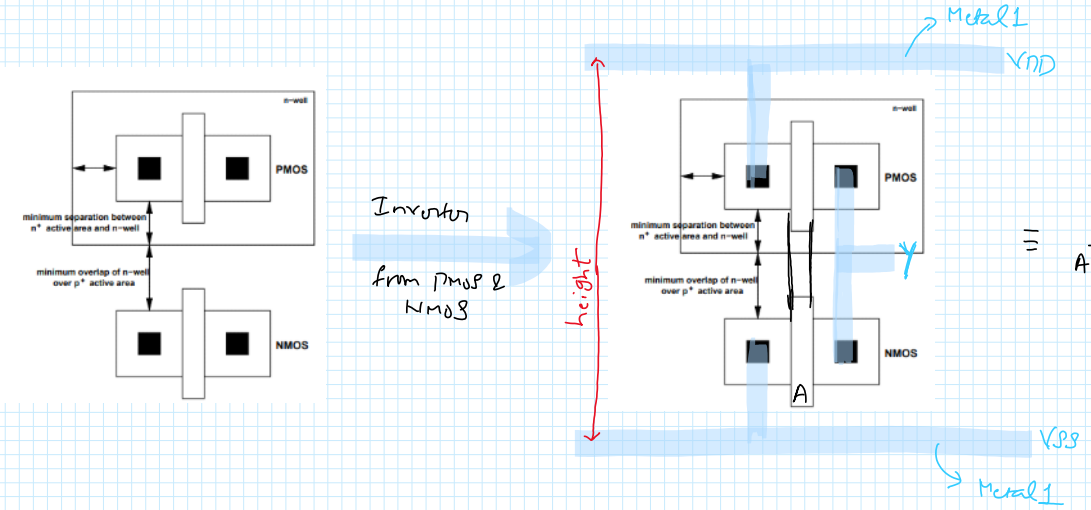
∴ In a "standard cell library", we need to have atleast the following "views" of the standard cells (logic cells)

.V or .Vhd .Cir/.Spc/.Sp/.Cdl .gdsII

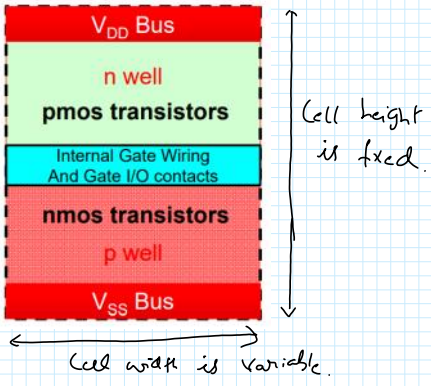
* .V/.Vhd can be easily written and verified
* Assignment - I covers the creation of Spice netlist for logic cells.
* We will now discuss the creation of the layout
* Layout is done using the top-view of the chip since the design parameters W & L are better observed from the top-view than the side view

Top-view of a MOSFET

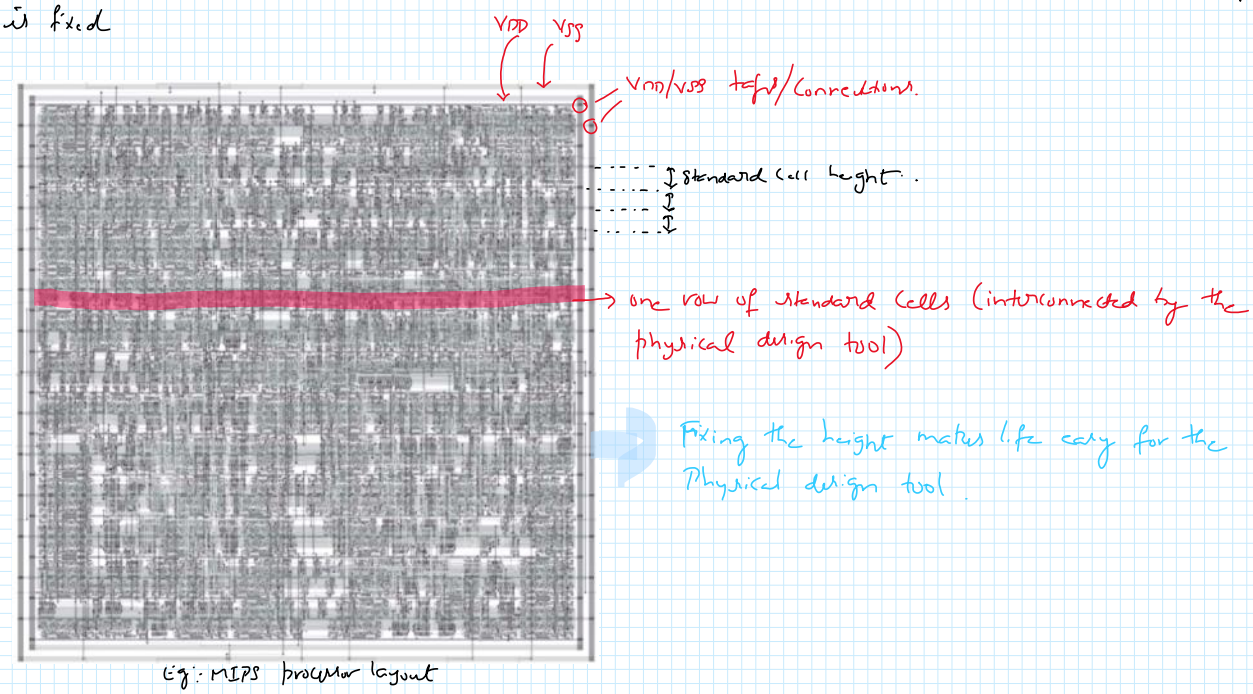




* The height of a standard cell is fixed for a given technology (optimized) The height must be fixed to allow the physical design tool to make connections between cells and converge in a faster way



i.e the cell height of all cells/gates (eg:- NAND2X2, NOR2X2, INVX2, DFF, 3-i/p gates, 4-i/p gates) etc is fixed



Eg: MIPS processor layout

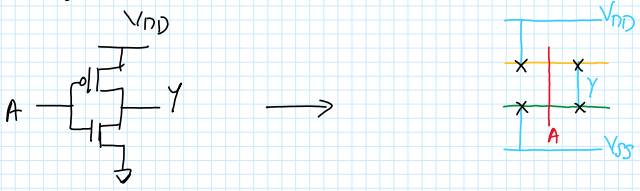
* Before drawing standard cell on a software it is usually visualized on pen & paper

* Before drawing standard cell on a software, it is usually visualized on pen & paper using "STICK DIAGRAM".

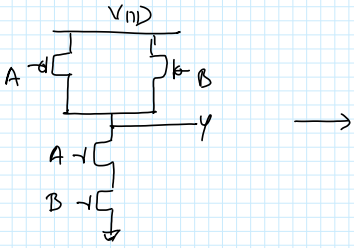
Consider the following colour coding:

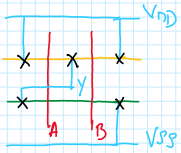
- Metal 1
- P diffusion
- N diffusion
- Polysilicon
- X Contact

(a) Inverter

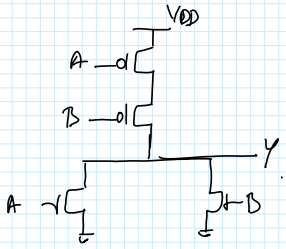


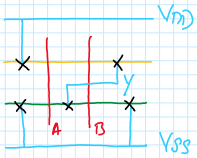
(b) 2-i/p NAND





(c) 2 i/p NOR





d) h-i/p NAND & h-i/p NOR :- try it by yourself