EE 618 (ZELE)
CMOS Analog VLSI Design
Quiz-2

Date : 16th October 2023 **Duration**: 1 Hour **Max. Marks** : 25

ACADEMIC HONESTY POLICY—IIT BOMBAY (https://www.iitb.ac.in/newacadhome/rules.jsp)
Copying in exams has serious consequences.

Do not communicate with other students during exams
Do not carry unauthorized material during exams
Do not make changes in valued answer books
Do not communicate with others during toilet breaks during exams

State your assumptions clearly, if any.

Ignore body effect ($\gamma = 0$) unless it is explicitly mentioned or shown in the circuits below.

Q1. For the circuits below, calculate the total output noise voltage (V_{nout}^2) and input referred noise voltage(V_{ineq}^2). Show the intermediate steps. [18 Marks]

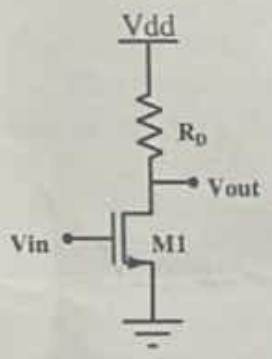

Fig. 1 (a) [3 marks]

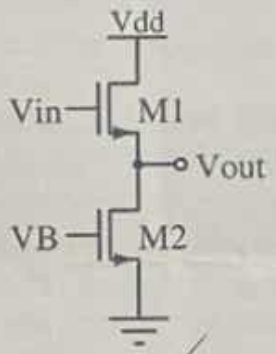

Fig. 1 (b) [3 marks]

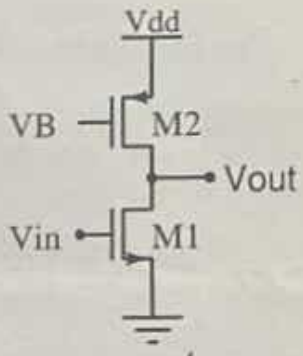

Fig. 1 (c) [3 marks]

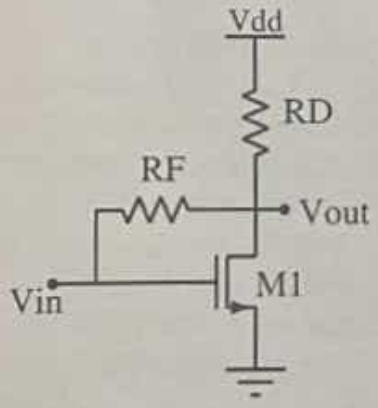

Fig. 1 (d) [3 marks]

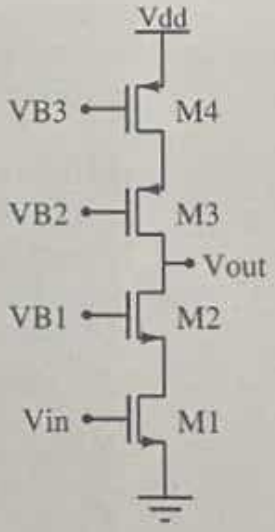

Fig. 1 (e) [3 marks]

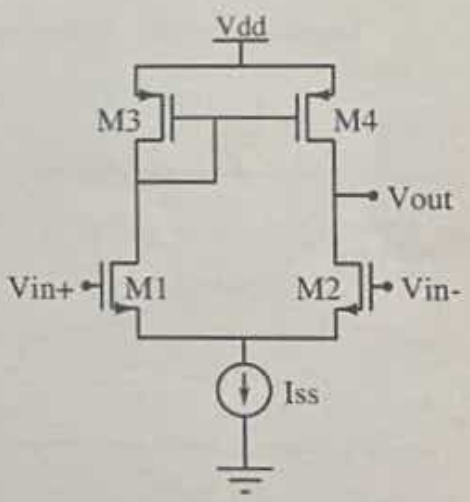

Fig. 1 (f) [3 marks]

$\frac{r_o}{g_m}$ $\frac{}{r_o + \frac{1}{g_m}}$ g_{m1} $r_{out} = r_o \| \frac{1}{g_m}$ $g_m | g_{ds}$

Q2. Calculate the positive and negative slew rates for the circuit given below. Annotate each transistor state for each slew rate calculation. [3 Marks]

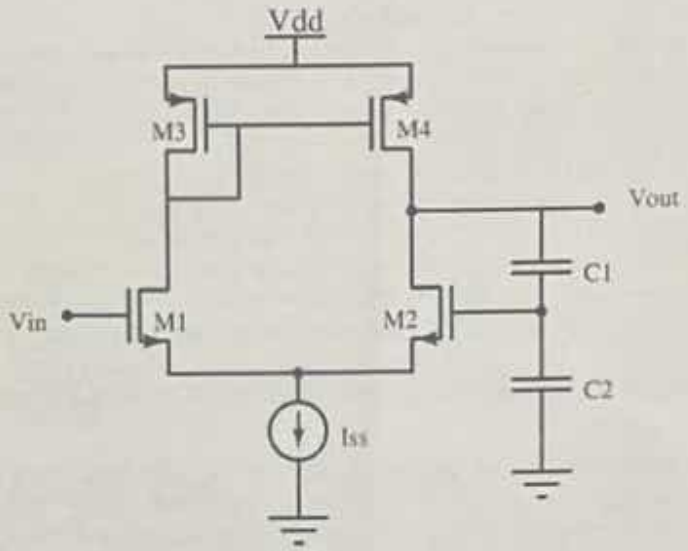

Fig. 2

Q3. Draw the detailed schematic diagram of CMOS bandgap reference circuit using PNP bipolar transistors. Clearly annotate each detail. Derive the expression for the output voltage of your circuit. You can assume $V_{DD} = 1.5V$. [4 Marks]

$C_1 \| C_2$

$\frac{C_1 C_2}{C_1 + C_2}$

$I_1 = I_2$.

$\downarrow$

$V_{BE1} = V_T \ln($