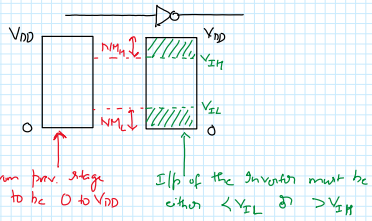
Lecture-6

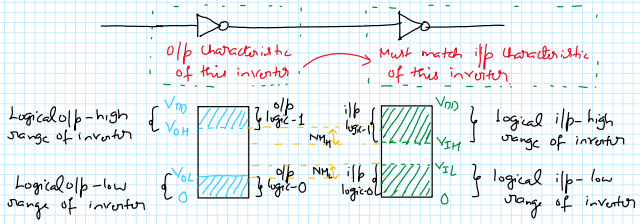
* Re-evaluate Noise Margin

* In the class, we discussed NM_H & NM_L as

$NM_H = V_{DD} - V_{IH}$ & $NM_L = V_{IL} - 0$ considering a single inverter.



* But practically, each inverter drives another inverter (or other logic)



* The next stage inverter will consider any voltage below V_{IL} @ its input as logic-low & will consider any voltage above V_{IH} @ its input as logic-high.

* The previous stage can o/p any voltage between V_{DD} & V_{OH} as output-high (depending on its i/p) & it can o/p any voltage between 0 & V_{OL} as output-low (depending on its i/p)

* When the previous stage outputs V_{OH} as o/p (it is still a valid logic-high voltage), the amount of margin we have for the noise is reduced (i.e an addition of noise can make the i/p to the next inverter below V_{IH} or $(V_{OH} - Noise) < V_{IH}$, leading to wrong o/p).

∴ The worst case Noise margins are:

$NM_H = V_{OH} - V_{IH}$

& $NM_L = V_{IL} - V_{OL}$

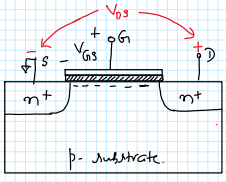
Best case:

$NM_H = V_{DD} - V_{IH}$

$NM_L = V_{IL} - 0$

Capacitance of MOSFET:

a) Due to channel:-



* When the MOSFET is ON (linear or saturation), there exists a capacitance between gate & source (C_{GS})

i.e top-plate of cap → Gate Metal

dielectric → Gate oxide

& bottom-plate of cap → Channel connected to source

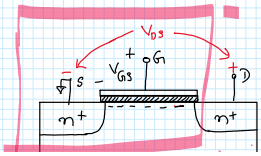
* When the MOSFET is in linear region, there also exists a capacitance b/t Gate & Drain (C_{GD})

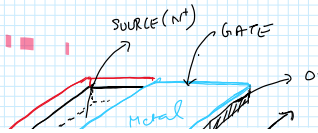
(Remember, in saturation, the channel does not extend to the drain because of depletion, hence no capacitance b/t gate & drain)

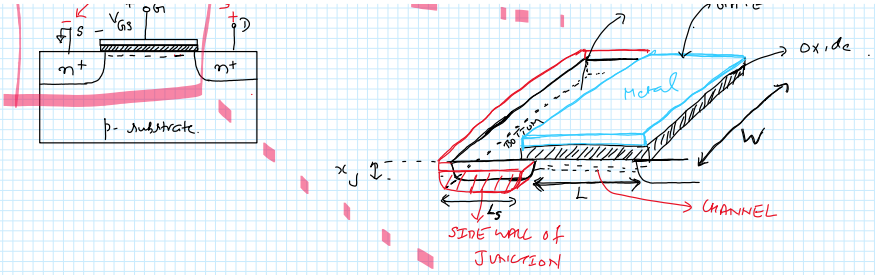
∴ Effectively -

when MOS is in linear region

b) Due to junctions (P-N):-







* There is a P-N junction on the bottom side of the source (and corresponding top surface of substrate)
  If C_j is the junction cap / unit-area, $C_{bottom} = C_j \times W \times L_s$

* There are P-N junctions on three sides of the source (except for the fourth side towards the Gate).
  The depth x_j is fixed for a given process. If C_{sw} is the side-wall cap / unit area,
  If C_{jsw} is the side-wall capacitance,

$$C_{jsw} = C_{sw} \times \left[\underbrace{(x_j \times L_s)}_{\text{Sidewall 1 area}} + \underbrace{(x_j \times L_s)}_{\text{Sidewall 2 area}} + \underbrace{(x_j \times W)}_{\text{Sidewall 3 area}} \right]$$

$$= \underbrace{C_{sw} x_j}_{C'_{jsw}} \left[2L_s + W \right]$$

C'_{jsw} → Depends on the technology

$$C_{jsw} = C'_{jsw} [2L_s + W]$$

- Capacitance due to junctions, also called diffusion capacitance is

$$C_{diff} = C_{bottom} + C_{jsw}$$
$$= C_j \times AREA + C_{jsw} \times PERIMETER$$
$$C_{diff} = C_j L_s W + C_{jsw} [2L_s + W]$$

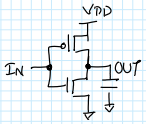
* Look out for "as, ad, ps, pd" spice parameters in your assignment-1

Power Consumption -

Three main factors contribute for power.

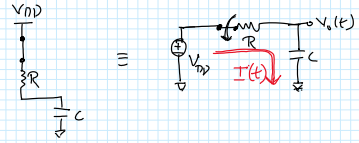
(a) Dynamic power consumption (P_{dyn}) :-

* Consider the inverter circuit -



a) When IN = Logic-0, PMOS → ON & NMOS OFF.
Acting like switches

Any 'ON' switch has a finite resistance & the equivalent model.



The energy supplied by the source is computed by integrating source power

i.e $E_{source} = \int_0^\infty V_{DD} \cdot I(t)\, dt$

For a switching RC circuit, $I(t) = \frac{V_{DD}}{R} \left[e^{-t/RC} \right]$ [Assuming zero charge on C initially i.e cap was discharged previously]

$\therefore E_{source} = V_{DD} \cdot \frac{V_{DD}}{R} \int_0^\infty \left(e^{-t/RC} \right) dt$

i.e cap was discharged previously]

$$\therefore E_{source} = V_{DD} \cdot \frac{V_{DD}}{R} \int_0^\infty \left(e^{-t/RC}\right) dt$$

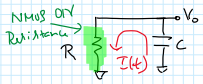
$$= \frac{V_{DD}^2}{R} \; e^{-t/RC} \Big|_0^\infty (-RC) = \boxed{V_{DD}^2 C}$$

Energy from source

The energy stored on a capacitor is $\boxed{\frac{1}{2}CV^2}$ (Energy on cap)

$\Rightarrow \frac{1}{2}CV^2$ is lost on the resistor (dissipated as heat)

* Now consider the case when input is logic high and the cap was previously charged to V_{DD} by the PMOS switch. The equivalent model is :-



At the end of this, the total charge on the capacitor is zero (i.e, V_o is 0, or the cap is fully discharged, i.e logic-low output)

Since all the charges on the capacitor are lost, the energy of cap ($\frac{1}{2}CV^2$) must be dissipated on the resistor.

$\therefore$ $\frac{1}{2}CV^2$ is lost on the resistor, this time on the NMOS side !!
(dissipated as heat)

* At the end of the operation, a total of CV^2 ($\frac{1}{2}CV^2$ on PMOS side & $\frac{1}{2}CV^2$ on NMOS) energy is lost/dissipated in the circuit [this energy is provided by the supply V_{DD}]

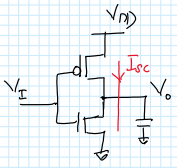
$\therefore$ Energy dissipation $\rightarrow \propto CV^2$

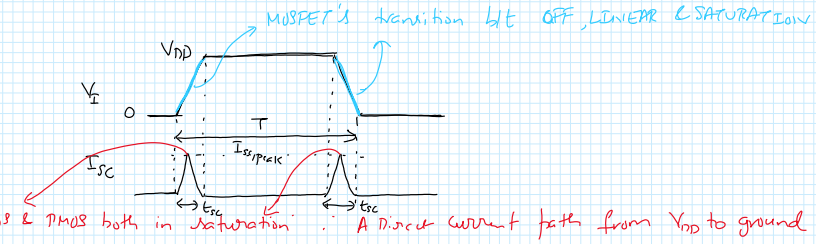
$$\text{Power} = \frac{\text{Energy}}{\text{Time}}$$

* Assuming that the NMOS & PMOS (in our circuit above) are periodically switching with period T (or frequency f),

$$\therefore P_{dyn} = \frac{CV_{DD}^2}{T} = CV_{DD}^2 f$$

(b) Power due to short-circuit path (P_{SC}) :-





NMOS & PMOS both in saturation $\therefore$ A direct current path from V_{DD} to ground

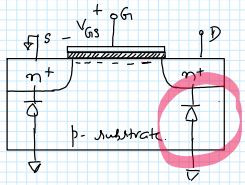
$$P_{SC} = V_{DD} I_{SC,avg} = V_{DD} \left[\frac{\frac{1}{2} \times t_{SC} \times I_{SC,peak} + \frac{1}{2} t_{SC} \times I_{SC,base}}{T} \right]$$

→ assuming current profile is perfect triangle (Area = $\frac{1}{2} \times b \times h$)

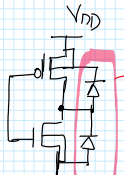
$$= V_{DD} I_{SC,peak} t_{SC} f$$

— × — × —

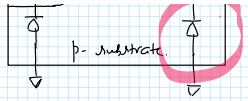
(c) Static power consumption (P_{stat}) (due to leakage current) :-



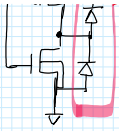
≡



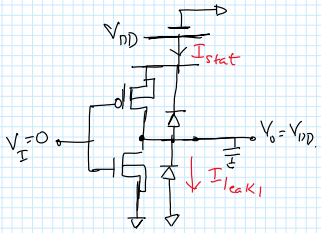
→ Reverse biased diodes (Drain-bulk)
(Source-bulk diode will have zero potential & it is ignored)



≡



(Source – bulk diode will have zero potential & it is ignored)



$$P_{stat} = V_{DD} \times I_{stat}$$

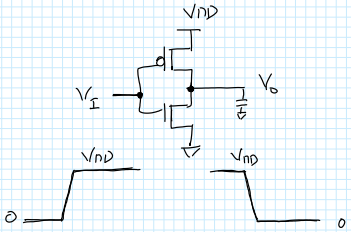
Total Power Consumption, $P_{tot} = P_{dyn} + P_{sc} + P_{static}$

_____ × _____ × _____

Note on the short-circuit current :-

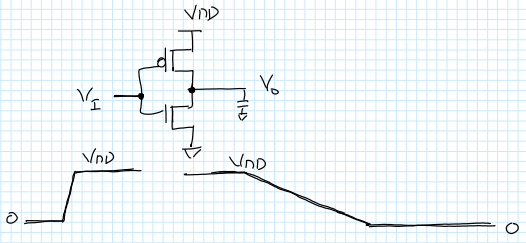
For a given input transition consider two cases.

(a) Very small capacitance :-



* This case, the PMOS will be in saturation majority of the transition time
⇒ Higher short-circuit current

(b) Very large capacitance :-



* This case, the PMOS will be in saturation only for a small interval of transition time
⇒ Reduced short-circuit current

∴ Peak short-circuit current is a function of input AND output voltage transition times.