EE671: VLSI Design
Spring 2024/25

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LECTURE – 22
PHYSICAL DESIGN

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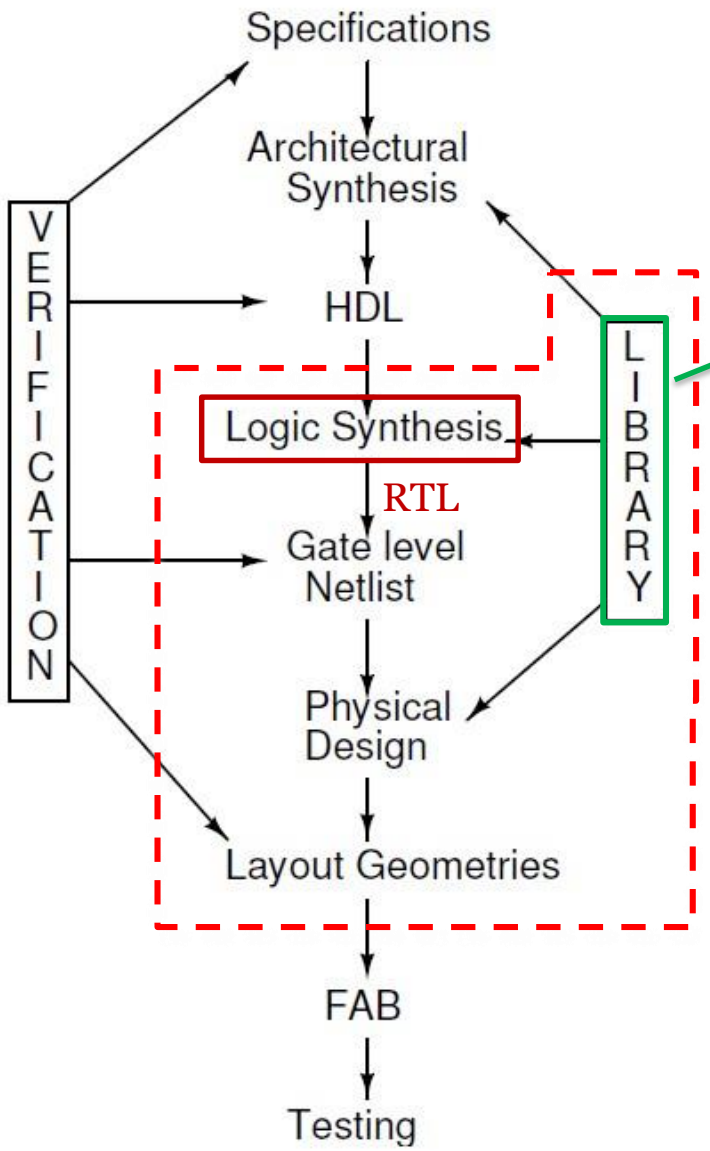
LOGIC SYNTHESIS

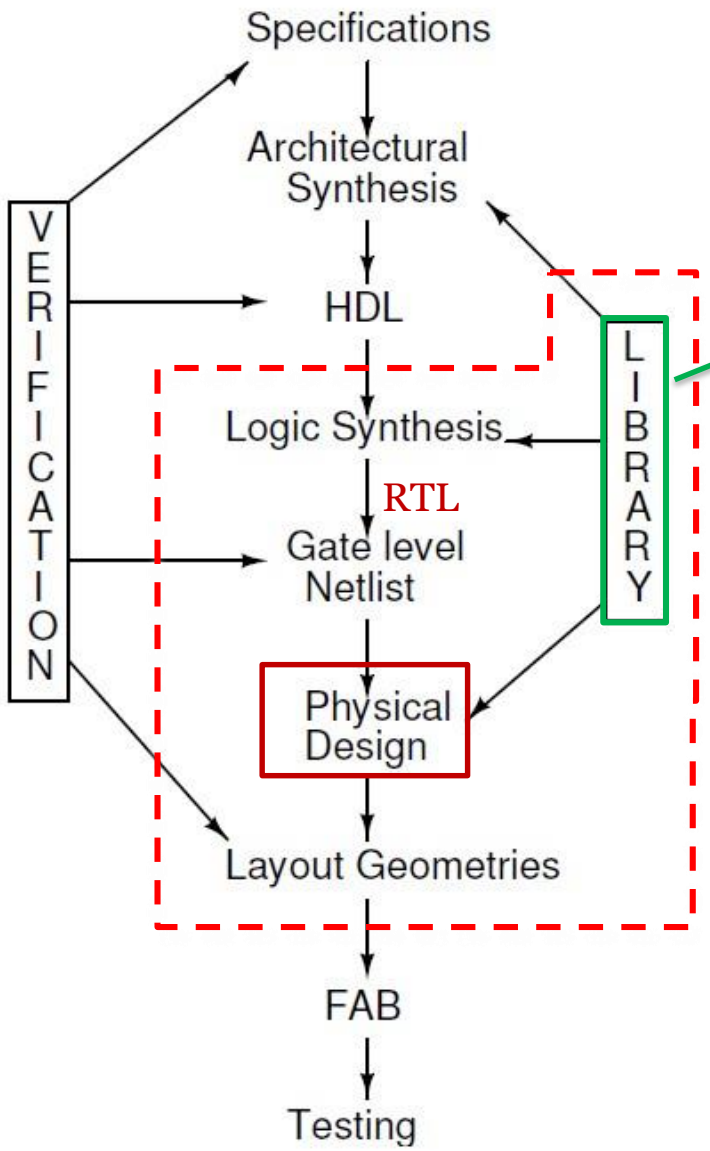


STANDARD CELL LIBRARY:
.V, .LEF. LIB, .SP, .GDSII/.MAG

LOGIC SYNTHESIS:

- INPUT: HDL (VERILOG – BEHAVIORAL/STRUCTURAL CODE)
- OUTPUT: RTL (REGISTER TRANSFER LEVEL VERILOG)
- RTL: COULD BE OR COULD NOT BE MAPPED TO A TECHNOLOGY (STD. CELL LIBRARY)

PHYSICAL DESIGN



STANDARD CELL LIBRARY:
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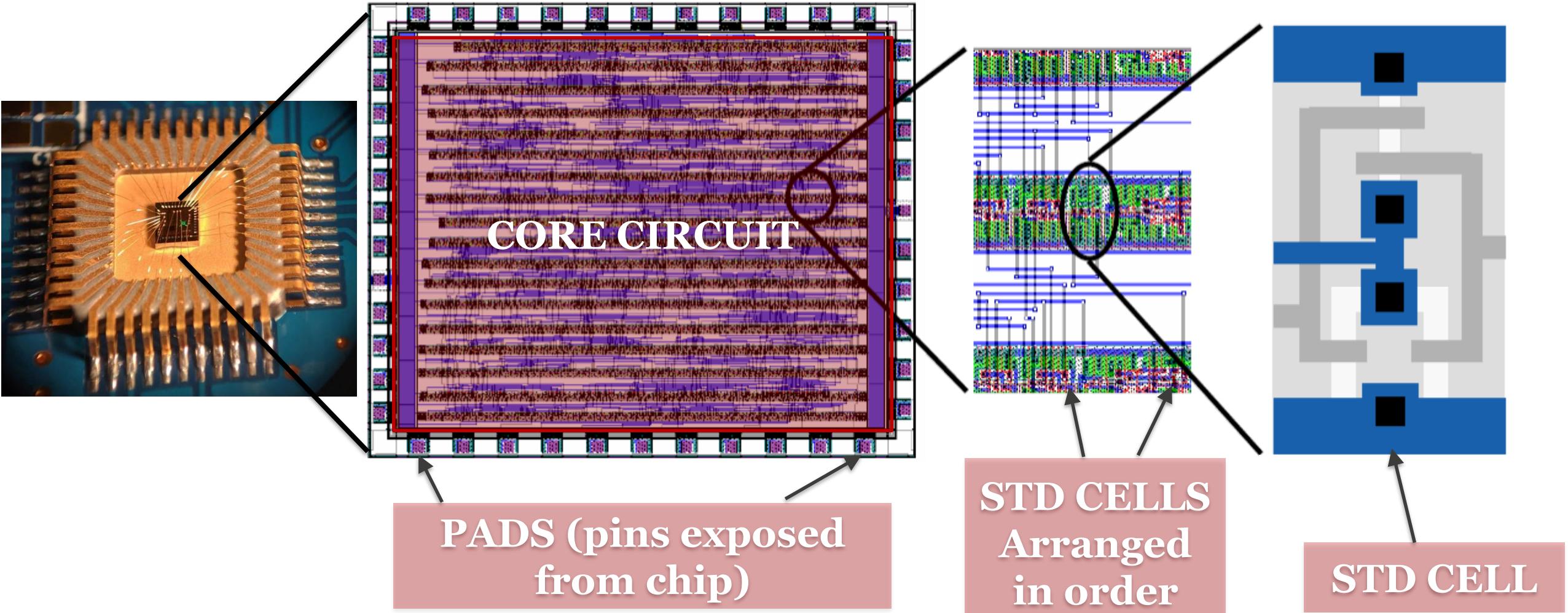
PHYSICAL DESIGN:

- INPUT: RTL (MAPPED TO STD. CELL LIBRARY)
- OUTPUTS:

FINAL CHIP LAYOUT (GDSII), FINAL CHIP RTL, FINAL CHIP LEF, FINAL CHIP TIMING DATA (SDF)

- GDSII: WILL BE SENT OUT TO FABRICATION FOUNDRY TO PRODUCE THE CHIP

MOTIVATION



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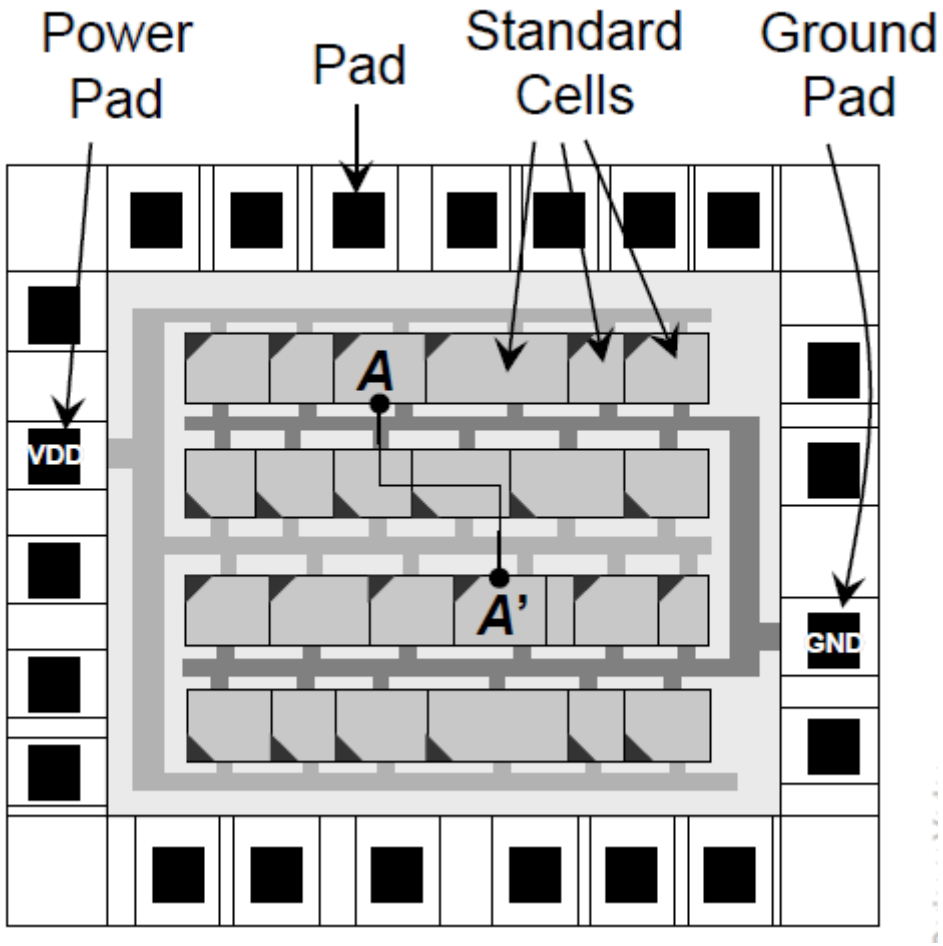
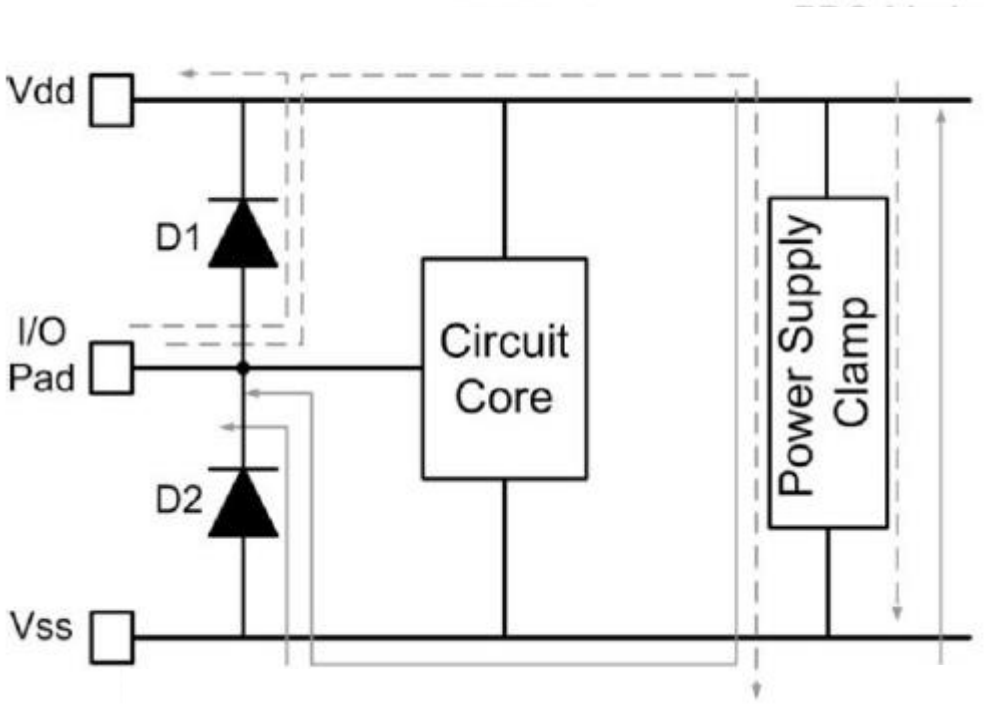
MOTIVATION

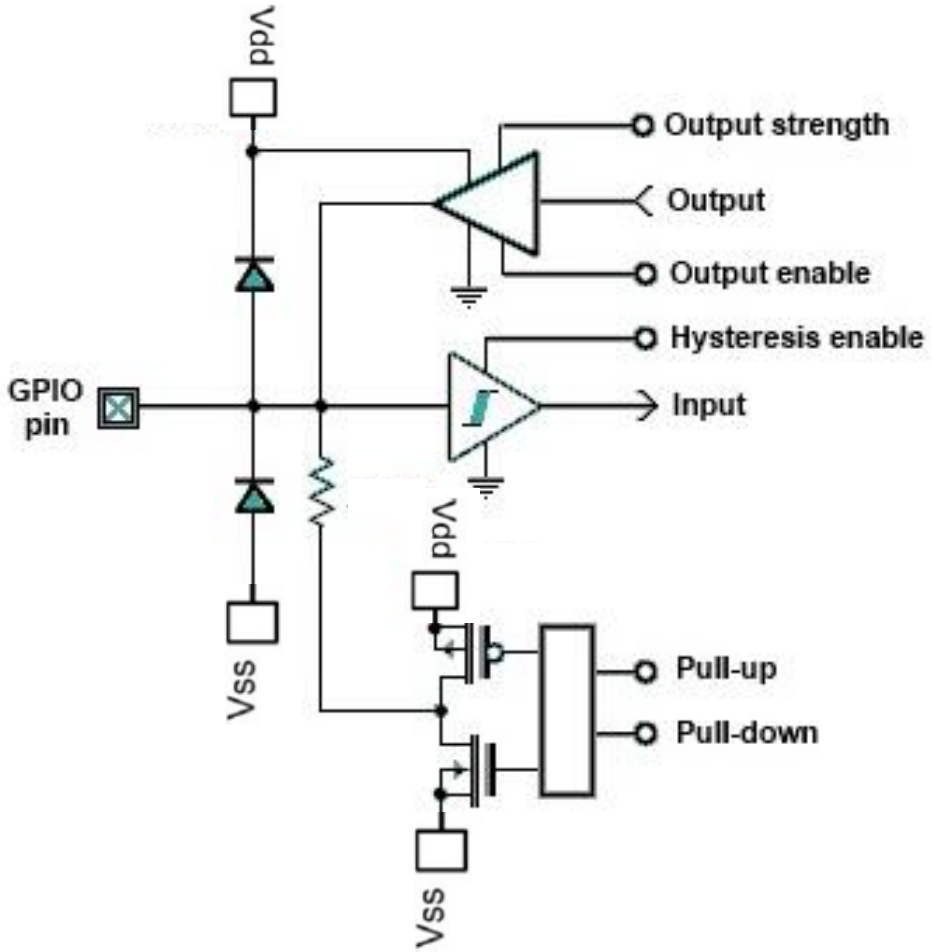


- Standard cell library:
  - comprises of all standard cells – combinational & sequential elements
- IO Library:
  - Comprises of IO pads – VDD pads, VSS pads, analog pads, digital input/output pads
  - ESD protection part of the IO pad (usually circuit under pad)

TYPICAL ESD PROTECTION CIRCUIT



Typical Analog I/O PAD



Typical bi-directional, programmable digital I/O PAD

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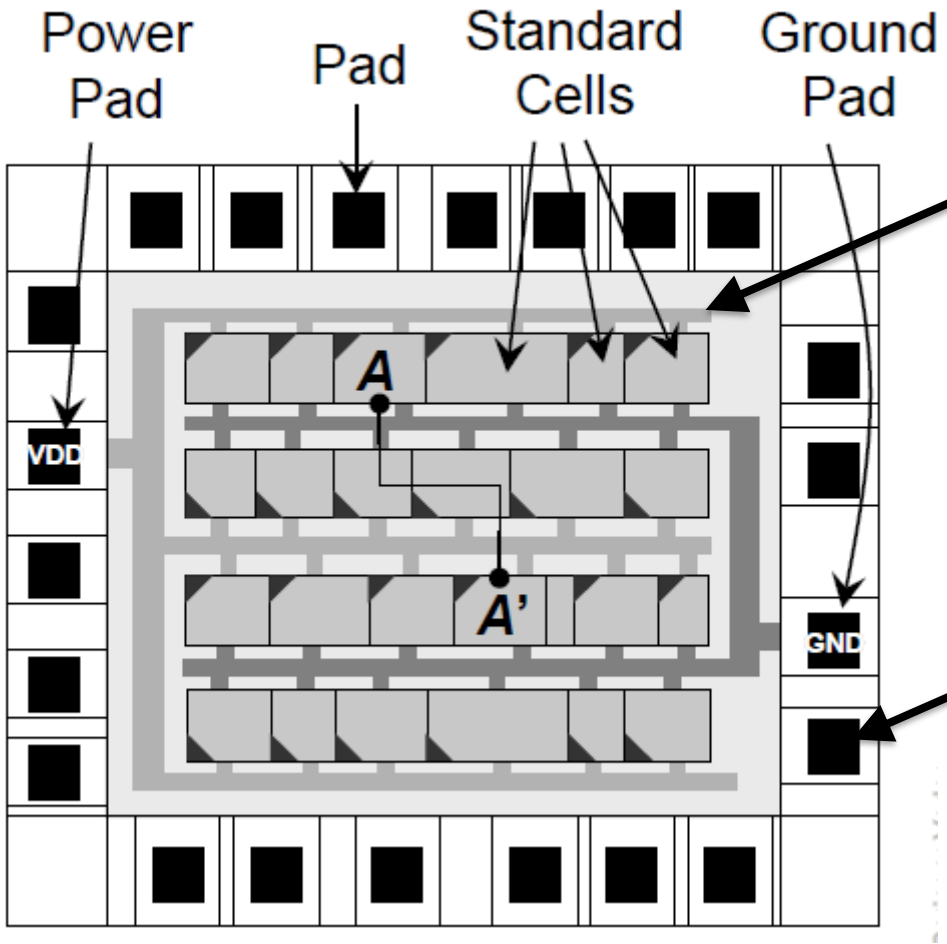
FULL CHIP PICTURE

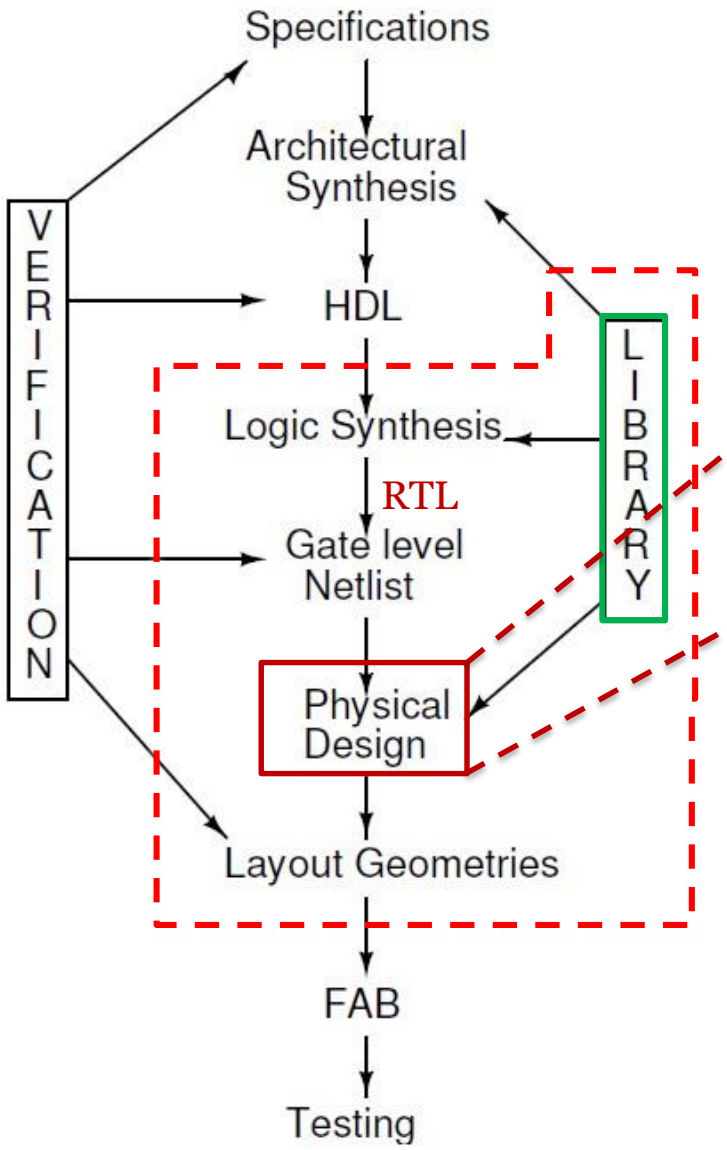


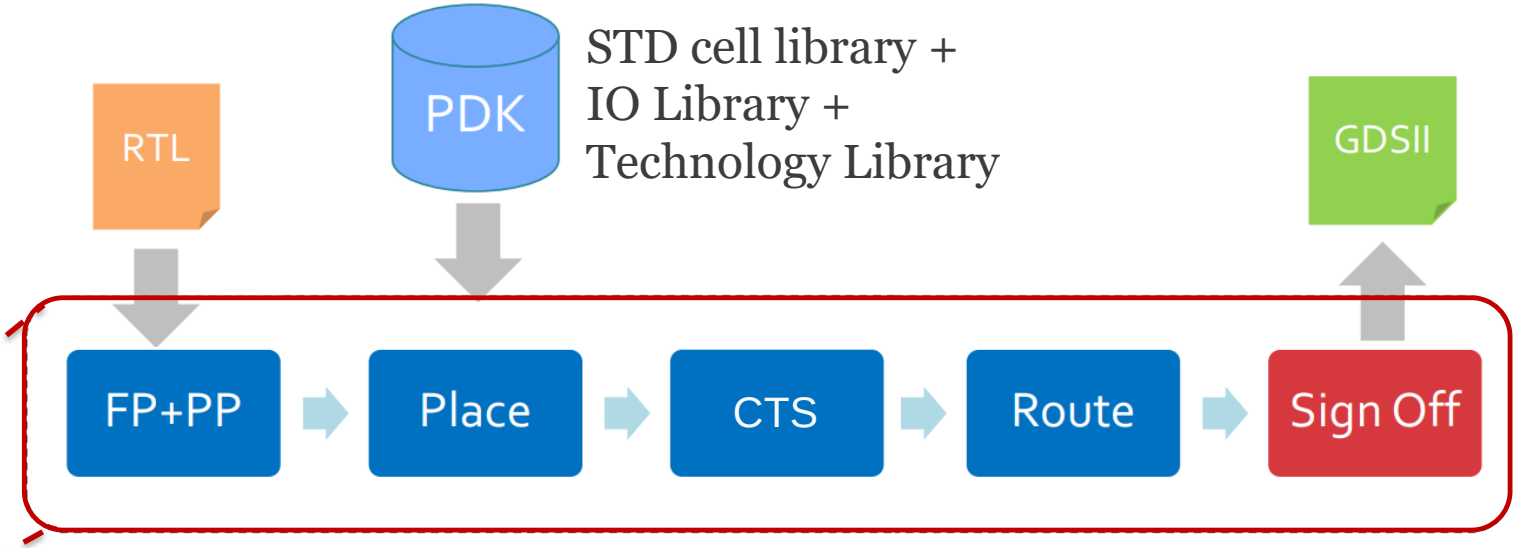
Core circuit area made of standard cells.

Analog or digital IO pads depending on the nature of the signal. The circuit is sitting under the metal pad (black shade) outside the core area.

The metal pad will be wire-bonded to the package

PHYSICAL DESIGN





1. FP + PP: Floor planning + Power planning
2. Place: Placement
3. CTS: Clock tree synthesis
4. Route: Routing (Global and local)
5. Sign-off: final checks before gdsII submission
   a) DRC: Design rule check
   b) LVS: layout – vs - schematic
   c) STA: Static Timing Analysis

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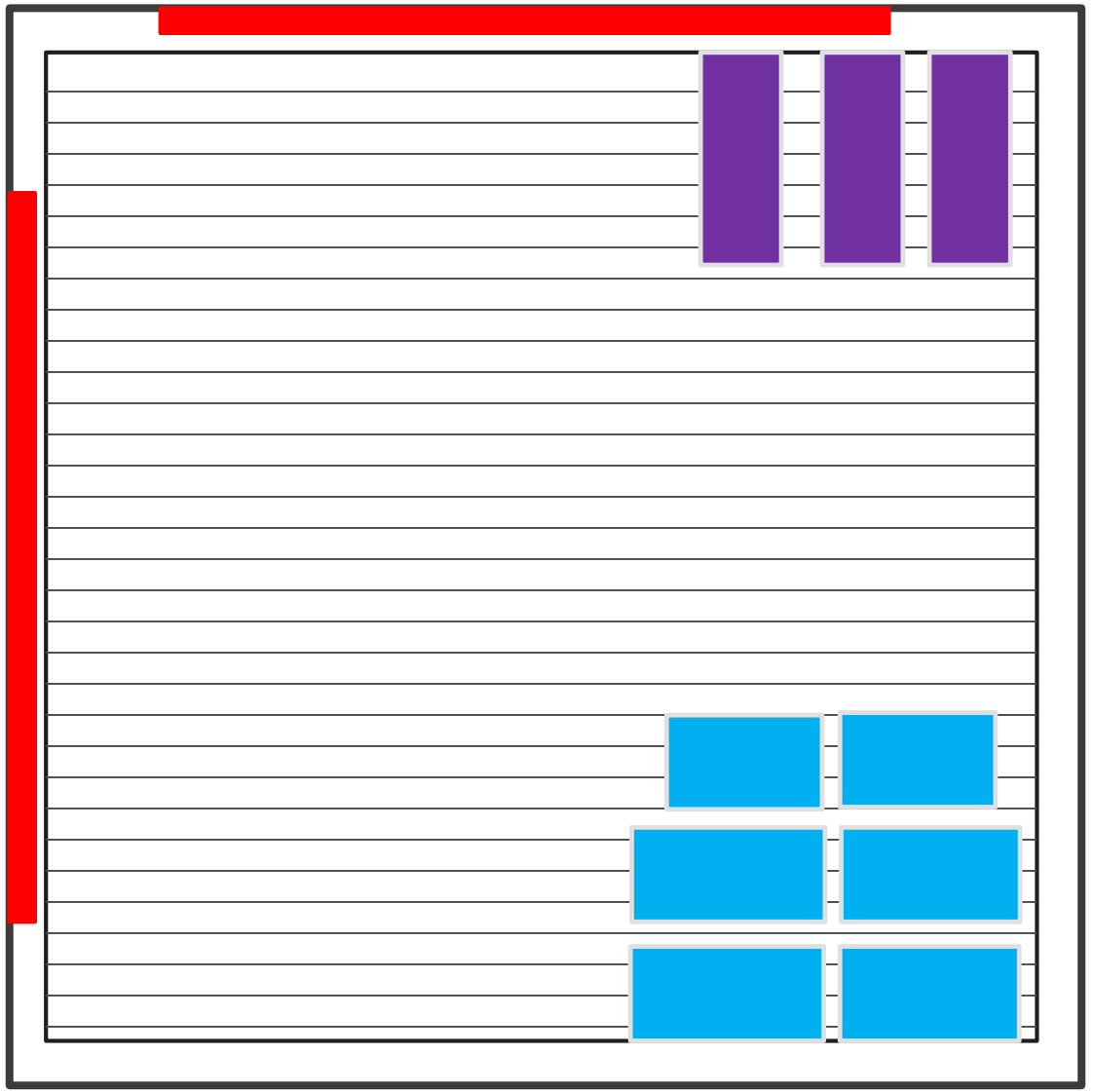
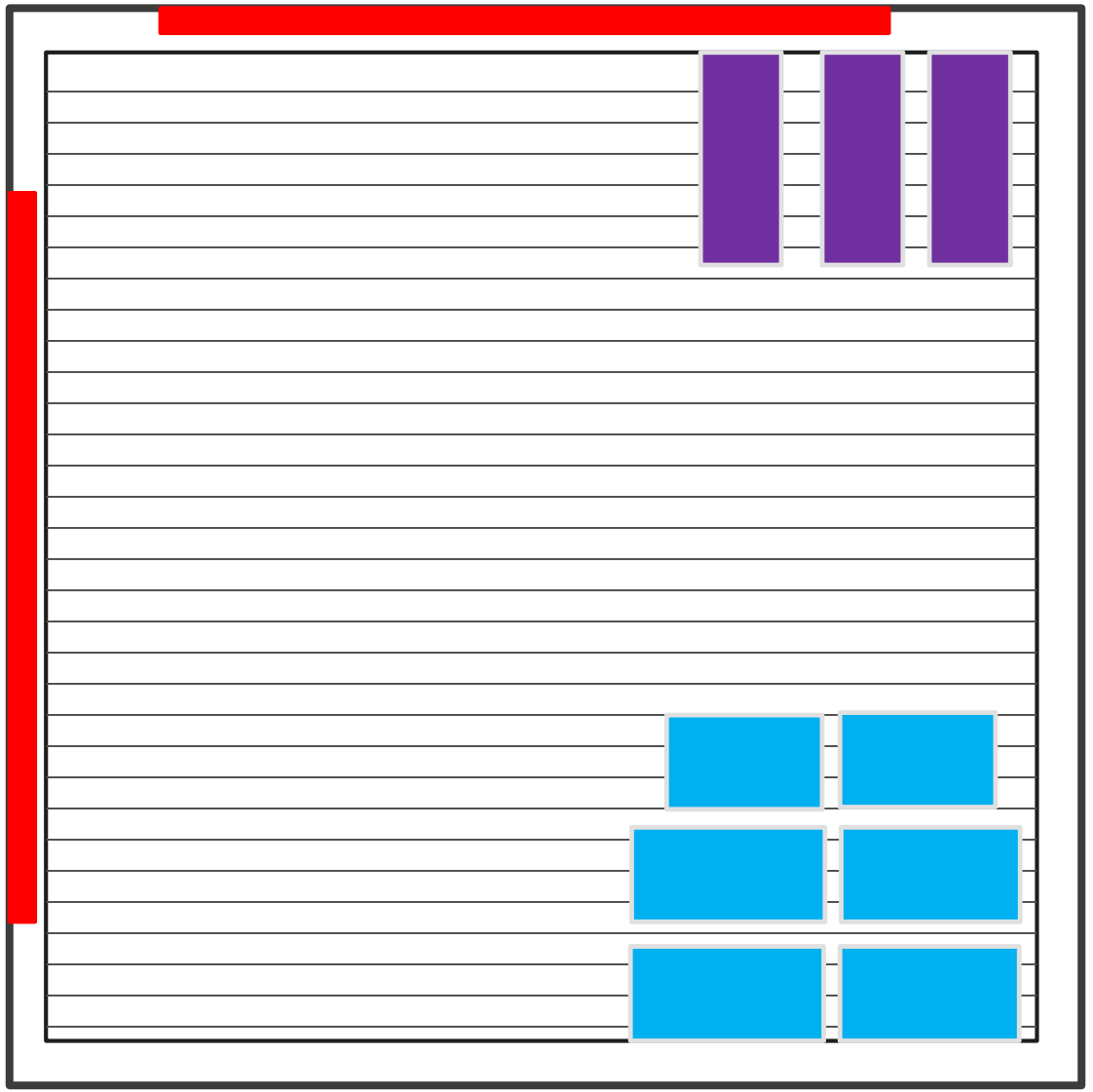
PHYSICAL DESIGN: FLOORPLAN

- Floor planning:
- Define core area size (Area: Width & Height)
- Create cell rows (std cell height)
- IO placement:
  - Define what kind of IO (analog/digital/VDD/VSS) should reside where
- Macro cell placement:
  - Macros are modules for which you already have a layout (Ex: third part memory, ARM core etc.)



PHYSICAL DESIGN: FLOORPLAN

- Macro Placement:
- Make smart choices:
  - Timing: be aware of what block talk to what so that you can place them closer (for minimal routing)
  - Macro pins oriented towards nearest standard cells
  - Distance of memory macro from standard cells
  - Plan to avoid routing congestion (number of connections from macro)



PHYSICAL DESIGN: FLOORPLAN

- Macro Placement:
  - Example congestion planning

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PHYSICAL DESIGN: FLOORPLAN

- Macro Placement:
  - Example congestion planning
  - Move macros away from IO if the macro does not have any connections to IO
  - Place memory cells to avoid routing congestion

Floorplan Height

Floorplan Width

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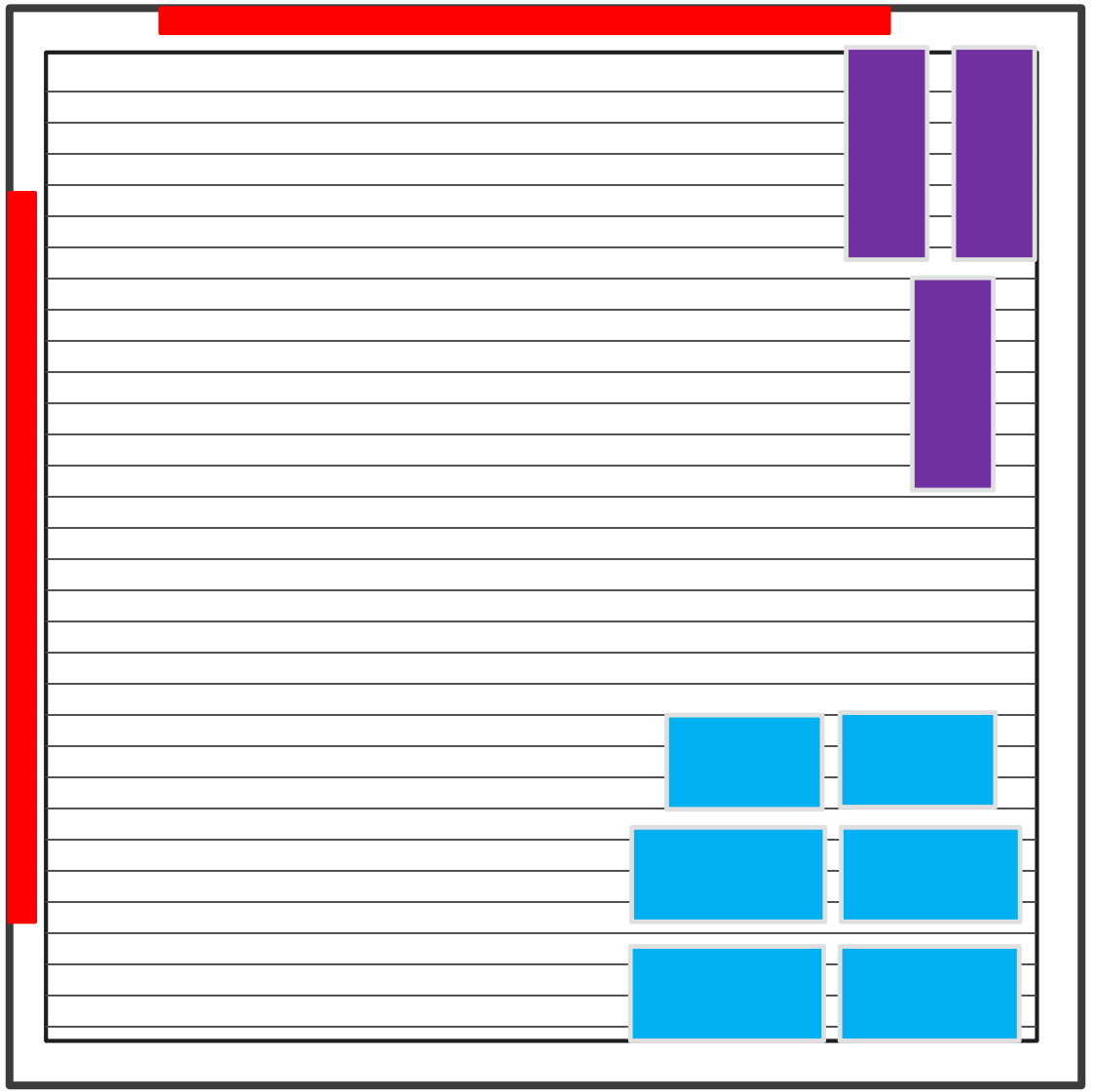

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Floorplan Width

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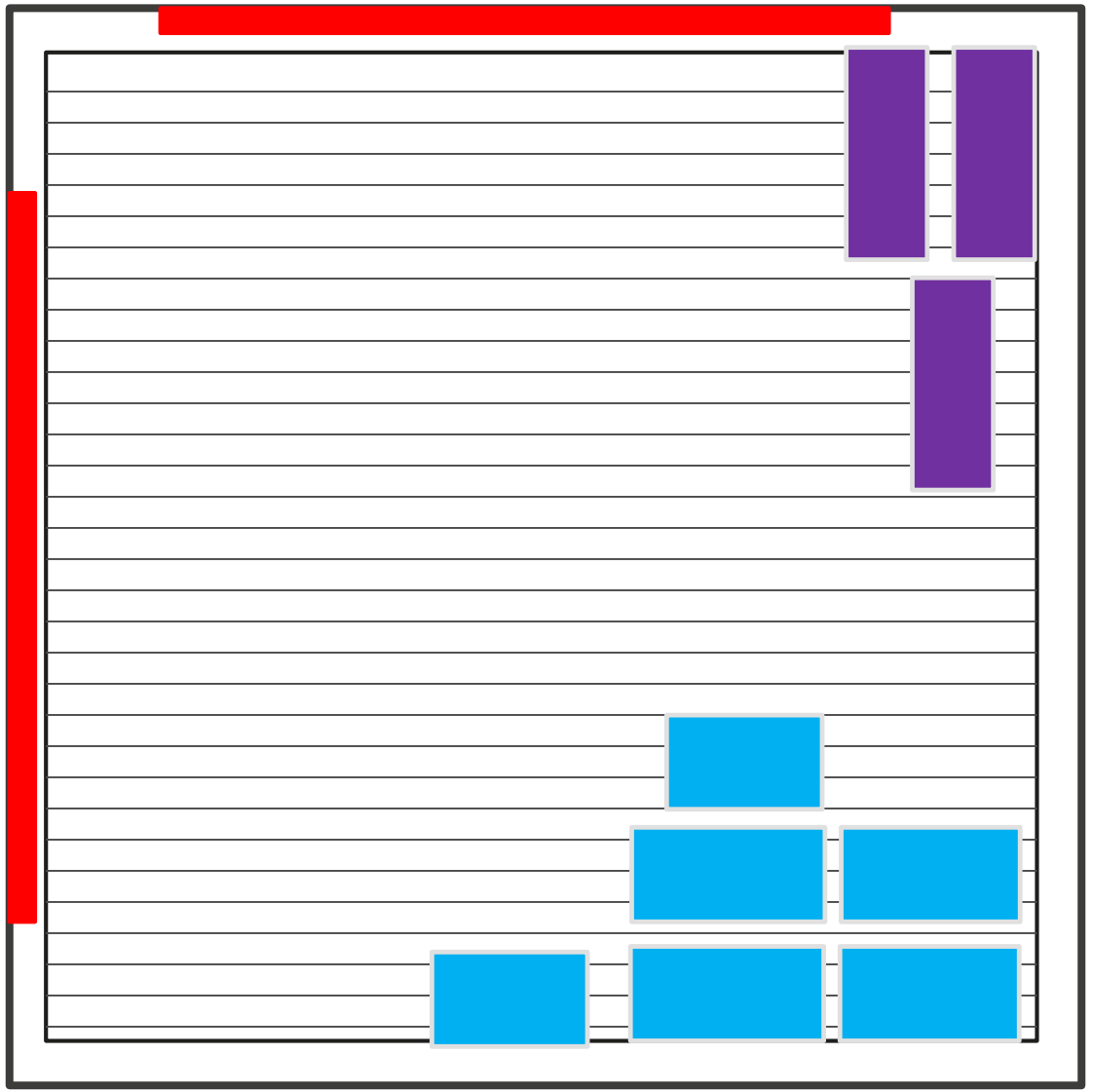

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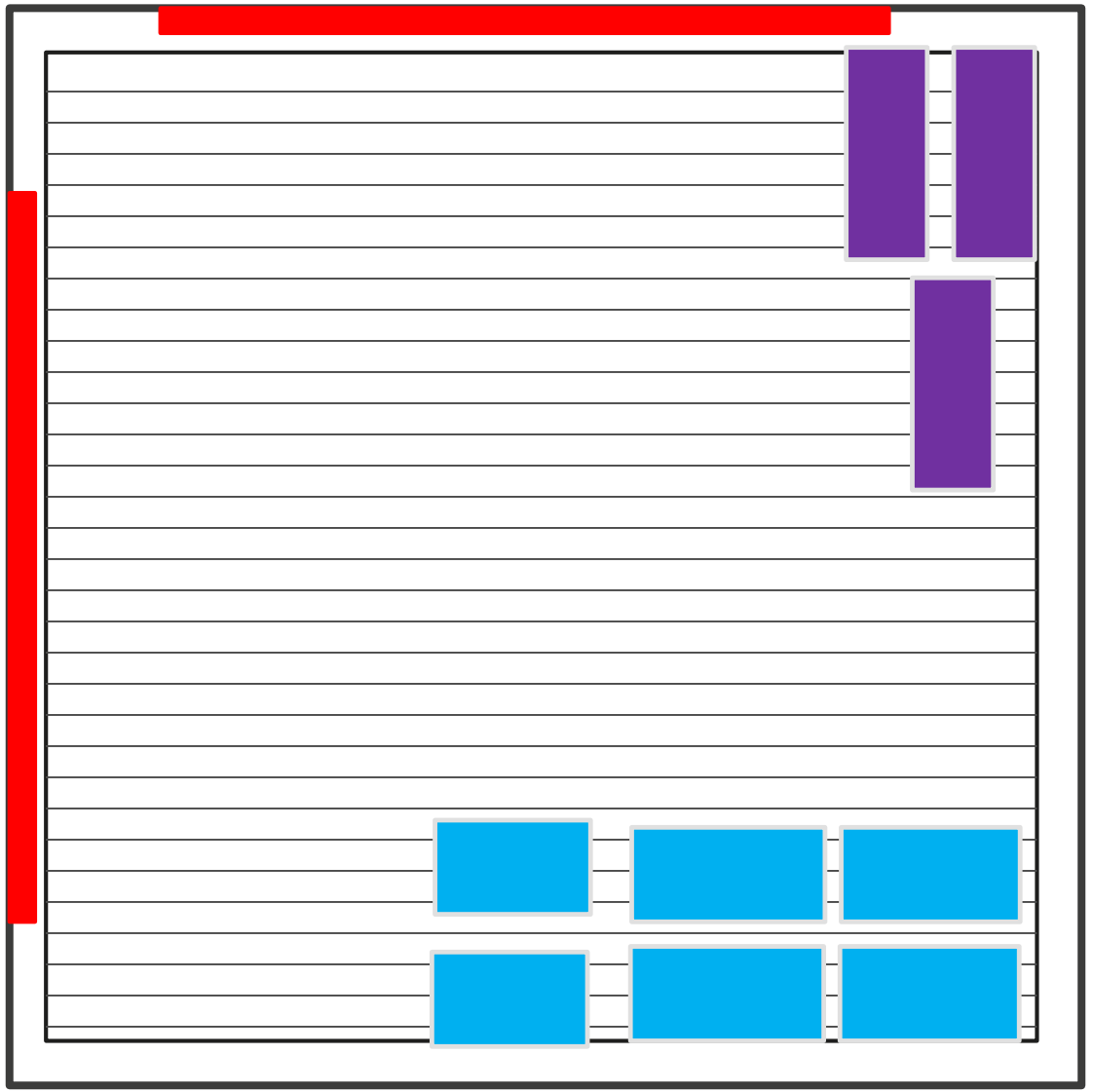

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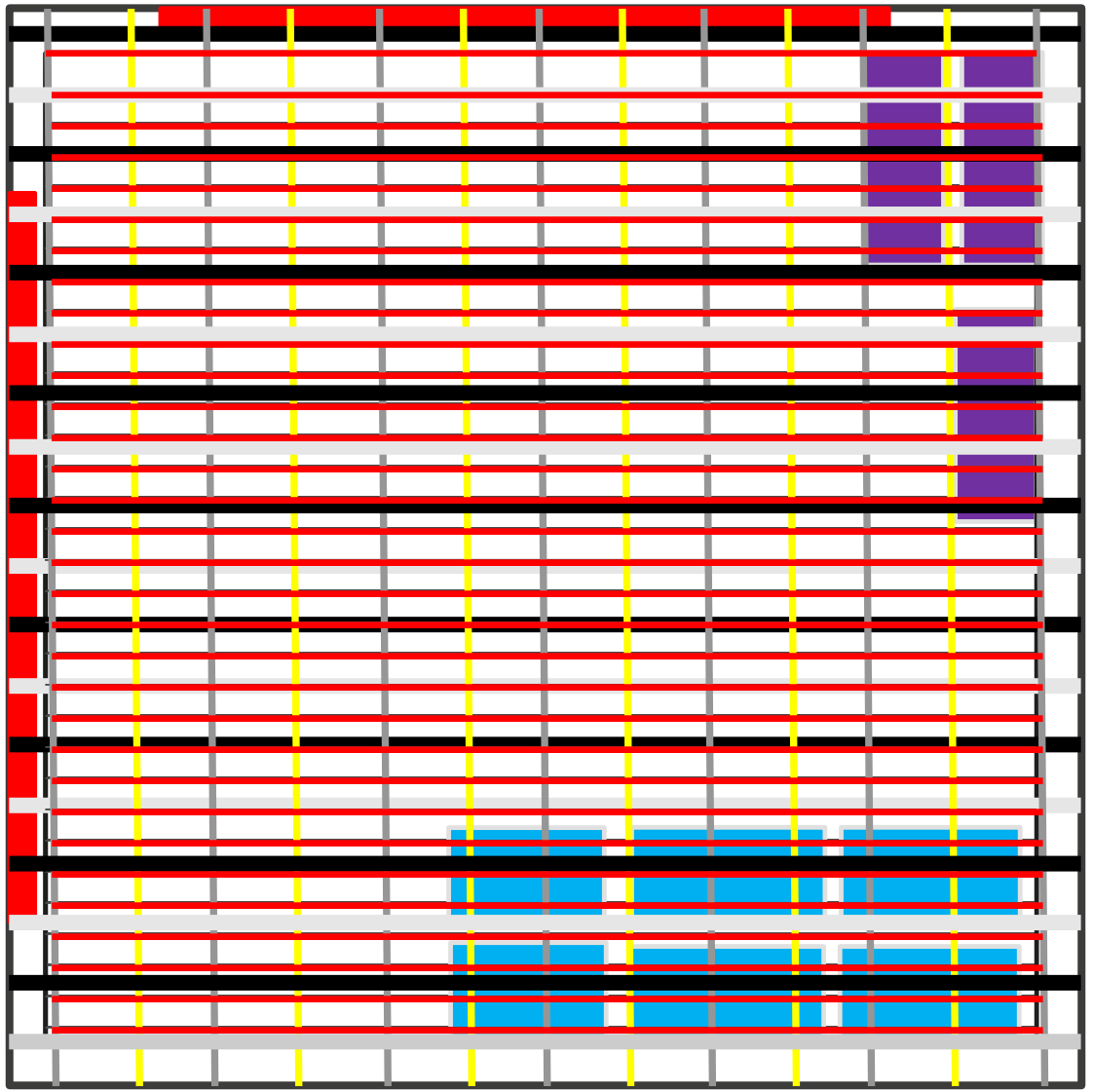
PHYSICAL DESIGN: FLOORPLAN

- Power Planning:
- Supply VDD/VSS to standard cells and Macros
- Complex designs:
  - Be aware of the power consumption of blocks – IR drop on the power rail/grid – degrades circuit performance



Floorplan Height

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