EE671: VLSI Design
Spring 2024/25

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LECTURE – 34
SRAM CONTINUED

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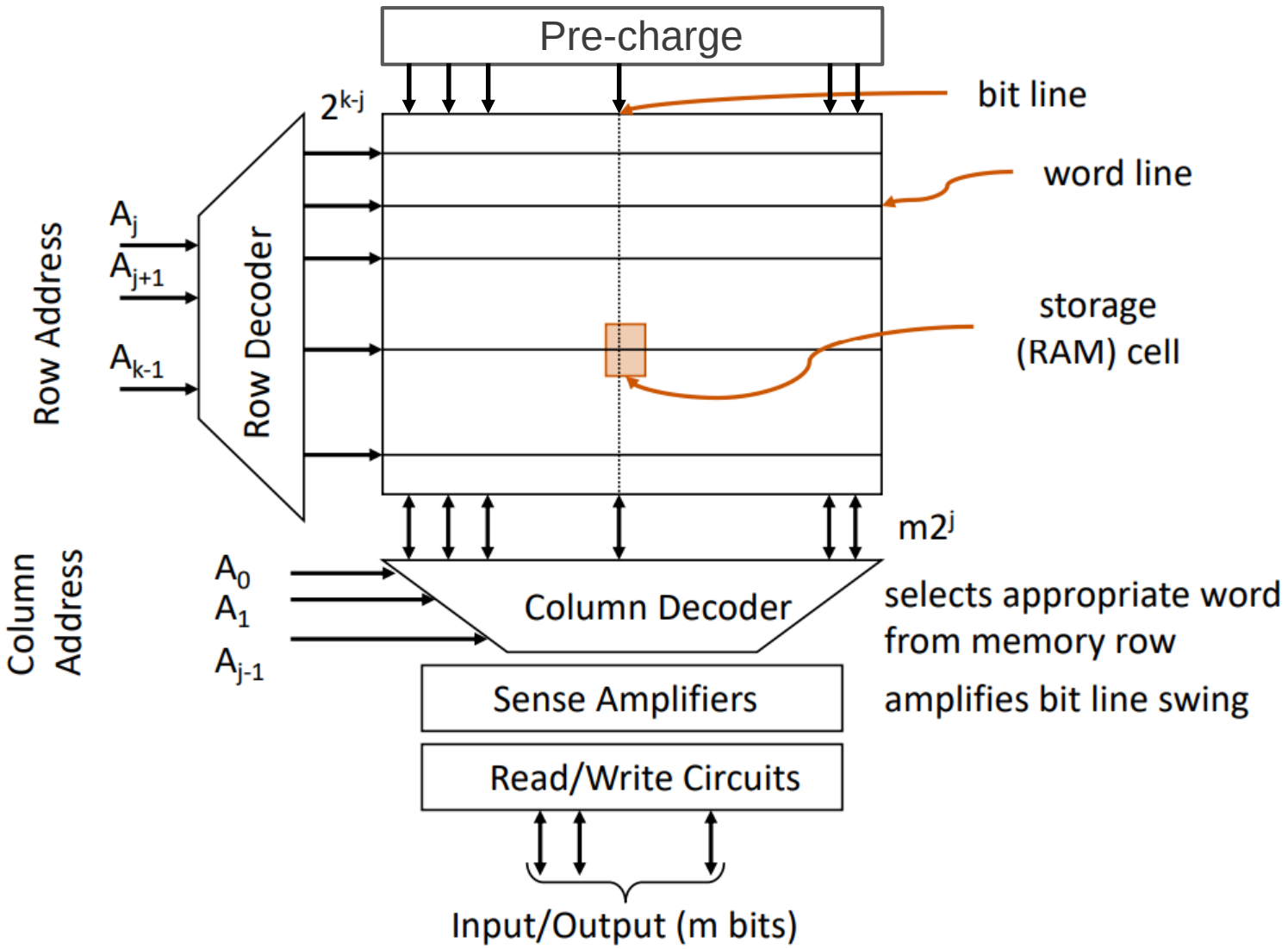
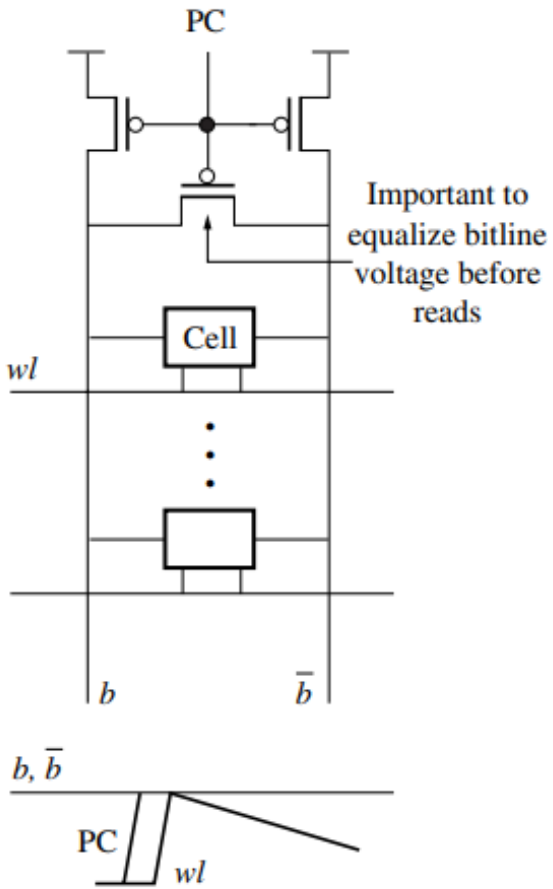
SRAM: Full Picture



- We have looked at the Row decoder (logical effort design)
- Looked at design of individual bit-cell
- Next, we will look at the pre-charge circuit, column decoders, sense amplifiers

COLUMN PULL-UPS: PRE-CHARGE

- To remove all history → perform pre-charge before every read and write
- The nature of pre-charge (PC) circuit depends on the amplification (also called sense amplifier (SA)) topology

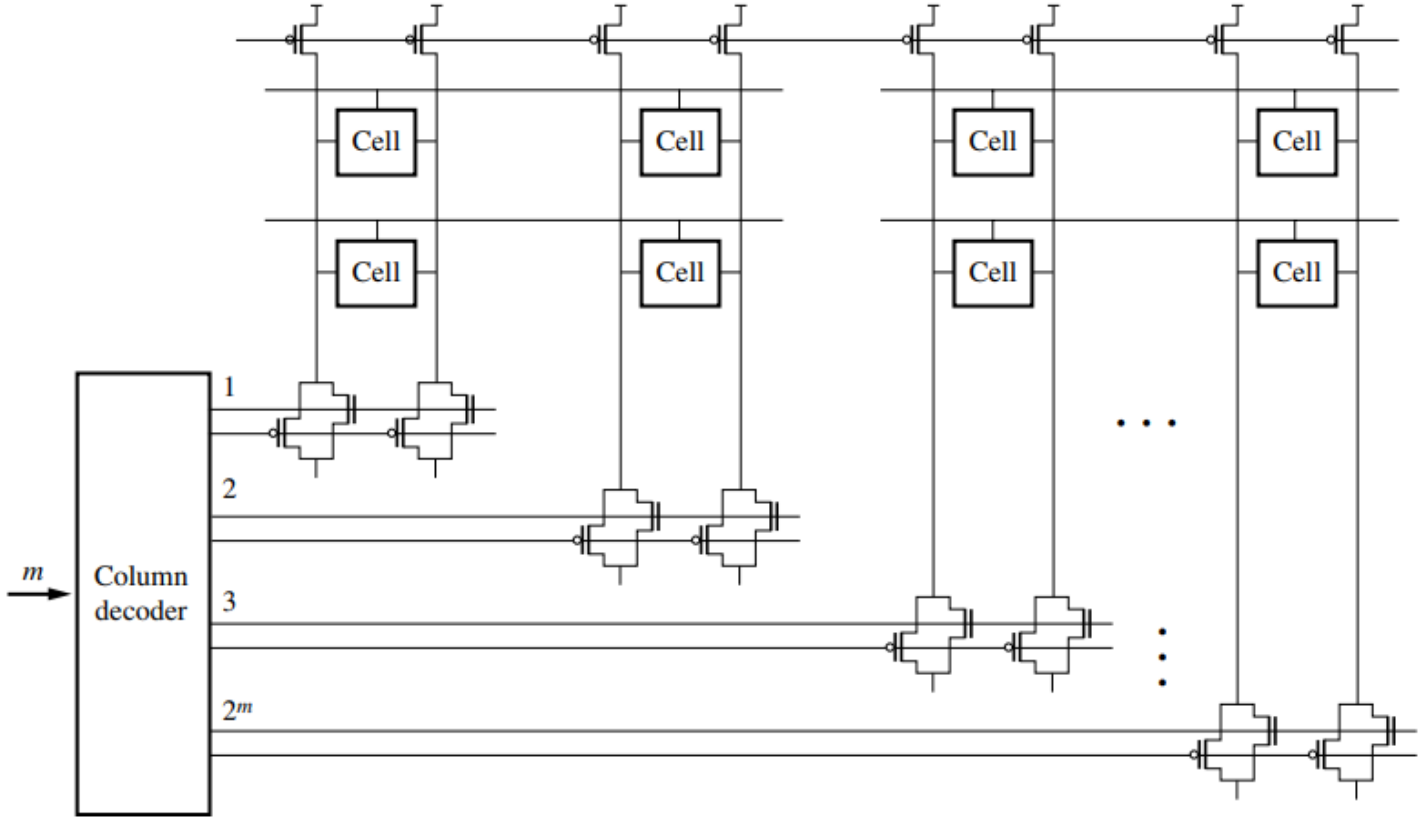


Suitable for voltage based amplifiers

- Sequence:
  - PC is low by default (Pre-charging bit lines)
  - PC goes high
  - After some finite time → WL goes high
  - Read operation starts
  - Bitlines start developing delta voltage
  - Sense amplifier (SA) enabled after finite time to amplify this delta voltage
  - Once logic levels are obtained at the output, disable WL, SA and enable PC

Column Decoder (Column Mux)

- After PC, the columns involved in read/write are to be enabled using MUX
- Usually this MUX is a simple TG (we looked at implementing MUX using TG earlier)



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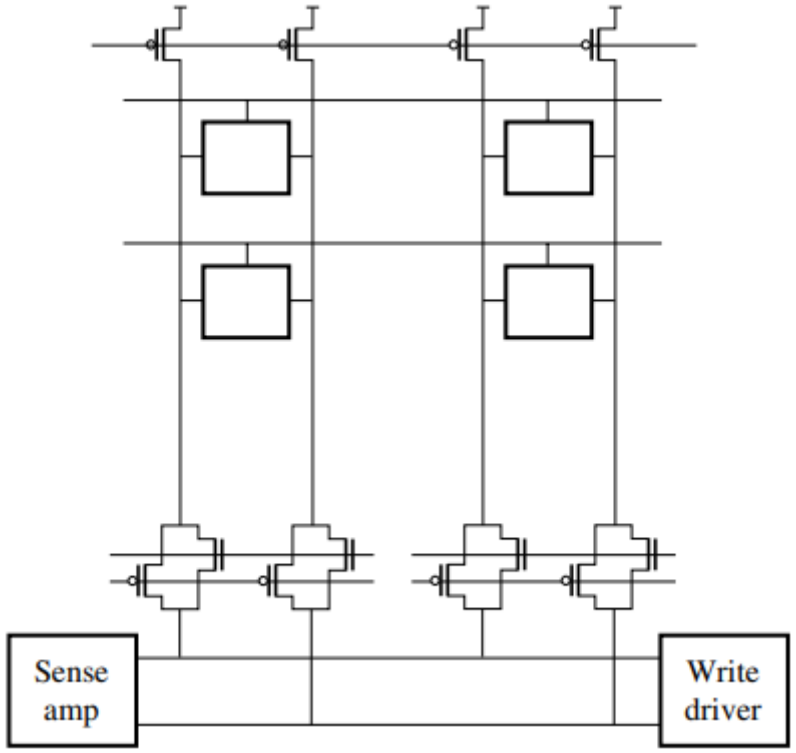
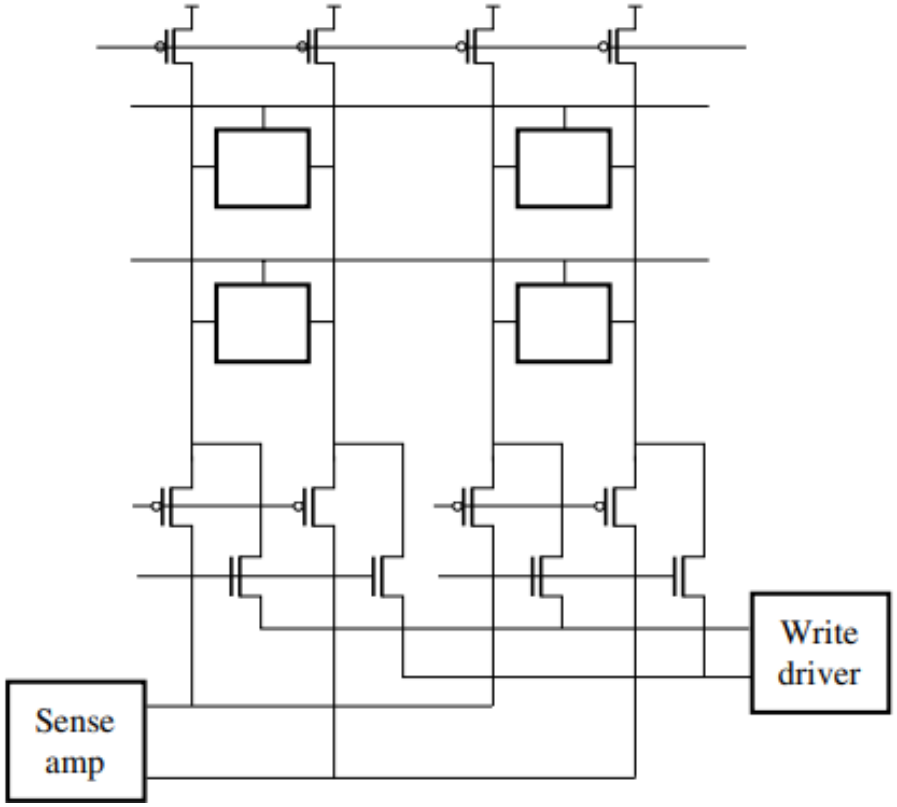
Column Decoder (Column Mux)

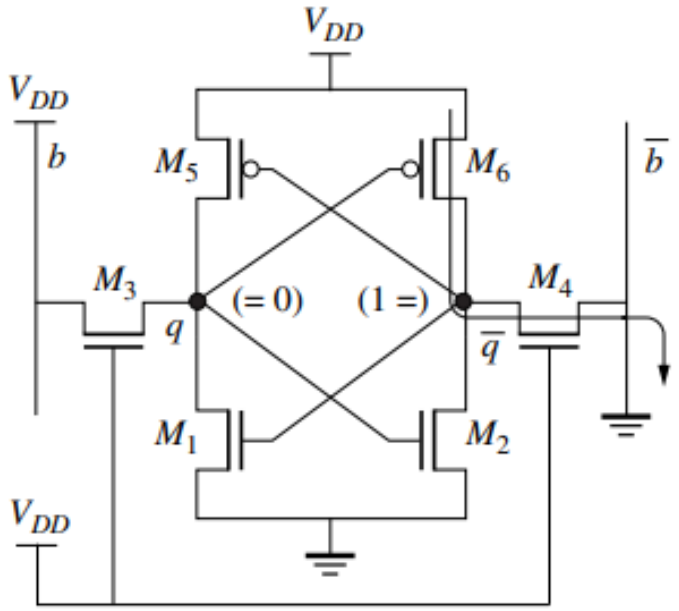
- The read and write operation paths can be separated as shown below
- SA is enabled during read and write driver is enabled are enabled during write after selecting the required columns



Column Decoder (Column Mux)

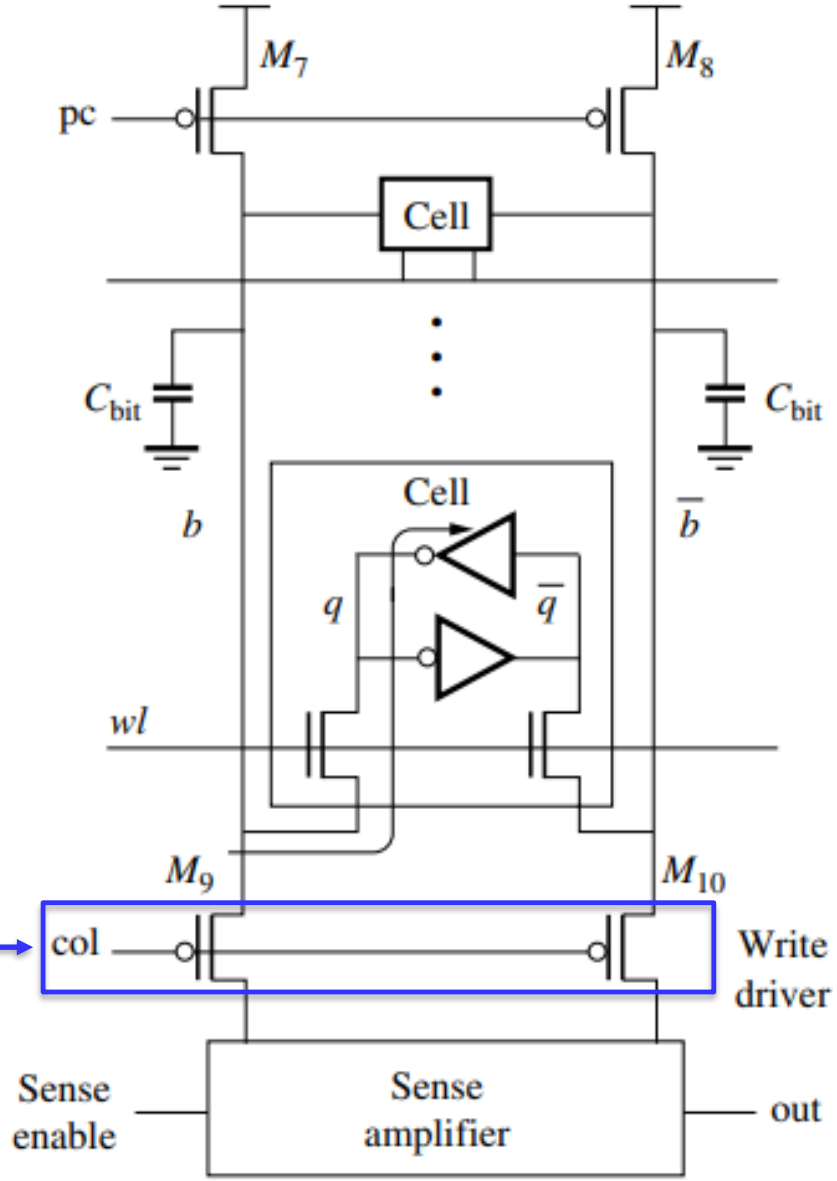
- Note that, during read all lines are V_{DD} (pre-charge), so we only really need PMOS devices during read operation
- During write, essentially, we are discharging bitlines to ground → we need NMOS
- This automatically provides the enabling of read/write using the same column decoder

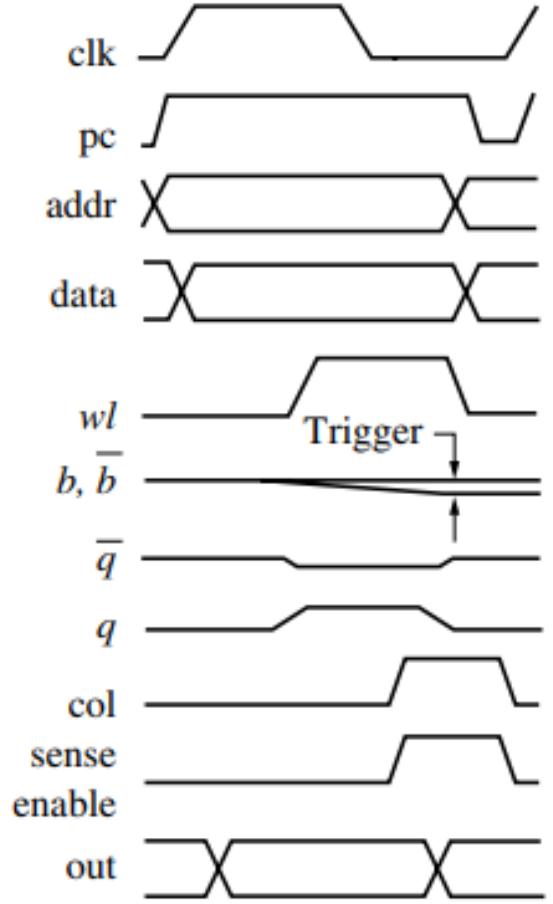




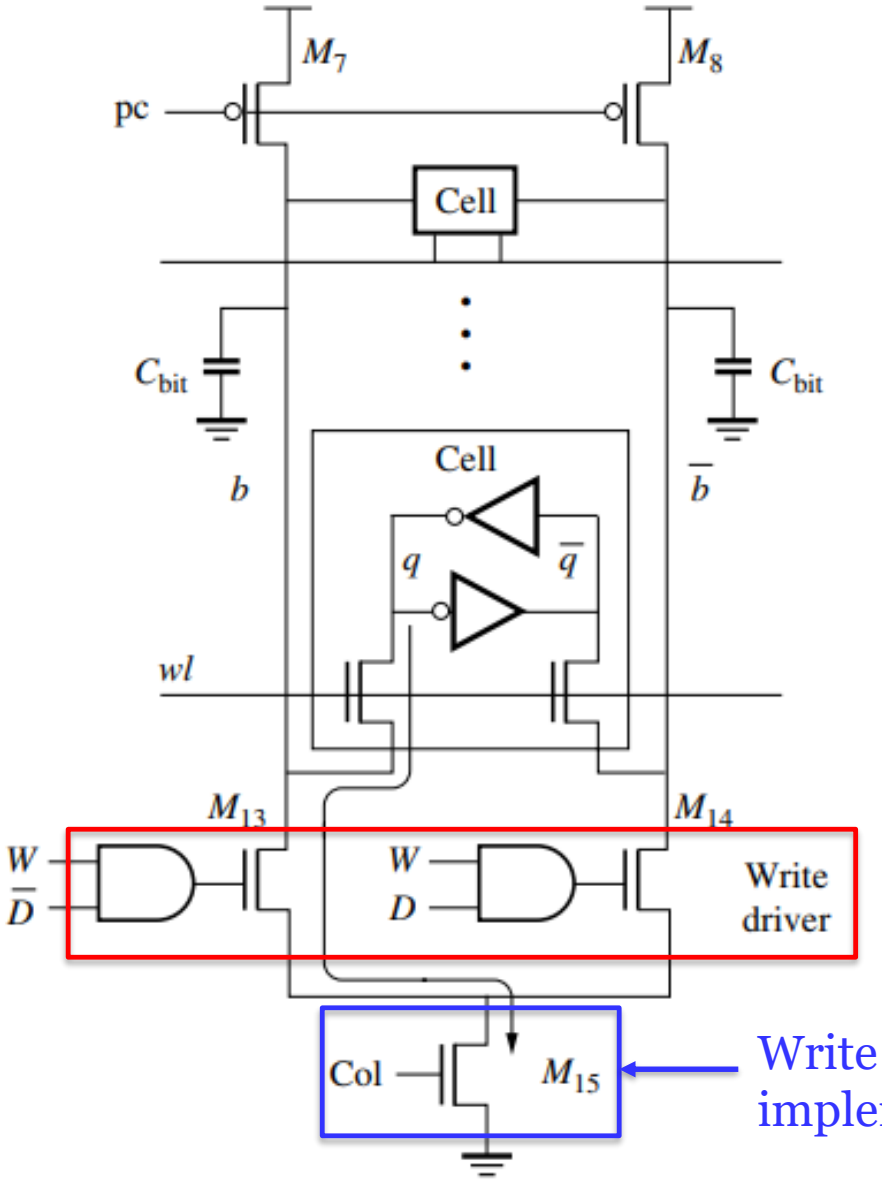
Complete Read Circuit (one column)

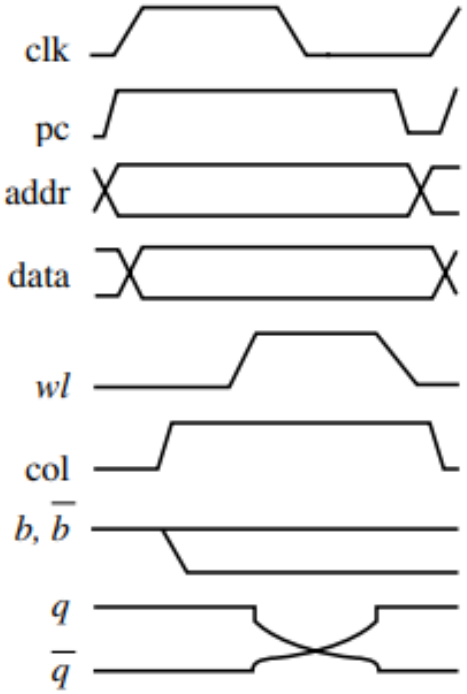
Read column mux (PMOS only implementation)





Complete Write Circuit (one column)

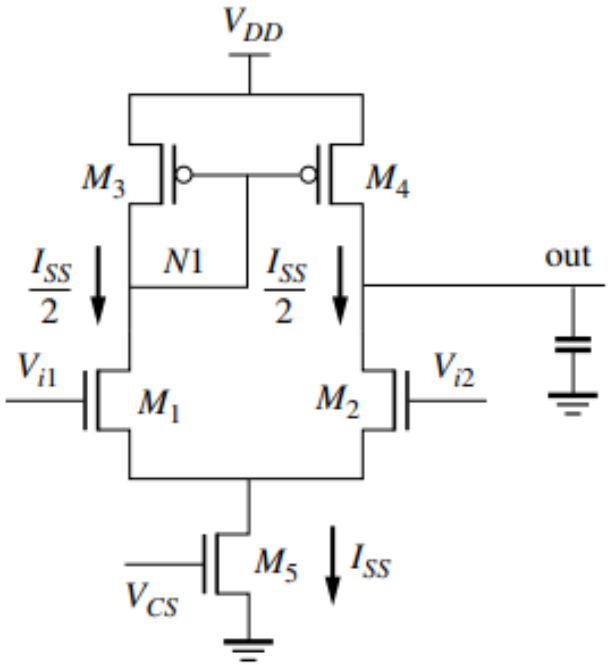


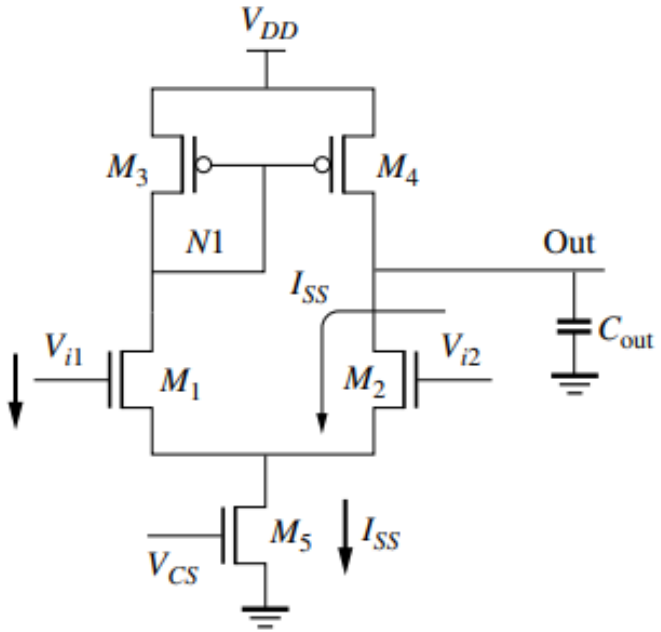


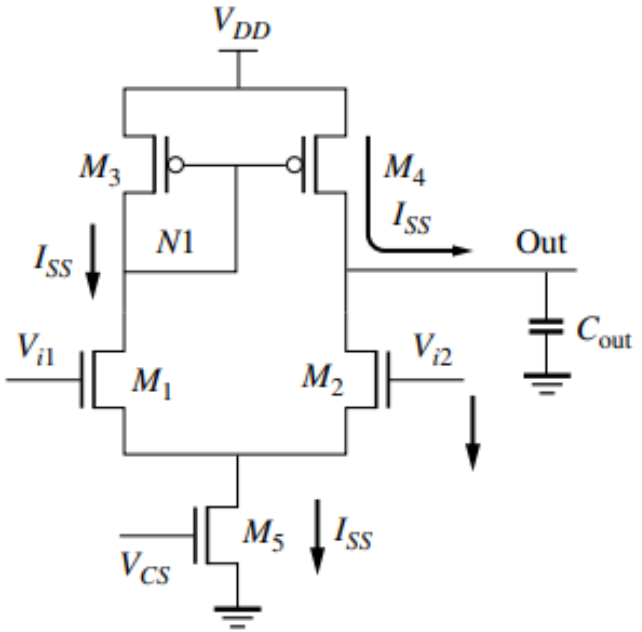
Write column mux (NMOS only implementation)

SENSE AMPLIFIER

- Option-1: A simple differential amplifier
  - Provides good common-mode rejection (common-mode noise)
  - Typical: 100 mV to 200 mV input voltage required
  - Static power consumption!

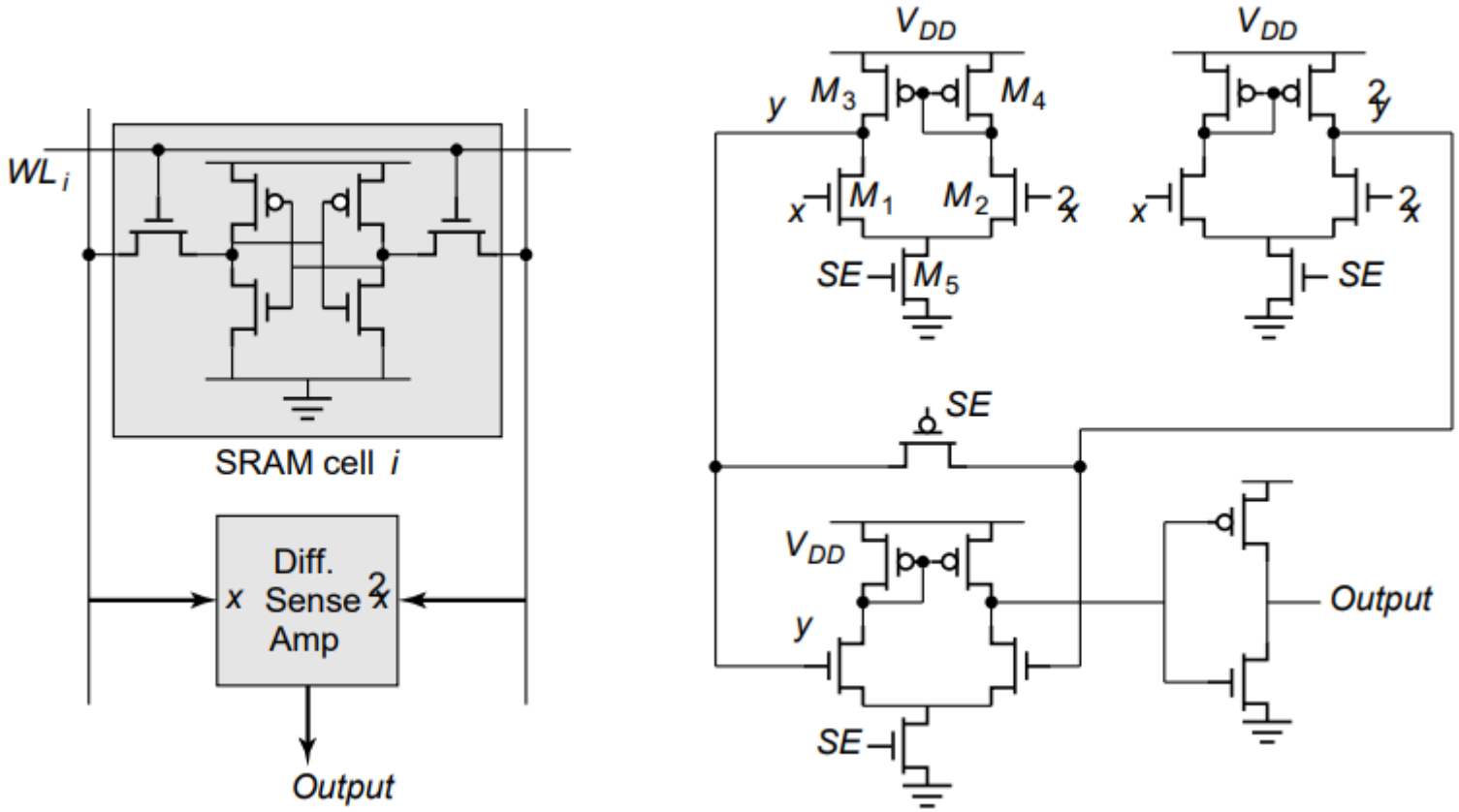






SENSE AMPLIFIER

- Option-1: A simple differential amplifier
  - Could also increase stages: but delay increases



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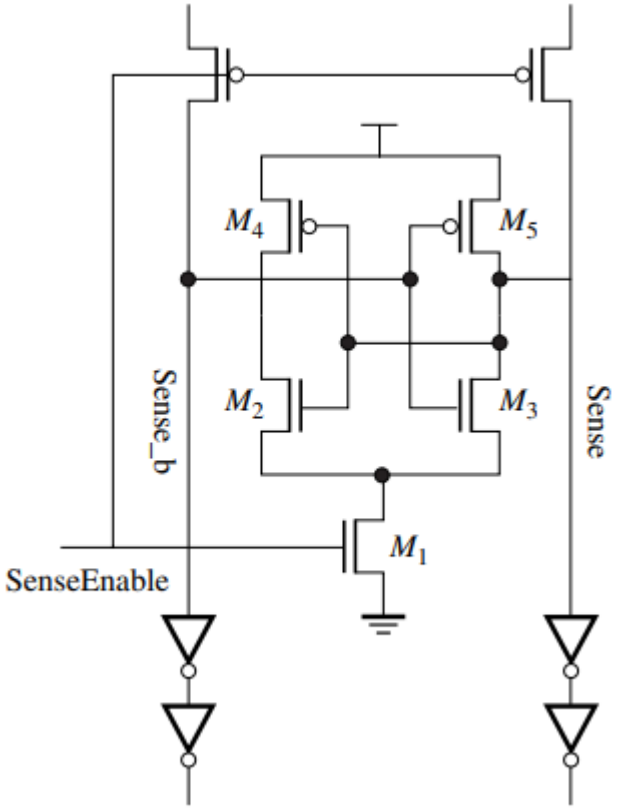
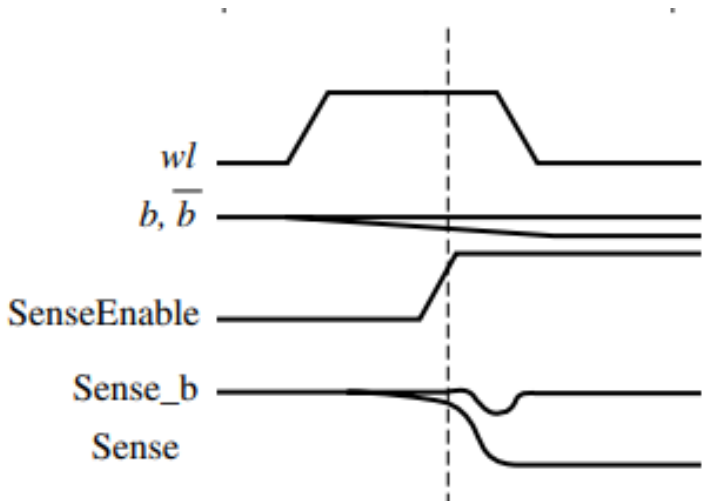
Sense Amplifier

- Option-2: Latch based amplifier (positive-feedback)
  - Cross-coupled inverter
  - Inverters reset to VDD in off state (switches not shown in diagram below)
  - Also used as comparators in ADCs





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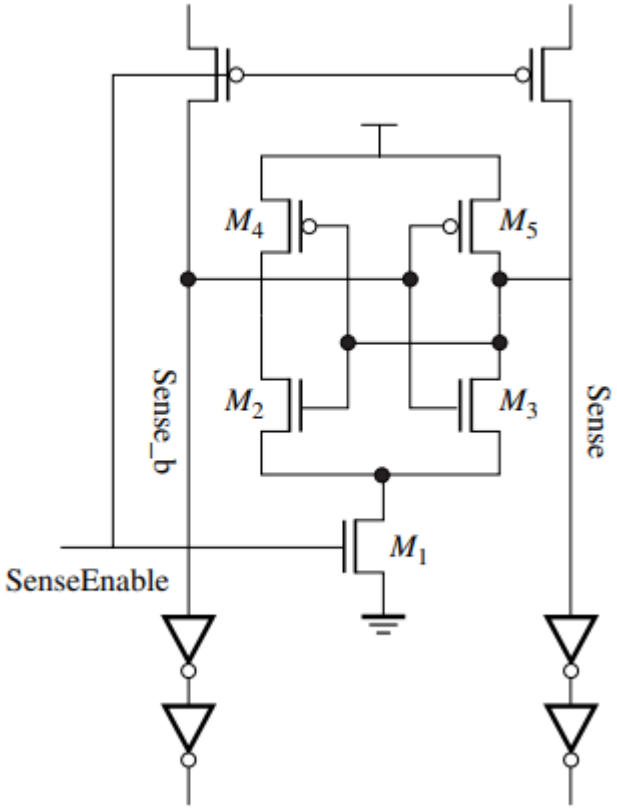
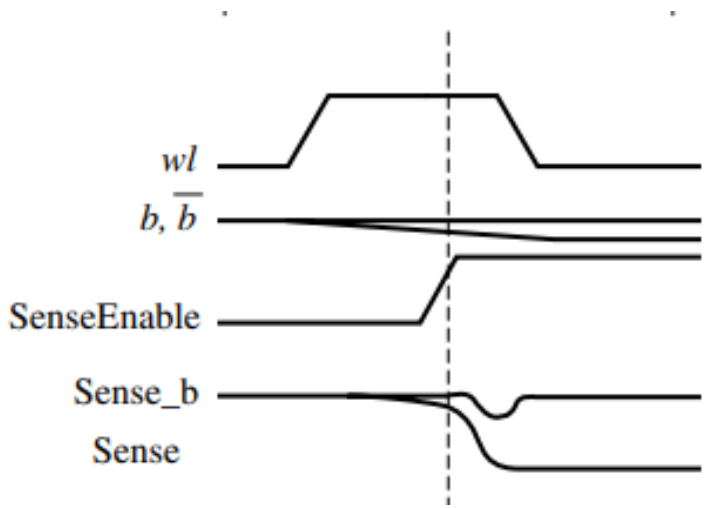
Sense Amplifier

- Option-2: Latch based amplifier (positive-feedback)
  - Critical that SenseEnable is fired at the right moment
  - If SenseEnable fired early: The latch will flip in a different direction due to noise
  - If SenseEnable fired late: unnecessary read delay (slower memory)



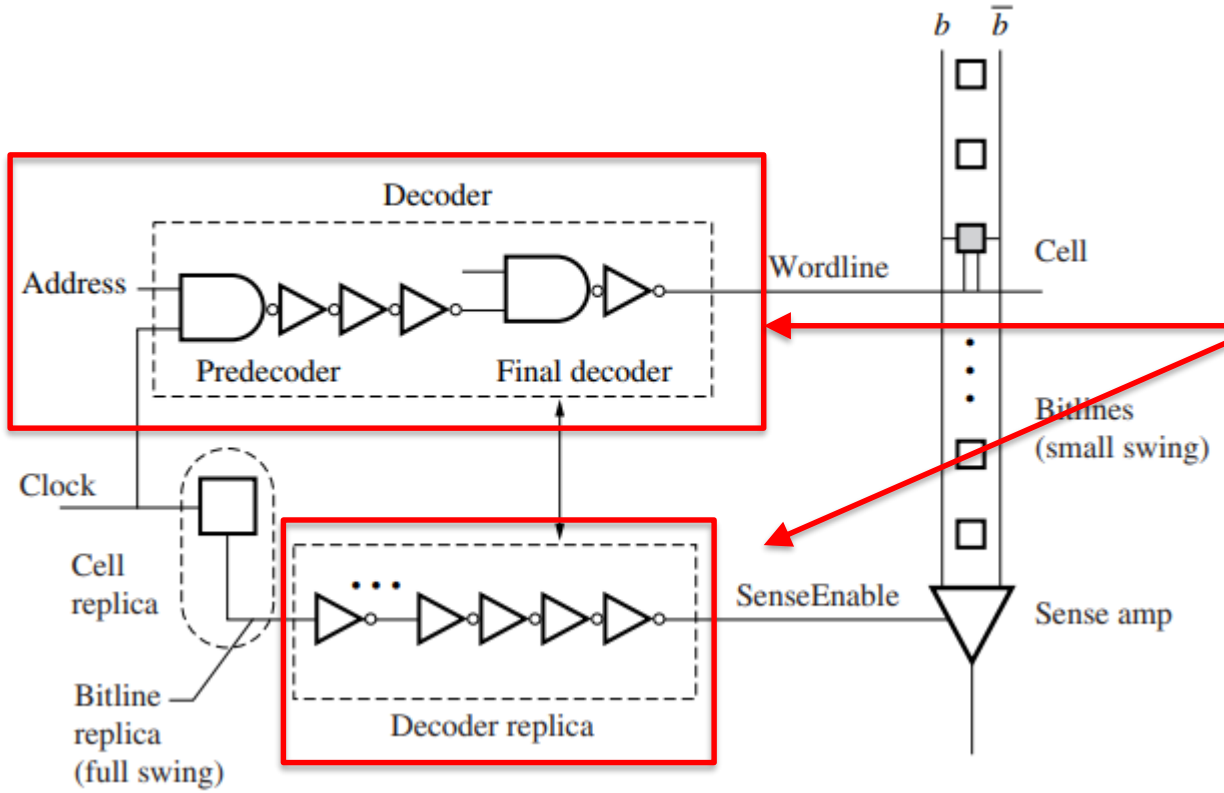


Sense Amplifier

- Option-2: Latch based amplifier (positive-feedback)
  - Critical that SenseEnable is fired at the right moment
  - The fabrication process corner (Transistors faster or slower post fabrication) – recall our discussion on the Process-Voltage-Temperature (PVT) corners in .lib
  - All signals associated with read must internally track the change in process !!
  - i.e., say the MOSFETs are slower post fabrication → row decoder circuits are slower than expected → WL is fired later than expected → the sense amplifier input might not have enough to amplify → sense amplifier enable must also be delayed
  - Similar effects can take place if the individual bit cell itself is slower or faster!
  - Therefore, while generating all control signals (WL, SenseEnable, etc.), we must design a process **dependant** circuit

Replica Decoder

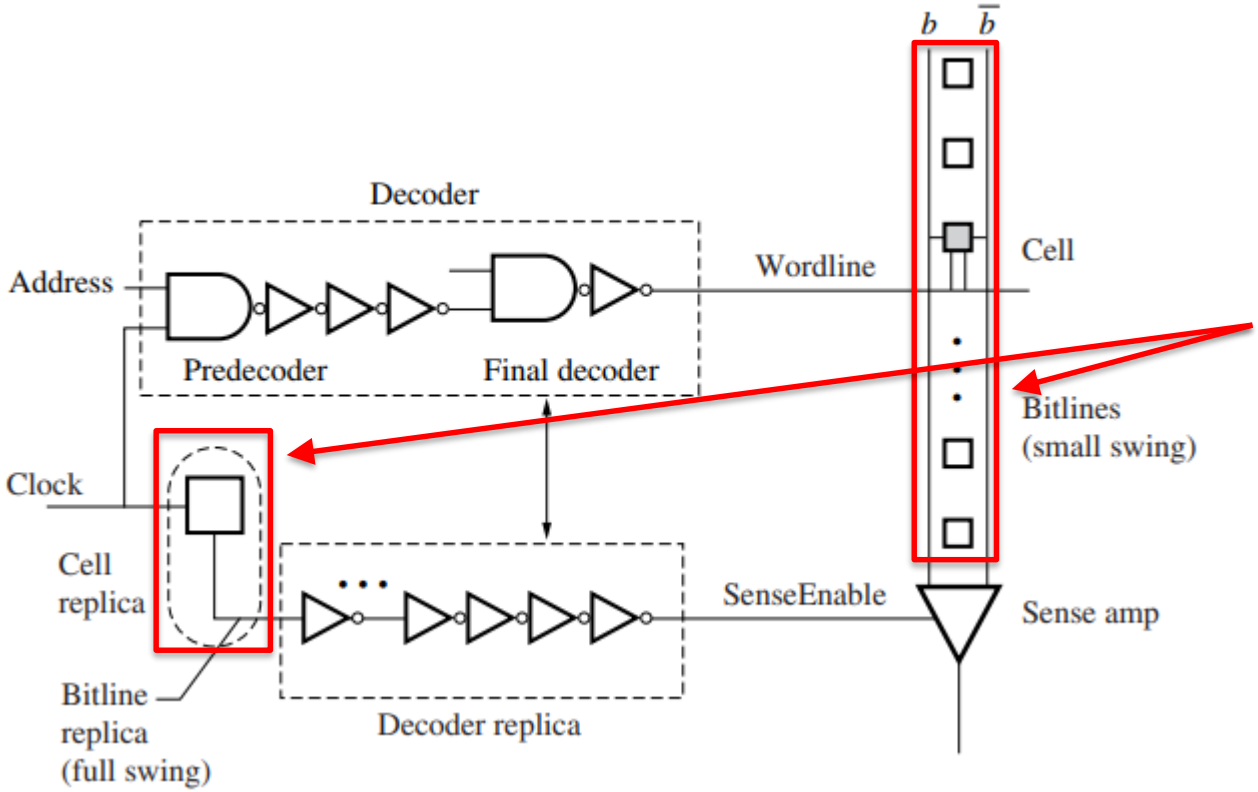
- Process variation handled through a replica decoder circuit
  - A replica of one path in the address decoder



SenseEnable delay tracks the WL decoder delay due to process variation

REPLICA BIT-CELL

- Process variation handled through a replica decoder circuit
  - A replica of one bit-cell

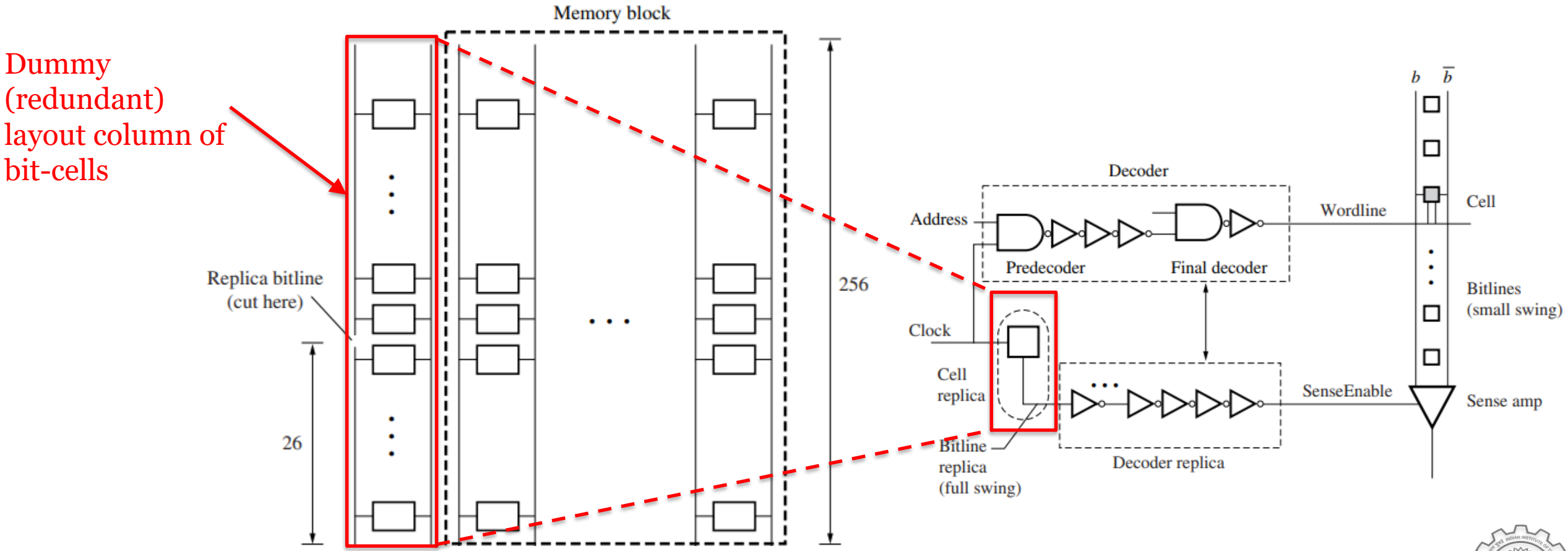


SenseEnable delay tracks the bit-cell delay due to process variation

- However, note that the replica of the bit-cell has to swing to logic levels but actual bit-cells only have to swing 100 mV ~ 200 mV depending on the SenseAmp → how to match timing in this case?

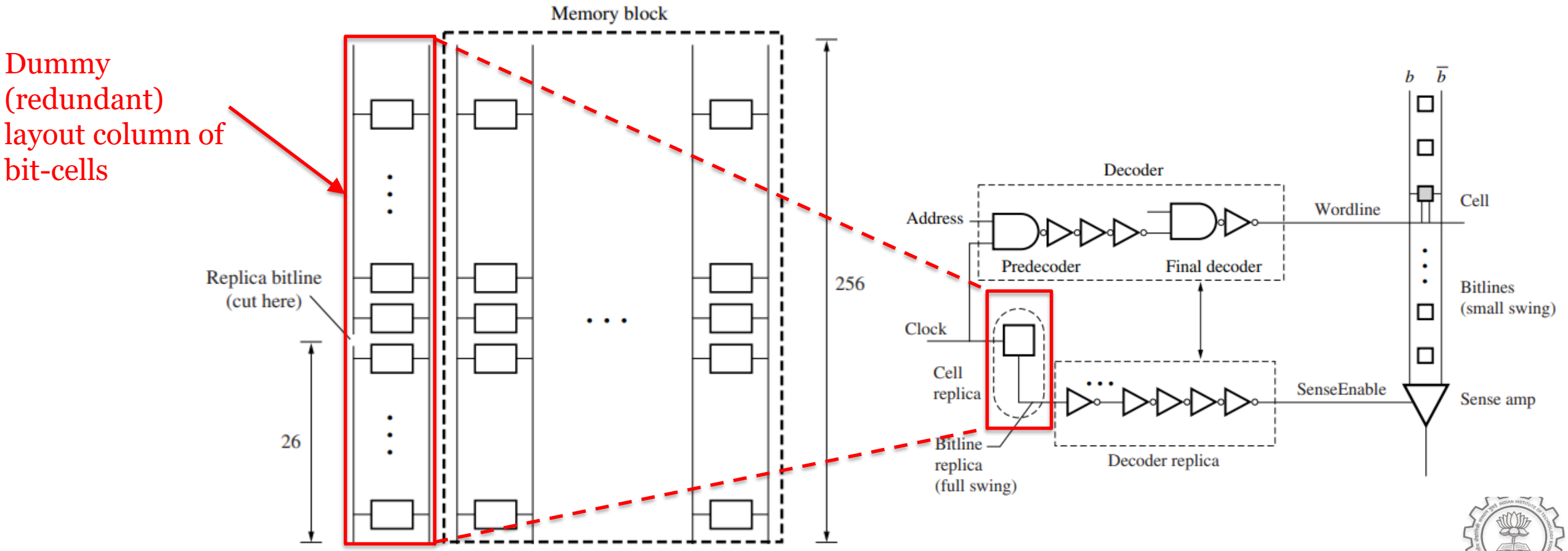
REPLICA BIT-CELL

- Process variation handled through a replica decoder circuit
  - Typically a redundant bit-cell column is placed in the array (left and right side of the layout) to account for edge effects in the fabrication

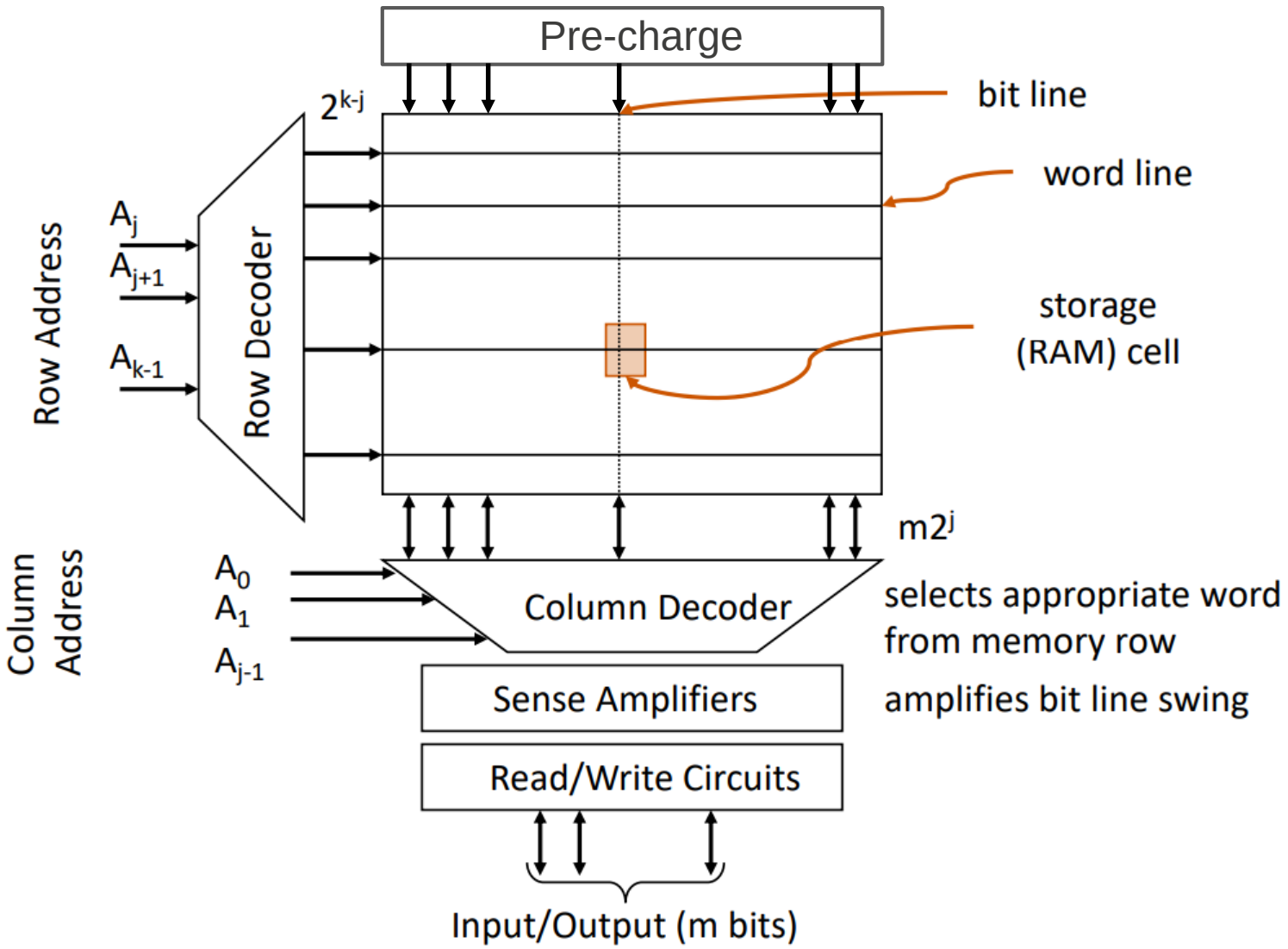


REPLICA BIT-CELL

- Process variation handled through a replica decoder circuit
  - Replica bit-line has to swing to logic levels but actual bit-cells only have to swing 100 mV ~ 200 mV depending on the SenseAmp → Cut the replica bitline (example below 26 cells) to produce logic levels with the same ΔT required for the main bitline to produce ΔV

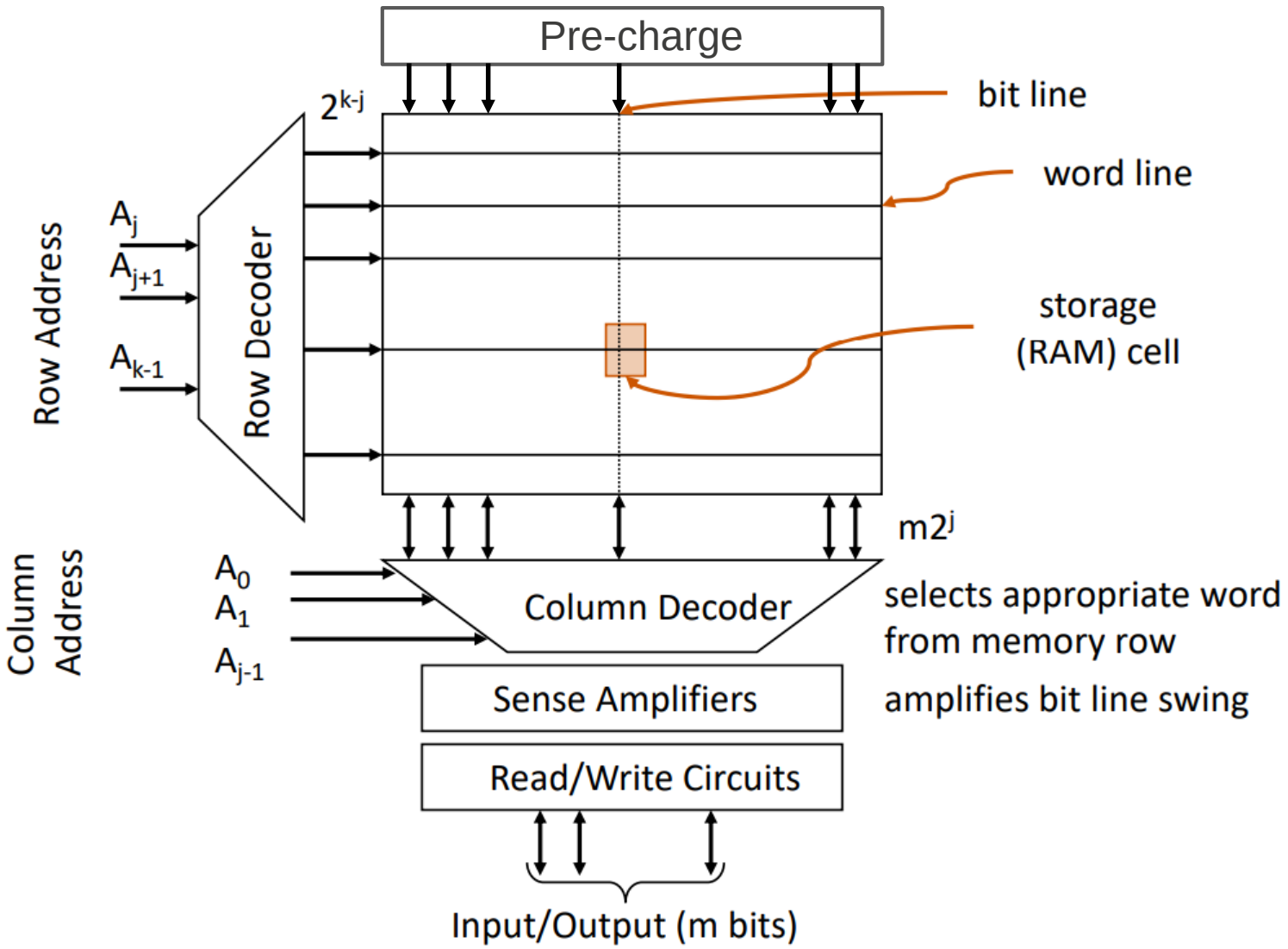


SRAM: Full Picture



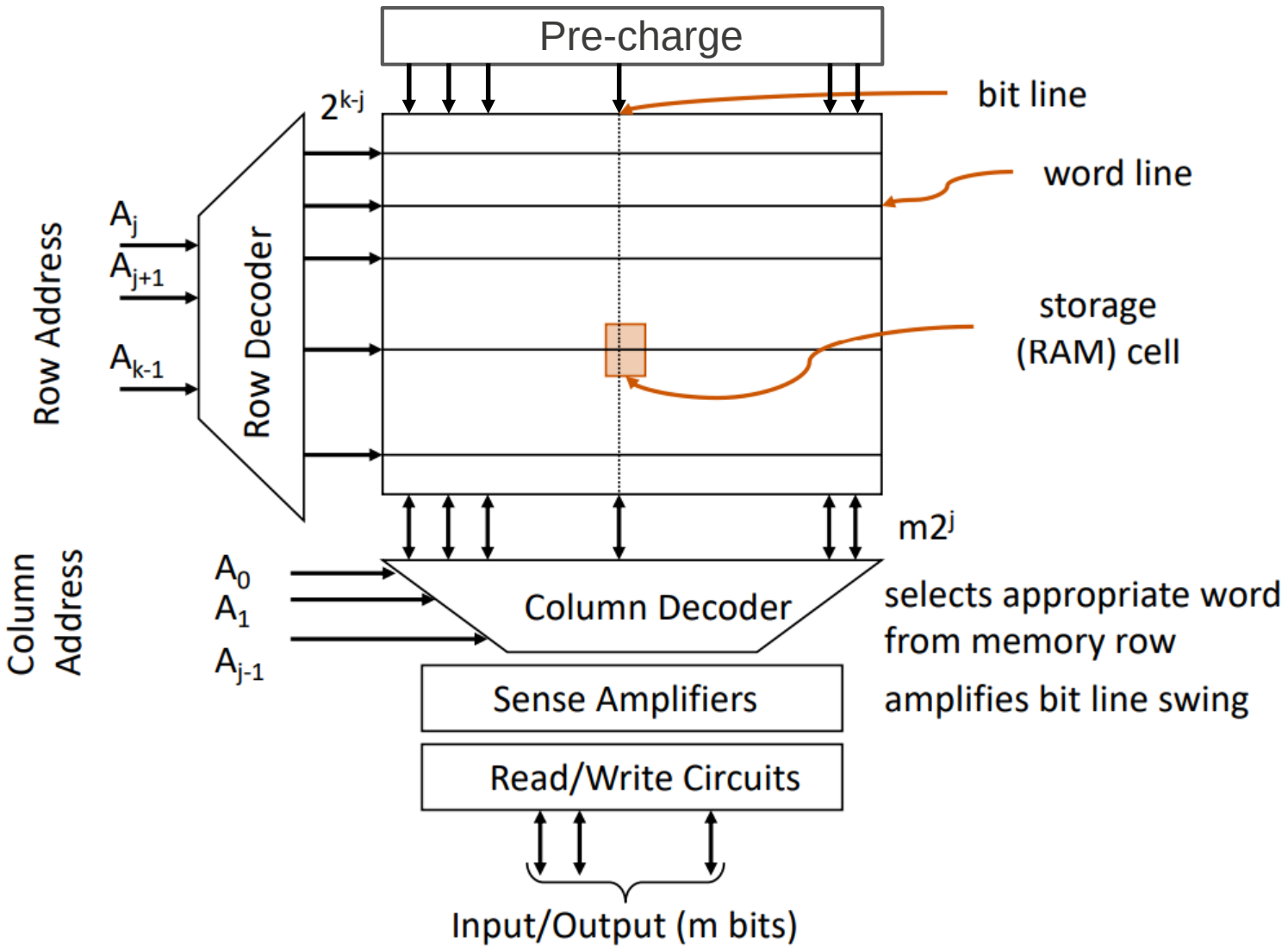
- Row Decoder: WL firing
- Col Decoder: Column Mux enable (Col)
- Precharge: to precharge bit-lines (PC)
- Sense Amplifiers: to read logic levels from bit lines (in a small time ΔT)
- Internally, need to generate SenseEnable signals (using replica)

SRAM: Full Picture



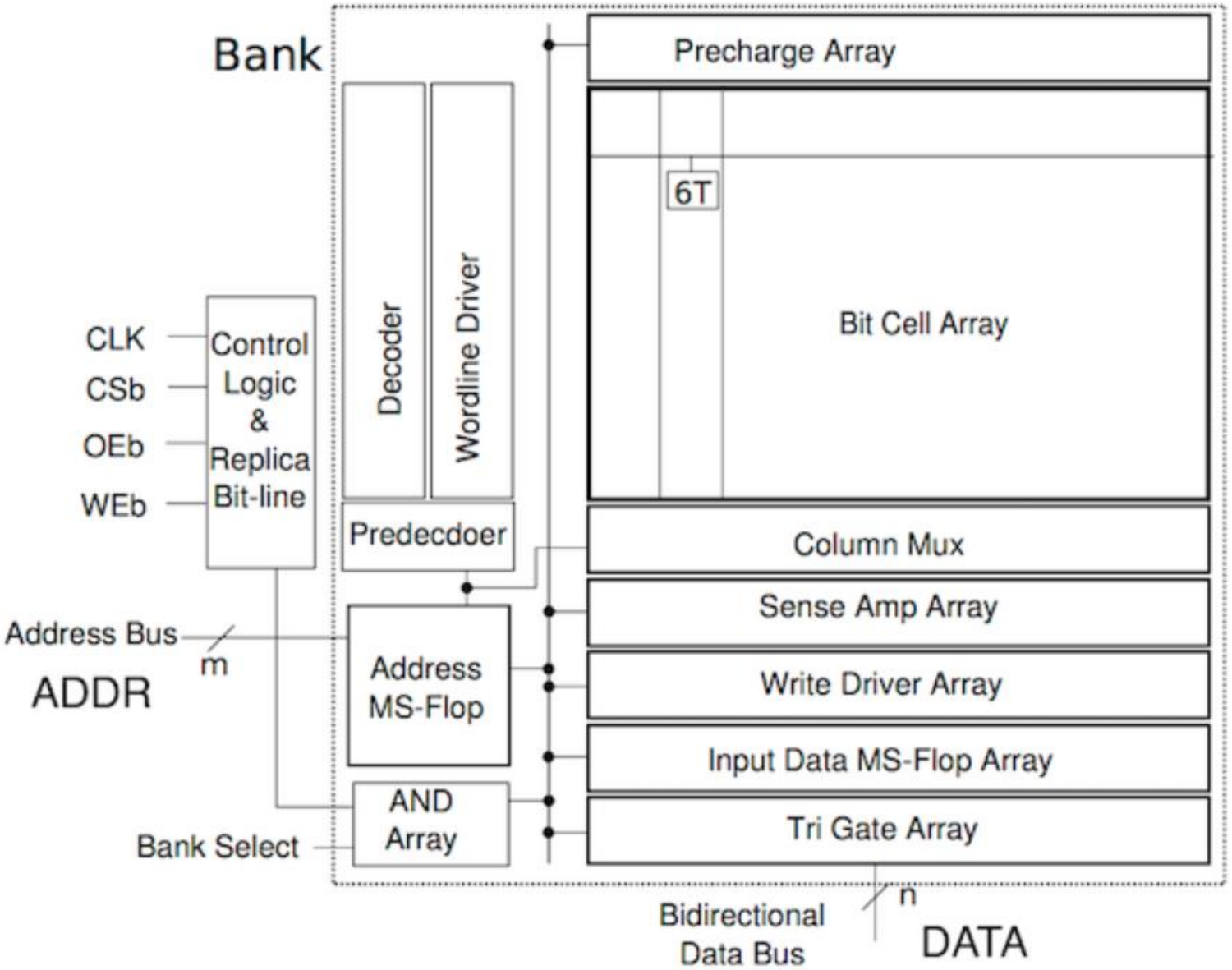
- **Write:**
- Apply address and Data to be written into registers
- Address decoder → WL and Col fires
- Appropriate BL and BLb are tied to VDD/GND
- Write ensured due to bit-cell sizing
- Disable WL, COL signals → operation done

SRAM: Full Picture



- **Read:**
- Pre-charge all BL & BLb
- Apply address
- Address decoder → WL fires
- Corresponding BL and BLb start generating ΔV in ΔT
- COL mux and SenseEnable fires
- SenseAmplifier amplifies and puts data into output register
- Remove all signals → operation done

EXAMPLE TYPICAL SRAM: FULL PICTURE



- CLK
- CSb: Chip Select (active-low)
- OEb: Output Enable (active-low)
- WEb: Write Enable (active-low)
- ADDR: input bus
- DATA: In/Out bus

EXAMPLE TYPICAL SRAM: LAYOUT