EE671: VLSI Design
Autumn 2024-25
Lecture-1

Laxmeesha Somappa

Department of Electrical Engineering

IIT Bombay

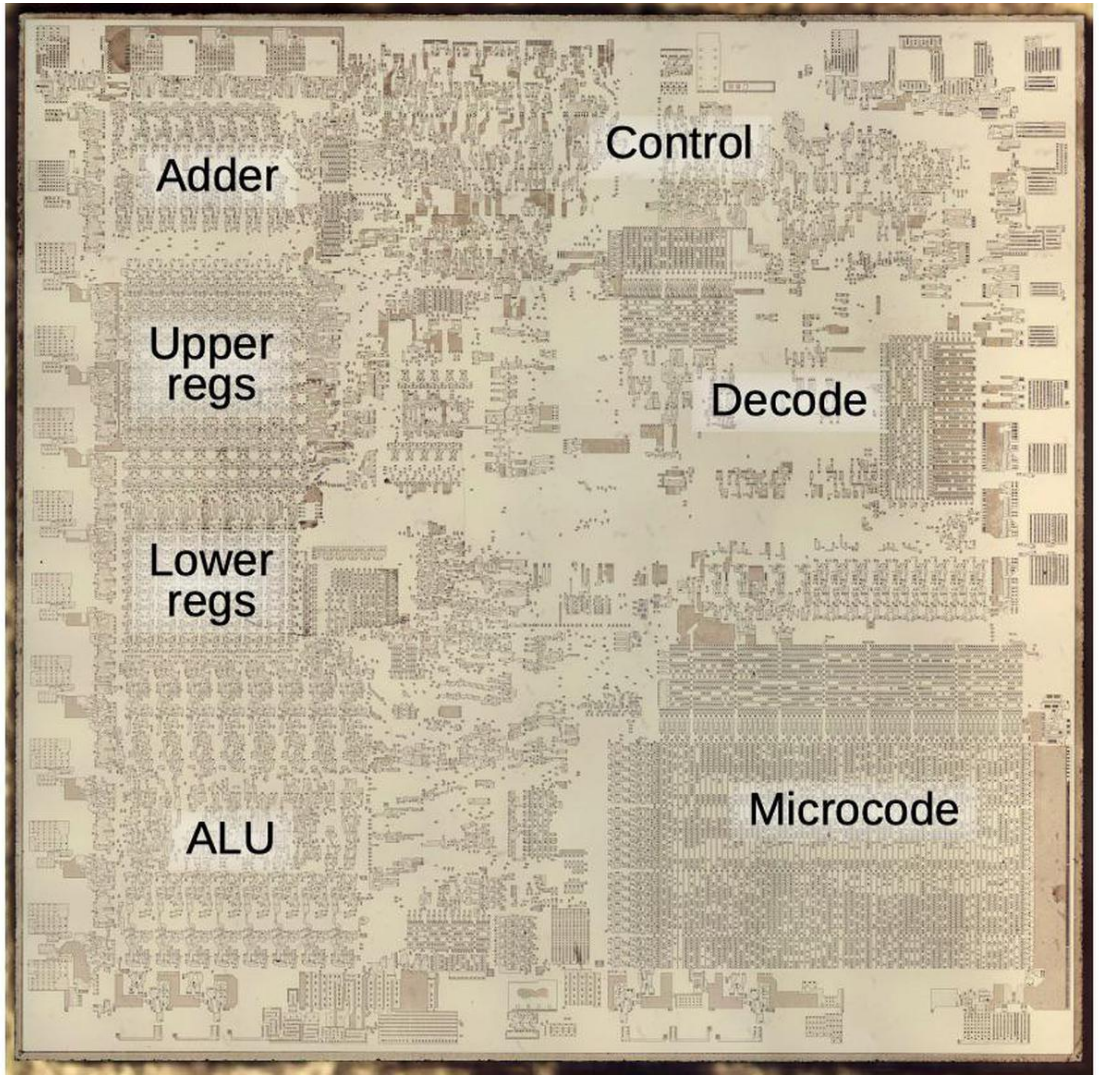
laxmeesha@ee.iitb.ac.in

OVERVIEW OF CHIP FABRICATION (COURTESY:BRANCH EDUCATION YOUTUBE)

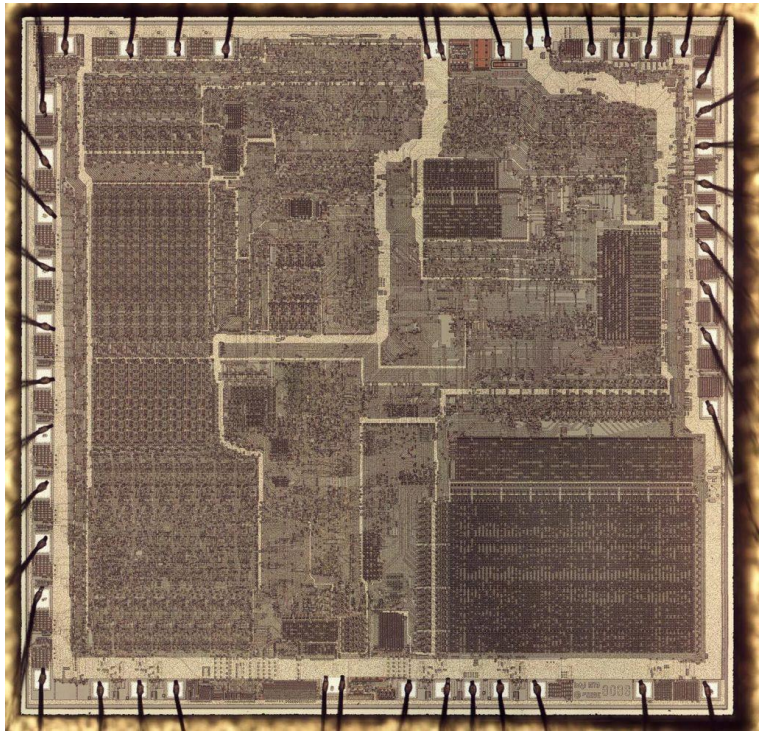
Click to the Video on Chip Fabrication

laxmeesha@ee.iitb.ac.in

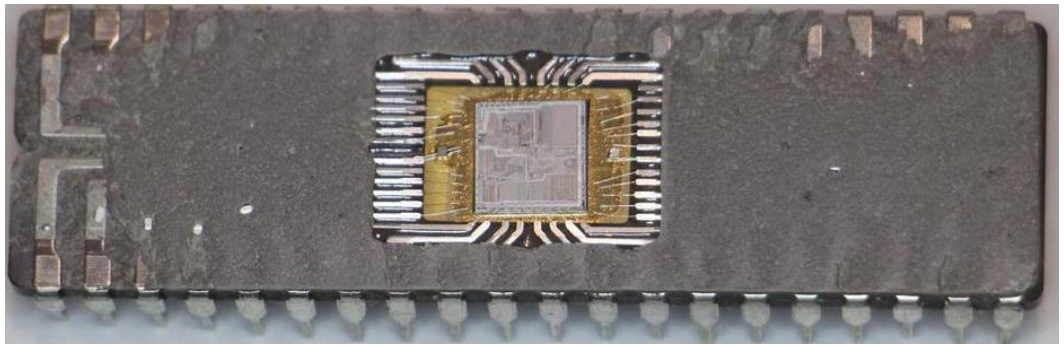
Intel 8086



8086 IC/Chip/Die



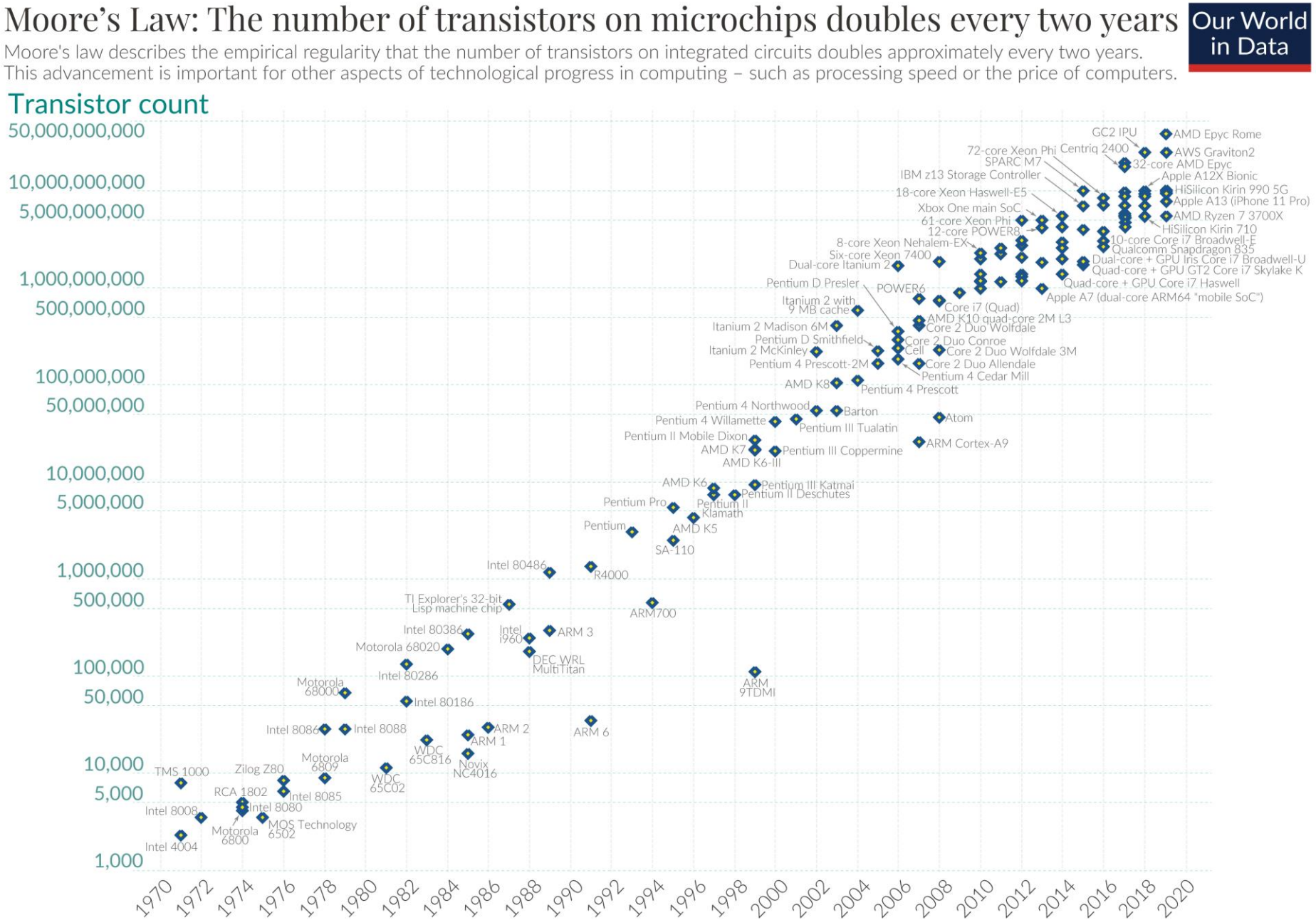
Bondwires on PADs



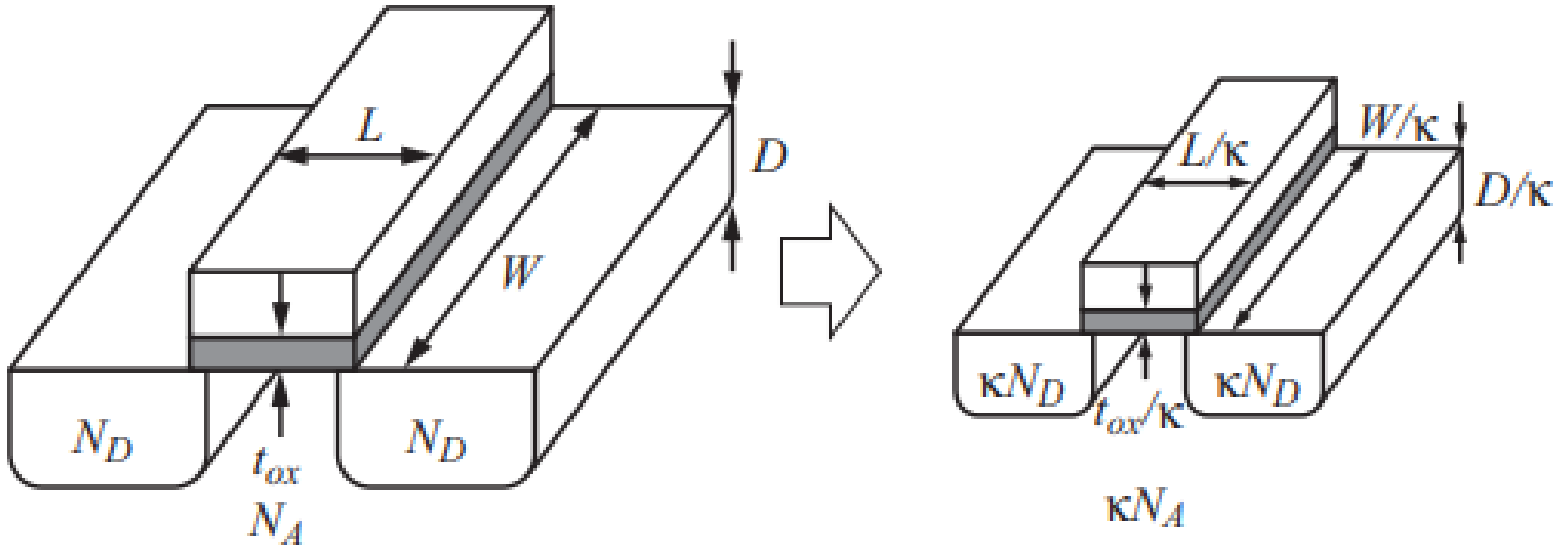
40 pin Dual-Inline Package (DIP)

laxmeesha@ee.iitb.ac.in

TRANSISTOR SCALING (MOORE'S LAW)



TRANSISTOR SCALING



- W: MOS Width, L: MOS Length (design choice)
- W_{min}: Minimum MOS Width, L_{min}: Minimum MOS Length
- t_{ox}: Oxide thickness (fixed for a given technology)
- ND: Doping concentration (fixed for a given technology)
- κ: Scaling factor (from one technology to another)

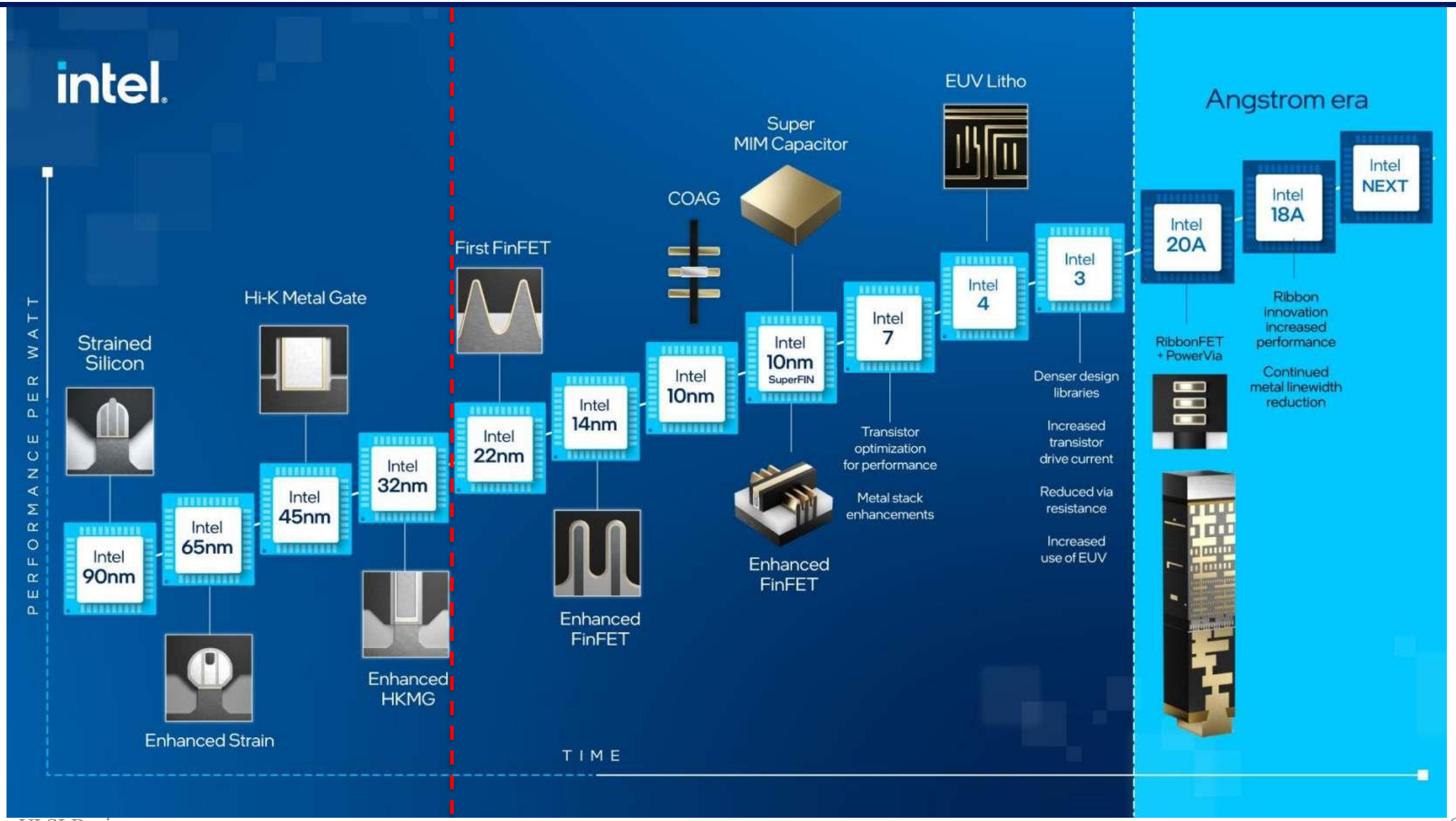
TRANSISTOR SCALING

- What are the benefits in technology scaling?
  - Transistors length becomes smaller → Faster
  - Circuits get Smaller & Faster
  - More transistors fit in a chip (same area)
  - Double advantage in performance: Speed and Density (increased functionality)

- If all dimensions (length, width of MOS) scale by a factor "κ"
  - Area shrinks by a factor κ^2
  - $\kappa = \sqrt{2}$, Area shrinks by half (remember Moore's law)
  - The dimension/feature size is called a "Technology node"
  - Eg: 180nm → 130nm → 90nm → 65 nm → 45nm etc.

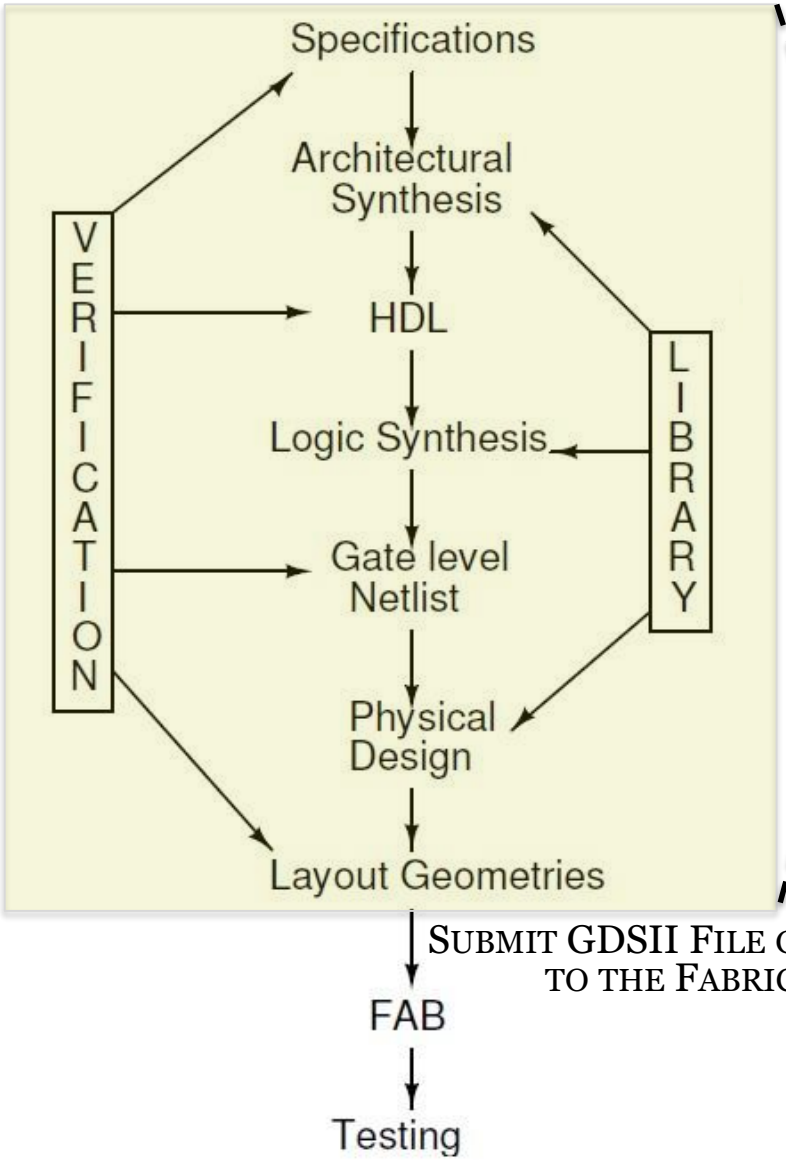
laxmeesha@ee.iitb.ac.in

TRANSISTOR SCALING (LOOKING AHEAD)

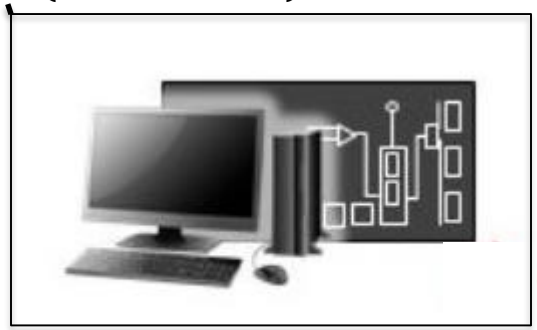


COURTESY: INTEL

BRIEF OVERVIEW OF VLSI DIGITAL DESIGN

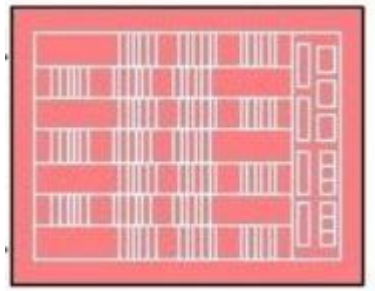


DESIGN CYCLE: DONE USING SOFTWARES (CAD TOOLS) ON COMPUTERS/SERVERS



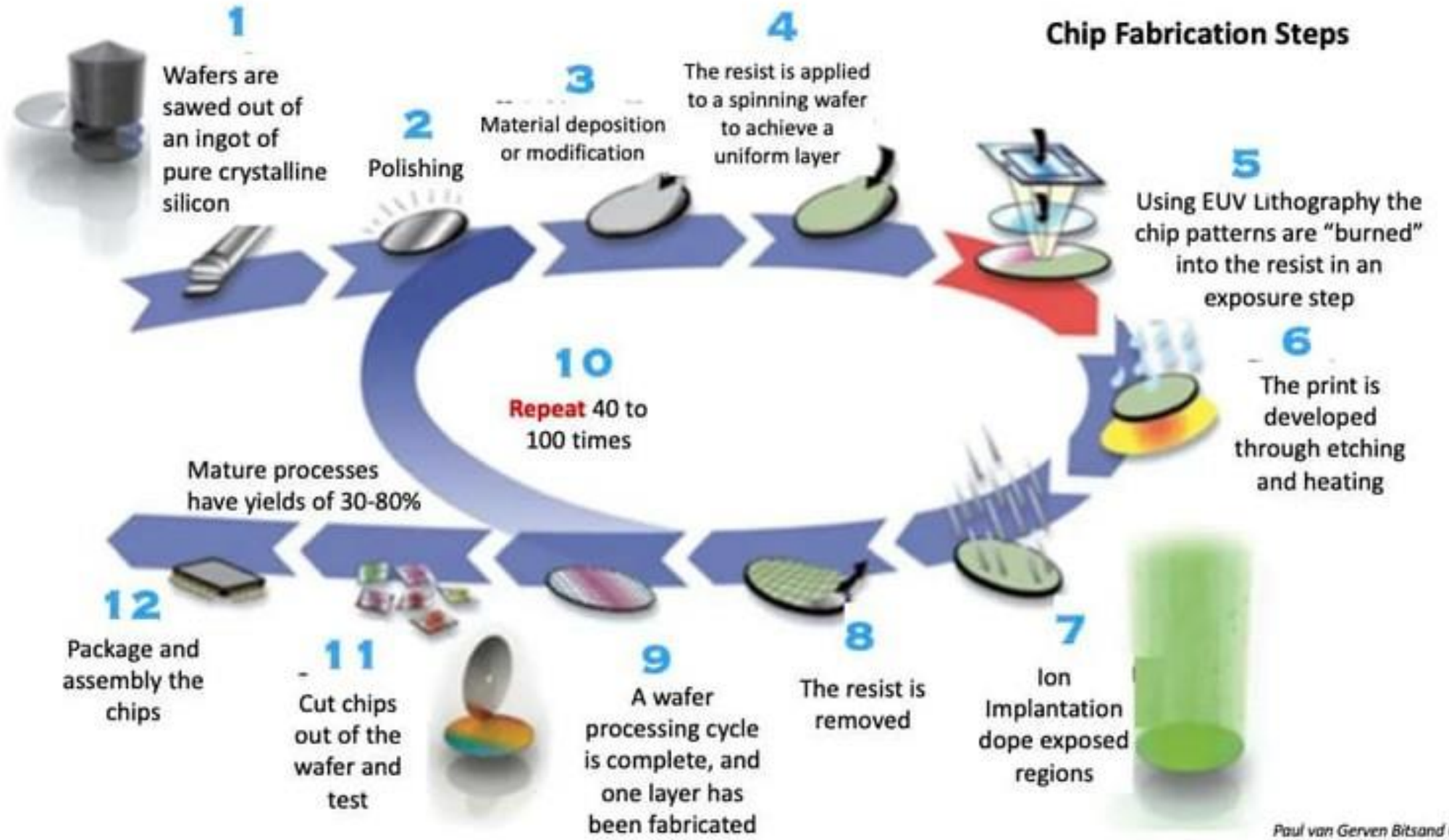
SUBMIT GDSII FILE GENERATED FROM TOOL TO THE FABRICATION FACILITY

MASKS GENERATED FROM GDSII FOR FABRICATION. THESE MASKS WILL BE USED FOR LITHOGRAPHY IN THE FAB



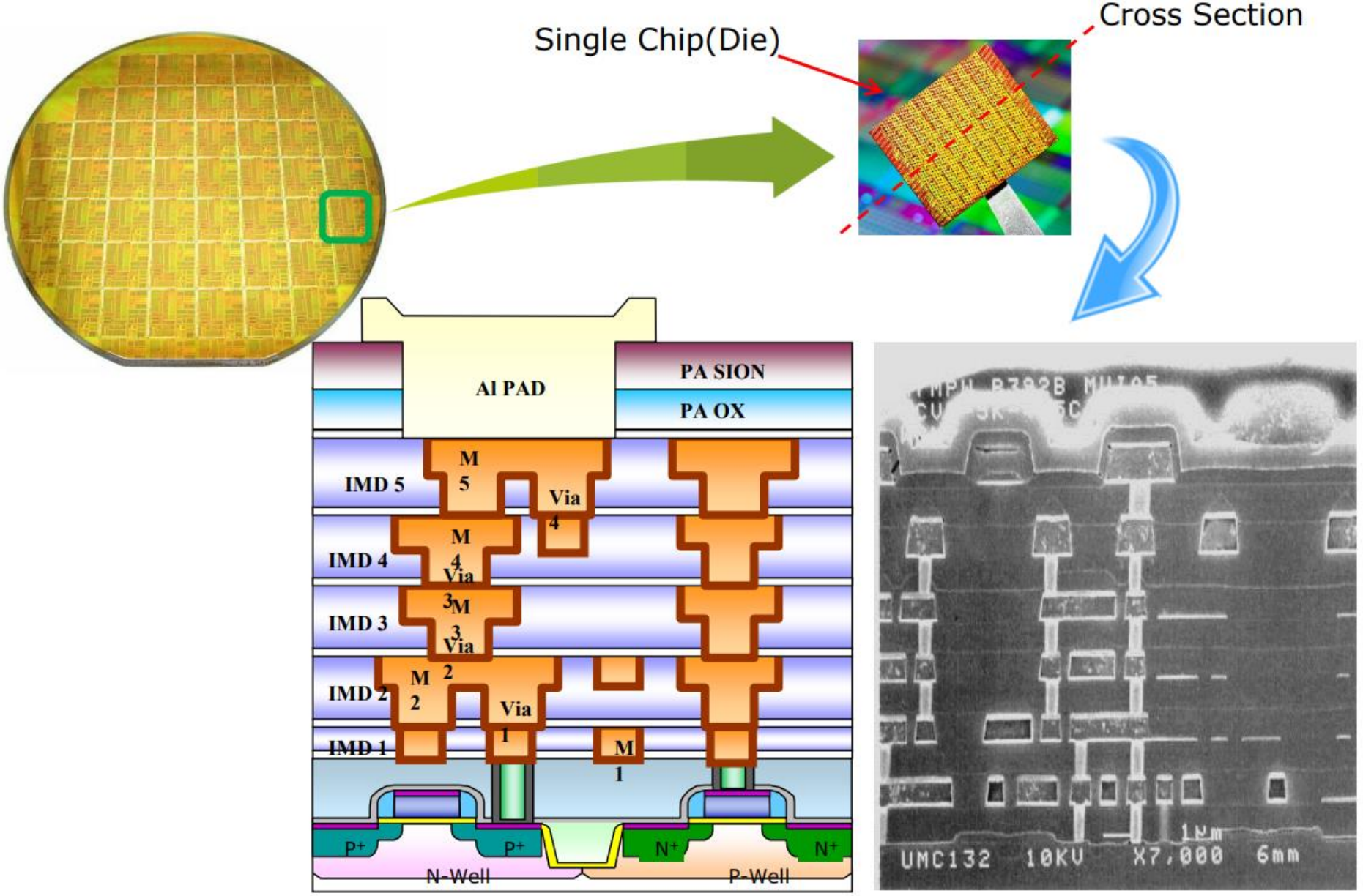
BRIEF OVERVIEW OF VLSI DIGITAL DESIGN: FAB

FAB STEPS COVERED IN EE669: VLSI TECHNOLOGY



COURTESY: BITS&CHIPS

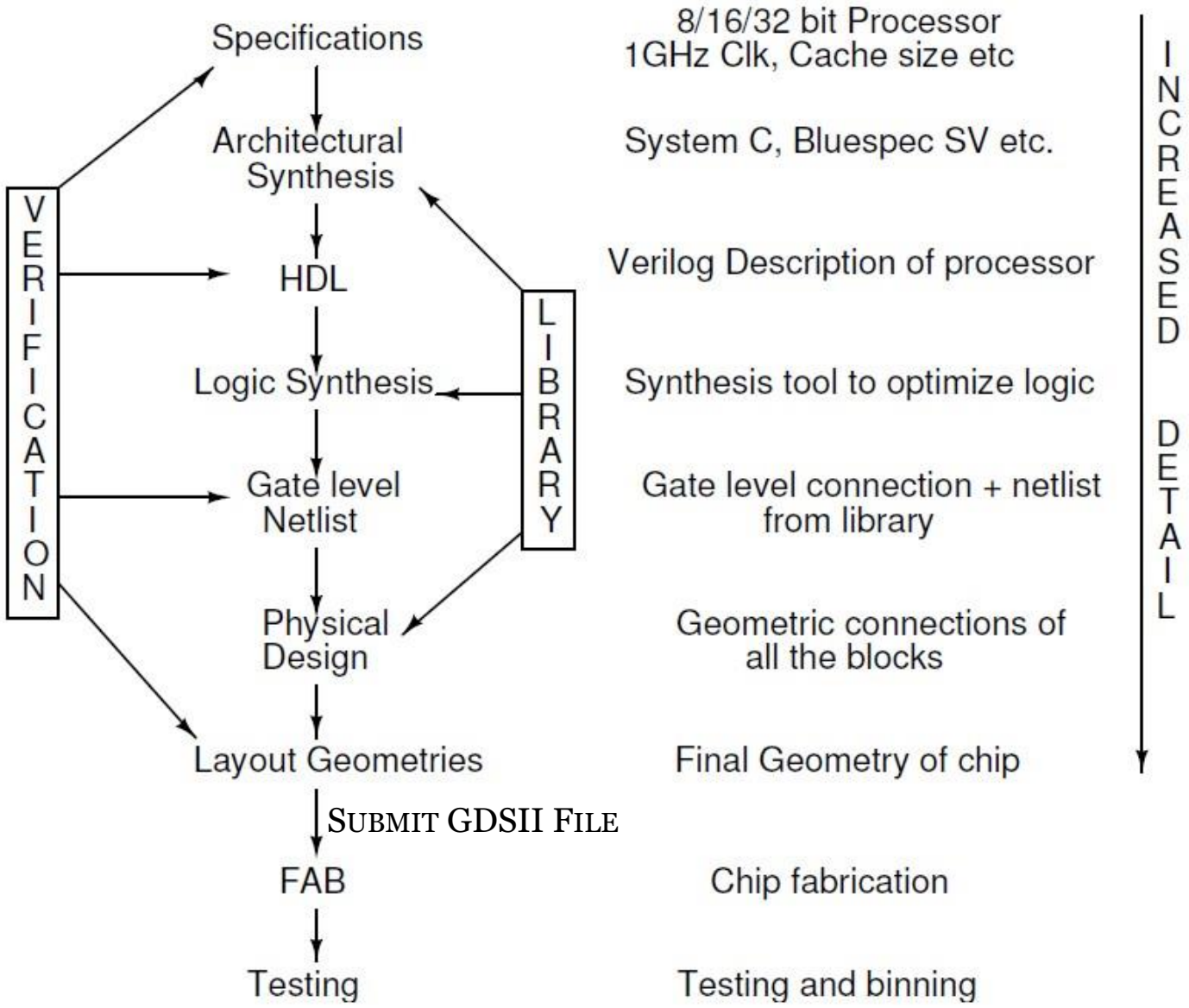
BRIEF OVERVIEW OF VLSI DIGITAL DESIGN: EXAMPLE DIE



COURTESY: INFENEON

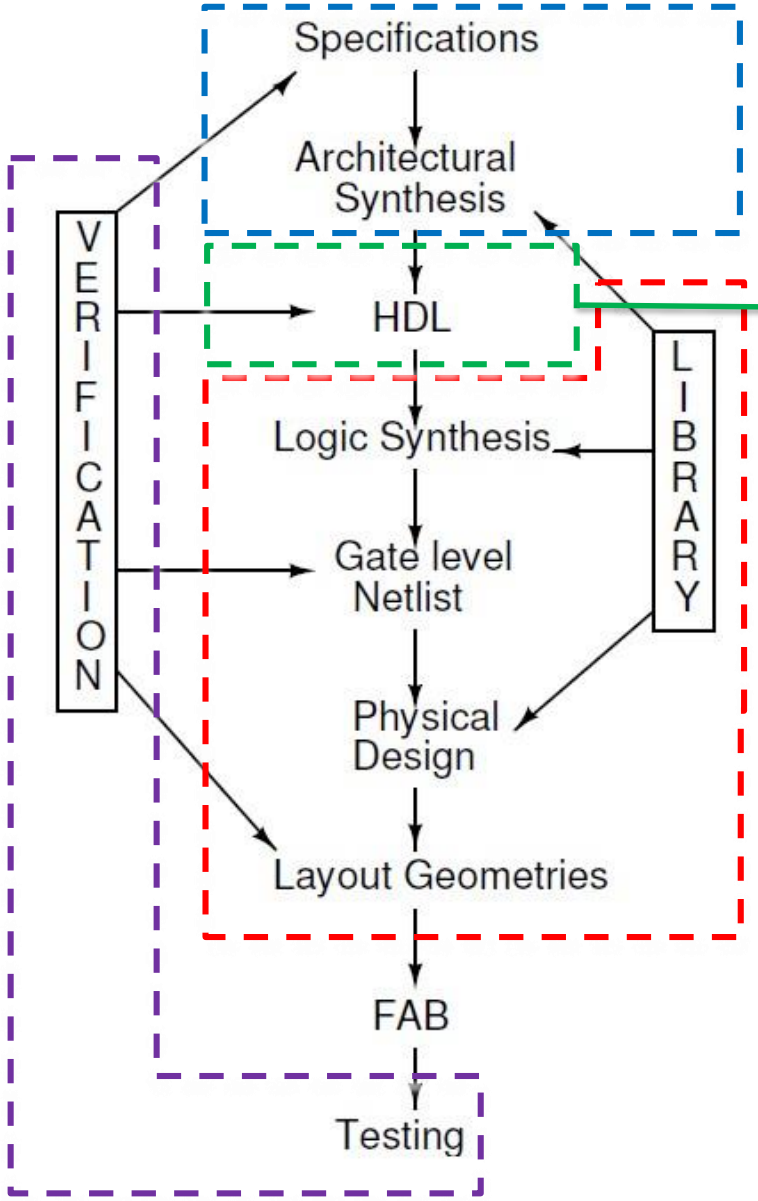
laxmeesha@ee.iitb.ac.in

BRIEF OVERVIEW OF VLSI DIGITAL DESIGN



COURTESY: INTEL

WHAT ARE WE LEARNING IN THIS COURSE?



EE739: PROCESSOR DESIGN
EE789: ALGORITHMIC DESIGN OF DIGITAL SYSTEMS

EE721: HARDWARE DESCRIPTION LANGUAGES

EE709:TESTING & VERIFICATION

EE671 – THIS COURSE!
PRE-MIDESM: LIBRARY DEVELOPMENT
POST-MIDSEM: RTL TO FAB
COURSE WILL NOT COVER FPGA DESIGN – THIS WILL BE TAKEN UP IN EE705 (VLSI DESIGN LAB)

COURTESY: INTEL