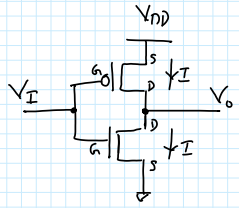
Lecture - 5

Recall the NMOS & PMOS I-V curve from the previous lecture.

* For the inverter circuit shown below,



For the NMOS $V_{DS,N} = V_o$

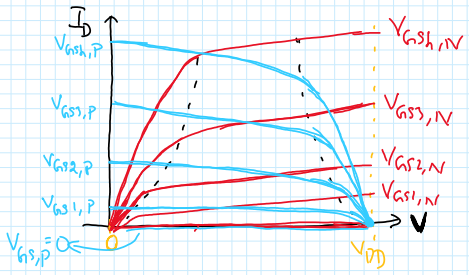
For the PMOS $V_{SD,P} = V_{DD} - V_o$

* To transform the I-V curve of both NMOS & PMOS to a common axis (i.e I_D vs V_o instead of V_{DS}), observe the following :-

→ $V_o = V_{DS,N}$

→ $V_o = V_{SD,P} + V_{DD}$ → Add V_{DD} to the I-V curve of PMOS

∴ The I-V curve for the inverter will be :-



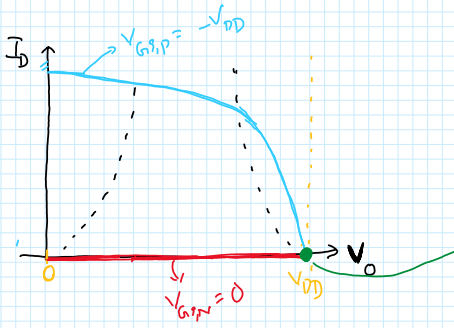
— curve is for an NMOS device with $V_{GSh,N} > V_{GS3,N} > V_{GS2,N} > V_{GS1,N} > V_{TN} > 0$

— curve is for a PMOS device with $V_{GSh,N} < V_{GS3,N} < V_{GS2,N} < V_{GS1,N} < -V_{TP} <$ or $V_{SGh,N} > V_{SG,3N} > V_{SG2,N} > V_{SG1,N} > |V_{tp}| > 0$.

— × — × —

* To determine the operating regions of the inverter, we need to see when the I-V of the PMOS & NMOS intersect (i.e finding solution for $f_1(V) = f_2(V)$)

Case I : $V_I = 0$



when $V_I = 0$:-

$V_{GS,N} = 0$ (cut-off) NMOS & $V_{SG,P} = V_{DD}$ (ON & maximum V_{SG}) PMOS

→ * The intersection of these two curves & hence the solution

⇒ The solution is $V_o = V_{DD}$

* From this I-V curve, we also notice that NMOS is in cut off and PMOS is in linear region.

* We can also prove this from the conditions

NMOS

$V_{GS,N} = 0 < V_{TN}$

∴ NMOS in cut-off

PMOS

$V_{SG,P} = V_{DD} > |V_{TP}|$ ∴ ON

↳ $V_{SD,P} \geq V_{SG} - |V_{TP}|$ for saturation

$V_{GS,N} = 0 < V_{TN}$

- NMOS in cut-off

$V_{SG,P} = V_{DD} > |V_{TP}|$ ∴ ON

↳ $V_{SD,P} \geq V_{SG,P} - |V_{TP}|$ for saturation

$V_S - V_D \geq V_S - V_G - |V_{TP}|$

$V_D \leq V_G + |V_{TP}|$

$V_{DD} \leq 0 + |V_{TP}|$ → Not true

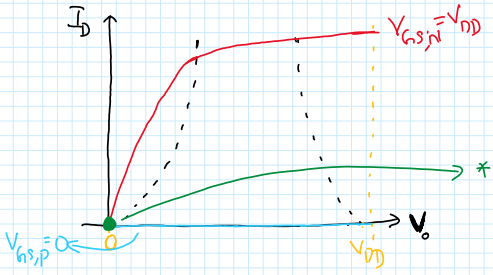
- PMOS is in linear region

Case II: $V_I = V_{DD}$

When $V_I = V_{DD}$:-

$V_{GS,N} = V_{DD}$ (ON, & maximum V_{GS}) — NMOS

$V_{SG,P} = V_{DD} - V_{DD} = 0$ (OFF) — PMOS



* The intersection of these two curves & hence the solution

⇒ The solution is $V_o = 0$ V

* From this I-V curve, we also notice that PMOS is in cut off and NMOS is in linear region.

* We can also prove this from the conditions

NMOS

$V_{GS,N} = V_{DD} > V_{TN}$ (ON)

↳ $V_{DS,N} \geq V_{GS,N} - V_{TN}$ for saturation.

$0 \geq V_{DD} - V_{TN}$ → Not true

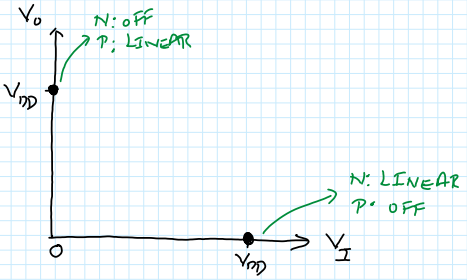
- NMOS is in linear region

PMOS

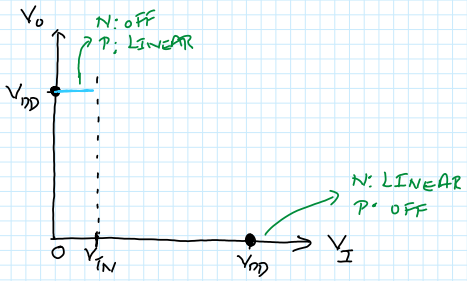
$V_{SG,P} = 0 < |V_{TP}|$

— × —

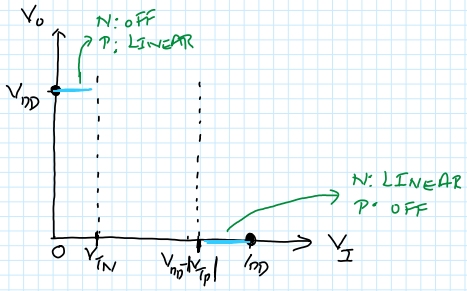
* Based on case-I & case-II ; we can draw the inverter transfer curve (V_I Vs V_o)



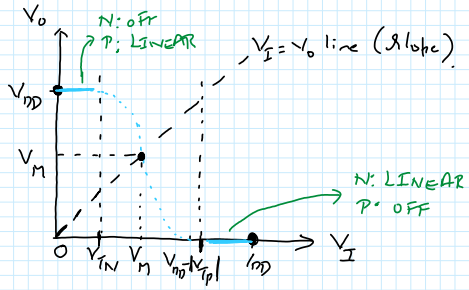
* As we increase V_I till V_{TN}, the NMOS will stay in cut-off & PMOS in linear (similar to case-I)



* Symmetrically, as V_I is reduced from V_{DD} to $V_{nD} - |V_{Tp}|$, the PMOS will stay in cut-off & NMOS will be in linear region (similar to case II)

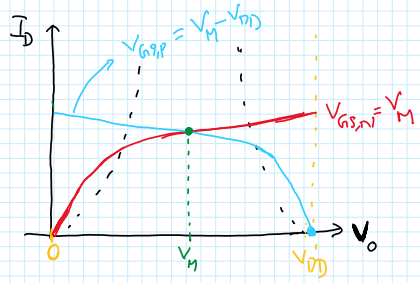


* The transfer curve will go from $V_o = V_{nD}$ to 0 as V_I goes from 0 to V_{DD}. In the process, it will intersect a line $V_I = V_o$ (i.e straight line with slope = 1)



* At the intersection point, $V_I = V_o = V_M$. Lets consider this as case III

Case III : $V_I = V_o = V_M$



When $V_I = V_o = V_M$:-

* Both PMOS & NMOS are ON & the two MOSFETs are in saturation (as shown in the left figure)
* The intersection point and the solution is $V_o = V_M$

NMOS

$V_{DS} \geq V_{GS} - V_{TN}$ for saturation

$V_M - 0 \geq V_M - 0 - V_{TN}$

$V_M \geq V_M - V_{TN}$ (true)

∴ NMOS is in saturation.

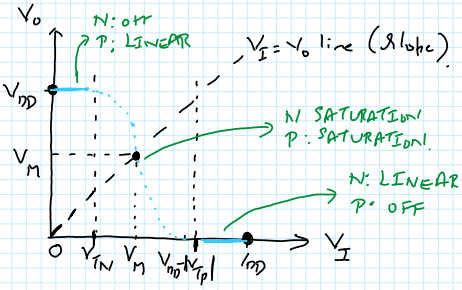
PMOS

$V_{SD} \geq V_{SG} - |V_{Tp}|$ for saturation

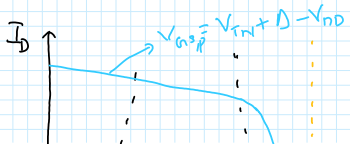
$V_{DD} - V_M \geq V_{DD} - V_M - |V_{Tp}|$

$V_M \leq V_M + |V_{Tp}|$ (true)

∴ PMOS is in saturation.



Case IV. $V_I > V_{TN}$ & $V_I < V_M$.



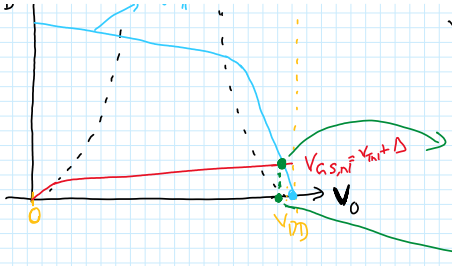
When $V_I = V_{TN} + \Delta$ - (Δ is small incremental voltage)

$V_{GS,N} = V_{TN} + \Delta > V_{TN}$.

(ON)

$V_{SG,P} = V_{DD} - V_{TN} - \Delta > |V_{Tp}|$

(ON)



$V_{GS,N} = V_{in} + \Delta > V_{TN}$ (ON) NMOS

$V_{SG,P} = V_{DD} - V_{TN} - \Delta > |V_{TP}|$ (ON) PMOS

* The intersection of these two curves & hence the solution, V_o is slightly below V_{DD}

* From the I-V curve, NMOS is in Saturation & PMOS is in linear region.

NMOS

$V_{DS} \geq V_{GS} - V_{TN}$ for saturation.

$V_o \geq V_I - V_{TN}$

$V_{DD} - \Delta_1 \geq \Delta_2 - V_{TN}$

$V_{DD} \geq \Delta_1 + \Delta_2 - V_{TN}$ (true)

∴ NMOS is in saturation

PMOS

$V_{SD} \geq V_{SG} - |V_{TP}|$

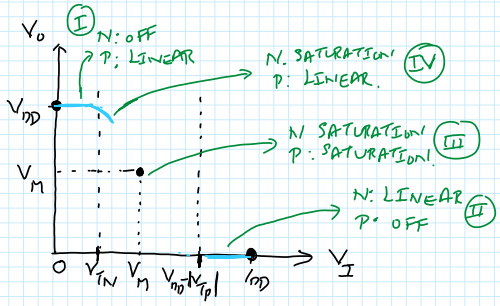
$V_{DD} - V_o \geq V_{DD} - V_I - |V_{TP}|$

$V_o \leq V_I + |V_{TP}|$

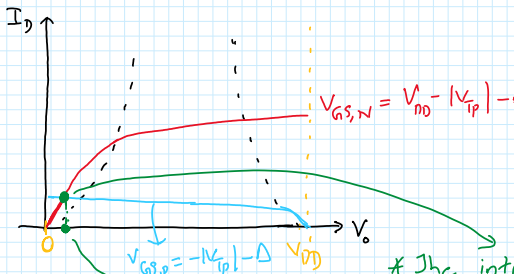
$V_{DD} - \Delta_1 \leq \Delta_2 + |V_{TP}|$

$V_{DD} \leq \Delta_1 + \Delta_2 + |V_{TP}|$ (False)

∴ PMOS is in linear region.



Case V: $V_I < V_{DD} - |V_{TP}| - \Delta$ & $V_I > V_M$



When $V_I = V_{DD} - |V_{TP}| - \Delta$ (Small incremental Voltage)

$V_{GS,N} = V_{DD} - |V_{TP}| - \Delta > V_{TN}$ (ON) NMOS

$V_{SG,P} = V_{DD} - (V_{DD} - |V_{TP}| - \Delta)$

$= |V_{TP}| + \Delta > |V_{TP}|$ (ON) PMOS

* The intersection of these two curves & hence the solution, V_o is slightly above 0

* From the I-V curve, NMOS is in linear & PMOS is in saturation region.

NMOS

$V_{DS} \geq V_{GS} - V_{TN}$ for saturation

$V_o \geq V_I - V_{TN}$

$\Delta_1 \geq V_{DD} - |V_{TP}| - \Delta_2 - V_{TN}$

$\Delta_1 \geq V_{DD} - (V_{TN} + |V_{TP}|) - \Delta_2$ (FALSE)

∴ NMOS is in Linear Region

PMOS

$V_{SD} \geq V_{SG} - |V_{TP}|$ for saturation

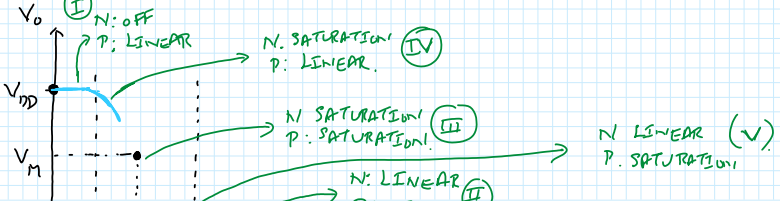
$V_{DD} - V_o \geq V_{DD} - V_I - |V_{TP}|$

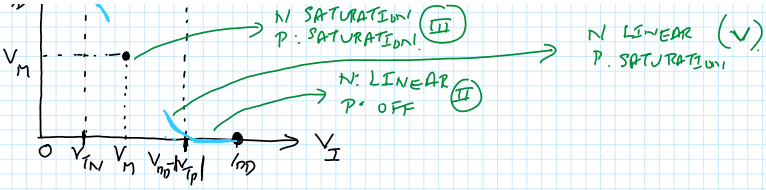
$V_o \leq V_I + |V_{TP}|$

$\Delta_1 \leq V_{DD} - |V_{TP}| - \Delta_2 + |V_{TP}|$

$\Delta_1 \leq V_{DD} - \Delta_2$ (true)

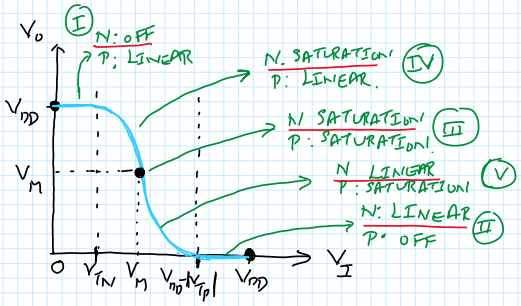
∴ PMOS is in Saturation.



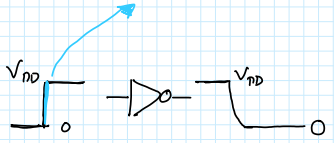


---

* Final transfer curve of an Inverter is -



* As V_I changes from 0 to V_{DD} } NMOS transitions from OFF → SATURATION → LINEAR
PMOS transitions from LINEAR → SATURATION → OFF



---

* Let's try to evaluate V_M (i.e the voltage @ which $V_I = V_O$)

* Recall that in case III ($V_I = V_O = V_M$), both NMOS & PMOS are in saturation.

$$I_{D,NMOS,SAT} = I_{D,PMOS,SAT} \quad \text{(ignoring channel length modulation)}$$

$$\frac{1}{2}\underbrace{\mu_n C_{ox}\left(\frac{W}{L}\right)_N}_{K_N}(V_{GS}-V_{TN})^2 = \frac{1}{2}\underbrace{\mu_p C_{ox}\left(\frac{W}{L}\right)_P}_{K_P}(V_{SG}-|V_{Tp}|)^2$$

$$K_N\left[V_M - V_{TN}\right]^2 = K_P\left[V_{DD} - V_M - |V_{Tp}|\right]^2$$

$$V_M - V_{TN} = \sqrt{\frac{K_P}{K_N}}\left[V_{DD} - V_M - |V_{Tp}|\right]$$

Define $\gamma = \sqrt{\frac{K_P}{K_N}}$

$$V_M - V_{TN} = \gamma\left[V_{DD} - V_M - |V_{Tp}|\right]$$

$$V_M[1+\gamma] = \gamma[V_{DD} - |V_{Tp}|] + V_{TN}$$

$$\boxed{V_M = \frac{V_{TN} + \gamma\left[V_{DD} - |V_{Tp}|\right]}{1+\gamma}}$$

* V_M (also called "Switching Voltage" or "Trip-point voltage" of an Inverter) is a function of V_{TN}, $|V_{Tp}|$, μ_n, μ_p, $\left(\frac{W}{L}\right)_N$ & $\left(\frac{W}{L}\right)_P$.

* The only design parameter (available for designers) is $\left(\frac{W}{L}\right)_N$ & $\left(\frac{W}{L}\right)_P$

* Consider the special case where $V_{TN} = |V_{Tp}|$ and $\gamma = 1$

$$V_M = \frac{V_{TN} + V_{DD} - V_{TN}}{2} = V_{DD}/2$$

$$V_M = \frac{V_{TN} + V_{DD} - |V_{TP}|}{2} = V_{DD}/2$$

i.e for a exactly symmetric inverter (switching voltage $V_M = V_{DD}/2$) $\beta = 1$ AND $V_{TN} = |V_{TP}|$.

$$\beta = 1 \Rightarrow K_n = K_p \Rightarrow \mu_n (W/L)_N = \mu_p (W/L)_P$$

$$\frac{(W/L)_P}{(W/L)_N} = \frac{\mu_n}{\mu_p}$$

* For same PMOS & NMOS channel length [usually L_{min}],

$$\frac{W_p}{W_N} = \frac{\mu_n}{\mu_p}$$

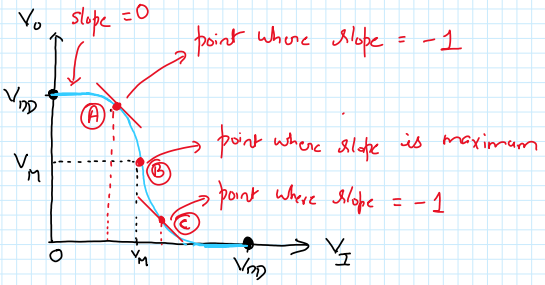
i.e the ratio of PMOS to NMOS width = ratio of electron to hole mobilities

* Typically $\mu_n = f \cdot \mu_p$ & $f = 2$ or 2.5 or 3.

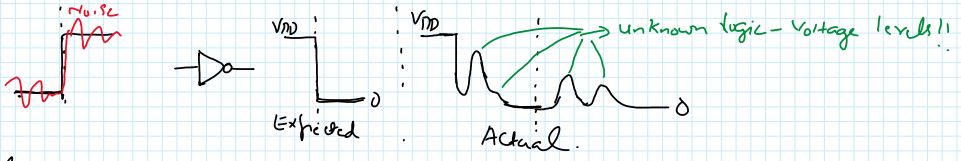
* Note that if $V_{TN} \neq |V_{TP}|$ (which is usually the case), $\frac{W_p}{W_N} \neq \frac{\mu_n}{\mu_p}$ for $V_M = V_{DD}/2$

— x — x — x —

* Lets go back to the transfer curve of the inverter.



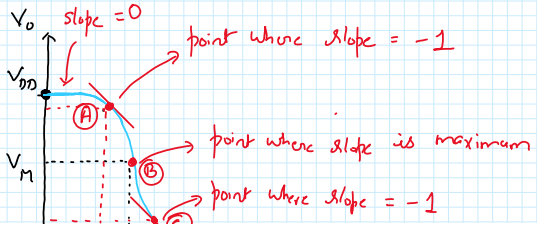
* The inverter's function is to operate as a digital switching logic without amplifying noise. Amplifying noise can change the logic level at the output

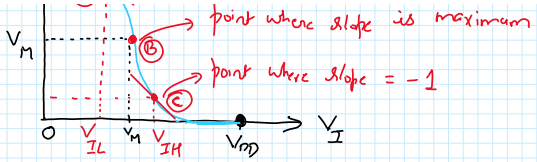


* For faithful operation, we need to define noise margins of the inverter (Max & Min inputs)

* Before Point (A) on the transfer curve, the magnitude of the slope is either 0 or < 1
  ⇒ No amplification happens (∵ slope corresponds to gain)

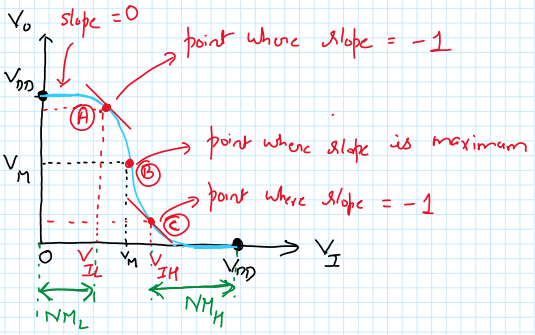
* After Point (C) on the transfer curve, the magnitude of the slope is either 0 or < 1
  ⇒ No amplification happens (∵ slope corresponds to gain)



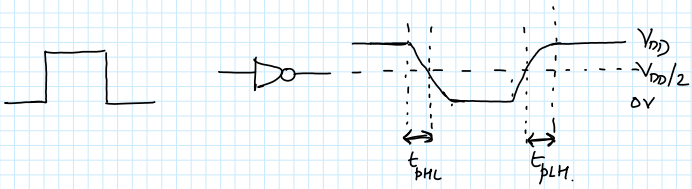


* V_I below V_{IL} are not amplified, V_I above V_{IH} are not amplified.
* In region (B) the inverter is acting as an amplifier with maximum gain [Both PMOS & NMOS in the saturation Region] → For analog designers
* We define Noise margin High (NM_H) & Noise Margin Low (NM_L)

$$NM_H = V_{DD} - V_{IH} \quad \& \quad NM_L = V_{IL}.$$

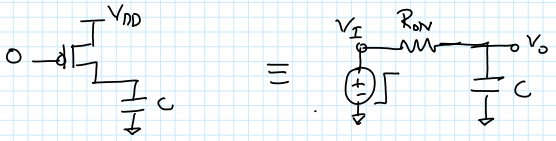


Transient characteristics of the inverter :-



* Let's define propagation delay as the time taken for the output to reach 50% of the maximum
  - ↳ $t_{p,HL}$ → propagation delay when o/p goes from high to low
  - $t_{p,LH}$ → propagation delay when o/p goes from low to high

* When $V_I = 0$, PMOS is ON & the equivalent circuit is



$$V_o = V_I\left(1 - e^{-t/RC}\right)$$

For $t = t_{p,LH}$, $\quad 0.5V_I = V_I\left(1 - e^{-t_{PLH}/RC}\right)$

$$\Rightarrow \quad t_{p,LH} = 0.69\, R_{ON,P}\, C.$$

* Recall that the PMOS goes OFF → SATURATION → LINEAR region Assuming the time spent in saturation region is very small (for first-hand pen-paper calculations),

$$R_{ON,P} = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_p\left(V_{DD} - |V_{TP}|\right)}$$

$$R_{ON,P} = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_P (V_{DD} - |V_{TP}|)}$$

* Similarly for NMOS; $t_{P,HL} = 0.69 R_{ON,N} C$

$$R_{ON,N} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_N (V_{DD} - V_{TN})}$$

* For Symmetric Inverter, $t_{P,LH} = t_{P,HL}$.

$$\therefore 0.69 R_{ON,P} C = 0.69 R_{ON,N} C$$

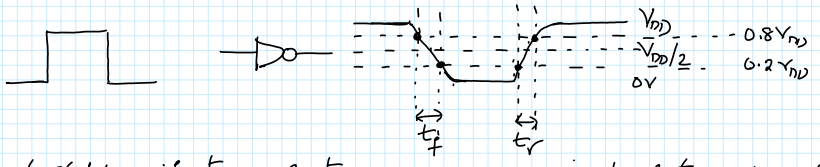
$$\Rightarrow \underbrace{\mu_n C_{ox}\left(\frac{W}{L}\right)_P}_{K_P^2}\left[V_{DD} - |V_{TP}|\right] = \underbrace{\mu_p C_{ox}\left(\frac{W}{L}\right)_N}_{K_N^2}\left[V_{DD} - V_{TN}\right]$$

$$\left(\frac{K_P}{K_N}\right)^2 \left[V_{DD} - |V_{TP}|\right] = V_{DD} - V_{TN}$$

$$\gamma^2 \left[V_{DD} - |V_{TP}|\right] = V_{DD} - V_{TN}. \quad \text{—(1)}$$

* Condition (1) above is true provided $V_{TN} = |V_{TP}|$ & $\gamma = 1$ [one of the easiest conditions]
This is the same condition we got for $V_M = V_{DD}/2$!!!

* We define rise-time (t_r) & fall-time (t_f) as 20% to 80% V_{DD} time & vice versa.



* Under the same concept, if $t_{P,LH}$ & $t_{P,HL}$ are symmetric t_f & t_r will also be symmetric!!

∴ Provided $V_{TN} = |V_{TP}|$, if by design $\gamma = 1$ (i.e. $\frac{W_p}{W_N} = \frac{\mu_n}{\mu_p}$), we get

(i) $V_M = V_{DD}/2$
(ii) $t_{P,HL} = t_{P,LH}$
(iii) $t_r = t_f$

} Symmetric Inverter.

— × — × —

* For an Inverter, we can define the following

(a) Static characteristics:
- (i) V_M (switching voltage)
- (ii) V_{IH}, V_{OH} & $N_{M,H}$, $N_{M,L}$ (Noise Margins)

(b) Dynamic characteristics.
- (i) $t_{P,LH}$ & $t_{P,HL}$ (Low to High & High-to-low propagation time)
- (ii) $t_p = \frac{t_{P,LH} + t_{P,HL}}{2}$ (total propagation time)
- (iii) t_r & t_f (Rise & fall time)

(iii) t_r & t_f (Rise & fall time)

* To design a symmetric inverter, i.e $\begin{bmatrix} V_M = V_{DD}/2 \\ t_{P,LH} = t_{P,HL} \\ t_r = t_f \end{bmatrix}$,

if $V_{TN} = |V_{TP}|$, For a given minimum length (L_{min}), $\frac{W_P}{W_N} = \frac{\mu_N}{\mu_P}$

→ This will be the starting point for your simulations.

→ In a practical Process Design Kit (PDK), $V_{TN} \neq |V_{TP}|$

⇒ To achieve symmetric conditions W_p, W_N must be tuned.