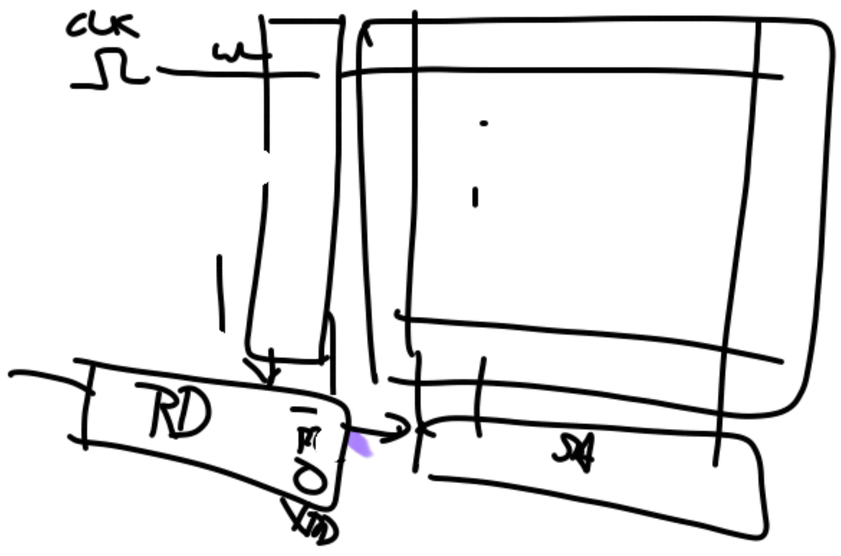


WRITE

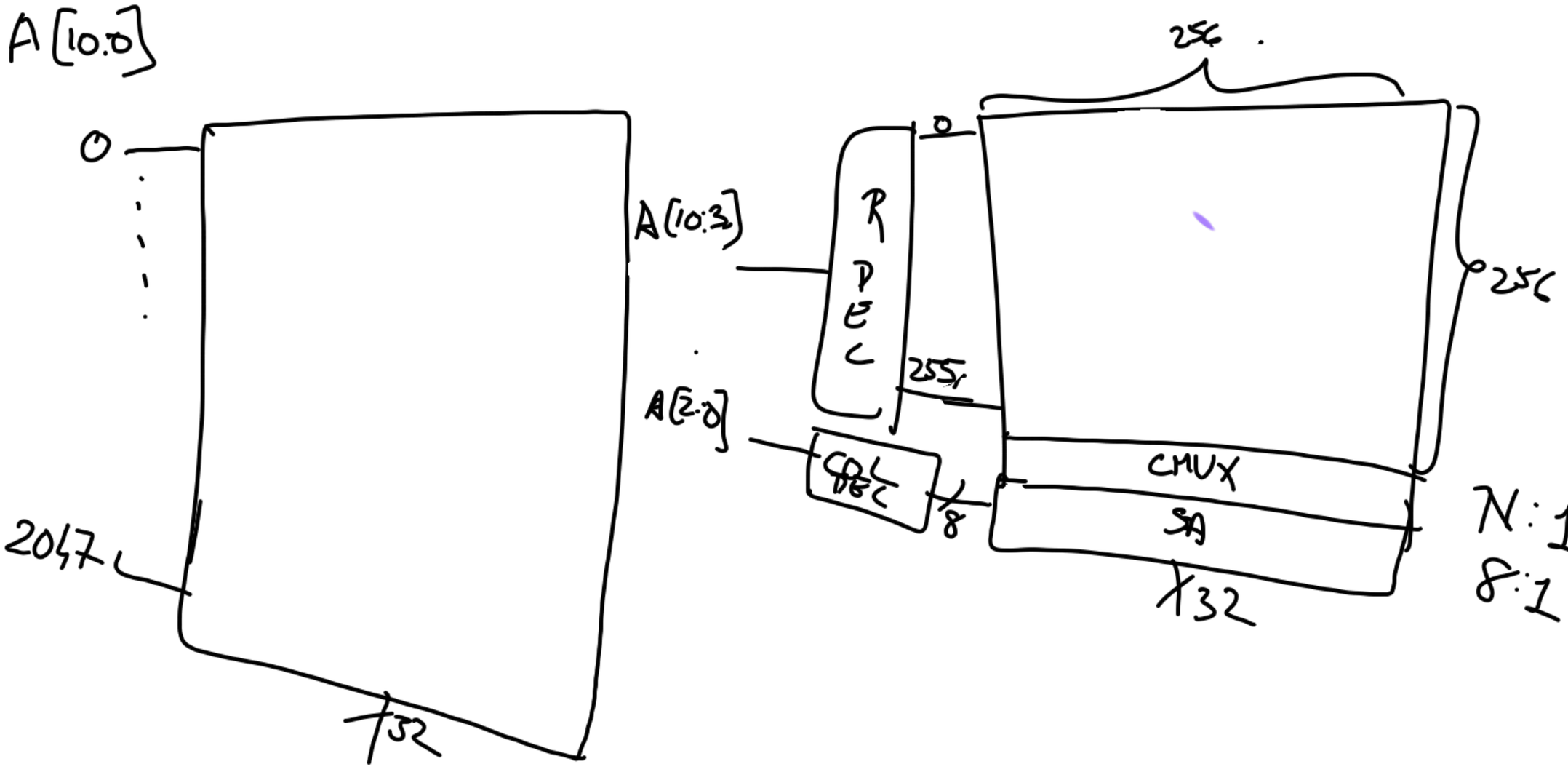
1) PC X
2) CG
3) WL

READ

1) PC X
2) WL ↑
3) ΔV → SAE, CG

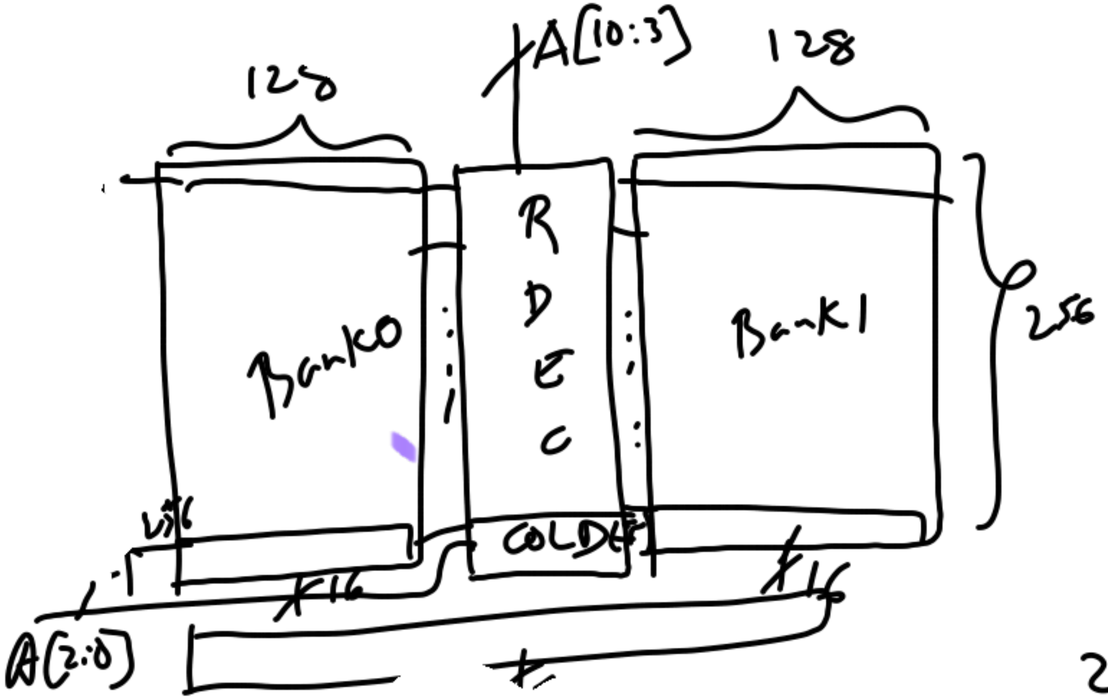
ROLDEC

2048 X 32 → 8KB

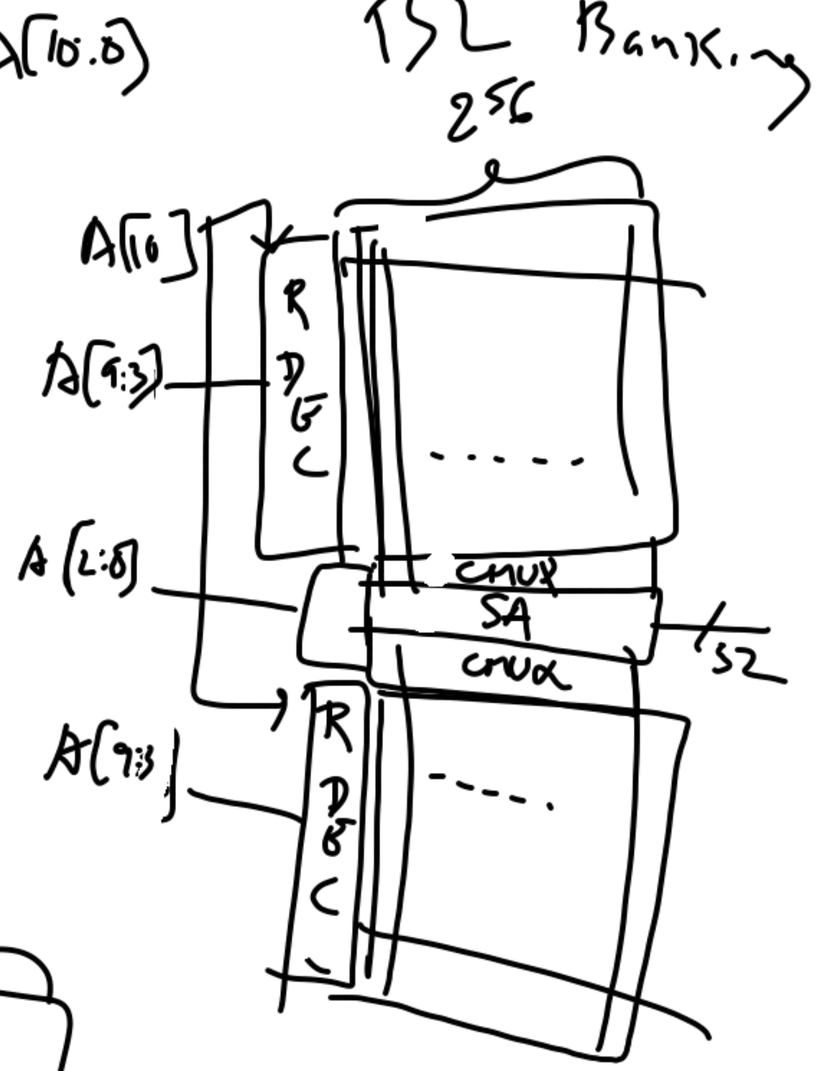


Butterfly

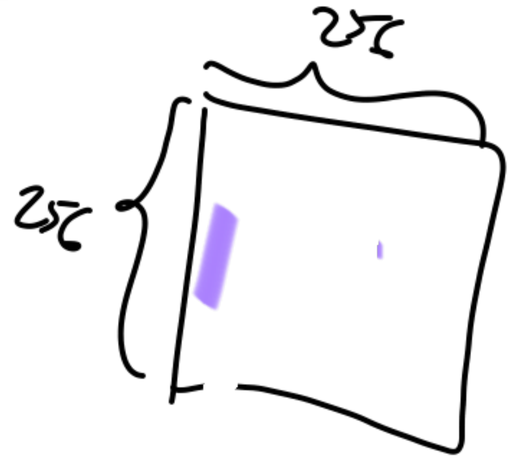
WL Banking



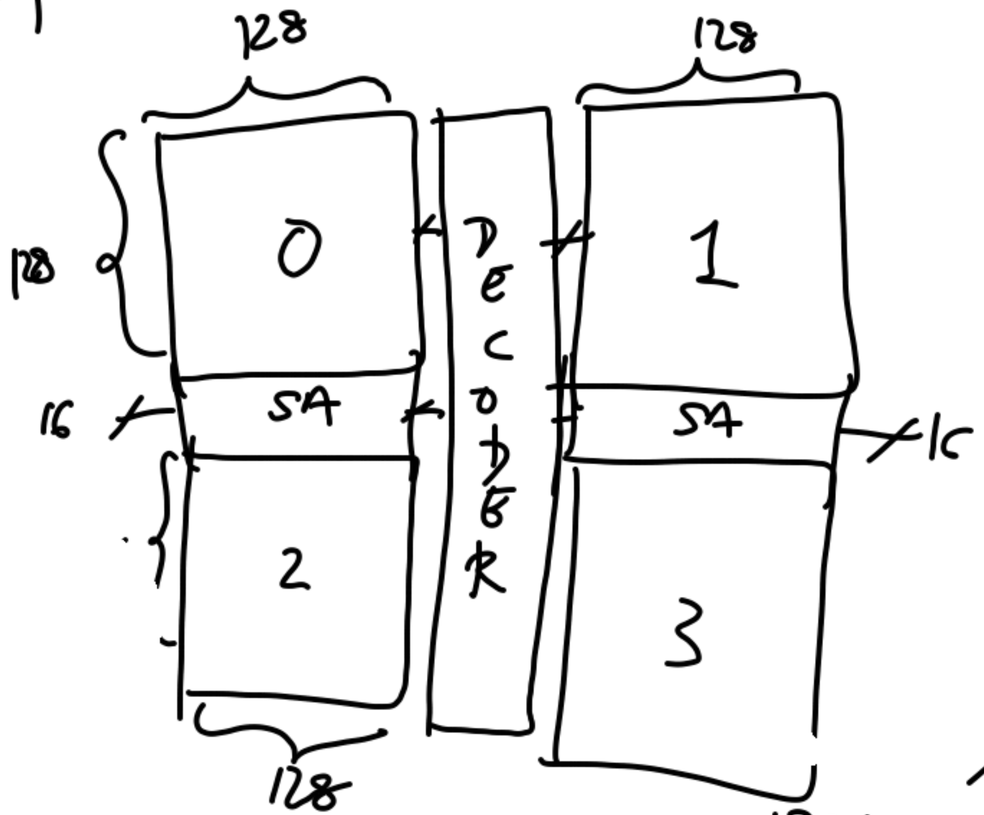
BL Banking

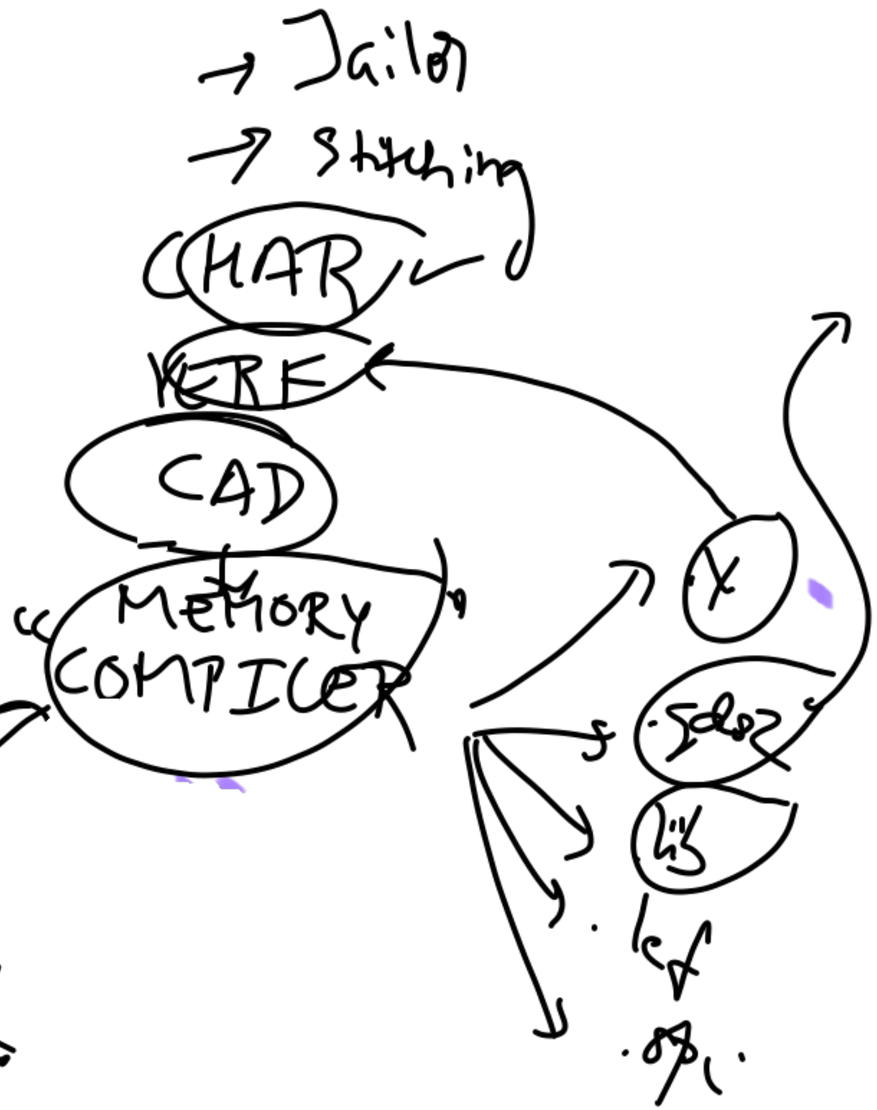


A[10] → Bank Sel



"OpenRAM"


128
128
128
128
16
16
0
1
2
3
SA
SA
Decoder
128x8_1_1


→ Jailor
→ Stitching
CHAR
KERF
CAD
MEMORY COMPILER
X
Y
LEF

8T → 10T

RBL

WBL

WBL

WWL

RWL

VDD

RBL

A[N:0]

WE

CLK

WRITE

READ

ADDRA

ADDRB

WEA

WEB

CLK

Data [M:0]

DINA

DOUTB

10T