EE671: VLSI Design
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LECTURE – 25
RTL TO GDS

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SOME IMPORTANT INFO

- RTL: Register transfer level → flow of data between registers (hdl)
- LIB: Liberty file → timing and power information of cells
- LEF: Library exchange format → abstract physical layout view of cells (pins,OBS,..)
- GDS: Graphic data stream → ASCII representation of actual layout
- DRC: Design rule check → ensure design meets manufacturing requirement
- LVS: Layout vs schematic → ensure layout and schematic are equivalent
- LEC: Logical equivalence check → ensure two designs (hdls) are equivalent
- CTS: Clock tree synthesis → distribution of clock with minimal skew
- STA: Static timing analysis → timing analysis methodology
- DEF: Design exchange format → black box view of a cell layout. Upgradation on LEF → has both logical and physical info of a block → need LEF to read DEF
- SPEF: Standard parasitic exchange format → RC delay info of interconnects
- SDF: Standard delay format → Cell + interconnect delay (total delay)
- Tap cells: well-tap and de-cap cells

STA TIMING CHECK

- For every path:
  - There is a Required arrival time (to avoid set-up and hold violation) – RAT
  - There is the Actual arrival time – AAT

- **Setup slack = RAT – AAT**
- **Hold slack = AAT – RAT**

- Positive slack: design works pretty well – easily meets timing
- Zero slack: design just works – in terms of timing
- Negative slack: design has timing violation