EE671: VLSI Design
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LECTURE – 33
SRAM CONTINUED

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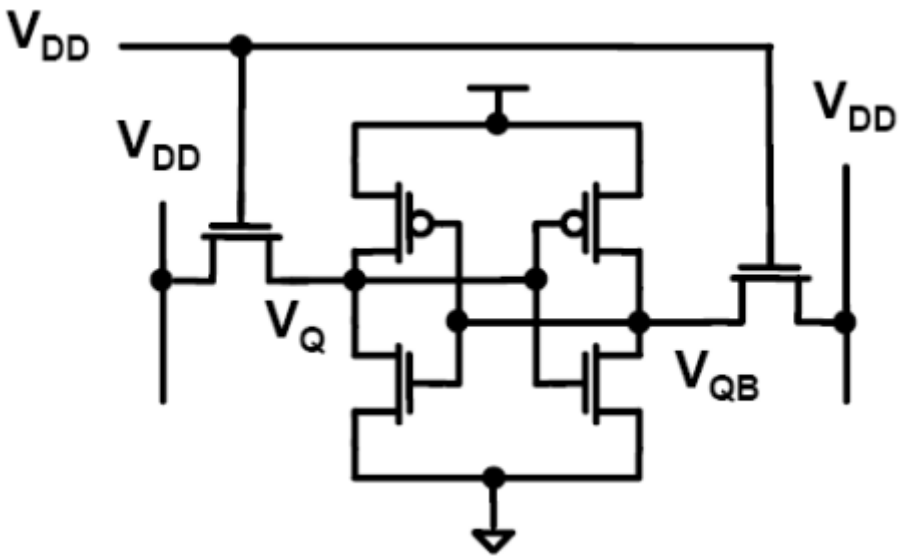
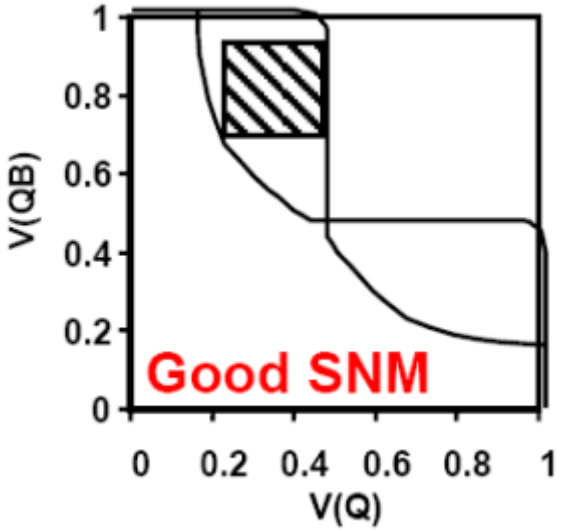
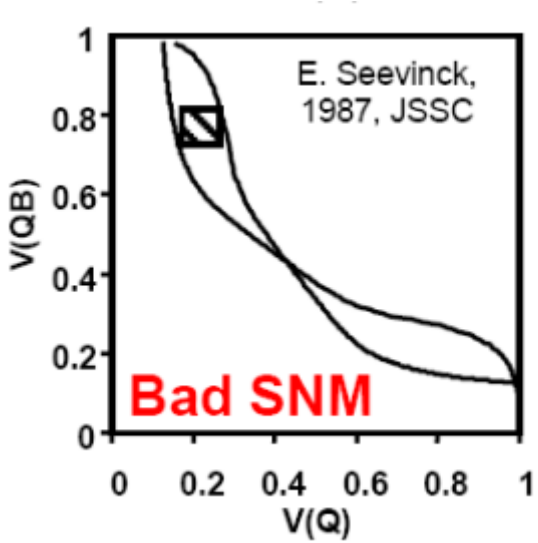
READ SNM

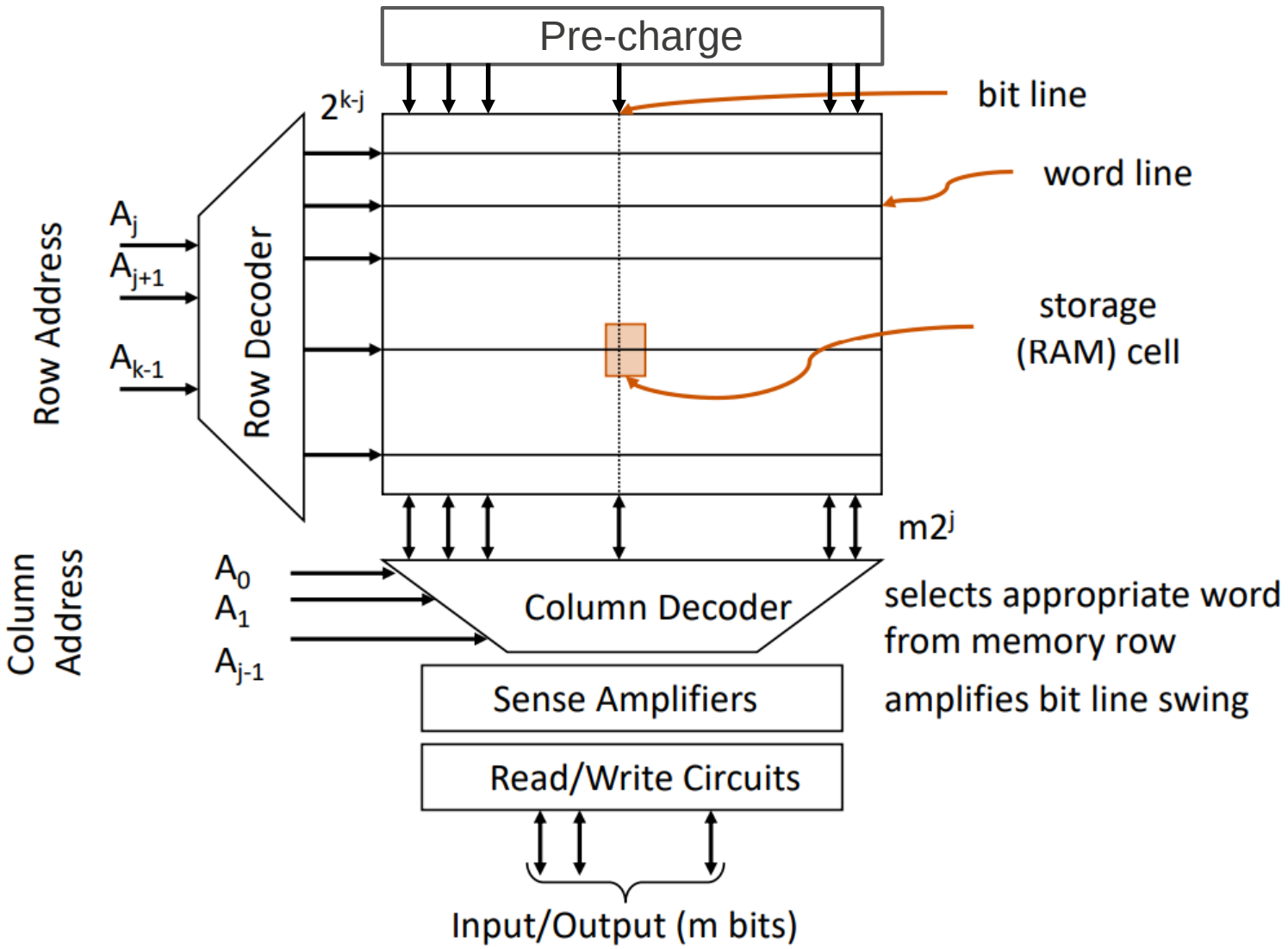






- Addition of access transistors → reduced the noise margin (compared to inverter)
- To avoid read destruction→ Static Noise Margin (SNM) must be increased
- Bigger the box you can fit inside the two transfer curves → better SNM !
- Design: start with the initial W values → keep optimizing to increase SNM
- But remember → entire idea behind SRAM is to reduce the area → we cannot size MOSFETs beyond a certain limit!

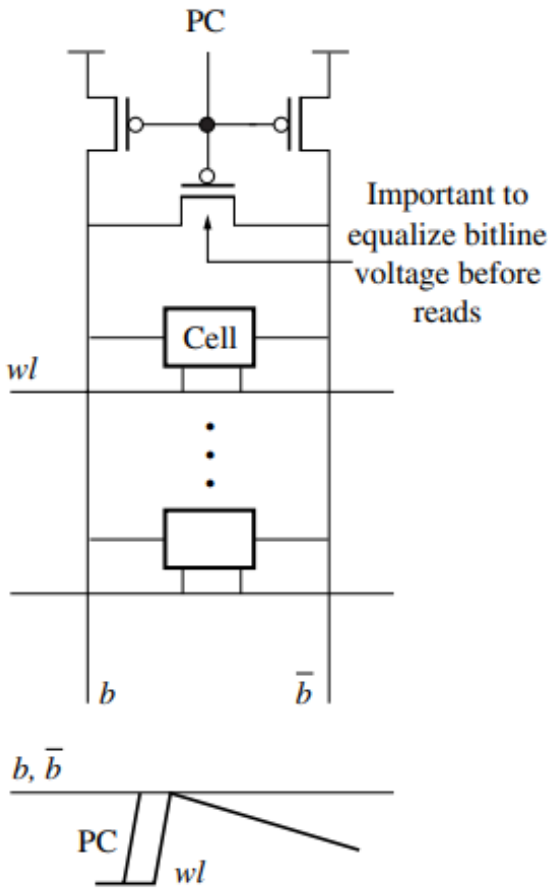
SRAM: Full Picture



- We have looked at the Row decoder (logical effort design)
- Looked at design of individual bit-cell
- Next, we will look at the pre-charge circuit, column decoders, sense amplifiers

COLUMN PULL-UPS: PRE-CHARGE

- To remove all history → perform pre-charge before every read and write
- The nature of pre-charge (PC) circuit depends on the amplification (also called sense amplifier (SA)) topology

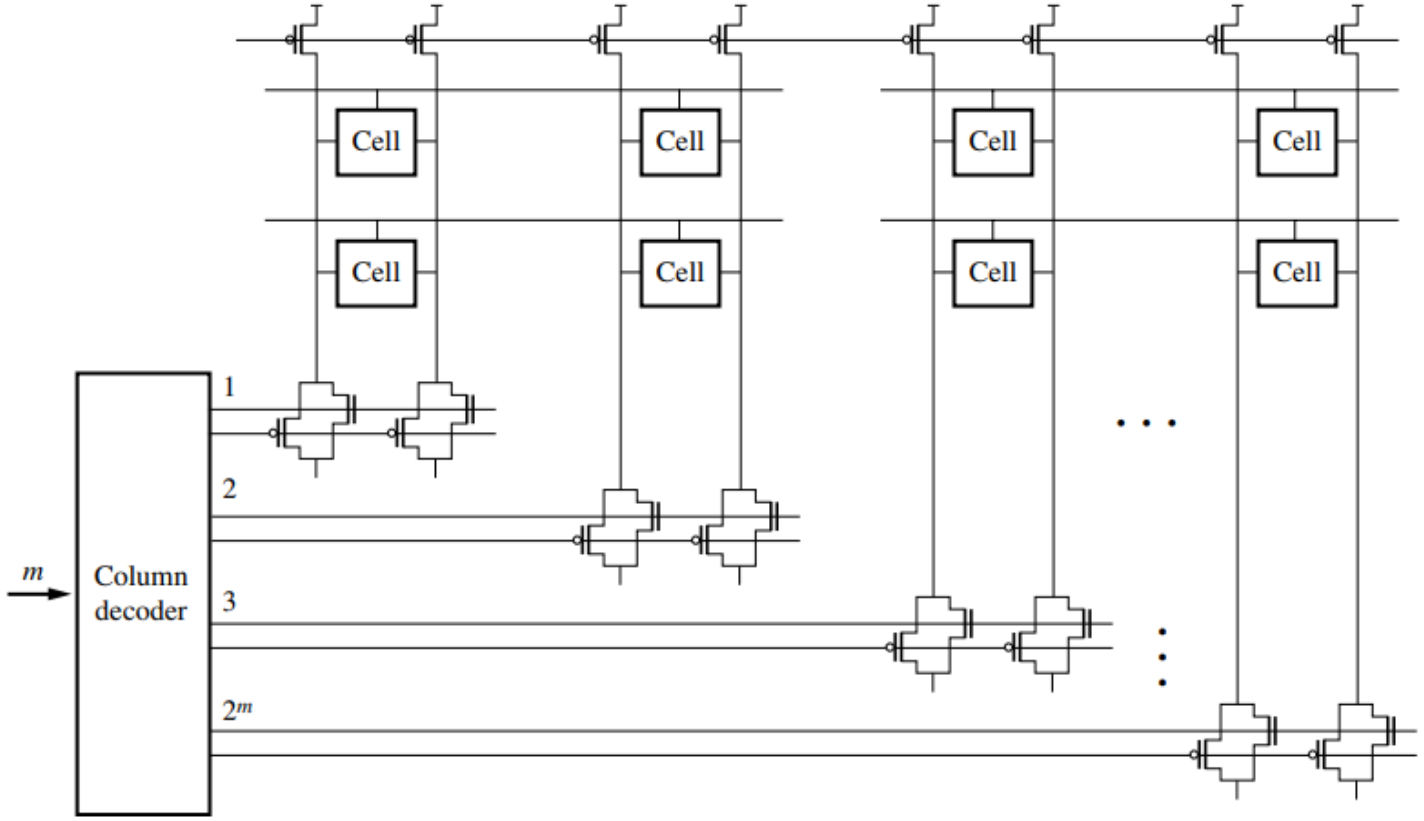


Suitable for voltage based amplifiers

- Sequence:
  - PC is low by default (Pre-charging bit lines)
  - PC goes high
  - After some finite time → WL goes high
  - Read operation starts
  - Bitlines start developing delta voltage
  - Sense amplifier (SA) enabled after finite time to amplify this delta voltage
  - Once logic levels are obtained at the output, disable WL, SA and enable PC

Column Decoder (Column Mux)

- After PC, the columns involved in read/write are to be enabled using MUX
- Usually this MUX is a simple TG (we looked at implementing MUX using TG earlier)



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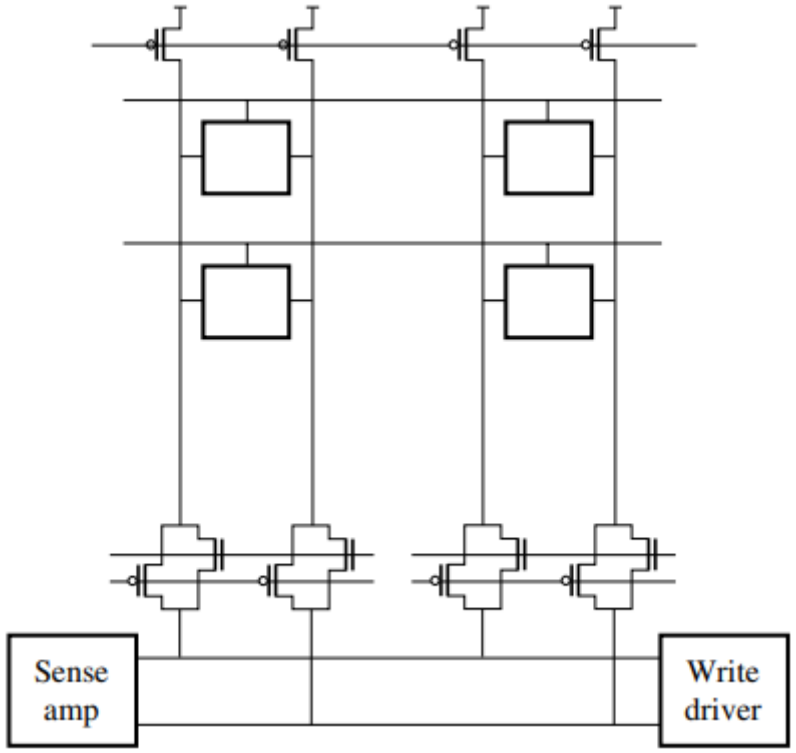
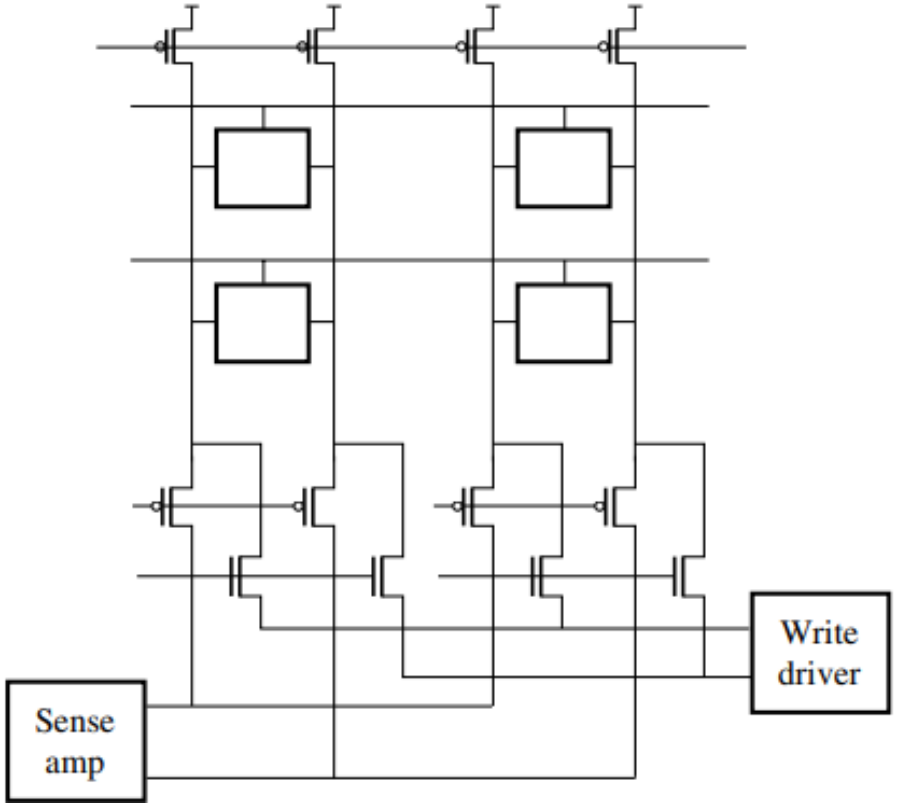
Column Decoder (Column Mux)

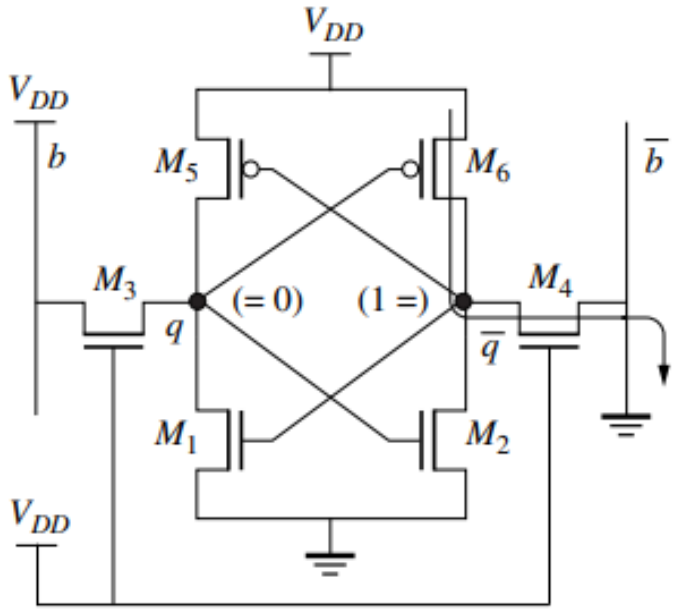
- The read and write operation paths can be separated as shown below
- SA is enabled during read and write driver is enabled are enabled during write after selecting the required columns



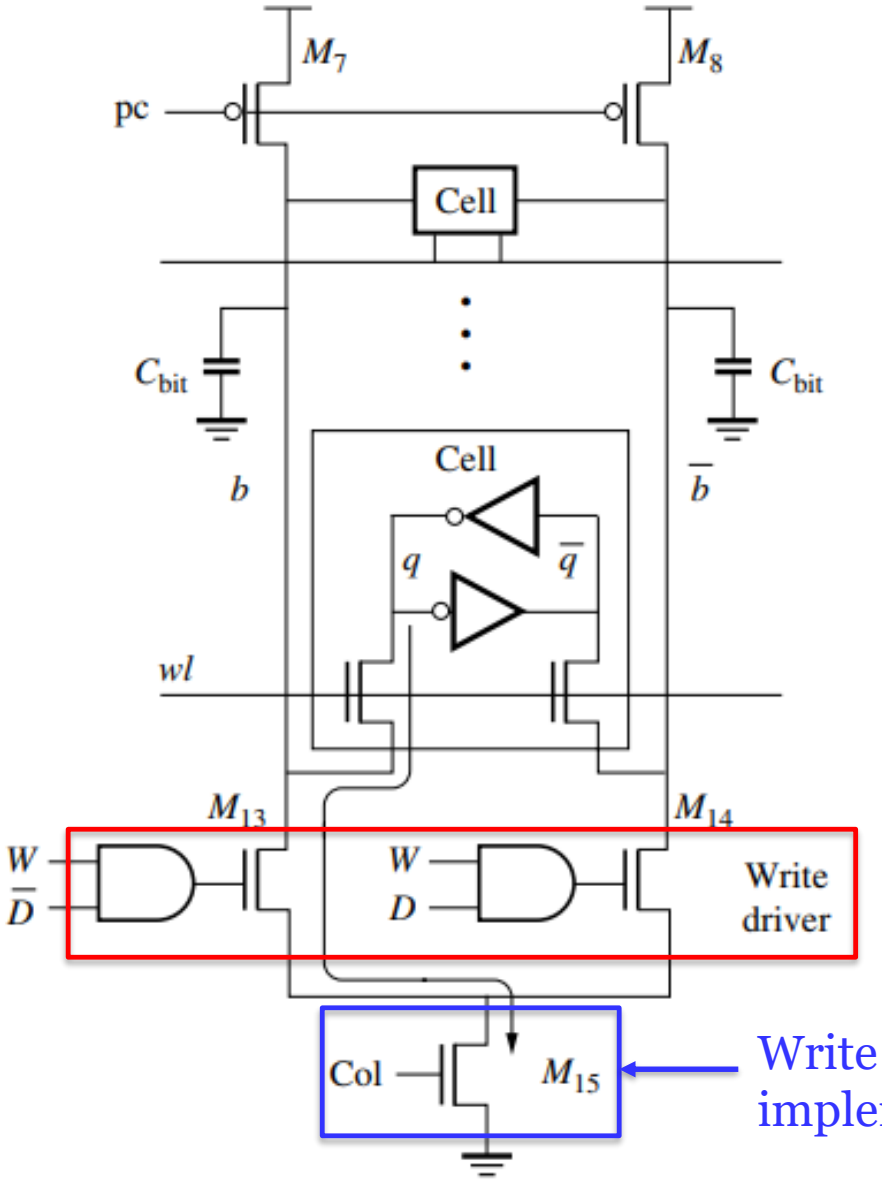
Column Decoder (Column Mux)

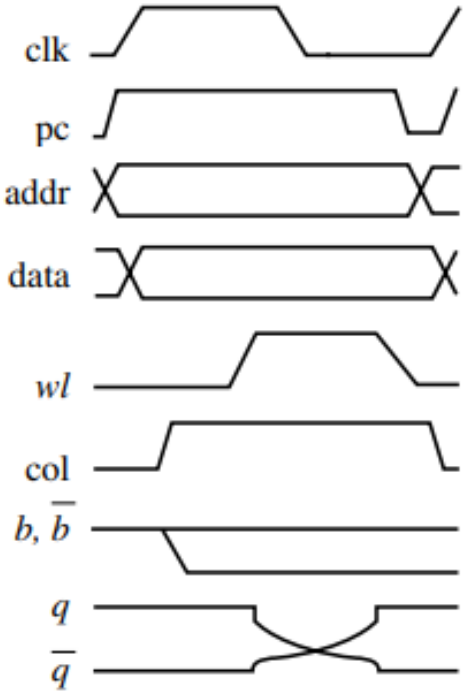
- Note that, during read all lines are V_{DD} (pre-charge), so we only really need PMOS devices during read operation
- During write, essentially, we are discharging bitlines to ground → we need NMOS
- This automatically provides the enabling of read/write using the same column decoder





Complete Write Circuit (one column)

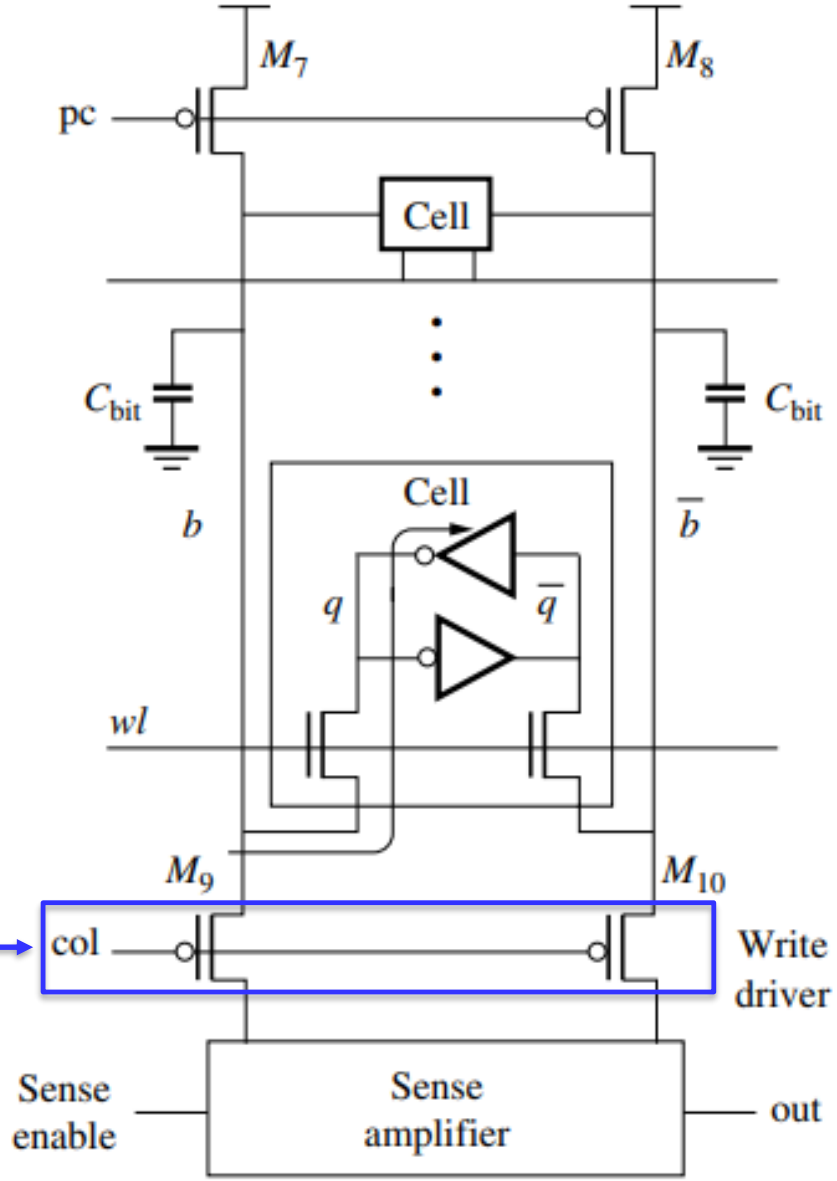


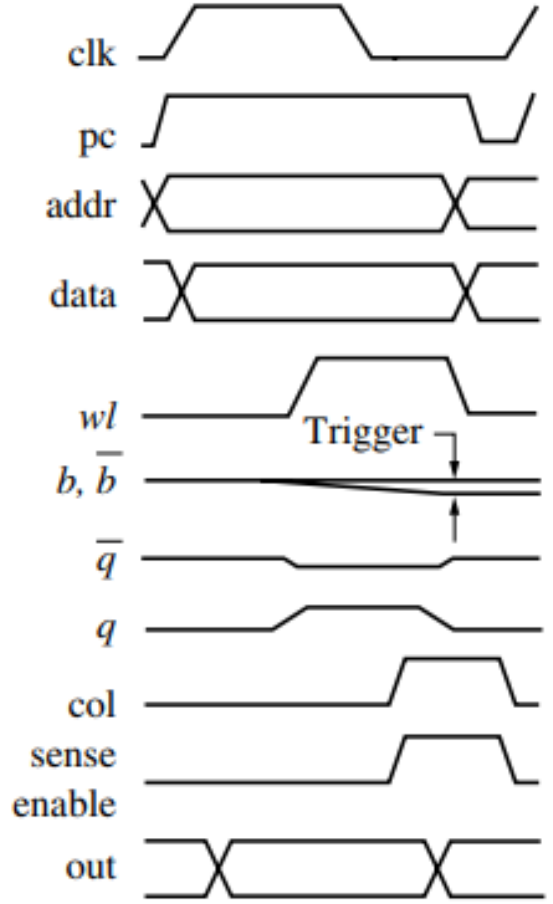


Write column mux (NMOS only implementation)

Complete Read Circuit (one column)

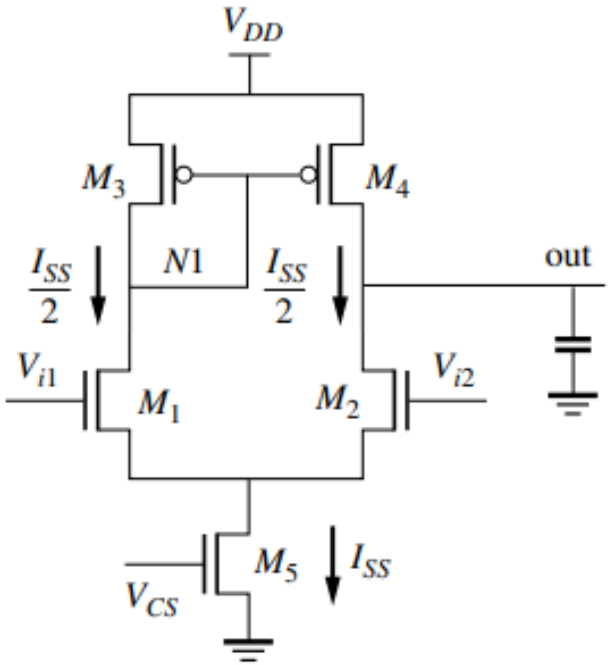
Read column mux (PMOS only implementation)

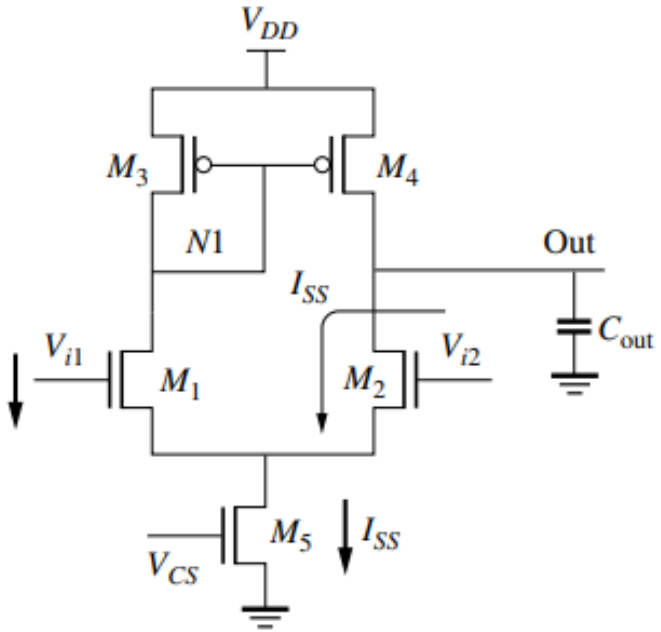


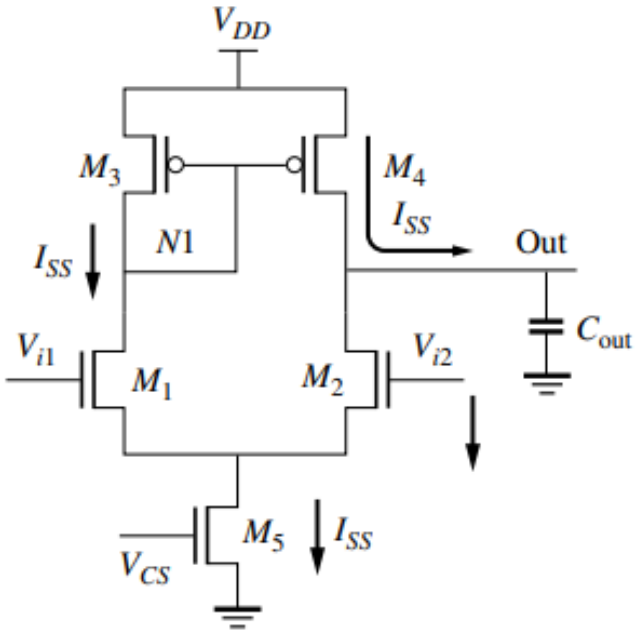


SENSE AMPLIFIER

- Option-1: A simple differential amplifier
  - Provides good common-mode rejection (common-mode noise)
  - Typical: 100 mV to 200 mV input voltage required
  - Static power consumption!

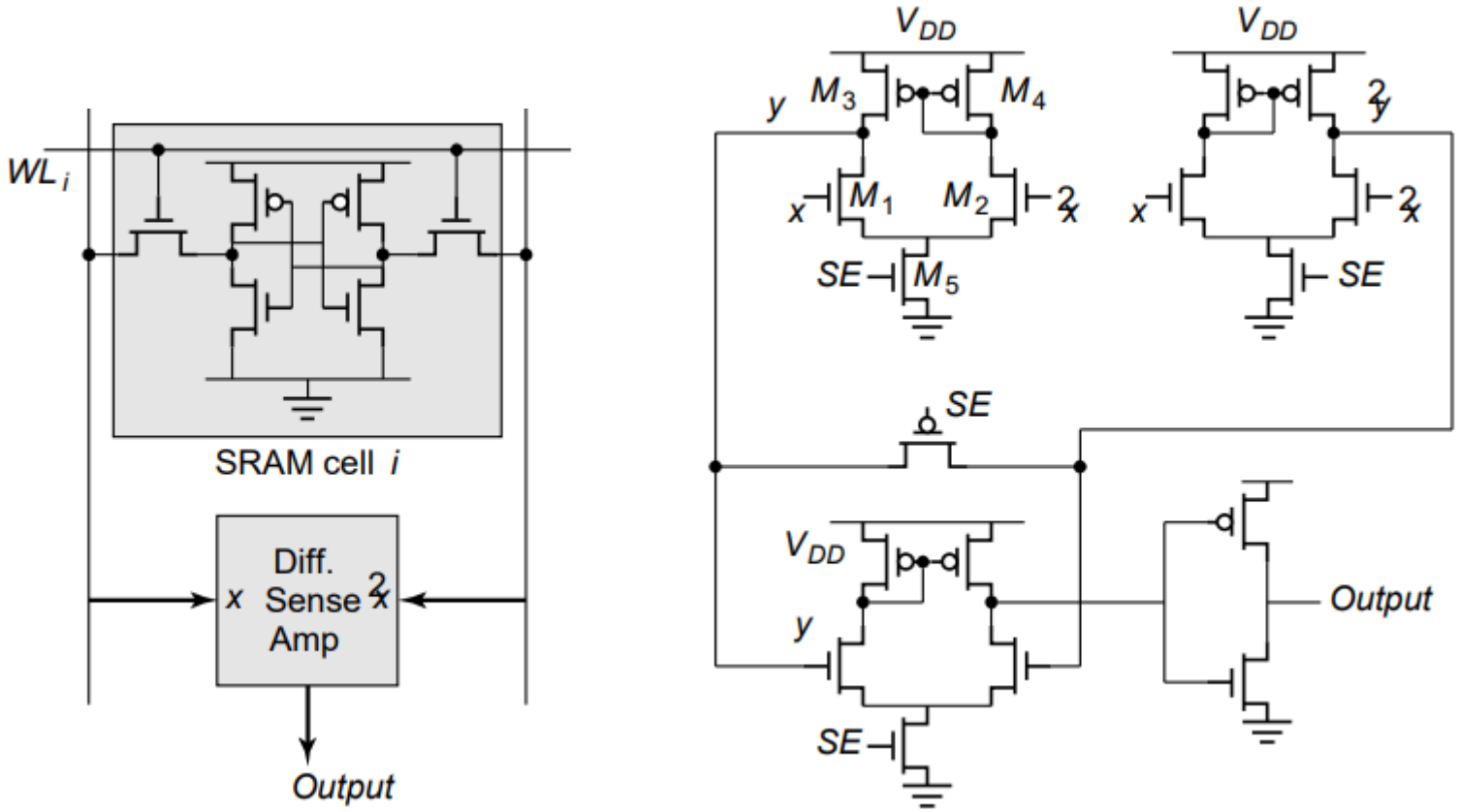






SENSE AMPLIFIER

- Option-1: A simple differential amplifier
  - Could also increase stages



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