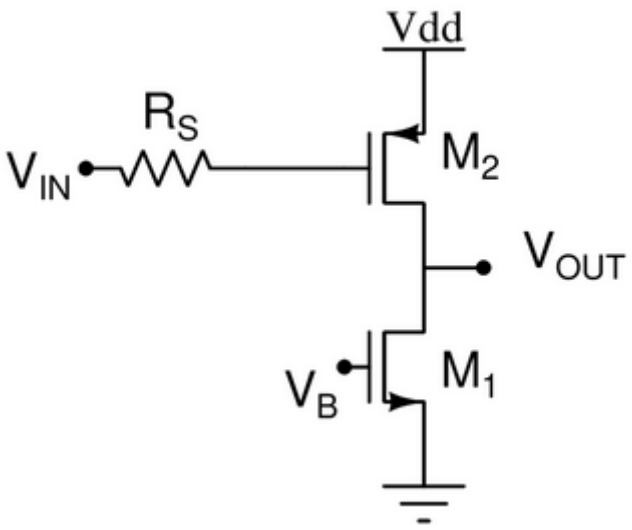
EE618 (ZELE)

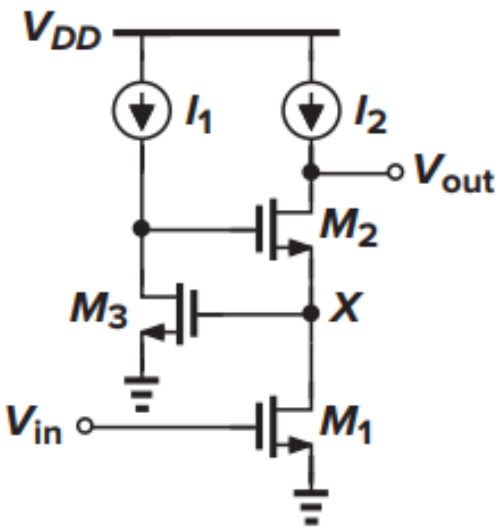
CMOS ANALOG VLSI DESIGN

Question Bank

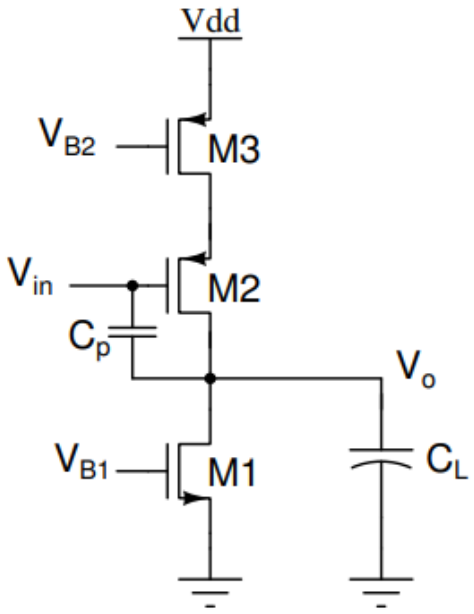
1) In this circuit shown, R_s=1kΩ and both the transistors are identical. Assume the parasitic capacitances have the same values for both the transistors. I_{d1}= I_{d2}= 1mA, C_{GS}=250fF, C_{GD}=80fF, g_{m2}=1mS, λ_n= 0.1V^{-1}, λ_p = 0.2V^{-1}. Consider channel length modulation. Find **input pole frequency** in **MHz**. Two decimal point accuracy is expected. (1M=10^6)



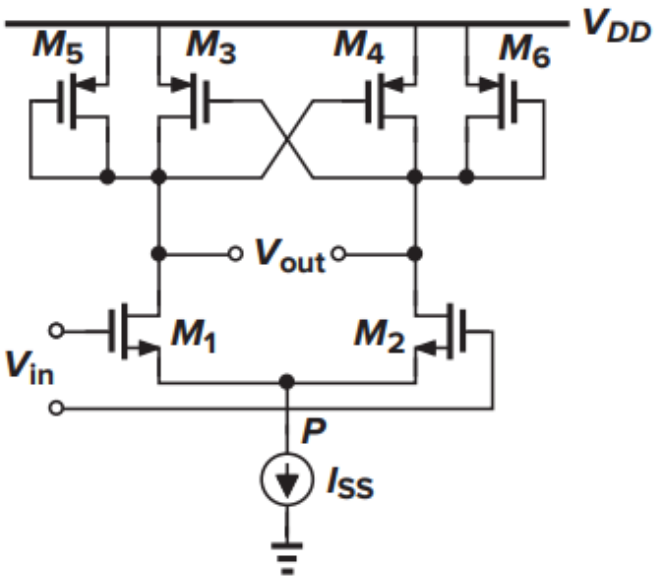
2) Calculate the voltage gain Av for the below circuit.



3) All transistors have same g_m and g_{ds}. $g_m >> 2\ g_{ds}$. Ignore body effect and transistor capacitances.
   i) Calculate the DC gain.
   ii) Derive the expression for transfer function (frequency response).
   iii) Draw the bode plot for both magnitude and phase.



4) Calculate input referred thermal noise voltage for below circuit.



5) Calculate input referred thermal noise voltage for below circuit.