EE 618 (ZELE)

CMOS Analog VLSI Design: Question Bank

Note: Use the following wherever not specified explicitly, V_{DD}= 3V, V_{Tn} = 0.7 V and V_{Tp} = -0.8 V. Neglect body effect. Assume low frequency small signal model whenever required.

1. For the CS Amplifier in Figure 1 with diode connected load, find the $V_{in,max}$ (in V). Given V_{DD} = 1.8 V, $gm_1 = gm_2$, $V_{IN} = V_{OUT}$= 0.6 V, $V_{TN} = |V_{TP}|$ = 0.4 V.

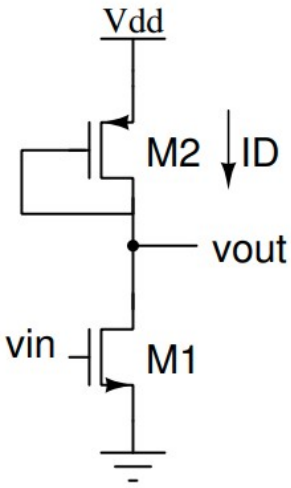

Figure 1

2. Given that M1 and M2 are in saturation, if the voltage at node Y is increased by a small value ΔV, then find the change in the voltage at node X.

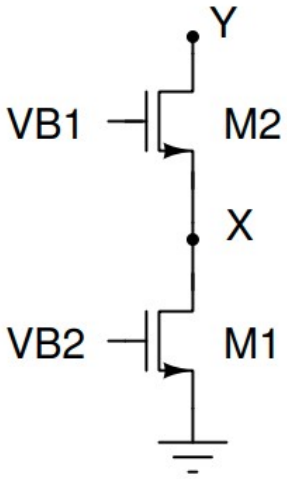

Figure 2

3. Assuming all the transistors are in a saturation, find a small signal voltage gain for the following circuit:

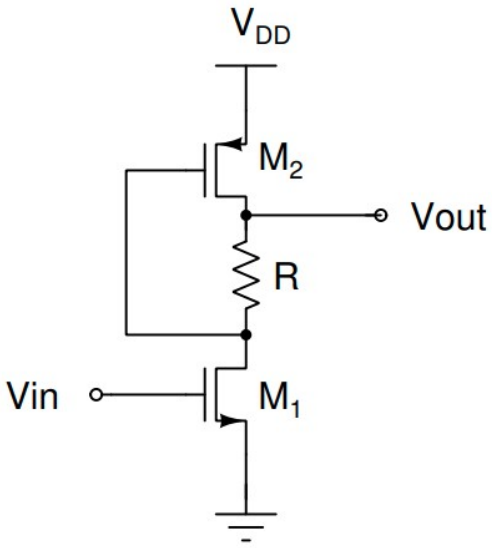

Figure 4

4. Assuming all transistors are in a saturation, find a small signal voltage gain for the following circuits: