EE 618 (ZELE)
CMOS Analog VLSI Design
ENDSEM

Date : 22nd November 2023 **Duration**: 3 Hours **Max. Marks** : 64

ACADEMIC HONESTY POLICY—IIT BOMBAY (https://www.iitb.ac.in/newacadhome/rules.jsp)
Copying in exams has serious consequences.
Do not communicate with other students during exams. Do not carry unauthorized material during exams
Do not make changes in valued answer books. Do not communicate with others during toilet breaks during exams

State your assumptions clearly, if any.

Q1) Design a Butterworth low-pass filter to meet the following specifications using the tables/charts provided. Ripple Bandwidth = 28.28 MHz, Stopband frequency =282.8 MHz, Stopband Attenuation = 50 dB [23]

a) Using Table/Graph provided, identify the order of filter. [1]
b) Draw RLC prototype of the filter with correctly scaled LC values annotated to meet the specifications above. Use the element values from Table 5.2 provided. [2]
c) Using signal flow graph technique, develop integrator (block diagram) based filter schematic. Show intermediate steps. [4]
d) Draw a schematic of G_m-C integrator using differential pair and ideal current sources. Using a symbol for G_m-C integrator (with multiple inputs and single ended output), draw complete filter schematic. Label polarities and node names. [4]
e) Assuming G_m = 0.177 mS, find out the values of all required capacitors. [2]
f) Draw schematic diagram for parasitic insensitive switched-capacitor integrator. Make sure polarities and clock phases are properly annotated. [2]
g) Use the integrator from (f) in (c) to construct a switched-capacitor filter schematic. Also annotate the clocking scheme for filter. [4]
h) Choose clock frequency. Justify your choice. [1]
i) For all Switched-capacitor integrators, C_U = 0.25pF (input capacitor). Calculate values of C_I (feedback capacitors) of all integrators. [3]

Q2. In Fig. 1, all transistors are in saturation such that $g_{m1} = g_{m2}$, $g_{m3} = g_{m4}$, $g_{m5} = g_{m6}$. Derive the small signal output impedance and the voltage gain expressions in terms of g_{m1}, g_{m3} and g_{m5}. [4]

a) Find small signal output impedance and voltage gain for $(W/L)_{4,3} = 1.2\,(W/L)_{5,6}$. Simplify in terms of g_{m1} and g_{m5} only. [2]
b) Comment on the output impedance obtained in the above case. [1]

Hint - Use half circuit method by looking at either of the output nodes. Ignore r_o of all the transistors.

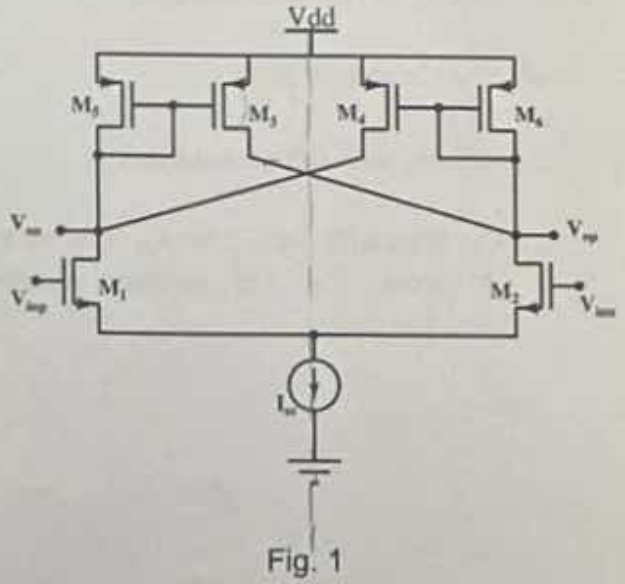


Fig. 1

Q3. Draw the complete transistor level schematic of p-mos input (differential-pair) folded cascode OTA with single ended output. The total current drawn from the supply V_{DD} is $4I_{SS}$. The differential pair tail current value is $2I_{SS}$. Label the transistors and node names with polarities. You can assume appropriate gate bias voltages are available. [3]

a) Derive the expression for effective G_m, R_{out} and DC gain of the OTA in terms of g_m and r_o of corresponding transistors. ($g_m r_o >> 1$ for each transistor) [2]

b) Calculate the positive and negative slew rate. Draw schematic to show the transistors which are ON for each slew rate calculation. The load capacitor at the output is C_L. [2]

c) Convert the above schematic into fully differential design with common mode feedback (CMFB). (You can use any CMFB technique). [3]

Q4. Ignore channel length modulation, flicker noise and body effect. Capacitor C_{large} represents short for ac analysis.

For Fig.2(a), derive the expression for:

a) Output noise voltage. [2]

b) V_{out} / V_{in}. [2]

c) Input referred noise voltage $\overline{v_n^2}$. [1]

For Fig.2(b), derive the expression for:

d) Output noise voltage. [2]

e) V_{out} / I_{in}. [2]

f) Input referred noise current $\overline{i_n^2}$. [1]

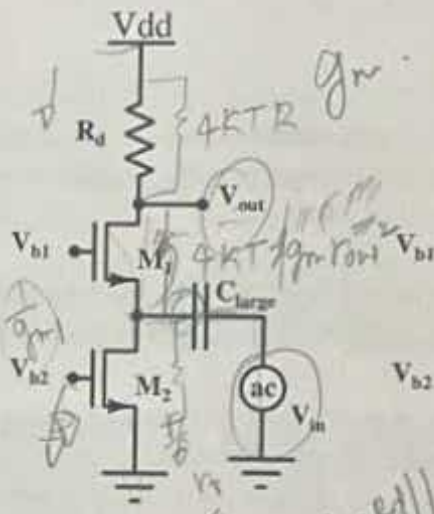


Fig. 2(a)

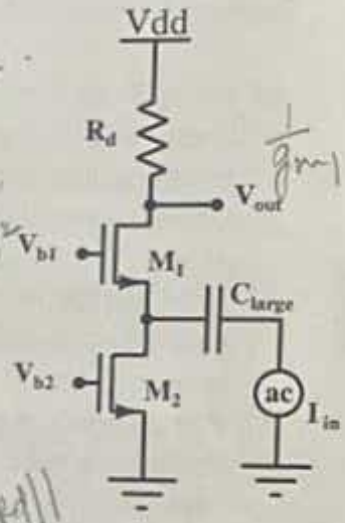


Fig. 2(b)

Q5. Calculate $V_{out}(\phi) - V_{out}(\overline{\phi})$ in following cases: (Show detailed intermediate steps)

a) The Opamp is ideal. [2]

b) Opamp with offset voltage V_{os}. [1]

c) Op Amp with finite gain A_{OL}. Derive the expression in terms of A_{OL}. (Ignore offset voltage). [2]

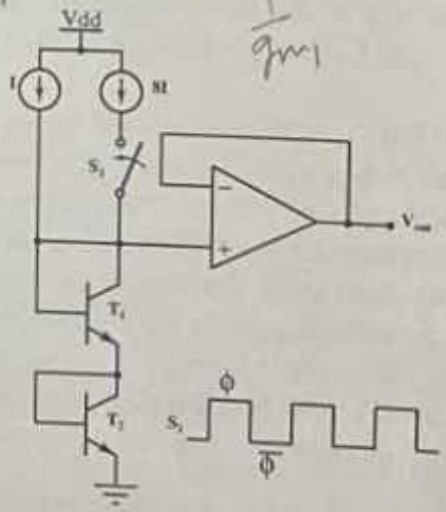


Fig. 3

Q6. For the switched-capacitor circuit below, use charge conservation principle to derive the V_{out2} / V_{in} transfer function. Use z-domain analysis. [5]
Identify the circuit function. [1]

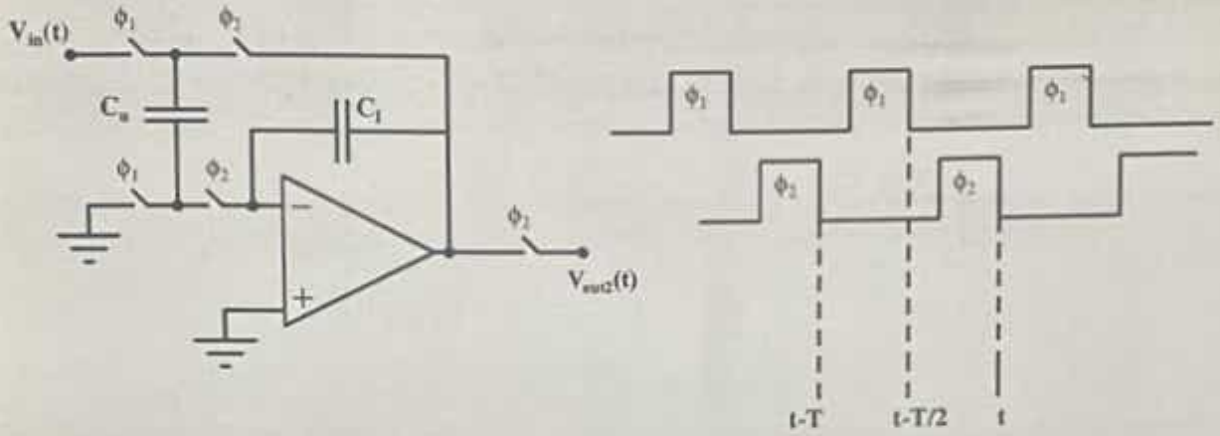
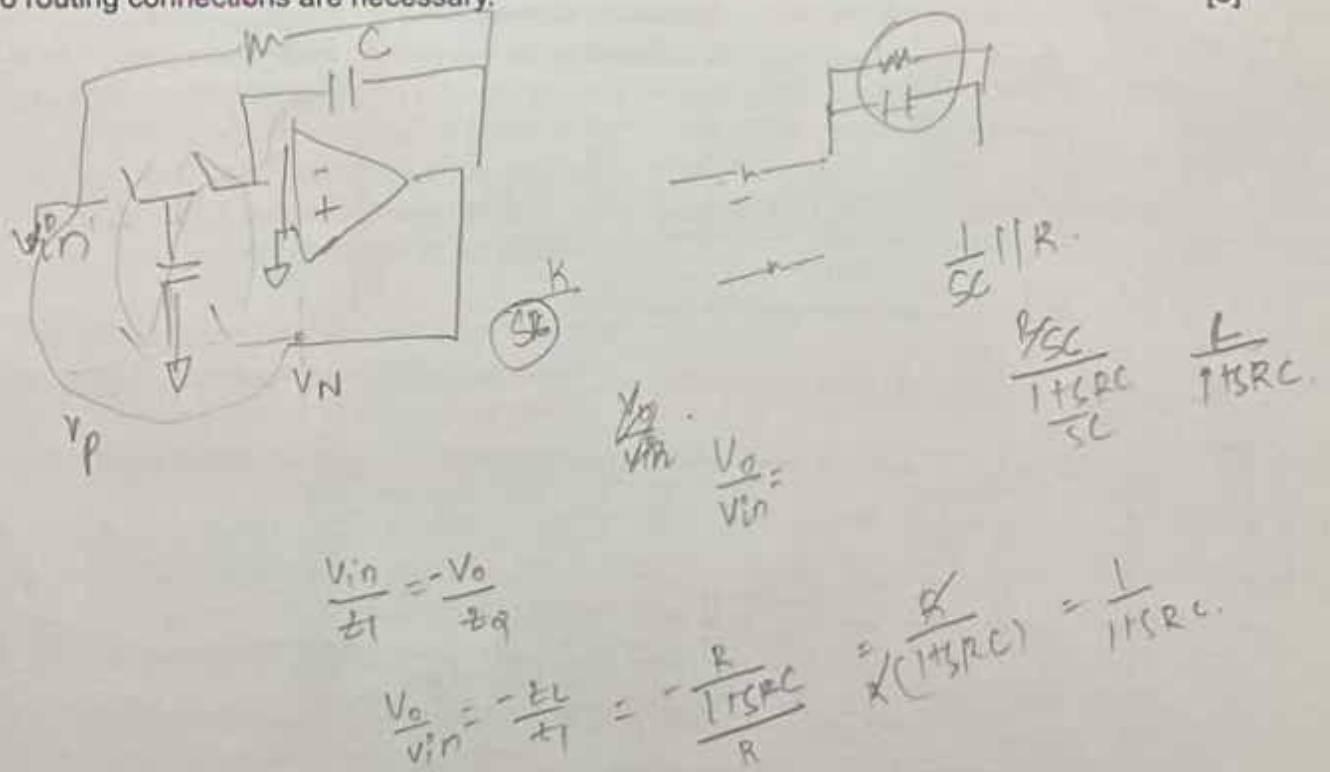


Fig. 4

Q7. As a layout designer, you are required to match the input differential pair NMOS transistors sized 7.2 µm / 45 nm each. Maximum finger width should be 0.5µm. Draw layout of the differential pair with common-centroid configuration. Annotate drain and source connections. Label width, length, and number of fingers for each unit transistor.
No routing connections are necessary. [3]



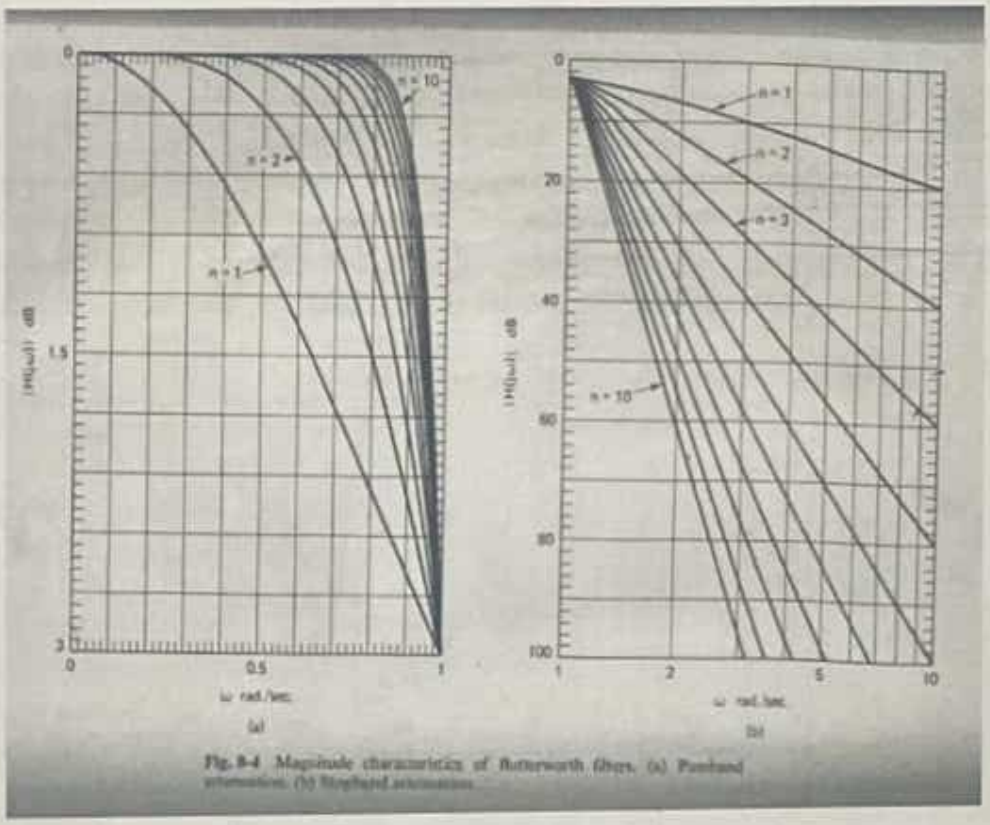


Fig. 8-4 Magnitude characteristics of Butterworth filters. (a) Passband attenuation. (b) Stopband attenuation.

Fig 5.1. Magnitude characteristics of Butterworth filters: (a) Passband attenuation, (b) Stopband attenuation

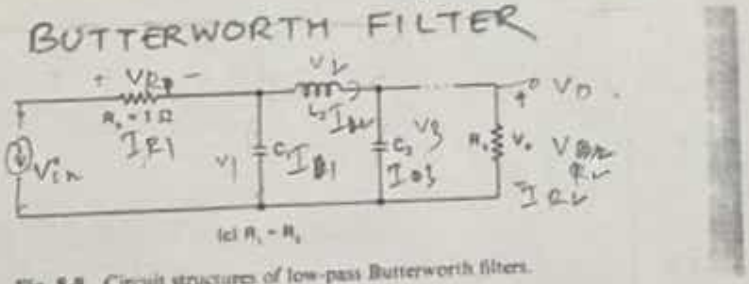


Fig. 8-9 Circuit structures of low-pass Butterworth filters.

FILTER ORDER

TABLE 8-1 Element Values for the Circuit in Fig. 8-9(c)

n	C_1	L_2	C_3	L_4	C_5	L_6	C_7	L_8	C_9
1	2.0000								
2	1.4142	1.4142							
3	1.0000	2.0000	1.0000						
4	0.7654	1.8478	1.8478	0.7654					
5	0.6180	1.6180	2.0000	1.6180	0.6180				
6	0.5176	1.4142	1.9319	1.9319	1.4142	0.5176			
7	0.4450	1.2470	1.8019	2.0000	1.8019	1.2470	0.4450		
8	0.3902	1.1111	1.6629	1.9616	1.9616	1.6629	1.1111	0.3902	
9	0.3473	1.0000	1.5321	1.8794	2.0000	1.8794	1.5321	1.0000	0.3473

Table 5.2. Element values for the Butterworth filter circuit