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PIC24FJ128GA310 Plug-in Module Manual

Overview

The PIC24FJ128GA310 Plug-in Module is designed to demonstrate the capabilities of the PIC24FJ128GA310 family using the Explorer 16 Demonstration Board. Most of the pins from the device (PIC24FJ128GA310) are mapped directly to the PIM connecter (100-Pin ICE). The exceptions are those pins that are remapped to provide remappable functionality to the pins in the PICtail™ Plus socket. The table below shows the exceptions of the PIC24FJ128GA310 pins that are not directly connected to the ICE connector.

Pin Mapping Which Does Not Do 1-to-1 Mapping

Pin Function	Device Pin (PIC24FJ128GA310)	PIM Pin (100-Pin Pin U1A)
CN83/RF7	54	69
INT0/CN84/RF6	55	68
RP2/SEG13/RTCC/CN53/RD8	68	55
RP4/SEG14/PMACK2/CN53/RD9	69	54

Board Schematic (Page 1 of 2) PMPRD/CN14/RD5-PMPWR/OC5/RD4-IC7/PMPCS2/RF0 SDA2/CN15/RD6 SCL2/CN16/RD7 RG15 Vss1 74 VDD1 TAO/RC14 RE5/PMPD5 PMPD5/RE5 TA1/RC13 RE6/PMPD6 PMPD6/RE6 TA2/OC1/RD0 RE7/PMPD7 PMPD7/RE7 IC4/RD1 T2CK/RC1 IC3/RD10 GCK/RC2 IC2/RD9 (RC3 T4CK/RC3 IC1/RTCC/RD8 T5CK/RC4 RC4 INT4/RA15 RA15/INT4 RG6/PMPA5/SCK2 PMPA5/SCK2/CN8/RG6 U1A INT3/RA14 RA14/INT3 RG7/PMPA4/SDI2 PMPA4/SDI2/CN9/RG7 Vss5 12 PMPA3/SD02/CN10/RG8 RG8/PMPA3/SD02 100-Pin ICE OSC2/CLKO/RC15 OSC1/CLKI/RC12 MCLR 0SC1 14 PMPA2/SS2/CN11/RG9 RG9/PMPA2/SS2 VDD5 VDD5 RA5 RA5 16 VDD2 VDD2 RA4 RA4 17 _{RAO} (RAO RA3 18 INT1/RE8 RE8/INT1 RA2 RA2) 19 INT2/RE9 RE9/INT2 RG2/SCL1 RB5/AN5 TB2/C1IN+/AN5/RB5 SDA1/RG3 RG3/SDA1 RB4/AN4 TC1/SCK1/INT0/RF6 RF6/SCK1 TB3/C1IN-/AN4/RB4 RB3/AN3 SDI1/RF7 RF7/SDI1 TB4/C2IN+/AN3/RB3 RB2/SS1/AN2 SD01/RF8 RF8/SD01 RB1/AN1 U1RX/RF2 RF2/U1RX U1TX/RF3 RBO/ANO RF3/U1TX VDDCORE VDD2 VDD3 VDD4 VDD5 VDDCORE_ICE C8 _____C7 ____.1 μF C5 C2 C3 C4 Γ._{1 μF} † **†**.1 μF †.1 μF †10 μF .1 μF .1 μF

