Advanced FPGA Design / System Level Design with Intel FPGAs
Course Duration: (8 Weeks)
Commencing from Sunday, 29th Jan 2023 (Hybrid Mode)

Day	Topics	Learning Outcomes
Day-1	Introduction to Intel FPGAs	• Low end, Mid-range and High-end FPGAs • Introduction to Intel Quartus Prime design software • Lite, Standard and Pro editions • Downloading and Installation • Licensing and Device Support • **MAX 10 and Cyclone V devices** • **Arria 10, Stratix 10 and Agilex devices** • Internal Architecture of FPGAs • LUT and ALM • Memory and DSP resources • Clocking and I/O resources
Day-2	Verilog HDL and Advanced Verilog	• Data Flow, Structural and Behavioral modeling • FSM Modeling • Memory designs • Functions and Tasks • Synthesis Support • HDL coding Techniques • SystemVerilog Support
Day-3	Intel Quartus Design Software Tool flow	• Creating and managing projects • Simulation using ModelSim and Questasim • Analysis and Elaboration • I/O Assignments using Pin Planner • IP Catalog • Synthesis and Fitter • Programming File Generation and FPGA Implementation
Day-4	Timing Analysis using Intel Quartus Prime Timing Analyzer	• Understanding the basic timing parameters • Timing Analyzer • Creating basic and complex timing constraints • Timing Exceptions, Analyzing timing reports • Generating better SDC files • Achieving Timing Closure • Timing Closure recommendations for hyperflex devices • How to overcome setup and hold violations • Clock Domain Crossing Considerations • Last Mile Strategies • Tcl based Scripting flow
Day-5	FPGA Debugging Techniques	• Introduction to Signal Tap Logic analyzer • In System Sources and Probes • System Console

Day-6	Internal and External FPGA Memory	• Introduction to Intel FPGA Internal and External memory • Memory Initialization file • On chip RAM and SDRAM • In System memory content editor
Day-7	Platform designer	• Introduction to Platform designer • Create a system • Avalon and AMBA AXI interfaces • Incorporate the platform designer system into the Intel Quartus prime design software • Debug using Signal Tap and System console
Day-8	Embedded System using NIOS and ARM based SoC	• Introduction to Soft core processor • Embedded System using NIOS • Configure the NIOS II processor using Intel Quartus software and platform designer tool • Hardware Design Flow and Software Design Flow • ARM based SoC • Communication between HPS and FPGA • Introduction to HLS • Intel HLS Compiler and HLS Implementation for Matrix Multiplication and FIR filter

Hardware:

- Hands on Labs with MAX 10, Cyclone V and Arria 10 devices
- Timing Analysis and Platform designer sessions with Stratix 10 devices
- Design Migration Examples

Lab Exercises:

1. Basic Combinational and Sequential Logic Examples
2. FSM and Memory designs
3. High Speed Interfaces (DDR/Ethernet)
4. Embedded System design using NIOS II and NIOS V
5. Embedded System design using Cyclone V and ARM
6. Hardware and Software Design Flow
7. Timing Analysis and Timing Closure exercises
8. Intel FPGA Simulation and debug lab exercises
9. HLS implementation of 32-bit square root component, Matrix Multiplication and FIR Filter-RTL Vs HLS Examples
10. Intel FPGAs for AI/ML and Acceleration applications

Course Fee: Rs.15, 000/- (Excluding 18% GST)

25% discount for IETE Members.

50% discount for Students & Teaching Staffs.

Fee inclusive Course materials, Certificate and other miscellaneous charges.

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