EXPERIMENT No.4 :-Flip Flop Ic

1. Aim:-Study of Flip flop Ic

1. OBJECTIVE:-Verification of state tables of RS, JK, T and D flip-flops using various gates

3.THEORY:- : A Flip flop is a table electronic circuit that has two stable state .That is , its output is either +5V(logic 1) or 0V(logic 0) .A Flip Flop can be referred as memory device since its output will remain unchanged until its input is not changed. It is used to store one binary digit

R-S FLIP FLOP: A R-S Flip Flop is one that has two inputs R & S and two outputs Q & Q‟. AnR-S Flip Flop can be constructed using various gates gates.

Figure shows R-S Flip Flop constructed using four NAND gates.

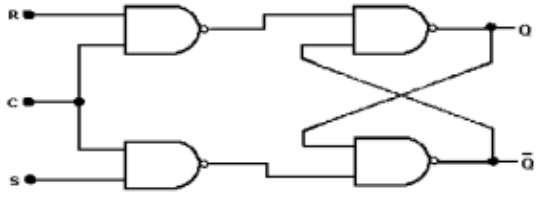


fig:-R-S flip flop

TRUTH TABLE:-*R-S FLIP FLOP*

CLK	S	R	Q (t+1)
0	X	X	NO CHANGE
1	0	0	NO CHANGE
1	0	1	0
1	1	0	1
1	1	1	FORBIDDEN

D- FLIP FLOP:- To avoid the forbidden case that occur in R-S Flip Flop, when R=S=1, D Flip Flop is implemented. In the D Flip Flop, there is only one input D as show in figure .We can transmit the value of D at the output of the Flip Flop when CLK is high.

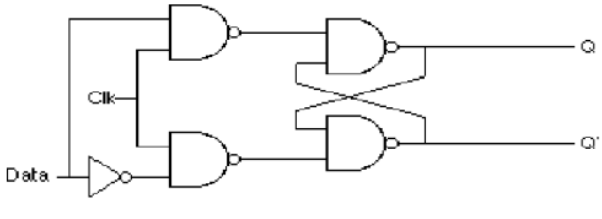


fig:-D-flip flop

TRUTH TABLE:-*D-FLIP FLOP*

CLK	D	Q (t+1)
0	X	NO CHANGE
1	1	1
1	0	0

J-K FLIP FLOP: - Setting R=S=1 with a R-S Flip Flop Q and Q‟ will set to the same logic level.This is an illegal conditions .The J-K Flip Flop accounts for this illegal input. It is used to build counter. The values of J and K determine what a J-K Flip Flop does on the next clock edge.When both are low, the Flip Flop retains its last state. When J is low and K is high, the Flip Flop resets. When J is high and K is low, the Flip Flop sets. When both are high the Flip flop toggles.In this last mode, the J-K Flip Flop can be used as a frequency divider.

CIRCUIT DIAGRAM:-

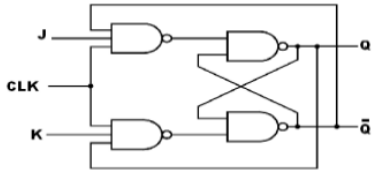


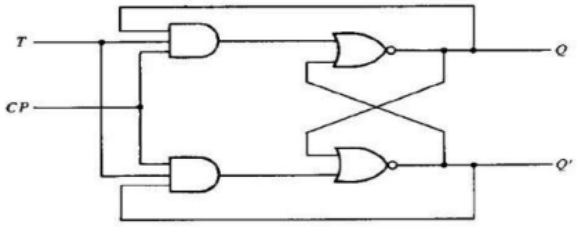
fig:-J-K FLIP FLOP

TRUTH TABLE:-*J-K FLIP FLOP*

CLK	J	K	Q (t+1)
0	x	X	NO CHANGE
1	0	0	NO CHANGE
1	0	1	0
1	1	0	1
1	1	1	TOGGLE

T- FLIP FLOP:- The T- Flip Flop is known as Toggle Flip flop. The T Flip flop is a modification of the J-K Flip flop by connecting both inputs J and K together. Figure shows the logic diagram of T flip flop ,logic symbol and truth table of T Flip flop is also shown.When T=0, both AND gates are disabled and hence there is no change in the previous output.When T=1(J=K=1) output toggles. Toggles means that the output is 0 when the previous state is 1 otherwise output is 1 when the previous state is 0. So the output is a complement of the previous output.

CIRCUIT DIAGRAM:-



fig;-T-FLIP FLIP

TRUTH TABLE:- *T-FLIP FLOP*

Preset State	Flip flop Input	Next State
Qn	T	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0

CONCLUSION:- In conclusion, this experiment has not only enhanced our theoretical understanding of flip-flop operation but also provided hands-on experience in working with essential digital logic components. As we move forward in our study of digital electronics, these insights will serve as a solid foundation for more advanced projects and applications.