The reduction for this problem is from CircuitSAT to SAT, which is an acyclic circuit with AND, OR, NOT gates and a single output wire to many different literals. Let w be the number of distinct wires in the circuit, then the size of the circuit is $\theta(w)$. But for a reduction like this, if there are many literals per clause, and each clause may have at most n literals, then the mapping/reduction may take $\theta(w^n)$, which is exponential but not polynomial time.