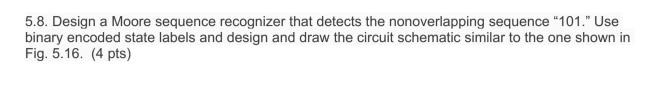
CSc 137 HW #4 (12 pts)

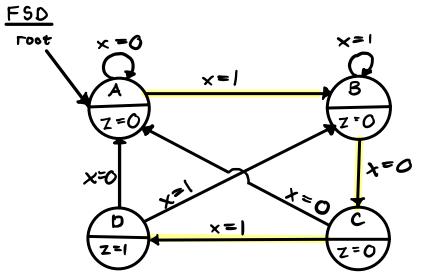


5.9. Design a Mealy sequence recognizer that detects the nonoverlapping sequence "101." Use binary encoded state labels and draw the circuit schematic similar to the one shown in Fig. 5.16. (4 pts)

5.10. Design a Moore sequence recognizer that detects the overlapping sequence "1001." Use binary encoded state labels. . (Step 1. FSD only) (4 pts)

5.8. Design a Moore sequence recognizer that detects the nonoverlapping sequence "101." Use binary encoded state labels and design and draw the circuit schematic similar to the one shown in

Fig. 5.16. (4 pts) Moore: depends on current state only



log a (# of states) = # of bits

output generator (OG)

	current state	output 2
ABCD	0000	000

Create NSG	from FSD
A=00	B=01
C=10	p=11

3

5

	Cor	rent	Input	Output		
	States		·	Output Next State		
			×	d,	do	
A	0	0	0	$\circ$	0	Å
A	0	0	I	0		В
B	0	1	0		0	C
$\beta$	$\bigcirc$	)	1	0		B
C		0	0	0	0	A
С	C	0	1			D
D	1	1	0	0	0	A
	l		1			B

$$d_{1} = \overline{X}\overline{A}B + XA\overline{B}$$

$$= 0$$

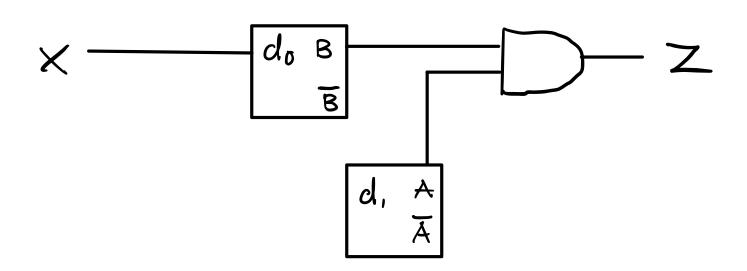
$$d_{0} = X = \overline{A}\overline{B}X + A\overline{B}X + A\overline{B}X + ABX$$

$$Z = AB$$

$$d_{0} = \emptyset$$

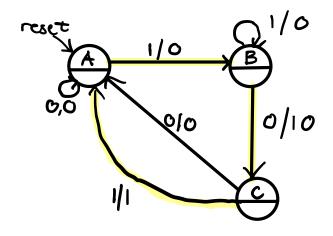
$$d_{0} = \times$$

$$Z = AB$$



5.9. Design a Mealy sequence recognizer that detects the nonoverlapping sequence "101." Use binary encoded state labels and draw the circuit schematic similar to the one shown in Fig. 5.16. (4 pts)

Mealy: both state & input



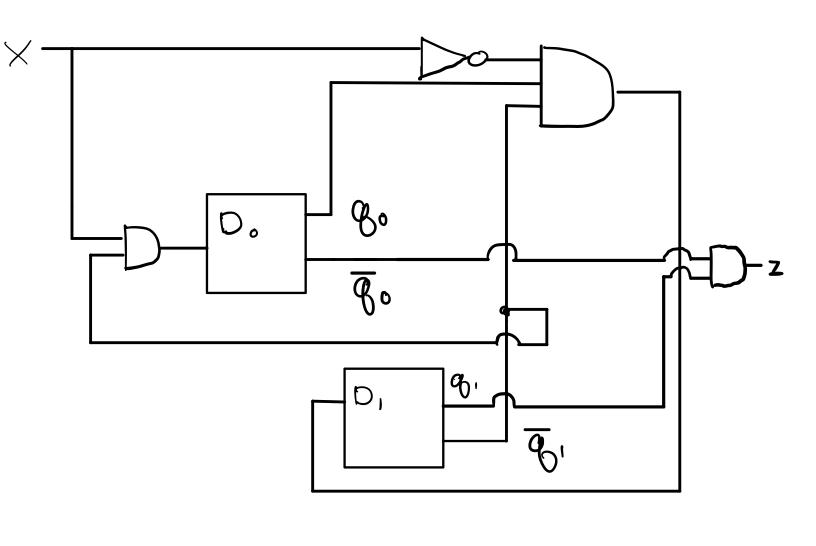
	current state	input	next state	out	
	<b>&amp;</b> , <b>&amp;</b> ,	×	d, d.	Z	
+	00	0	00	0	
	00	1	0 1	0	
3	0 1	0	10	0	
	0 1	1	01	0	
\ _	10	0	00	0	
	10	ſ	00		
	(	0			
		\			

$$d_{1} = \overline{g_{1}g_{0}} \times \overline{x}$$

$$d_{0} = \overline{g_{1}g_{0}} \times + \overline{g_{1}g_{0}} \times \overline{x}$$

$$= \times \overline{g_{1}}$$

$$Z = g_{1}g_{0}$$



5.10. Design a Moore sequence recognizer that detects the overlapping sequence "1001." Use binary encoded state labels. . (Step 1. FSD only) (4 pts)

