Problems 1.3, 1.4, 1.5, 1.14 (3 points each)

Reading assignment: Section 1.1 to1.4 (all sub-sections)

Advance reading assignment: Section 2.1 through .4 all sub-sections

1.3) What is the 16-bit FP representation of -5.375 in hex with 1 bit sign, 4-bit biased exponent, and 11-bit fraction, where bias offset = 7?

-5.375 to binary

$5 = 101_2$

$.375 \times 2 = 0 + .75$

$.75 \times 2 = 1 + .50$

$.50 \times 2 = 1 + .00$

$\rightarrow -(101.011)_2$

$= -(1.01011)_2 \times 10^2$

biased exp = unbiased exp + biased offset

b.exp = 2 + 7

= 9

= 1001

1 1001 01011000000

1 bit sign | 4 bit biased exp | 11 bit fraction

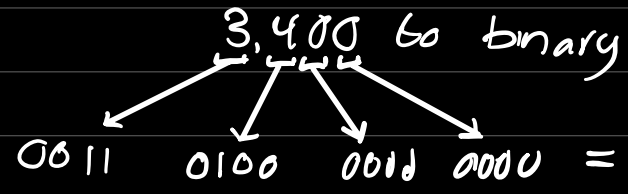
conversion

$(1100\ 1010\ 1100\ 0000)_2$

12_{10} 10_{10} 12_{10} 0_{10}

$(CAC0)_{16}$

1.4) What is the real number equivalent to FP number 0x3400 with 1-bit sign, 4-bit biased exponent, 11-bit offset = 7?



0011 0100 0000 0000

1 bit sign | 4 bit biased exp | 11 bit fraction

biased exponent = unbiased exp +/- biased offset

$= (0110)_2 - 7$

$= 6 - 7$

$= -1$

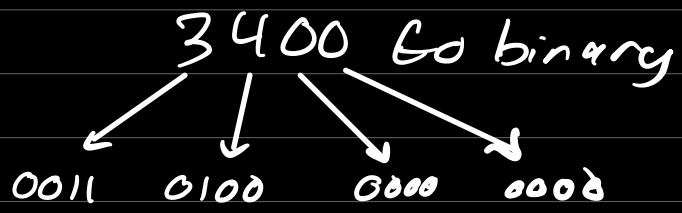
fraction bits $= 0.100\ 0000\ 0000 = 1 \times 2^{-1}$

real number $= +/- (1 + \text{fraction bits}) \times 2$

$= + (1 + 0.5) \times 2^{-1}$

$= 0.75$

1.5 What is the real equivalent to FP equivalent to FP number 0x3400 with 1-bit sign, 4-bit biased exponent, 11-bit fraction, and biased offset = 8



0 011 0100 0000 0000
sign bit | 4 bit bias | 11 bit fraction

2^{10}

biased exponent = unbiased exp +/- biased offset
$= (0110)_2 - 8$
$= 6 - 8$
$= -2$

fraction bits $= 0.100\ 0000\ 0000 = 1 \times 2^{-1}$

real number $= +/-(1 + \text{fraction bits}) \times 2^{\text{biased exp}}$
$= +(1 + 0.50) \times 2^{-2}$
$= 1.5 \times 0.25$
$= 0.375$

1.14) What is a Von Neumann architecture bottleneck?

The Von Neumann architecture bottleneck is a limitation of accessing memory in basic computer architecture. The three main operations fetch, decode, and execute can all occur in memory, which presents the problem of only being able to do one at a time sequentially. Executing an instruction is fast but reading/writing to memory is very slow by comparison, meaning you have to wait for more memory before processing something. This problem is exacerbated by the fact that the performance of CPUS increases faster over the years compared to memory.

The disadvantage of Von Neumann architecture is that memory for instructions and data are unified and shared with one data bus and one address bus between processor and memory. Instructions and data have to be fetched in sequential order, known as the Von Neumann Bottleneck, which limits the bandwidth of memory accesses. It is common in microprocessors today to have the level 1 cache separated into instruction and data caches which helps bandwidth.