HW#5

CSc 137

Problem I: Consider the sequential circuit in Figure 5.31 where the adder is a CLA. Its simplified circuit is shown in Figure 5.32. Assuming that the Flip-Flips register set-up time, clock-to-q, and clock-skew are each 0.1 ns, AND gate = 0.2 ns and EXOR = 0.3 ns determine the upper bound for its clock frequency. (10 pts)

set-up, clock-to-q, clock skew : 0.1ns

AND gate = 0.2ns

EXOR = 0.3ns

$$\underbrace{0.1 + 0.1 + 0.1}_{\text{set-up, clock-to-q, clock skew}} + \underbrace{0.2(2)}_{\text{AND}\times 2} + \underbrace{0.3}_{\text{EXOR}}$$

upper bound = 10 ns

clock freq in hz : $\frac{1}{10 \cdot 10^{-9}}$ ns

$= 100,000,000$ hz

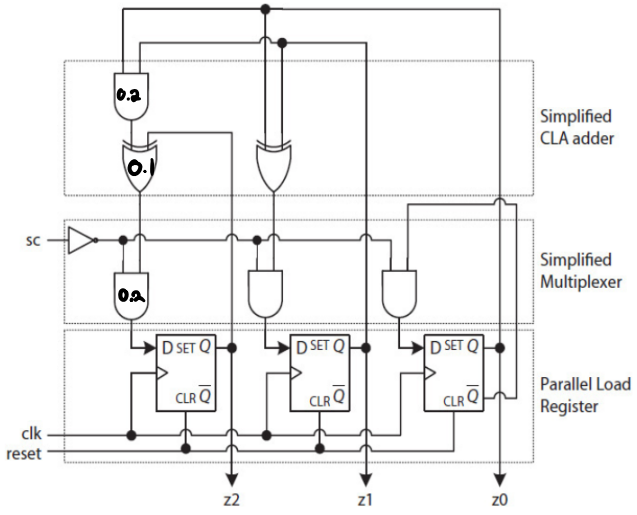

FIGURE 5.32 A synchronously cleared bit-parallel mod-8 up-counter using a simplified CLA adder and a simplified MUX.

In order to design a bit-parallel *k*-bit counter slice, the slice must include both the *i* and *o* interface signals that were discussed earlier in the design of

Problem III: Textbook problem 5.11 (only FSD) (5 pts)

5.11) Design Mealy sequence recognizer that detects the overlapping sequence "1001". Use binary encoded state labels.