Kevin Cendana

HW#6

CSc 137, Singh

(20 Points)

For problems 6.1 through 6.3: Suppose the propagation delay of an 8-bit adder is 0.8ns, adder/subtractor is 1.1ns, 2-to-1 mux is 0.3ns, and 4-to-1 mux is 0.6ns. Also, assume register setup time (τ_{st}), clock-to-q (τ_{cq}), and clock-skew (τ_{cs}) are all 0.05ns. (15 points)

6.1 Calculate the required maximum clock frequency for each of the following data paths:

a. Single-cycle data path in Fig. 6.2.

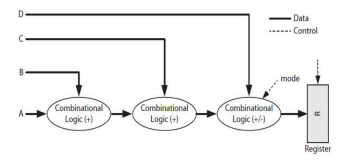


FIGURE 6.2 A single-cycle two-function data path that computes either $A + B + C + D$ or $A + B + C - D$ in one clock cycle.

$\tau \geq 2\Delta_{ADD} + \Delta_{ADD/SUB} + \tau_{st} + \tau_{cq} + \tau_{cs}$

① delay in ns: $0.8_{\text{adder}} + 0.8_{\text{adder}} + 1.1_{\text{adder/subtractor}} + 0.05_{ns}(3)_{T_{st}+T_{cs}+T_{cq}} = 2.85\,ns$

② ns → μs: $2.8\,ns \cdot \frac{10^{-3}\,ms}{1\,ns} = 0.028\,\mu s$

③ time → frequency (μs): $\frac{1}{\text{period}} = \frac{1}{0.00285\,\mu s} = \sim 351\,mhz$

b. Multi-cycle data path in Fig. 6.3.

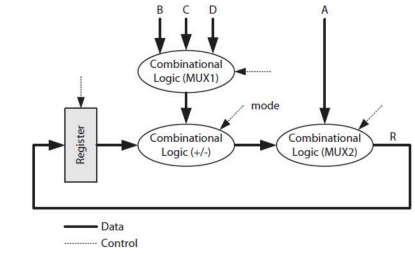


FIGURE 6.3 A multicycle data path requiring four clock cycles to compute $A + B + C + D$ or $A + B + C - D$.

① delay in ns: $\tau \geq \Delta_{MUX1} + \Delta_{ADD/SUB} + \Delta_{MUX2} + \tau_{st} + \tau_{cq} + \tau_{cs}$

$0.3_{mux1} + 1.1_{add/sub} + 0.6_{mux2} + 0.05(3)_{T_{st}+T_{cs}+T_{cq}} = 2.15\,ns$

② ns → μ: $2.15\,ns \cdot \frac{10^{-3}\,\mu s}{1\,ns} = 0.00215\,\mu s$

③ time → Freq: $\frac{1}{\text{period}\,(\mu s)} = \frac{1}{0.00215} = \sim 465\,mhz$

c. Pipelined data path in Fig. 6.4.

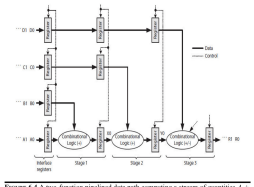


FIGURE 6.4 A two-function pipelined data path computing a stream of quantities $A_i + B_i + C_i \pm D_i$ for $i = 0, 1, 2$, etc.

① $4 \cdot 0.15 + (4-1) \cdot 0.15 + 3 * 0.15 + 0.8(2) + 1.1 = 4.2\,ns$

② ns → μ: $4.2\,ns \cdot \frac{10^{-3}\,\mu s}{1\,ns} = 0.0042\,\mu s$

③ time → freq: $\frac{1}{0.0042\,\mu s} = 238\,mhz$

6.2 Estimate the speedup between the following data paths when generating N = 1000 quantities $A_i + B_i + C_i \pm D_i$ for i = 0, 1, 2, …, 999. Ignore the data reading and writing delays. (5 points)

a. Problem 6.1a vs. 6.1c

$$\text{Speed up} = \frac{NK}{K+N-1} = \frac{(1000)(3)}{3+1000-1} = \frac{3000}{1002}$$

$$= 2.99$$

Extra Credit: 10 points

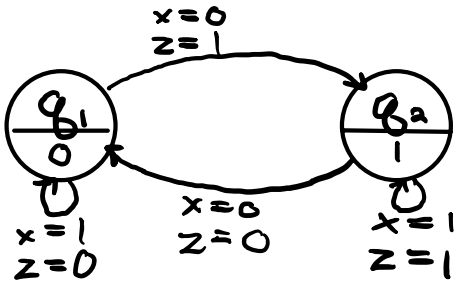
5.1 Non-return-to-zero inverted (NRZI) is a data coding scheme used to communicate with USB devices. The output signal (z) of a NRZI generator transitions when the input bit (x) is 0 and remains at constant previous value (0 or 1) when the input bit is 1. That is, from right to left when the input to the NRZI generator is 0 0 0 0 0 0, its output from right to left will transition as 1 0 1 0 1 0. Its output for consecutive 1s at the input, however, will remain at the previous output value. For example, the NRZI generator outputs from right to left z: 0 0 0 0 0 1 0 1 1 1 1 0 1 0 1 1 for input X: 1 1 1 1 0 0 0 1 1 1 0 0 0 0 1 1 read from right to left. Likewise, for X = 0xCF0C, Z: 0xEFAE. Design the NRZI generator. Design the circuit for the NRZI (Hint: design a Mealy FSM). (5 points)

ex) l → r

curr: 1 1 1 0 1 0 1 1 1 1 0 1 0 0 0 0

in: 1 1 0 0 0 0 1 1 1 0 0 0 1 1 1 1

out: 1 1 0 1 0 1 1 1 1 0 1 0 0 0 0 0



current state	input	next	output
q_0	x	d_0	z
0	0	1	1
0	1	0	0
1	0	0	0
1	1	1	1

$d_0 = z + \bar{q_0}\bar{x} + q_0 x$

x AND q_0 OR $\bar{x}$ AND $\bar{q_0}$ OR z

= x XNOR q_0 OR z