HW#7

CSc 137

(25 points)

P1. In order to minimize the duration of a read cycle, the _oe can be asserted at any time within a maximum time after the _ce is asserted, as illustrated in the timing diagram. **(5 pts)**

A. True

B. False

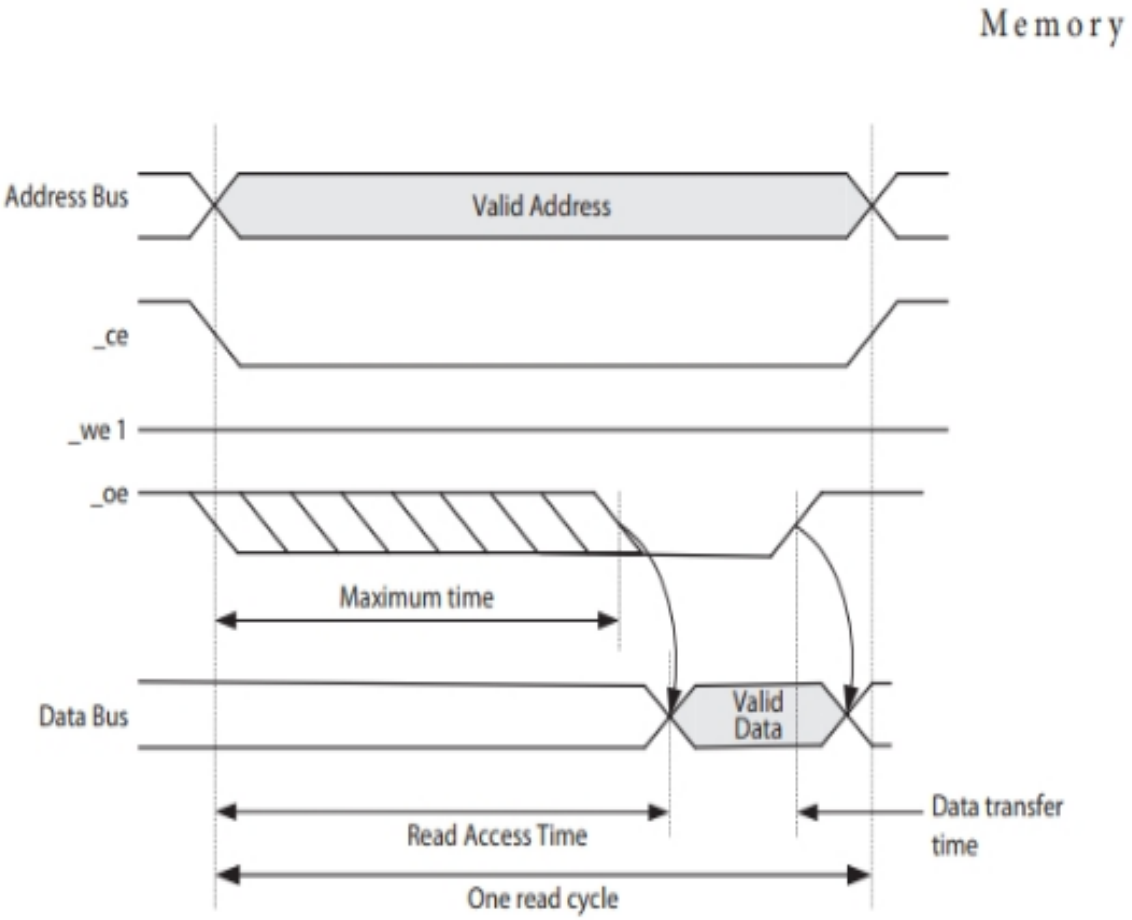

FIGURE 7.16 An SRAM read cycle from the memory point of view.

P2. A memory write cycle is similar to a read cycle, except that data must be placed on the data bus at the same time that _ce is asserted or within a maximum delay after _we is asserted to minimize the time the data bus is used. Figure 7.17 illustrates an SRAM memory write cycle. **(5 pts)**

I. A memory cycle is initiated by which component in the computer motherboard?

① dram controller

II. A memory cycle, typically, how many CPU clock cycles to complete?

② usually multiple, depends on type of memory, clock frequency, memory access mode

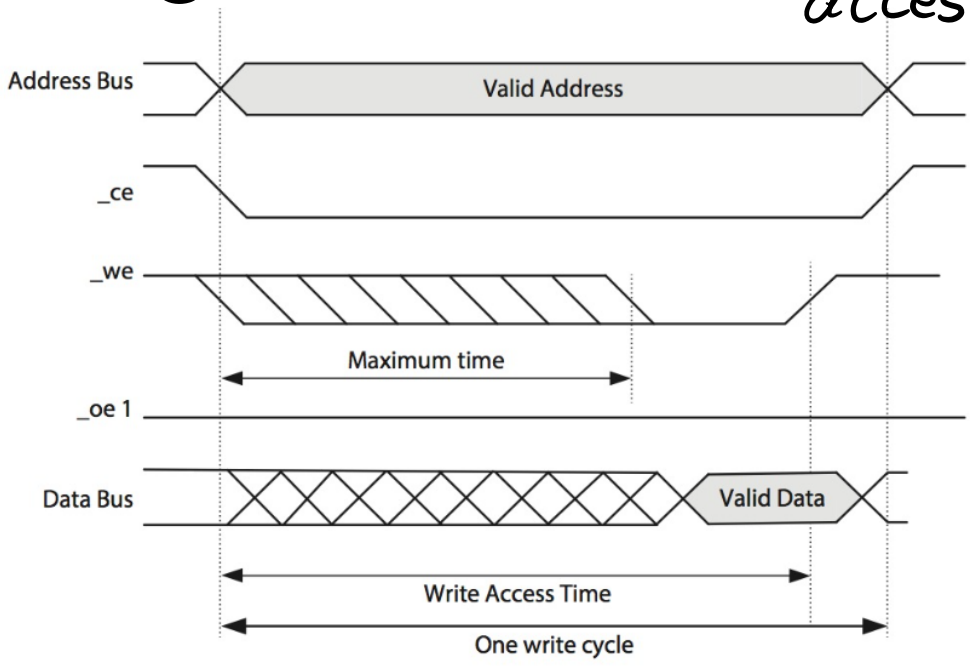

FIGURE 7.17 An SRAM write cycle from a memory point of view.

7.10 Consider a 32-bit data bus SDRAM. Given that the clock frequency of the bus is 200MHz, what is the peak memory bandwidth in megabyte per second (MBs)? **(5 pts)**

SDRAM peak memory bandwidth =
(data bus width/8)* Clock freq
32 bit 200mhz

$(32\text{ bit}/8) \cdot 100\text{ MHz} = 800\text{ MBs}$

7.11 Consider a 64-bit data bus SDRAM. Given that the clock frequency of the bus is 200MHz, what is the peak memory bandwidth in megabyte per second (MBs)? **(5 pts)**

$(64\text{ bit}/8) \cdot 100\text{MHz} = 1{,}600\text{ MBs}$

7.12 Consider a 32-bit data bus DDR SDRAM. Given that the clock frequency of the bus is 200MHz, what is the peak memory bandwidth in megabyte per second (MBs)? **(5 pts)**

DDR SDRAM peak memory bandwidth =
(data bus width/8)* Clock freq *2
32 bit 200MHz

$(32\text{ bit}/8) \cdot 200 \cdot 2 = 1{,}600\text{ MBs}$