

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORT, LAT and TRIS registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, **ODCx**, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than V_{DD} (e.g., 5V on a 5V tolerant pin) by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification for that pin.

See the “**Pin Diagrams**” section for the available pins and their functionality.

11.2 Configuring Analog and Digital Port Pins

The **ANSELx** register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding **ANSELx** and **TRISx** bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding **ANSELx** bit must be cleared.

The **ANSELx** register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default. Refer to the Pinout I/O Descriptions (Table 1-1 in Section 1.0 “**Device Overview**”) for the complete list of analog pins.

If the **TRISx** bit is cleared (output) while the **ANSELx** bit is set, the digital output level (V_{OH} or V_{OL}) is converted by an analog peripheral, such as the ADC module or Comparator module.

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the pins defined as Analog in Table 1-1 in Section 1.0 “**Device Overview**”) can cause the input buffer to consume current that exceeds the device specifications.

11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be an **NOB**, as shown in Example 11-1.

11.3 Input Change Notification

The input change notification function of the I/O ports allows the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the CN functionality of each I/O port. The **CNENx** registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the **CNPUx** and the **CNPDx** registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note: Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

```
MOV    0xFF00, W0    ; Configure PORTB<15:8>
                        ; as inputs
MOV    W0, TRISB     ; and PORTB<7:0>
                        ; as outputs
NOP                                ; Delay 1 cycle
BTSS   PORTB, #13    ; Next Instruction
```