AM Receiver
Lab Report

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1.Introduction

The purpose of this lab is to help us have a better understanding of some fundamental building blocks of electronic circuit, signal modulation, and some basic principles of multistage circuit design.

The function of the AM receiver is to receiver the AM radio signal via an antenna and output the received signal through a speaker. The received AM signal has two components, a relatively low frequency baseband signal (0-200 kHz for audio signal) that contains the information, and a high frequency carrier signal to modulate the baseband signal. The AM speaker has 4 stages as shown in fig 1.1 below, the first stage is to amplify the received AM signal, the second stage demodulates the AM signal, the third stage amplifies the demodulated AM signal (baseband signal), and the last stage outputs the baseband signal.

This report demonstrates the specific theory discussion and the analysis each of the individual stages and the whole system.

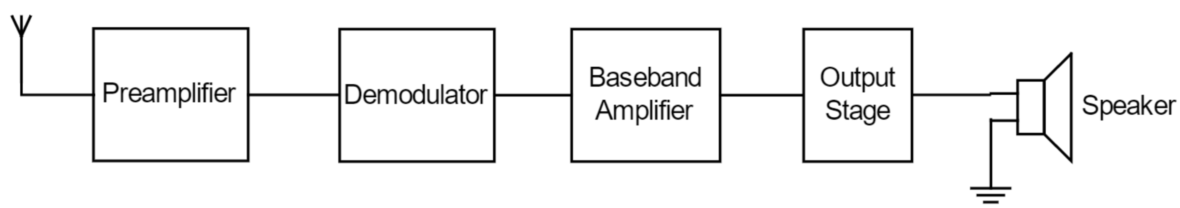

Fig 1.1 System level diagram of AM receiver

2.Preamplifier

2.1 Objective

The first stage of the AM receiver is the preamplifier, namely it amplifies the weak AM radio signal received via the antenna that has a certain carrier frequency (it filters out the unwanted signal that has different frequency). It is capable of being tuned into the desired radio carrier frequency through a variable capacitor.

2.2 Theory

As shown in fig 2.1, the preamplifier consists of an amplifier that has a LC tank on top to select the desired frequency and a Darlington pair output stage for a high output impedance at the collector of T_2 for small output loads.

The resistances R_4, R_5, R_6, and R_7 ensure the transistors T_2 and T_1 remain in active mode, the capacitor C_2 is to remove the DC offset of the input signal, C_3 and C_b remove the noise and stabilize the two DC bias points. The resistor R_E biases the current at the base of T_1, we want the current to be large to get a large gain and small bandwidth, thus R_E needs to be as small as possible (we choose R_E to be 10Ω).

For the LC tank a small resister is drawn in the diagram to take the non-ideal inductor into account. Depending on the value of the inductor and the capacitor, the impedance of the tank will peak at the resonant frequency. The resonant frequency can be calculated by the following equation:

$$f_{res} = \frac{1}{2\pi\sqrt{L_T C_T}}$$

The cascading transistors T_3 and T_4 has a large input impedance to be very large. This resistance is $(\beta+1) * R_{b4} = (\beta+1)^2 * (r_{e4}+R_9)$. This will make sure the LC tank has a narrow bandwidth. Since any energy stored in the LC tank has the tendency to leak from the collector of T_2 to ground, namely as the energy in the tank losing the bandwidth of the tank is getting larger. To minimize the energy loss and the band width, a high impedance at the critical node is required. The resistance R_9 at the emitter of T_4 biased the current and increase the input impedance for the Darlington pair.

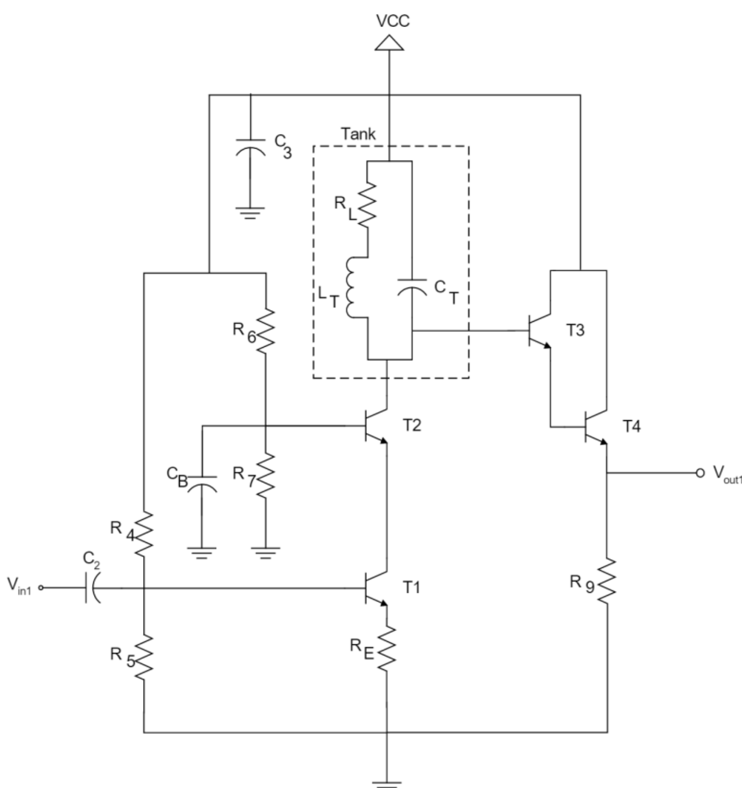

Fig 2.1 preamplifier schematic

2.3 Experiment

For the experiment, the group was assigned a resonant frequency of 1.04MHz, to achieve this resonant frequency we choose the resistor, capacitor and inductor value as follow:

$R_E = 10\Omega$	$R_6 = 1.3K\Omega$	$L_T = 150$ uH
$R_4 = 3.3K\Omega$	$R_5 = 1.7K\Omega$	$C_T = 150$ pF
$R_7 = 3.7K\Omega$	$R_9 = 1K\Omega$	

With those values the spice simulation gives us a resonant frequency of 1.06MHz.

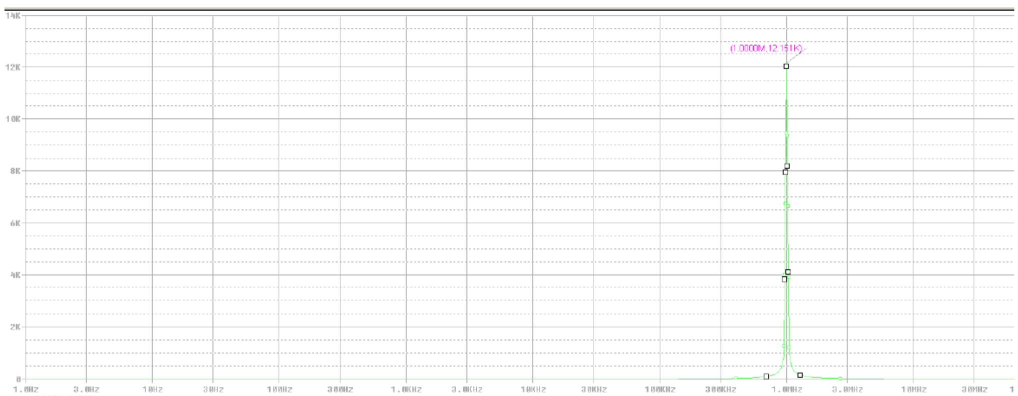

Fig 2.2 frequency response spice simulation

In the lab, we implemented a voltage divider at the input of the circuit, and since there were some oscillations in the circuit, we changed the value of R_5 and R_7 to $1K\Omega$ and the value of R_6 and R_4 to 1.5 $K\Omega$, we also changed the value RE to 100Ω. We changed the L_T and C_T in the tank to 82μH and 270 pF respectively. Then the resonant frequency appeared at 1.14 MHz with a maximum gain of 87 (theoretical input voltage is 6.7mV after the voltage divider) as shown in fig 2.3, and the plot of the frequency response is shown in the fig 2.4, the 3-dB band width is about 70KHz.

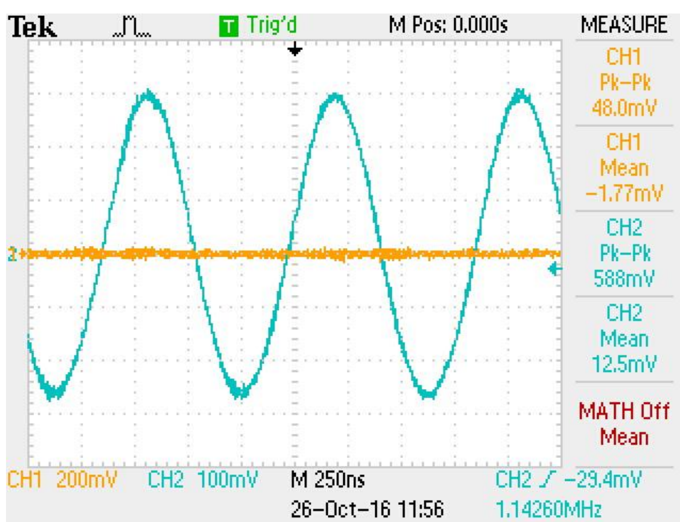

Fig 2.3 output voltage screen shot

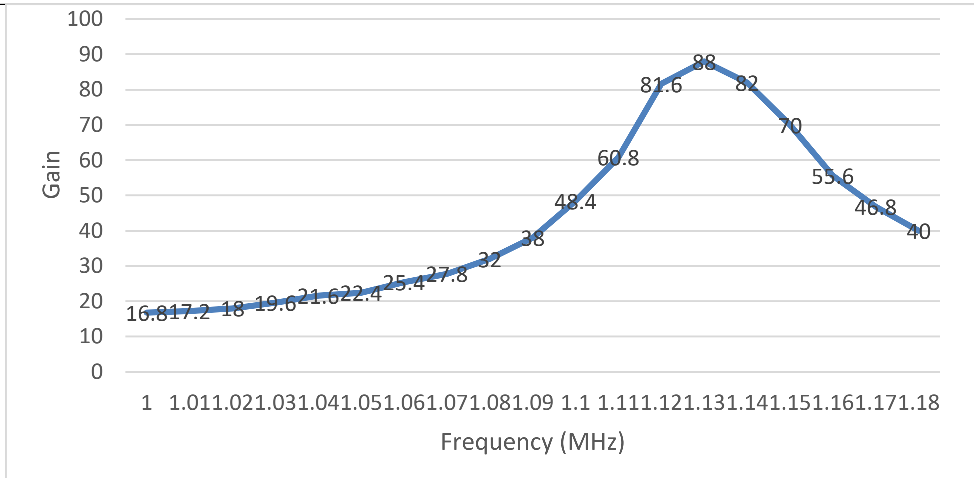

Fig 2.4 frequency response plot

2.4 Discussion

The preamplifier has enough gain but the bandwidth is a bit large, this could leave some undesired frequency not filtered out, and have an impact on the AM receiver's audio quality. This problem might be caused by the resistance RE being not large enough and makes the quality factor not large enough. Moreover, the value of RE could be too large, if we make the RE smaller, the gain will be larger and reduce the bandwidth.

3. Demodulator

3.1 Objective

The second stage of the AM receiver is the demodulator; it extracts the baseband signal from the AM signal input namely the upper envelop of the AM signal (as shown in the fig 3. 1). The circuit is shown as fig 3.2.

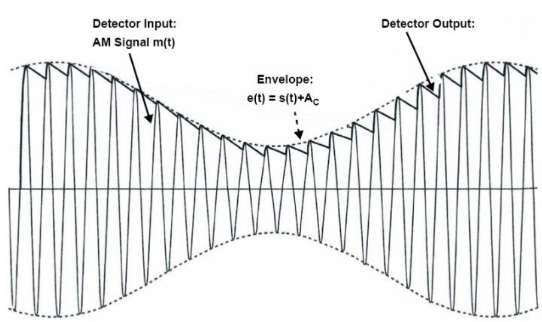

Fig 3.1 Modulated Signal

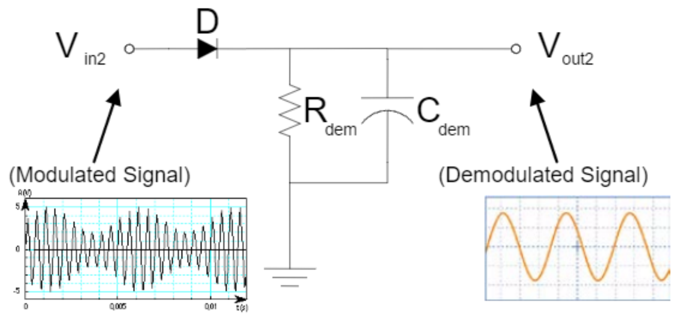

Fig 3.2 Circuit

3.2 Theory

As shown in fig 3.2 the diode allows only positive part of the AM signal to pass through. The capacitor charges when the input signal voltage is rising and it discharges slowly when the input signal is falling. Thus it is able to catch the next rising edge of the input signal, if the carrier frequency is much larger than the baseband signal frequency, the output signal will have a decent resolution that is very close to the baseband signal. The resistance and capacitance are chosen specifically to make the demodulator circuit to have a time constant that is smaller than the period of the baseband signal and larger than the period of the carrier signal (as shown in the equation below).

$$f_b < \frac{1}{2\pi RC} < f_c$$

3.3 Experiment

Since the wanted baseband signal is in the 0 – 20kHz range and the unwanted carrier signal is in the 200kHz -1 .2 MHz range. We chose our R_{dem} to be 150 kΩ and C_{dem} to be 47Pf so that the resulting cutoff frequency would be 22.6kHz, which is larger than 20kHz and significantly smaller than the carrier signal frequency. There will be 0.3V voltage drop across the 1N34A diode, so the DC point at the input of the modulator should be biased to compensate for the offset. In addition, the loading effect caused by the input resistance of the circuit that our demodulator passing signal into, will affect our time constant (makes it smaller since our Rdem here is large) and the behavior of the demodulator would be affected. In the actual operation, we decreased the value of R_{dem} and consequently increased the value of the C_{dem}, to make sure the cutoff frequency is in the wanted range without affecting demodulator.

We used the signal generator to build a modulated signal with baseband signal of 10kHz and carrier signal of 600kHz. The experiment result is shown below (fig 3.3),

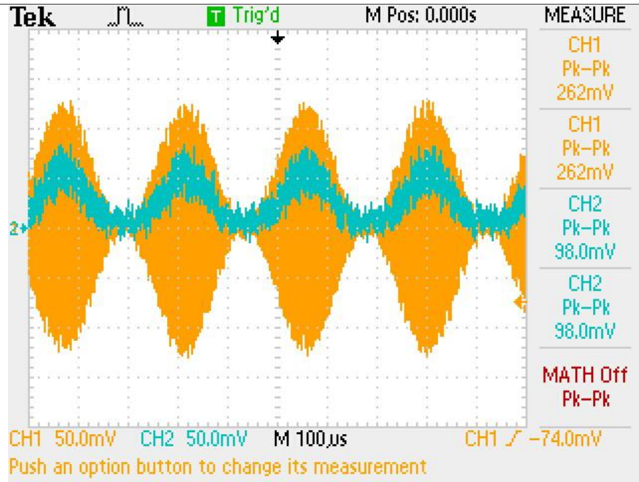

Fig 3.3

Also, the circuit should be designed in a way such that the gain won't be affected by the changes of the baseband signal frequency and the carriers signal frequency. To see if the rule is respected, we plotted the result that the baseband signal frequency was varied while the carrier signal frequency remained in constant (fig 3.4). Similarly, the result that the carrier signal frequency was varied while the baseband signal frequency remained constant (fig 3.5).

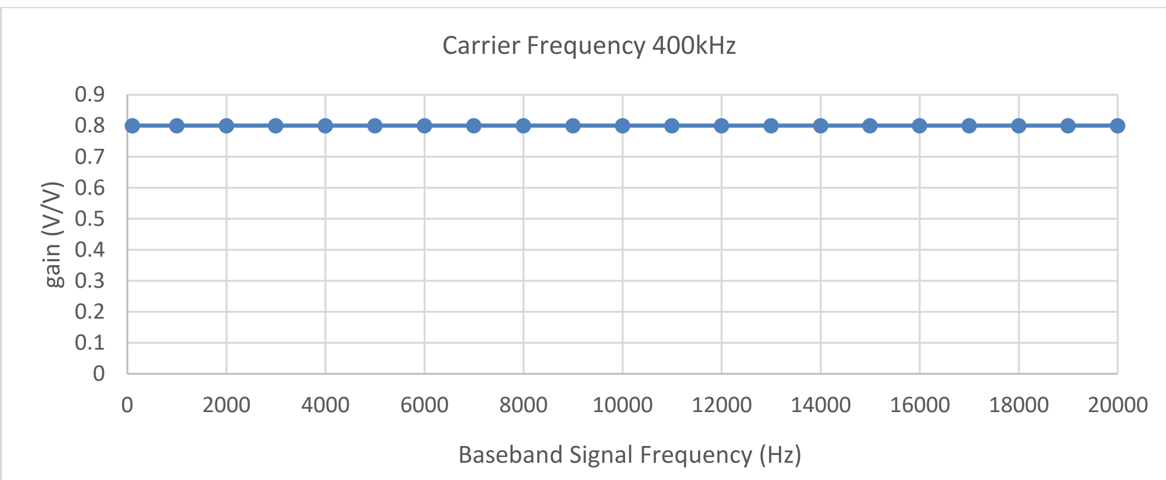

Fig 3.4 Carrier Frequency remained in constant

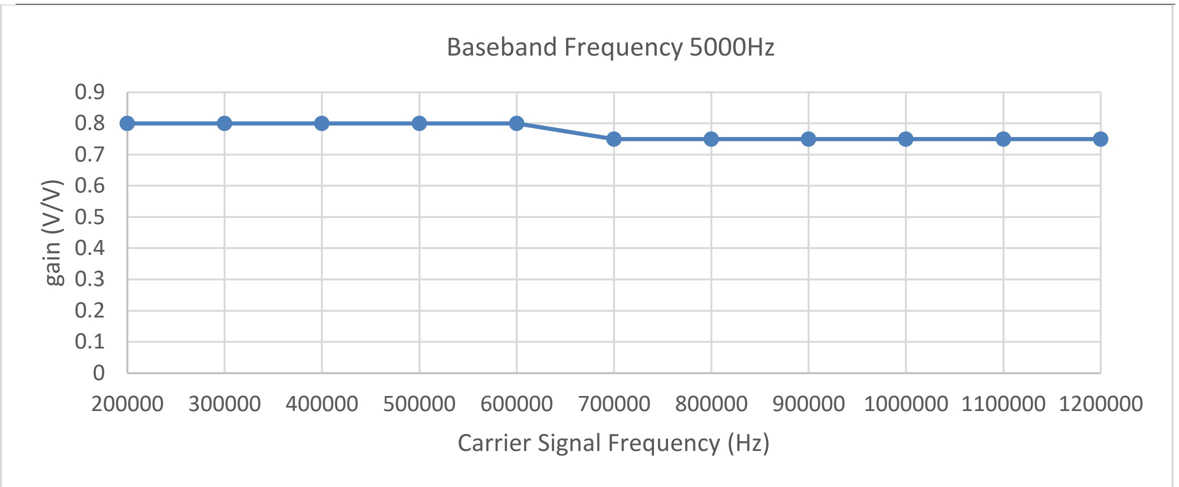

Fig 3.5 Baseband Frequency remained in Constant

3.4 Discussion

As expected, the modulated input signal is demodulated at the output, that is, the envelope is detected. However, the demodulated signal in our experiment is not ideal comparing to our simulation result (fig 3.6), which can be explained by the errors caused by the measurement and hardware devices. The gain is isolated from baseband signal frequency and carrier signal frequency, which is what the envelope detector should behavior.

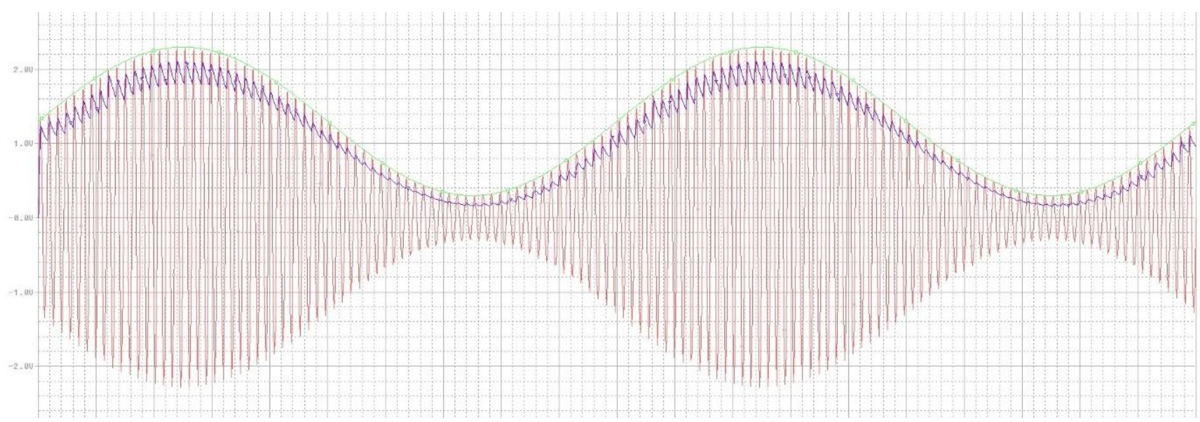

Fig 3.6 Spice simulation result

4.Baseband amplifier

4.1. Objective

The baseband amplifier is the third stage of the AM receiver; it amplifies the baseband signal input from the demodulator stage. At this stage the volume (the gain) can be controlled through a potentiometer.

4.2 Theory

As shown in the fig 4.1 below, the input of this stage is an RC circuit, the capacitor C_1 is aim to block any DC component of the input signal, and the resistance R_1 provides a DC path for bias current and ensures the positive input of the Op-Amp will have a 0V steady DC input. The operational amplifier is configured as a non-inverting amplifier and the gain equation is G= $\frac{R_2}{R_{pot}}$ +1 when C_1 is neglected, if C_1 is taken in to account the gain equation becomes:

$$G = \frac{R_1}{R_1 + \frac{1}{S_{c1}}} * (\frac{R_2}{R_{pot}} + 1)$$

Since a potentiometer is connected in to the circuit, the total gain of this stage can be changed by changing the resistance of the potentiometer. However, a larger gain leads to a smaller bandwidth since the product of the gain and the bandwidth should be a constant, making sure the bandwidth covers the frequency range of audio signal (0-20kHz) is necessary.

The input resistance of this stage is close to R_1 since R_1 is connect in parallel with the input resistance of the operational amplifier which is infinity. The output resistance is zero since the output resistance of an operational amplifier is considered to be 0.

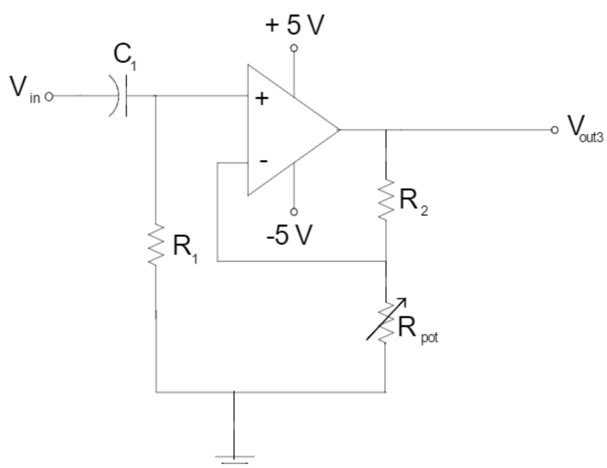

Fig 4.1 baseband amplifier schematic

4.3 Experiment

The assigned gain is 150 V/V for the baseband amplifier, we choose our R_2 and R_{pot} to be 450 KΩ and 3020Ω respectively. As shown in fig 4.2 our output voltage is 1.72V, the input voltage in too small to measure for the oscilloscope, thus we use the theoretical value which is 11 mV. This gives us a gain of 156 V/V. The frequency plot is shown in the fig 4.3 and the band width is very large and satisfied the desired band (0-20KHz) width completely, for the lower 3 dB cutoff frequency we assume to be 50 Hz since the function generator was unable to produce a wave that has such low frequency, the upper 3dB cutoff frequency is 26KHz, which gives us a bandwidth of 25.5kHz. The gain-bandwidth product is

GDWP=Gain*BW=156*26000=4056000

The gain is decreasing as we increasing the potentiometer as shown in fig 4.4.

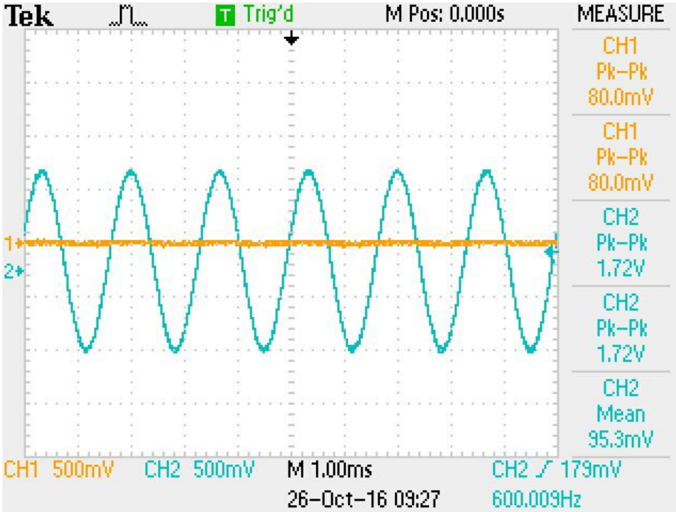

Fig 4.2 output voltage screen shot

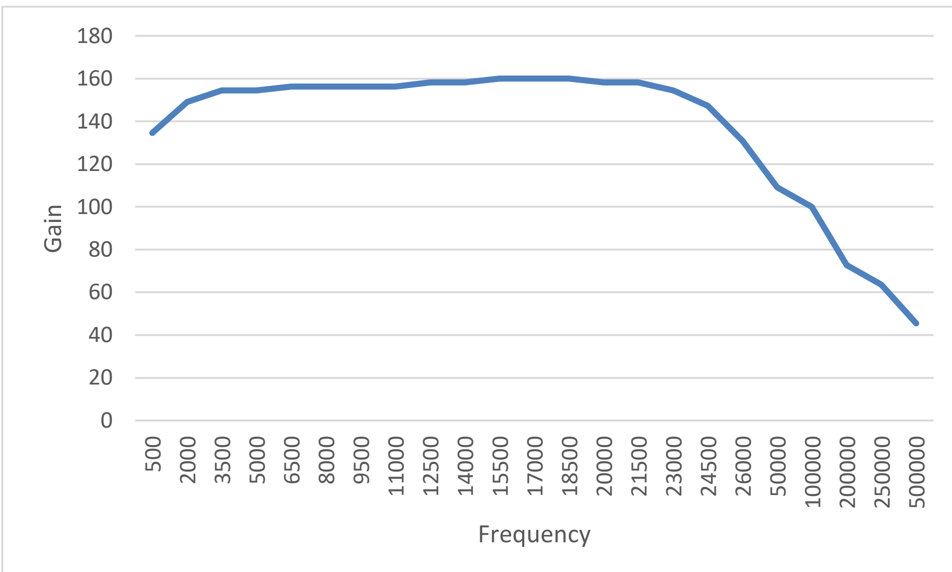

Fig 4.3 frequency response

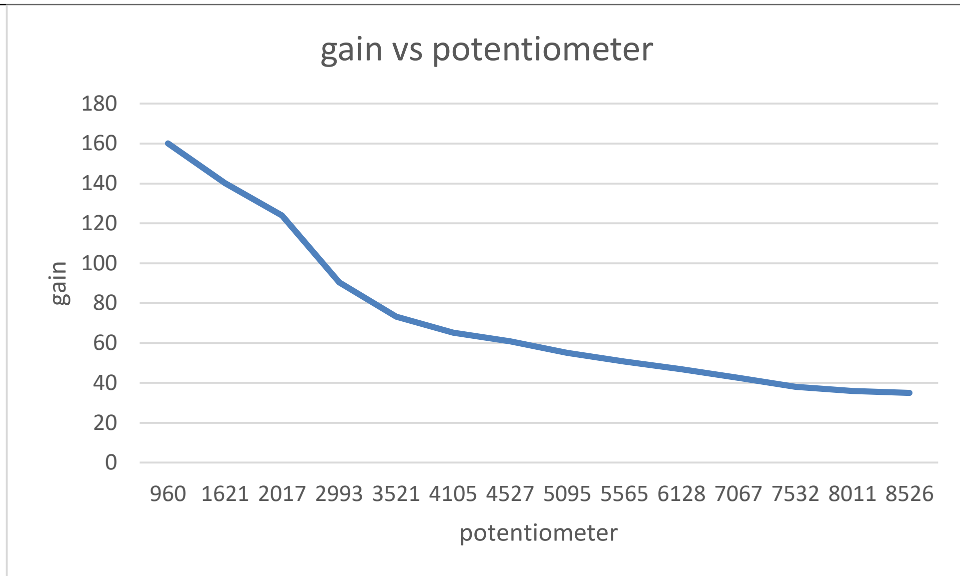

Fig 4.4

4.4 Discussion

The frequency response is different compare to our simulation; however, our baseband amplifier still satisfies the design requirement. The gain decreases as the resistance of the potentiometer increase just like the equation we derived in the theory part (G= $\frac{R_2}{R_{pot}}+1$). The input resistance is similar to the theoretical value (150KΩ). the offset might be caused by either the inaccuracy of resistor value of R_1, or the input resistance of the operational amplifier is not actually infinity.

5. Class A Output stage

5.1 Objective

The class A output stage is the last stage of the AM receiver. It serves as a power amplifier to supply sufficient power to the speaker which is a low impedance load. The circuit is shown below (fig5.1).

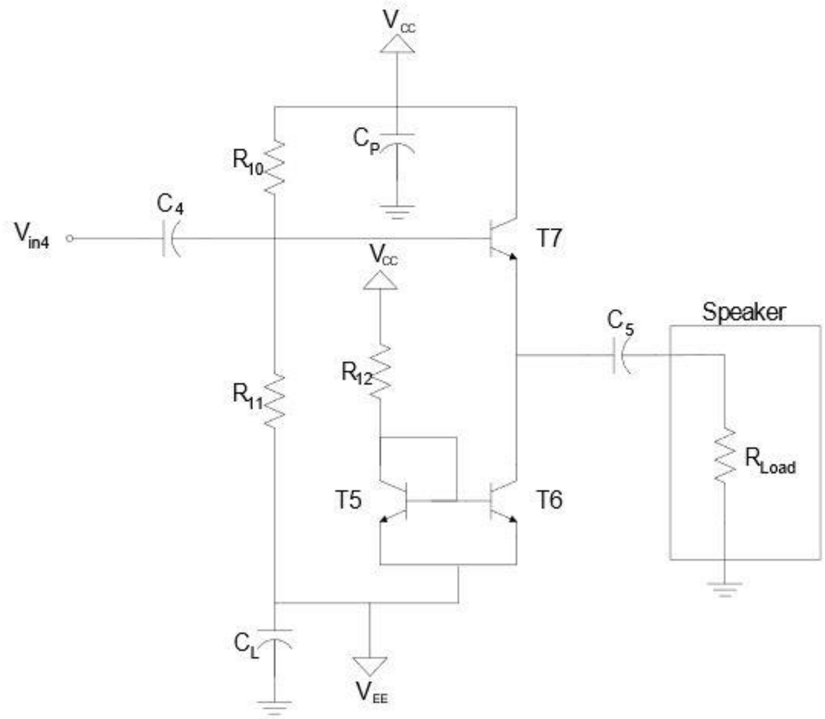

Fig 5.1 Circuit Schematic

5.2 Theory

As stated above, the class A output stage is a power amplifier connected to a speaker. The speaker has low input impedance which could draw lots of power. The class A output stage is not really power efficient since the transistor T7 is biased such that it is always on, T7 conducts for the entire circle of the input signal so that the circuit is always consuming power. The power is lost in the form of heat. However, class A output stage is easy to build and there can be no crossover or switch-off distortion to the output wave form.

The capacitor C_4 and C_5 are decoupling capacitors which is used to remove DC offset. The capacitor C_p filters the noise coming from the supplies. The resistor R_{10} and R_{11} are bias resistors for base voltage of T7. The current of the output stage is biased using a current source which is a current mirror (T5 and T6). The current mirror is biased by the resistor R_{12} so that the current passing through R_{12} is the same as the current going in the collector of T6. The I_{bias} is calculated by the equation below,

$$\boldsymbol{I_{bias}} = \frac{\boldsymbol{V_{CC}} - (\boldsymbol{V_{EE}} - \boldsymbol{V_{BE5}})}{\boldsymbol{R_{12}}}$$

The maximum output voltage swing is determined by the DC voltage supply and it cannot be too high or low such that the BJTs would be inactive.

$$V_{max} = V_{CC} - |V_{SAT}|$$
$$V_{min} = V_{EE} + |V_{SAT}|$$

However, the minimum voltage is also limited by the biasing current and the impedance of the load, which would cause the clipping effect.

$$V_{min} = - I_{bias} * R_L$$

The gain of this output stage is ideally unity.

5.3 Experiment

As we are asked to design the circuit such that the biasing current is sufficient to supply a 1V peak to peak amplitude signal to an 8Ω load, R_{12} is calculated to be less than 148.8Ω. To maintain the zero DC point at the output and the 0.7V voltage drop across V_{BE7}**,** we choose R_{12} to be 100Ω. Using KCL we can get the relation between R_{10} and R_{11}, if we set R_{10} to 1000Ω, R_{11} is 1687Ω. We also replaced the speaker with an 8Ω resistor as we don't need speaker in this experiment. When the circuit is operating, a large amount of current is flowing through T7. Since there is no short circuit protection in this circuit, it might lead to some serious consequences including burning the circuit. To dissipate the heat, we placed extra transistors in parallel with T5, T6, and T7. We also added two degeneration resistors with 10Ω at the emitter side of T5 and T6. In addition, to insure the stability of the circuit, we placed a small capacitor in parallel with T6. The experiment result is shown below (fig 5.2).

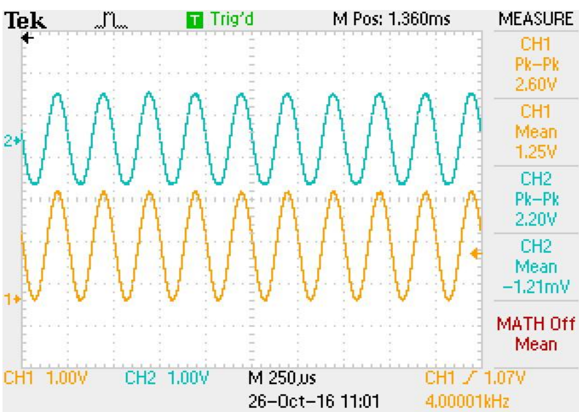

Fig 5.2 Maximum output voltage

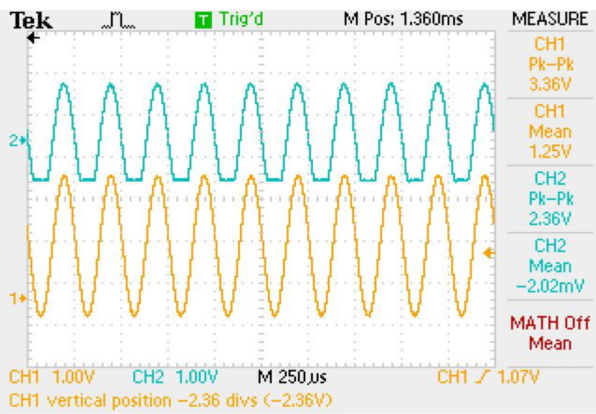

Fig 5.3 Output got clipped

Blue trace: output
Yellow trace: input

The maximum output voltage amplitude for our circuit is observed to be 2.2V. Fig 5.3 shows the output is clipped. The frequency responses are the same for large and small input signals. We chose 0.2V peak to peak for small signal input and 2V peak to peak for large signal input. The plots are shown below (fig 5.4 and fig 5.5).

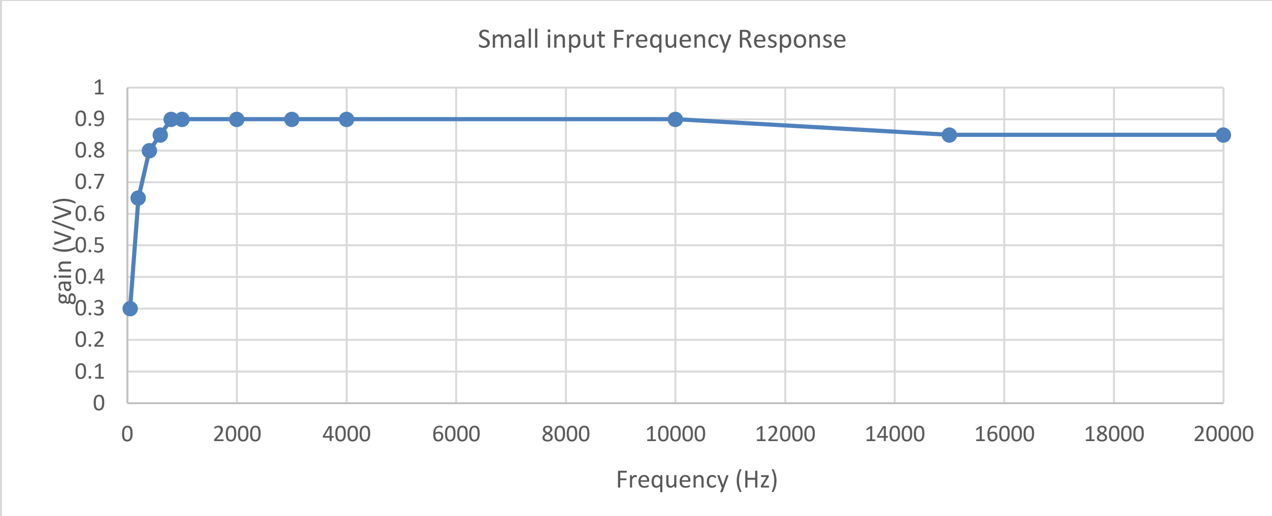

Fig 5.4 Small input frequency response

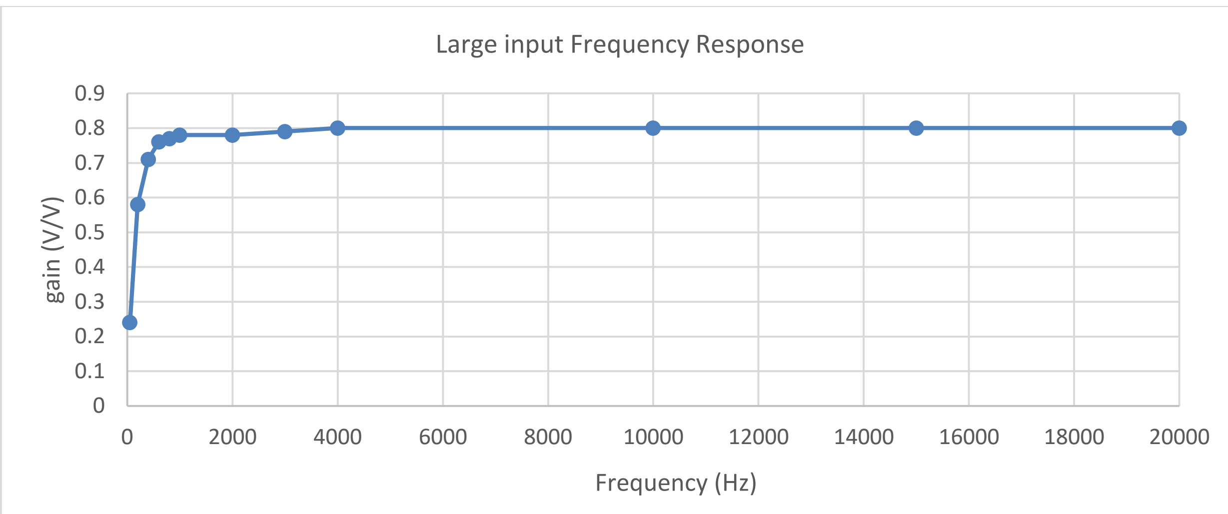

Fig 5.5 Large input frequency response

5.4 Discussion

The overall gain is 0.85 V/V, comparing to our simulation (fig 5.6), the result is satisfactory but still not ideal, which is normal because of the inaccuracy of the measurements and discrepancies of the lab components. The frequency response also matches the simulation result which gave a great rise as frequency increased. The clipping effect is also expected, which matched our circuit analysis and what we designed at the beginning of this lab.

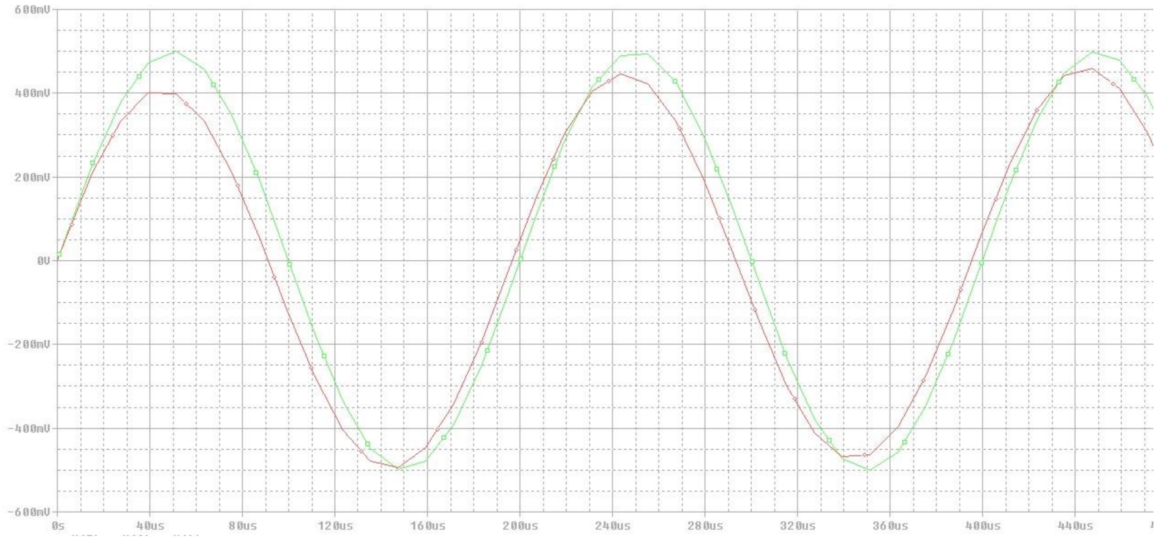

Fig 5.6 SPICE simulation

6. AM Receiver

6.1. Objective

The AM receiver is the integrated circuit of all individual components we have discussed up to this point. The AM receiver takes in AM signal on the magnitude of several mV and yield a much larger signal when the carrier frequency matches our designed parameters for the oscillation tank in preamplifier. The output is connected to a speaker. As we attenuate the audio frequency on the function generator, the speaker should play different notes according to corresponding frequencies.

6.2. Theory

Four stages are connected together as shown in the figure:

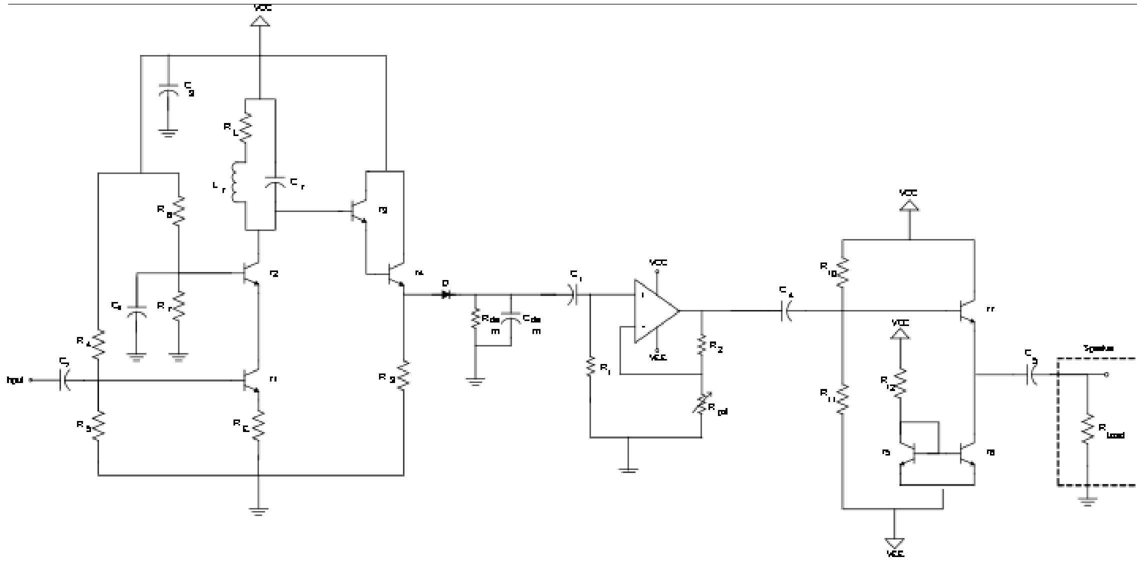

Fig6.2 AM Receiver Schematic

Components are connected in the following order:

Function generator → Pre-amplifier → demodulator → baseband amplifier → output stage

The role of each stage has been discussed in detail in previous sections under objectives. When connecting the circuit, loading effect of each stage plays an important role and has to be taken into consideration. For example, the output impedance from pre-amplifier is paralleled with the envelop circuit which in turn change components behavior. Our objective is to isolate each stage as much as possible in order to minimize the loading effect. To do so, one approach is to make sure the output impedance of the previous circuit is significantly lower than the input impedance of the following component. We also added a capacitor between pre-amplifier and envelope stages for the same reason.

6.3. Experiment

After the circuit has been connected together, we first tested the voltage at each individual node and see whether they match our expectation. Then we set up the AM signal input, which consists two parts: amplitude and frequency.

A voltage divider at the input side is made to ensure a relatively low voltage input (around 2mV, which is a good representation of real life AM signal). We use one 100Ohm and one 8.3KOhm resistors as voltage divider so the actual input to the circuit is as low as **1.2mV** peak to peak.

We then modelled the AM frequency input on the function generator based on our designed parameters. Since the resonant frequency of our pre-amplifier is experimentally tested to be 1.13MHz. According to the music tones frequencies chart given in the experiment handout, we set the <u>audio signal</u> to be 1.046KHz.

We measured the overall response to verify the circuit functionality. When we hold carrier frequency as constant while changing baseband frequency, we should not see a difference in gain as signal is getting amplified uniformly.

The overall response is observed and recorded:

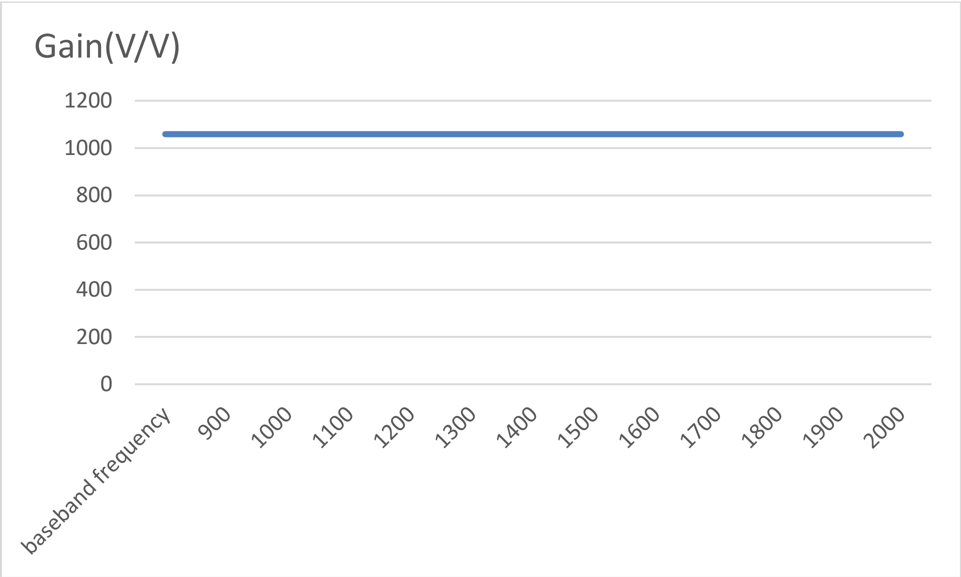

Fig 6.3.1 baseband frequency vs Gain when carrier frequency is hold as constant

We also tested the case where baseband is frequency and carrier frequency varies. The gain should be highest at the resonant frequency and drop to zero as the frequency moves away from the resonant frequency.

The overall response is observed and recorded:

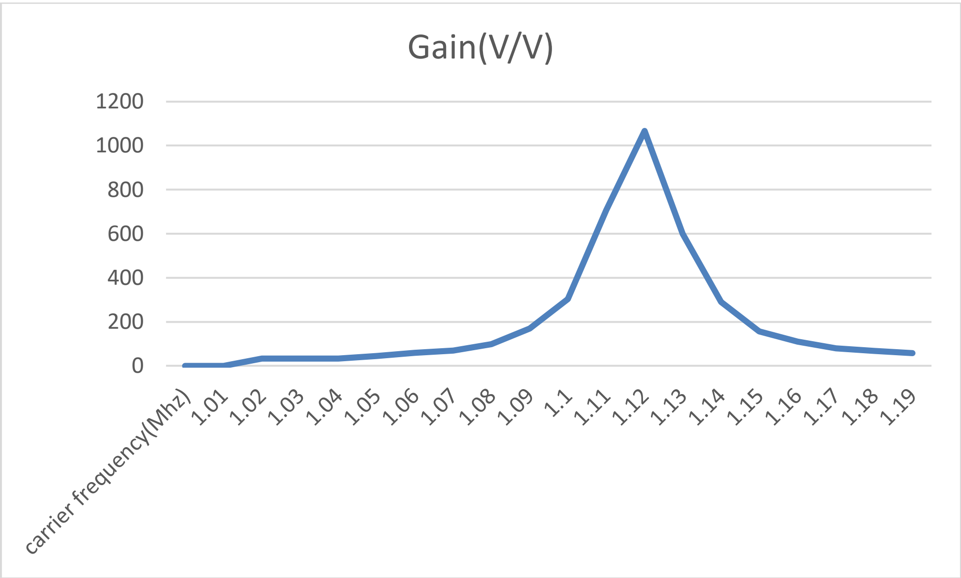

Fig. 6.3.2 Carrier frequency vs Gain when baseband frequency is hold as constant

The last step is to replace R_{load} with a low impedance speaker. As we change the baseband frequency, we heard different tones. Circuit under wireless connection was also tested. A stripped wire is connected to the circuit as an antenna instead of connected directly to the function generator. With a high voltage (2V), the circuit amplified the wireless signal and produced different sounds. The output plots are shown in fig 6.3.3 and fig 6.3.4 with two different frequencies.

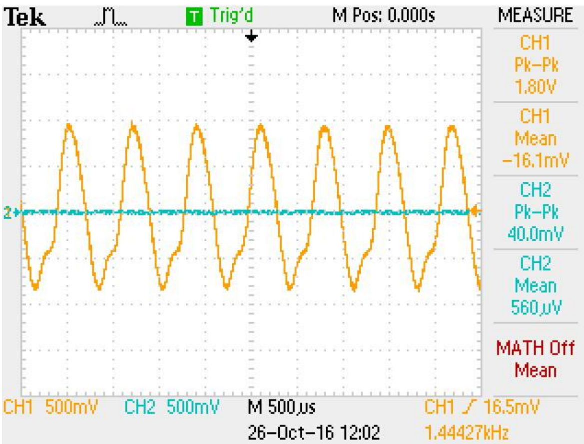

Fig 6.3.3 Frequency = 1.5kHz

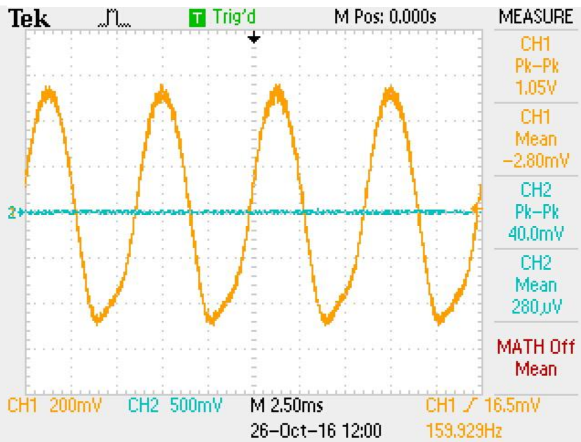

Fig 6.3.4 Frequency = 160Hz

The simulation result is shown in fig 6.3.5.

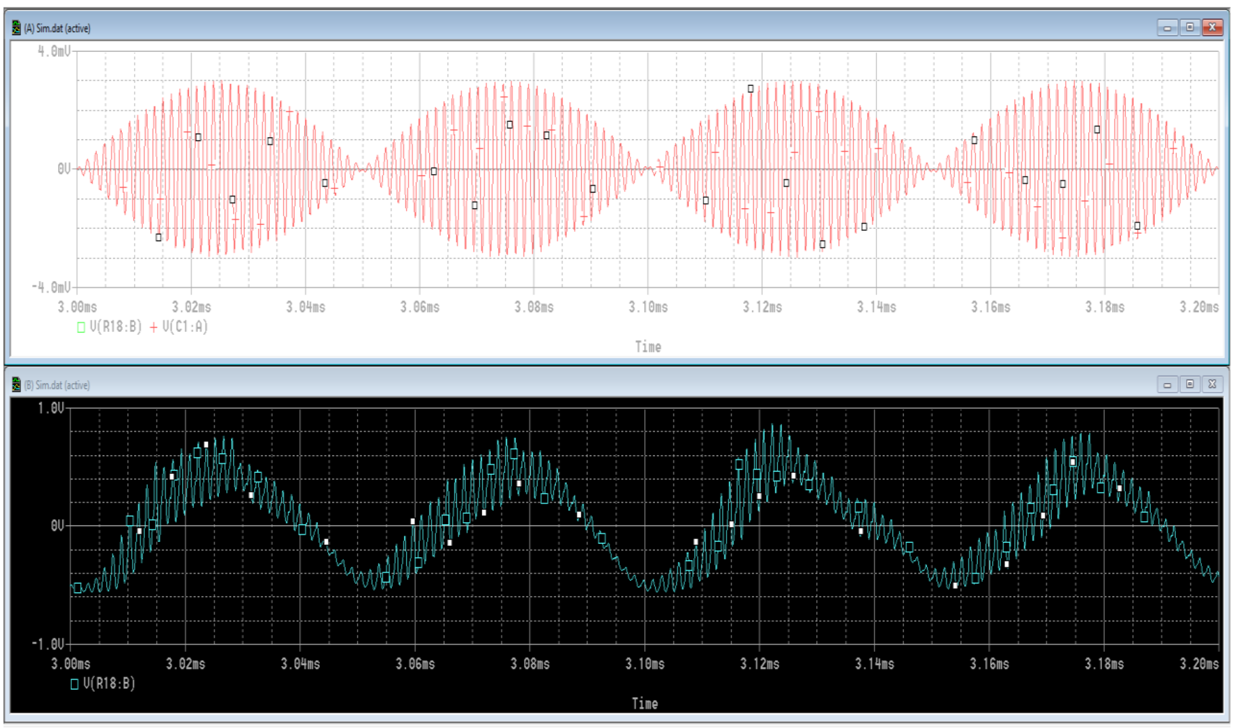

Fig 6.3.5 Input and Output

6.4 Discussion

We calculated the ideal gain of the circuit to be 14400V/V (120V/V*150V/V*0.8V/V). But we got a gain around 1000 V/V. Although the happens to be enough for audible sounds, there is still quite a difference. We believe this is due to the loading effect issue was still not fully resolved. We find the most challenging part of connecting individual parts together and getting optimal result is to analysis how different stages effect each other. Analyzing the entire circuit at once and ensure individual stage reaches its requirement is rather hard to accomplish. Also, parasitic capacitance, non-linearity in components, measurement errors etc. will also impact the overall performance of the circuit. But overall we are satisfied with the circuit since it meets demo requirements.

6.5. Wireless radio signal

Our ultimate goal for this lab is to design the AM radio receiver and receive different radio stations. This is the part where that function is realized. In order to amplify radio frequency at a specific frequency and filter out the rest, we replace the LC tank in pre-amplifier with a variable capacitor. By doing so, we can effectively select a desired carrier frequency while ignoring the rest. As a result, we could hear different radio stations and articulable human voice. However, the only problem resides in the circuit is the gain is relatively low. The output volume, consequently, was low. We tried to change component values to increase the overall gain, it was improved a bit but unfortunately the volume did not end up with the optimal level. We believe it is a shortcoming inherits from the circuit.

7.Conclusion

Overall, this experiment was a success, we managed to accomplished all requirements for individual stage. The integrated circuit also behaves relatively well as expected. This experiment is also enlightening. During the first few weeks, we designed the circuit solely based on prelab questions. We did not consider about how different stages will interfere with each other. When we head over to lab 5 and 6, the integration stage, we spent a lot of time troubleshooting because of this reason.

Moreover, we now understand the importance of testing stages one by one rather than putting everything together and hope for the best. Another lesson we learned was the simulation is often not what happens in real circuitry. SPICE is good to find out how varying components will affect outputs and thus provide a general guideline, but we do need to put in extra effort on designing circuits base on experimentation and calculation.

Finally, we will be wiser for next lab on breadboard usage. Currently our components are spread out on the entire breadboard and we had a hard time debugging the circuit. This issue can be avoided if we planned everything beforehand.