Assignment 5
COSC 2334
Fall 2021

1. Compare types of counters (Synchronous and Asynchronous) with their truth table and circuit diagram.

Ripple Counters Carry information one significant bit at a time through the counter.

Q_0	Q_1	Q_2	Q_3
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1

With the graph you can see that the ripple counter can only carry one significant diget at a time as you go through time

Synchronous Counters connects all its flip flop clocks to one input and they can change all a the same time

Q_A	Q_B	Q_C	Q_D
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
repeat			

Synchronous counters can hold everything "Synchronously" or at once, as seen in the graph

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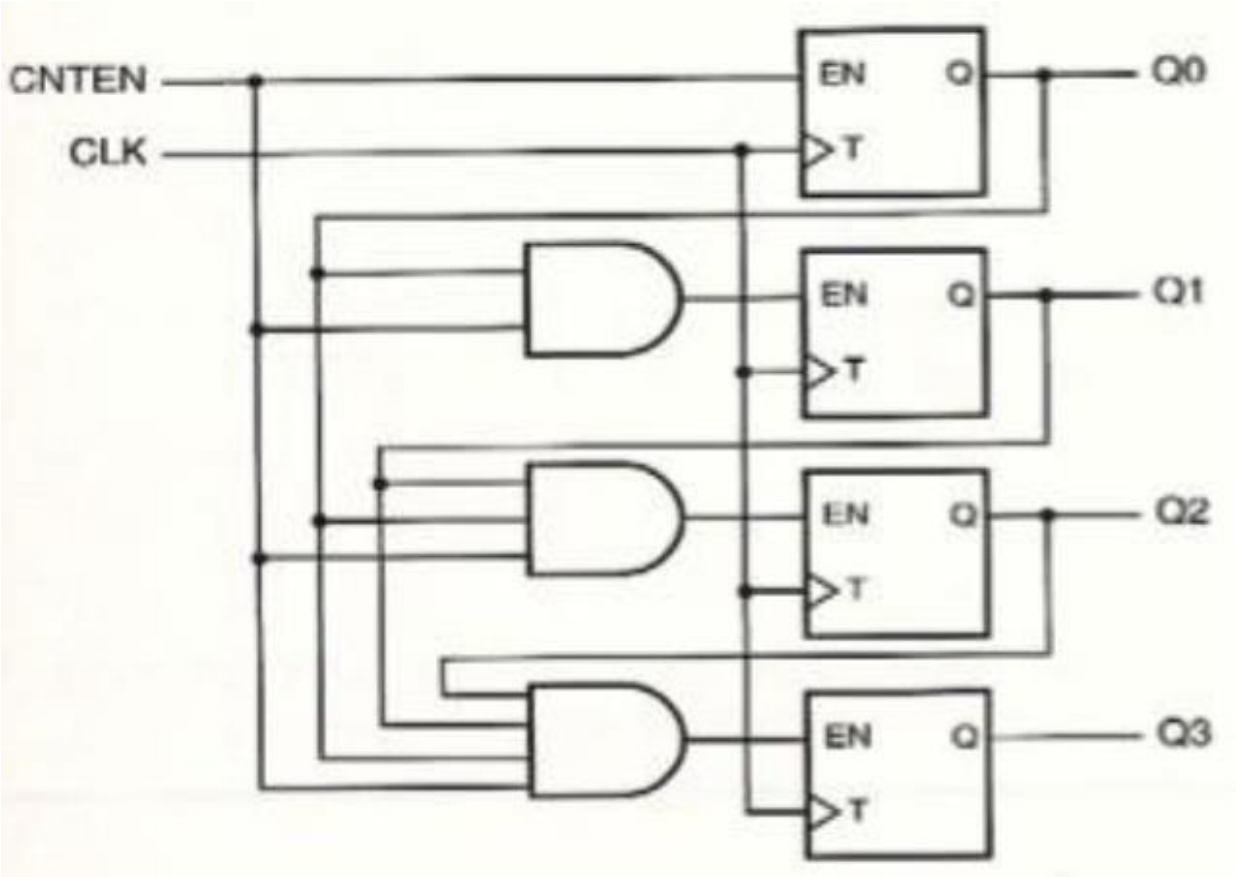
2. Given the following counter, the initial value of the counter for Q3Q2Q1Q0=0000.
   Let CNTEN=1. If the output is Q3. Determine:
   the number of input clock cycles to generate the first 1 for Q3.



If the counter is currently empty with all zeros, the 1 would need to travel through all of the flip-flps in order to reach q3.

So it would take 4 input clock cycles

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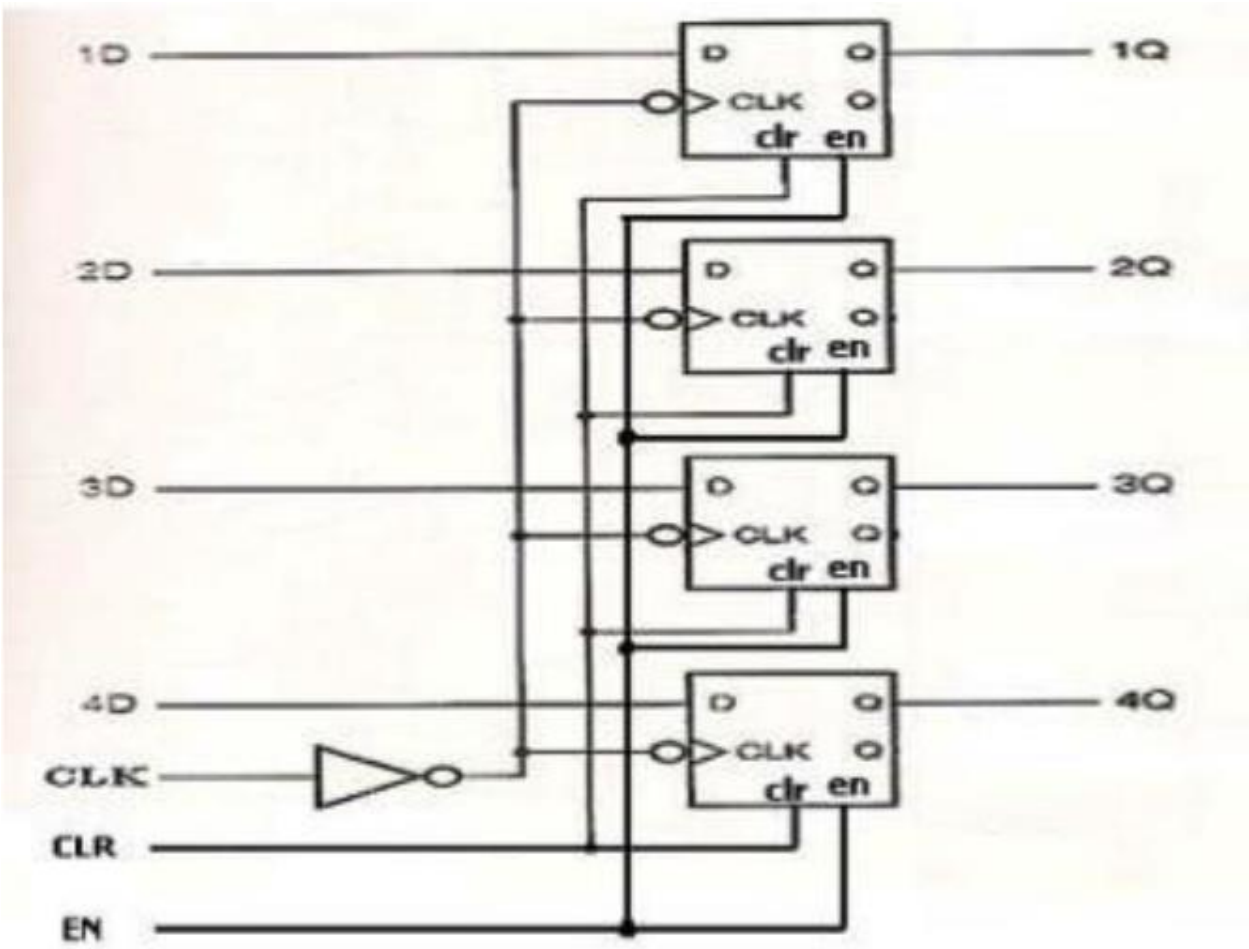
3. Given the following register. Where CLR is the reset: CLR = 1=> 4Q,3Q,2Q,1Q = 0000.
   Determine:
   (1). The value of output 4Q,3Q,2Q,1Q when 4D,3D,2D,1D = 1101, CLK = a positive edge, CLR = 0.
   (2). After (1), the value of output 4Q,3Q,2Q,1Q when 4D,3D,2D,1D = 1110, CLK = a negative edge, CLR = 0



1 Output: 1101

2 Output: 1101