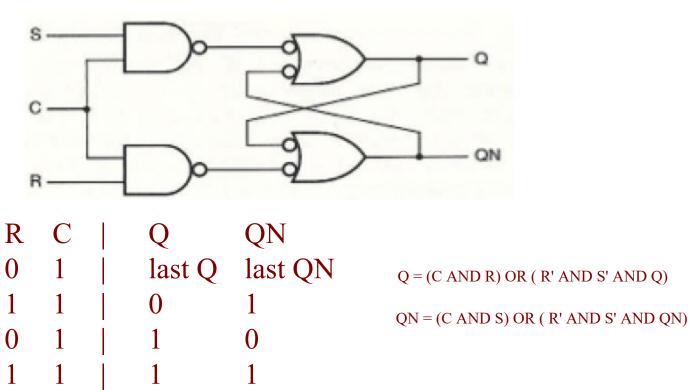
1. Given the following latch, where S, C, and R are the data input. Determine the value of Q and Q' in all situations (refer to the truth table and consider the gates).



S

X

X

2. Explain the latches and flip-flop applications and name the types of the latches and flip-flop that we have.

last Q last QN

Latches, are watching the input given and determining an output without an external clock value

Some latches have enablers and some do not, a latch with an enabler is a latch that can turn "off or on" and <u>enables</u> the latch determent new outputs

Flip-flop, are watching the input given and determining an output based on a clocking variable

Some Flip-flops are psitive edge triggered and some are negative edge triggered. This will produce an output based on whether the clock is powering up or powering down 3. Explain the difference between Master/Slave J-K flip-flop and Master/Slave S-R flip-flop. Hint: refer to the truth table and look at all the situations (draw their truth tables and explain it in a few lines) 3.

Master/Slave S-R Flip-flop

Master/Slave J-K Flip-flop

S	D	$\mathbf{C}$	$\circ$	QN	J	K	C	Q	QN
5		0	Last O		X	X	0	Last Q	Last QN
X	X	U 	Last Q	Last QN	0	0	""	LastQ	Last QN
0	0		Last Q	Last QN	0	1	···	0	1
0	1	'''	0	1	1	0	  ***	1	0
1	0	'''	1	0	1	1		Lost ON	Logt O
1	1	[""]	undef.	undef.	1	1		Last QN	Last Q

The main difference between the S-R Flip-flop and the J-K Flip-flop is the fact that the J-K flip flop loops back into its self in order to prevent a condition where there can be an undefined output. This allows for more posibilitys when using the J-K Flip-flop

4. Given the characteristic equation of D flip-flop with enable, where Q\* is the current state and Q is the previous state.

$$Q^* = EN \cdot D + EN' \cdot Q$$

Determine Q\*, when

(1) EN = 0, D=0 
$$Q^* = 0$$

(2), EN=1, D=0 
$$Q^* = 0$$

(3), EN=0, D=1 
$$Q^* = 0$$