CSA_Sess2_2021

Section 2

The reason for dividing memory into I-Cache and D-Cache is   2 points

- ☑ To increase the space of memory
- ☐ None of the mentioned
- ☐ To access the instruction word and data word in different cycles
- ☑ To access the instruction word and data word in the same clock cycle
- ☐ To reduce the cost of the memory

To increase the speed of processing in RISC Procressors   2 points

- ☐ Large size of stack memory is required
- ☐ None of the mentioned
- ☑ Large number of registers are required
- ☐ Large cache memory is required
- ☐ To divide the register file into a set of fixed size windows.

The temporary register at one level of register window are physically the same as ____ register in next level   1 point

- ☐ Local register
- ☐ Global Register
- ☐ None of the mentioned
- ☑ Parameter register
- ☐ Accumulator

The number of flipflops required in classical method is ____   1 point

- [ ] Independent of number of states
- [ ] Independent of number of control lines
- [ ] Equal to number of states
- [x] Log2 (number of states)
- [ ] None of the mentioned

The normalization operation in floating point addition operation is to____   2 points

- [x] Shifting of mantissa to make the exponents same
- [ ] None of the mentioned
- [ ] Make the exponents of the operands same
- [ ] Comparing the exponents
- [ ] Shifting of mantissa so that there are no leading zeros

The sequence of control signals generated in GCD Processor is i. Subtract   2 points
ii.Load Xr,Yr iii.Swap iv. Select XY

- [ ] I,ii,iii,iv
- [x] Iv,ii,Iii,i
- [ ] Iv,iii,ii,i
- [ ] I,iii,ii.iv
- [ ] Iii,ii,I,iv

The reason for providing buffer registers between the stages of pipeline are   2 points

- ☐ To synchronize between stages
- ☑ To store the intermediate results so that the data is not lost
- ☐ To minimize the delay
- ☐ To increase the pipeline efficiency
- ☐ None of the mentioned

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