DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER IV
Computer Engineering
SUBJECT: (CE-417)Computer System Architecture

Examination	**: Second Sessional**	**Seat No.**	**:**
Date	**: 14/02/2018**	**Day**	**: Wednesday**
Time	**: 10 am to 11.15 am**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed. **[12]**

(a) Describe all the dependencies which can occur in a Pipeline Architecture. **[2]**

(b) What are the pros and cons of Hardwired and micro-programmed control unit? **[2]**

(c) What is forbidden list, minimum latency and minimum constant latency? Explain with example **[2]**

(d) Show that the logic expression $C_n \oplus C_{n+1}$ is a correct indicator of overflow in the addition of 2's complement integers, by using an appropriate truth table. **[2]**

(e) What is the use of zero digit checker in Floating point add unit of the IBM system/360 model? **[2]**

(f) Derive working principle of carry look ahead adder. **[2]**

Q.2 Attempt ***Any Two*** from the following questions. **[12]**

(a) Perform the division of a dividend X = 28 and a divisor D =5 using the non-restoring algorithm. How the division operation can be performed for the signed numbers and How the sign of quotient and remainder is managed. **[6]**

(b) Find a method of encoding the microinstructions for minimum number of control bits for the given instruction set: **[6]**

Instn.	Control bits	Instn	Control bits
I1	C1,C2,C3,C4,C5,C6	I5	C7,C8
I2	C1,C3,C4,C6	I6	C1,C8,C9
I3	C2,C5,C6	I7	C3,C4,C8
I4	C4,C5,C8	I8	C1,C2,C9

(c) Multiply (+15 X -13) using the Bit pair Multiplier Algorithm and draw the datapath for the same. **[6]**

Q.3 Answer the followings **[12]**

(a) Derive the required control signals for a processor in which floating point addition and subtraction will be performed. Implement the control unit for the same using any hardwired method. Derive the final functions with respect to IAS computer. **[12]**

OR

Q.3 Answer the followings **[12]**

(a) Implement the TID diagram for a given reservation table **Fig. 1**. Only calculate minimum latency and forbidden list in addition to the diagram. [6]

(b) 1. Derive a general equation to represent positive and negative number for 2's complement form. **[3]**

2. Explain with neat diagram the working of floating point data path unit which can perform basic arithmetic operations. **[3]**

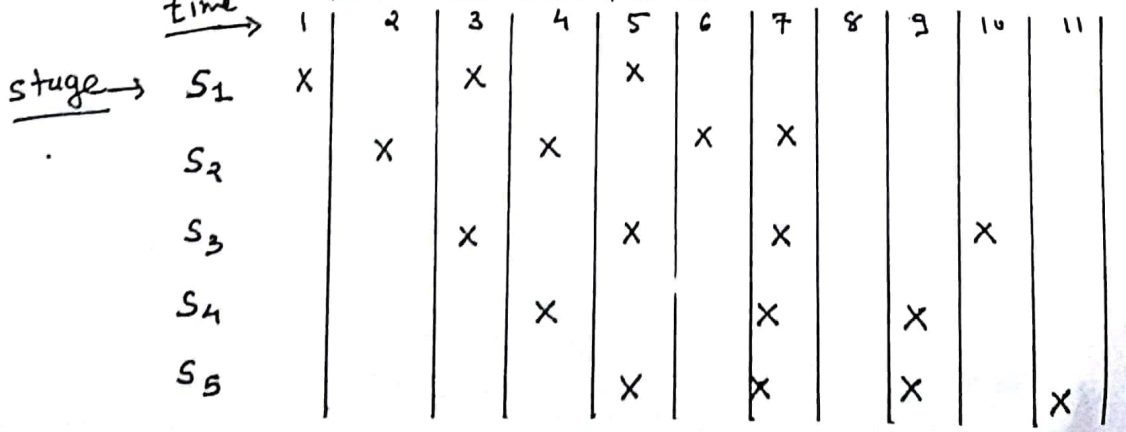

Fig. 1