

# FE8.1

## HIGH SPEED 4-PORT USB HUB CONTROLLER

### Data Sheet

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#### INTRODUCTION

The Terminus FE8.1 is an extremely compact High Speed 4-port USB hub controller. It is compliant to USB-IF “*Universal Serial Bus Specification Revision 2.0*” (USB 2.0) specification from every aspects but one – FE8.1 always reports itself as an Self-Powered hub, regardless of the actual system implementation. To achieve the absolutely minimal pin counts, there is no input signal pins left to monitor the local power status.

The FE8.1 is a highly integrated, high quality, and high performance solution for USB 2.0 4-port hub. With its tiny footprint and extremely low power consumption, it is the best choice for embedded application as well as standalone hub.

The high quality of FE8.1 is guaranteed by Design-For-Testing with comprehensive scan chains and Built-In-Self-Test modes which could exercise all High, Full, and Low Speed Analog Front End (AFE) components on the packaging and testing stages.

#### FEATURES

- USB 2.0 fully compliant AFE transceivers:
  - Upstream Facing Port supports High-

Speed (480MHz) and Full-Speed (12MHz) modes;

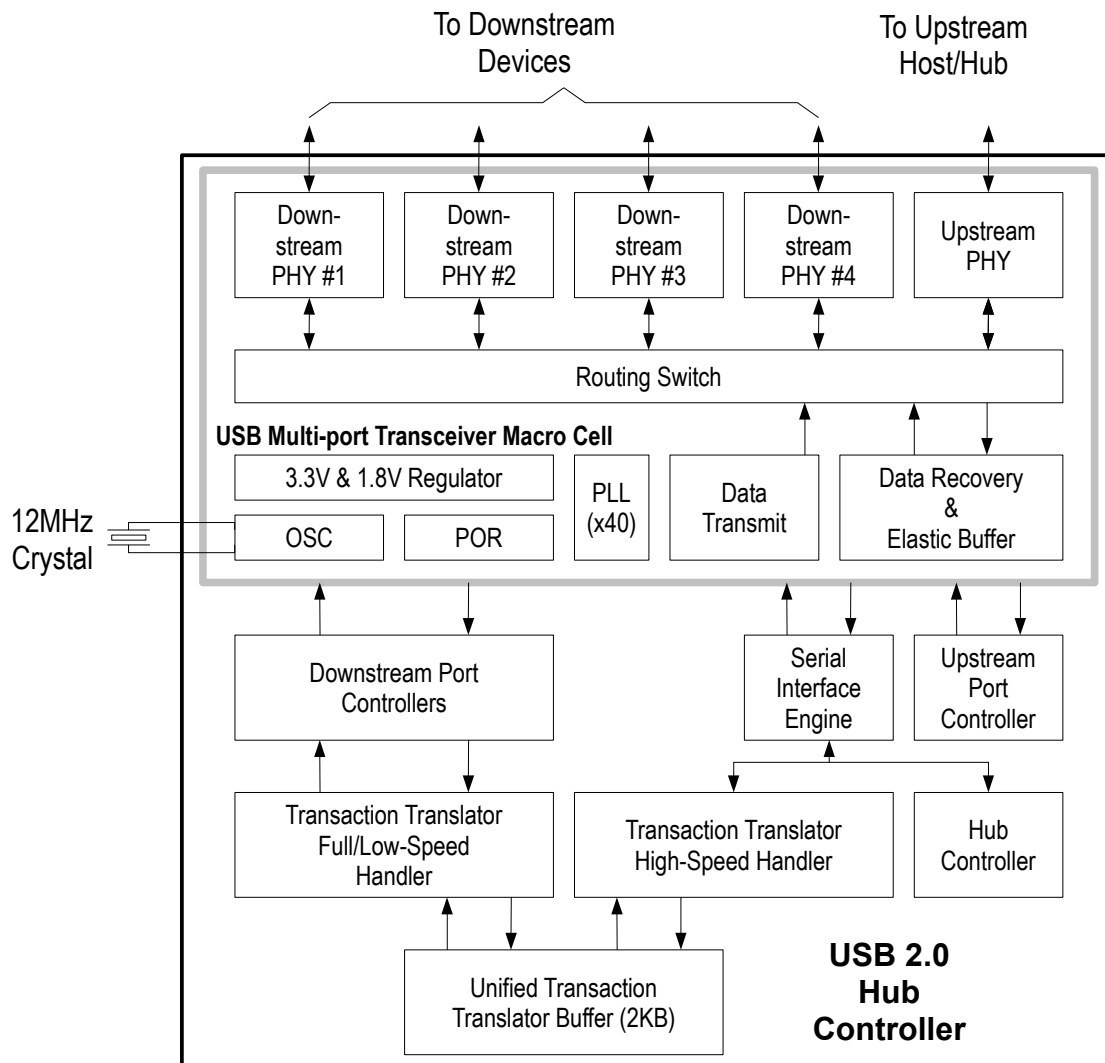
- 4 Downstream Facing Ports support High-Speed, Full-Speed, and Low-Speed (1.5MHz) modes;
- Integrated upstream 1.5K $\Omega$  pull-up, downstream 15K $\Omega$  pull-down, and serial resistors;
- Integrated 5V to 3.3V and 1.8V regulators;
- Integrated Power-On-Reset with power failure detection circuit;
- Integrated 12MHz Oscillator with feedback resistor and crystal load capacitors;
- Integrated 12MHz-to-480MHz Phase Lock Loop (PLL);
- *Single Transaction Translator* (Single TT) –
  - One TT for all downstream ports;
  - The TT could handle 64 periodic Start-Split transactions, 32 periodic Complete-Split transactions, and 6 none-periodic transactions;



## ORDER INFORMATION

P/N-Order Code	Description	Package Type	Packing	Minimum Order Quantity
TBD	High Speed 4-Port USB Hub Controller	16-pin SSOP (5mm x 4mm)	Tape & Reel	TBD
TBD		16-pin SSOP (5mm x 4mm)	Tube	TBD
TBD		16-pin WQFN (3mm x 3mm)	Tape & Reel	TBD

## BLOCK DIAGRAM



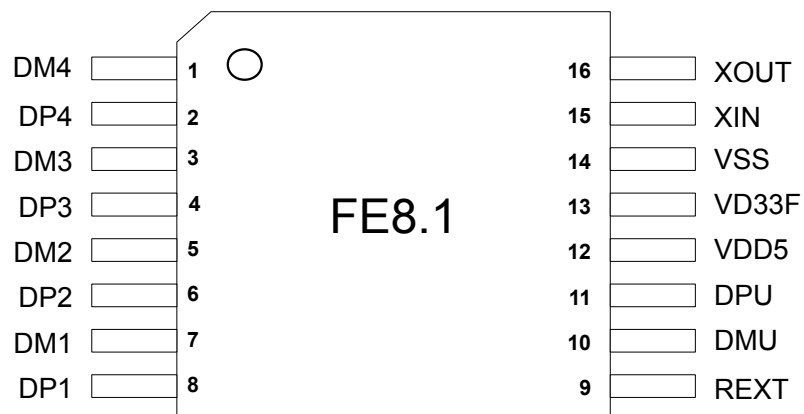
*Fig. 1: Block Diagram*

## PACKAGE I

16-Pin SSOP

(Body Size: 5mm x 4mm, Pitch: 0.64mm)

## PIN ASSIGNMENT



*Fig. 2: 16-Pin SSOP Pin Assignment*

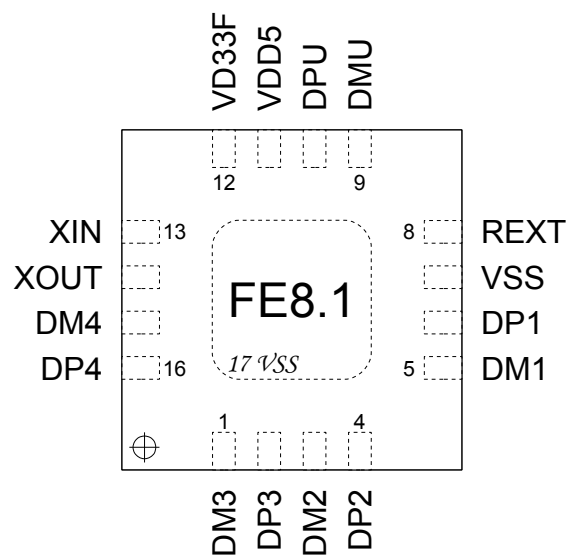
## PACKAGE II

### 16-Pin WQFN

(Body Size: 3mm x 3mm, Pitch: 0.5mm)

(Exposed Pad: 1.7mm x 1.7mm)

## PIN ASSIGNMENT



*Fig. 3: 16-Pin WQFN Pin Assignment*

## PIN DESCRIPTION TABLE

Pin Name	Pin No.		Type	Function	Note
	SSOP	QFN			
DM4	1	15	UTD	The D- pin of the 4 <sup>th</sup> Downstream Facing Port.	
DP4	2	16	UTD	The D+ pin of the 4 <sup>th</sup> Downstream Facing Port.	
DM3	3	1	UTD	The D- pin of the 3 <sup>rd</sup> Downstream Facing Port.	
DP3	4	2	UTD	The D+ pin of the 3 <sup>rd</sup> Downstream Facing Port.	
DM2	5	3	UTD	The D- pin of the 2 <sup>nd</sup> Downstream Facing Port.	
DP2	6	4	UTD	The D+ pin of the 2 <sup>nd</sup> Downstream Facing Port.	
DM1	7	5	UTD	The D- pin of the 1 <sup>st</sup> Downstream Facing Port.	
DP1	8	6	UTD	The D+ pin of the 1 <sup>st</sup> Downstream Facing Port.	
REXT	9	8		External Bias Resister A 2.7K $\Omega$ ( $\pm$ 1%) resister should be connected to VSS to provide internal bias reference.	
DMU	10	9	UTU	The D- pin of the Upstream Facing Port.	
DPU	11	10	UTU	The D+ pin of the Upstream Facing Port.	
VDD5	12	11	P	5V Power Input This is the 5V power input for integrated 5V $\rightarrow$ 3.3V regulator. However, if external 3.3V source is used, this pin should be <i>Tied-To-Ground</i> .	
VD33F	13	12	P	3.3V output filter capacitor for embedded 5V $\rightarrow$ 3.3V regulator, or 3.3V input from external source.	
VSS	14	7, 17	P	Ground (pin 17 of WQFN is the underbelly exposed pad)	
XIN	15	13	OSC	12MHz Crystal Oscillator input/External 12MHz clock input.	1
XOUT	16	14	OSC	12MHz Crystal Oscillator output.	1

### Type Abbreviation –

- UTD: USB Downstream Facing Port Transceiver (supporting High/Full/Low-Speed);
- UTU: USB Upstream Facing Port Transceiver (supporting High/Full-Speed);
- OSC: Crystal Oscillator (with integrated feedback resister, and crystal load capacitor);
- P: Power/Ground.

### Note 1 – Crystal Requirements

- Frequency accuracy: 12MHz  $\pm$  50ppm
- Load capacitance: 16pF  $\sim$  20pF



## **APPLICATION ALTERNATIVES**

The *FE8.1* can be either powered by 5V or 3.3V power source. If 3.3V power source is used, then VDD5 must be tied to ground to insure proper operations.



## ELECTRICAL CHARACTERISTICS

### ***ABSOLUTE MAXIMUM RATINGS***

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TS	-55	+150	°C
Power Supply Voltage	VDD5 VD33	-0.5 -0.5	+6.0 +4.0	V
ESD Human Body Mode (MIL-STD Class 2)		-2000	+2000	V
ESD Machine Mode (JEDEC Class B)		-200	+200	V
ESD Charged Device Mode		-500	+500	V
Latch Up (Class I, Level A)		-200	+200	mA

### ***Recommended Operating Ranges***

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Temperature	TA	0		70	°C
Operating Voltage	VDD5 VD33	4.5 3.0	5.0 3.3	5.5 3.6	V
LOW level voltage of digital input	VIL	-0.3		0.8	V
HIGH level voltage of digital input	VIH	2.0		5.5	V
Threshold voltage of digital input	VTH	1.45	1.58	1.74	V
Low-to-High level of Schmitt-trigger input	VT+	1.44	1.5	1.56	V
High-to-Low level of Schmitt-trigger input	VT-	0.89	0.94	0.99	V
LOW level voltage of digital output	VOL			0.4	V
HIGH level voltage of digital output	VOH	2.4			V
XIN input capacitance	Cin		32		pF
Internal Pull-Up Resister Range	R <sub>PU</sub>	39	65	116	KΩ



## POWER CONSUMPTION

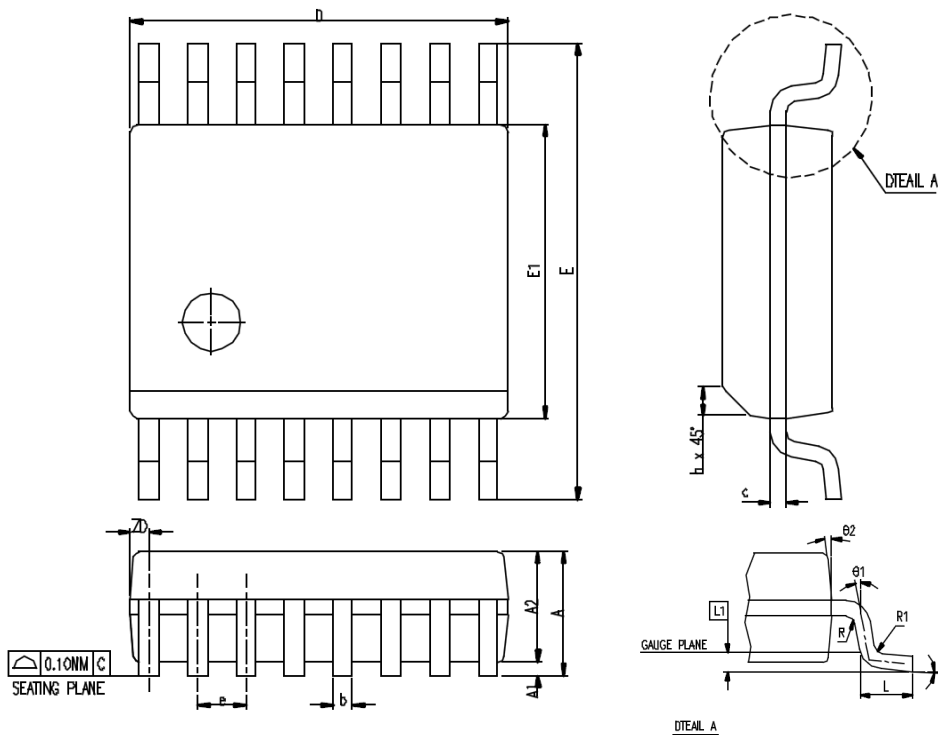
### ABSOLUTE MAXIMUM RATINGS

Symbol	Condition			Typical	Unit
	Active	Host	Devices		
I <sub>suspend</sub>	Suspend			740	μA
I <sub>cc</sub>	4	High-Speed	4 x High-Speed	86	mA
		High-Speed	4 x Full-Speed	40	mA
		Full-Speed	4 x Full-Speed	27	mA
	3	High-Speed	3 x High-Speed	74	mA
		High-Speed	3 x Full-Speed	40	mA
		Full-Speed	3 x Full-Speed	27	mA
	2	High-Speed	2 x High-Speed	62	mA
		High-Speed	2 x Full-Speed	40	mA
		Full-Speed	2 x Full-Speed	27	mA
	1	High-Speed	1 x High-Speed	51	mA
		High-Speed	1 x Full-Speed	40	mA
		Full-Speed	1 x Full-Speed	27	mA
	No Active	High-Speed	None	40	mA
		Full-Speed	None	27	mA

Note: The power consumption is measured when the bus is in IDLE state – there is no activities other than the Start-Of-Frame (SOF) and INTERRUPT-IN packets for the hub itself on the bus. The peak power consumption varies depending upon the system configuration, type of operations, and over-all bus utilization.

## PACKAGE I

16-pin SSOP (Body Size: 5x4 mm, Pitch: 0.64mm)



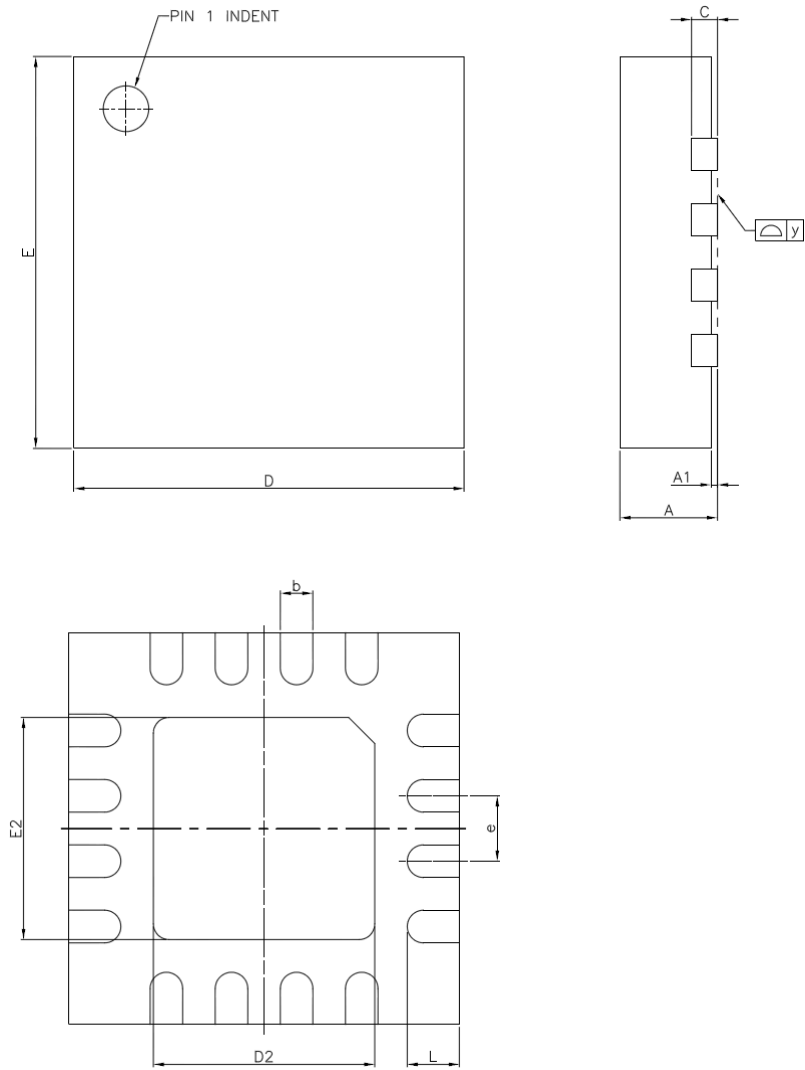
▲ \*NOTES : DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS.  
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 INCH PER SIDE.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			1.50			0.059
b	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025 BASIC		
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25		0.50	0.010		0.020
L1	0.254 BASIC			0.010 BASIC		
ZD	0.229 REF			0.009 REF		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ1	0°			0°		
θ2	5°	10°	15°	5°	10°	15°
JEDEC	MO-137 (AB)					



**PACKAGE II**

16-pin WQFN (Body Size: 3x3 mm, Pitch: 0.5mm, Exposed Pad: 1.7x1.7mm)



NOTE:  
1.THE TERMINAL #1 IDENTIFIER  
IS A LASER MARKED FEATURE

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
C	—	0.20 REF.	—
D	2.90	3.00	3.10
D2	1.65	1.70	1.75
E	2.90	3.00	3.10
E2	1.65	1.70	1.75
e	—	0.50	—
L	0.35	0.40	0.45
y	0.00	—	0.075

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