CIS341 Due: Oct. 27

Week 9 Assignment

Student name(s):

- 1. (50 points) The following table gives the parameters for a number of different caches. Your task is to fill in the missing fields in the table. The definitions of the cache memory parameters are as follows:
 - m: the number of address bits
 - C: the cache size (number of data bytes)
 - B: the block size in bytes
 - E: the associativity
 - S: the number of cache sets
 - t: the number of tag bits
 - s: the number of set index bits
 - b: the number of block offset bits

Cache	m	C	B	E	S	t	s	b
1.	32	4096	8		512	20		3
2.	48			2	256		8	4
3.	32	1024	32	1		22	5	
4.		2048	16	4	32	23		

CIS341 Due: Oct. 27

- 2. (50 points) Suppose we have a system with the following properties:
 - The memory is byte addressable, and the addresses are 12-bits wide.
 - The cache is two-way associative (E=2), with 4-byte blocks (B=4) and four sets (S=4).

The contents of the cache are as follows, with all addresses, tags, and values given in hexadecimal notations:

Set index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	00	0	20	21	22	23
U	11	1	28	29	2A	2B
1	44	1	60	61	62	63
1	55	0	68	69	6A	6B
2	77	0	90	91	92	93
2	88	0	98	99	9A	9B
3	ВВ	1	D0	D1	D2	D3
5	CC	1	D8	D9	DA	DB

For each of the following memory accesses, indicate if it will be a cache hit or miss when carried out in sequence as listed. Also, give the values of a read if it can be inferred from the information in the cache.

Operation	Address	Hit?	Read value (or unknown)
Read	0x111		
Read	0x222		
Read	0x444		
Read	0x888		
Read	0xBBB		