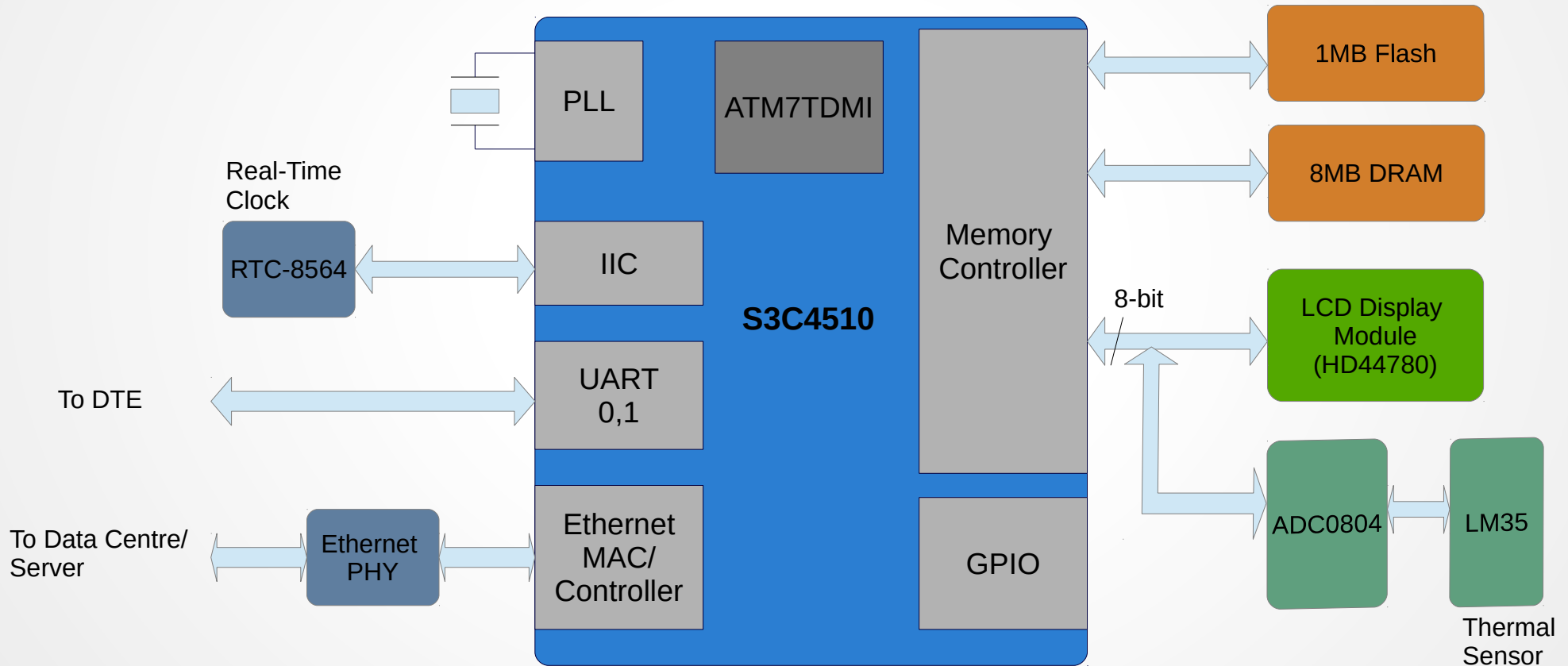
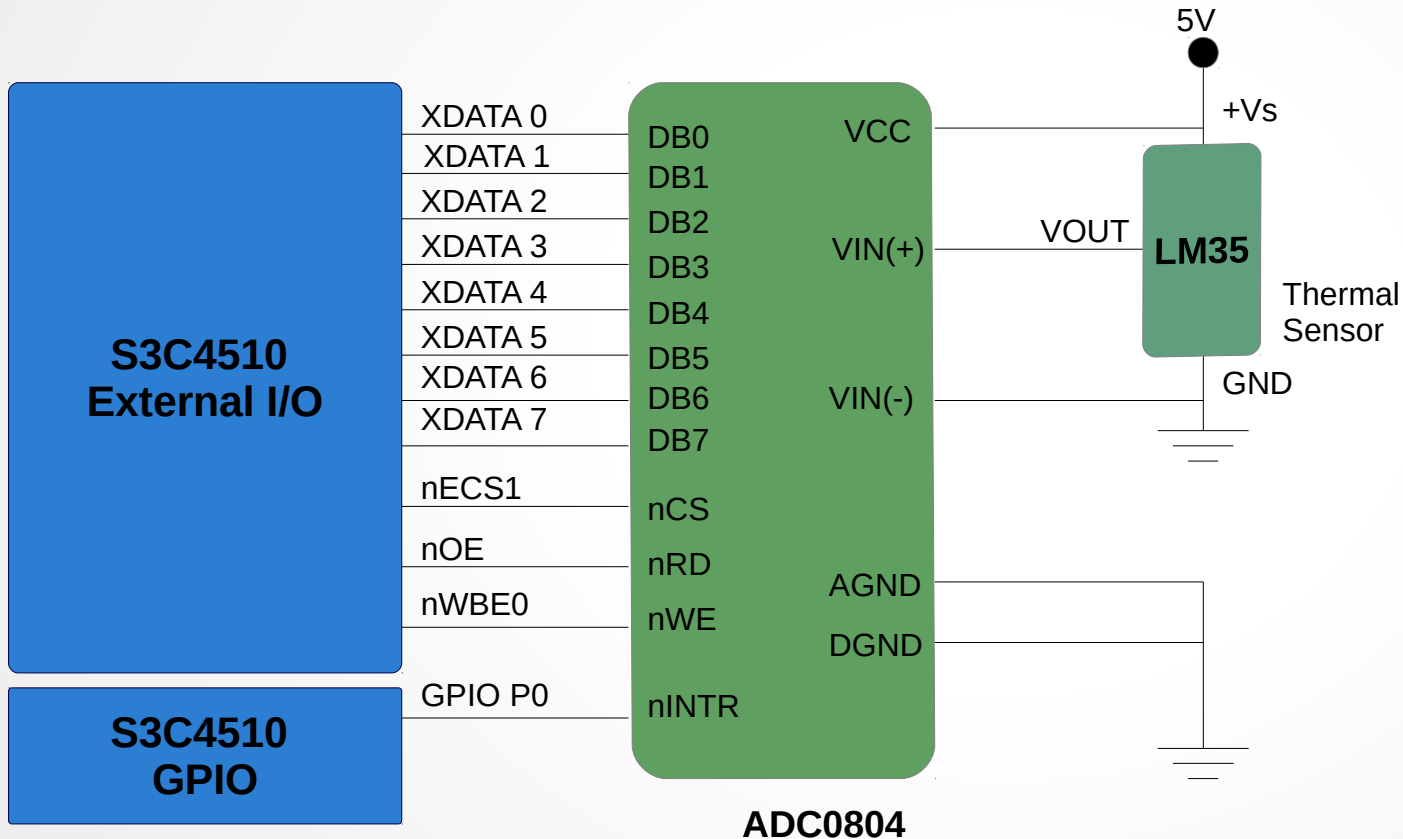


Board Level Block Diagram



Thermal I/F (Memory Bank 1)



- **Steps to read the thermal data:**
 - Set the external bus width to 8-bit
 - Write 0 to address of memory Bank-1 to trigger the ADC
 - Polling GPIO P0 to check if ADC finish the translation
 - Read data (digital) from ADC
- **ADC0804 is a 8-bit Analog-to-Digital convertor with 5V power supplied. The resolution is 5V/256**
- **LM35 sensor output resolution: "10mV/degree"**

Memory Bank Bus Width Configuration

- Controlled by EXTDBWTH register, bits [23:22] are used to configure External Memory bank 1 bus width

Table 4-20. EXTDBWTH Register Description

Registers	Offset	R/W	Description	Reset Value
EXTDBWTH	0x3010	R/W	Data bus width of each bank	0x00000000

[21:20] Data bus width for external I/O bank 0 (DSX0)

[23:22] DSX1, [25:24] DSX2, [27:26] DSX3

00 = Dissable

01 = Byte (8 bits)

10 = Half-word (16 bits)

11 = Word (32 bits)

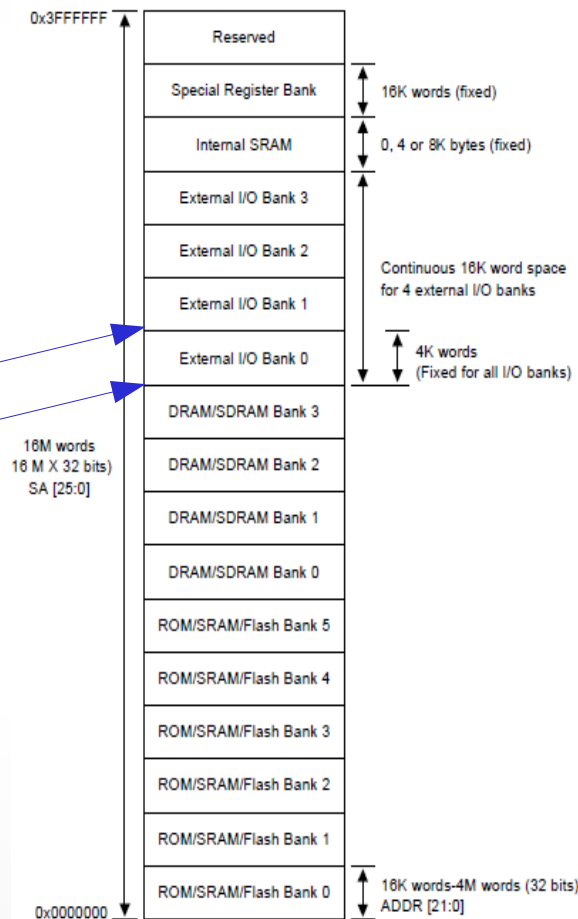
Bus Width
for bank 1

Bus Width
= 8 bits

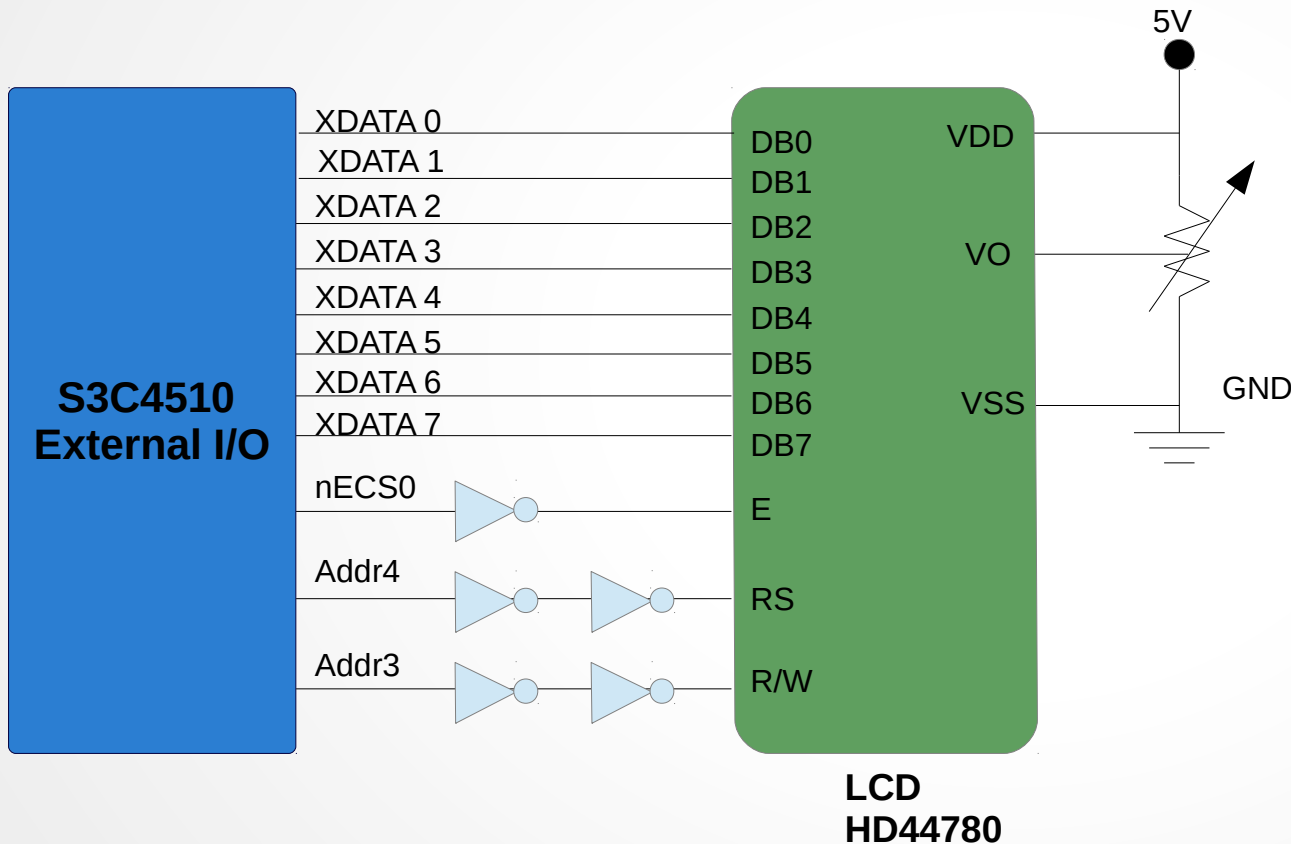
System Memory Map and External Memory I/O Address

Bank 1 Starting Address: 0x3604000

Bank 0 Starting Address: 0x3600000

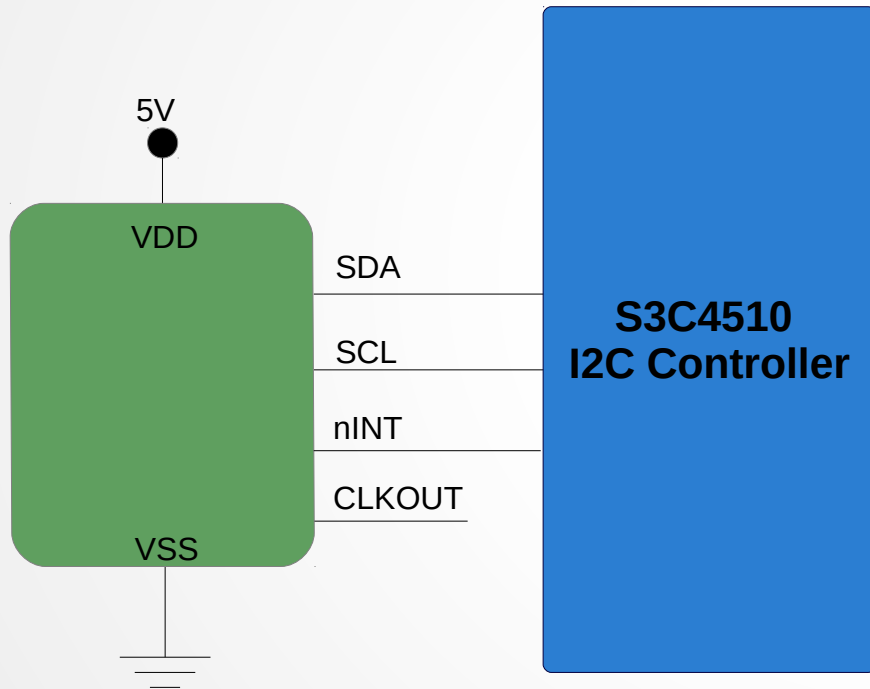


LCD I/F (Memory Bank 0)



- LCD has two registers selected and accessed by “RS” & “R/W” signal
 - a. RS = 0, R/W = 0: Write command or RAM address to instruction register
 - b. RS = 0, R/W = 1: Read “Busy Flag”
 - c. RS = 1, R/W = 0: Write data to data register(then to RAM automatically)
 - d. RS = 1, R/W = 1: Read data from data register
- RS and R/W signal are implemented by Addr4 and Addr3
- Inverters (74HC14) are used to match signal type and timing
- VO input voltage value is used to adjusted the lightness of LCD

I2C for RTC



- Key H/W features of RTC-8564

- a. I2C slave address: 0x51h
- b. Build in 32.768KHz OSC
- c. Max clock speed for I2C: 400KHz
- d. Programmable CLKOUT frequency