Midterm Project

ECE241 – Electronics I

Professor Shlayan

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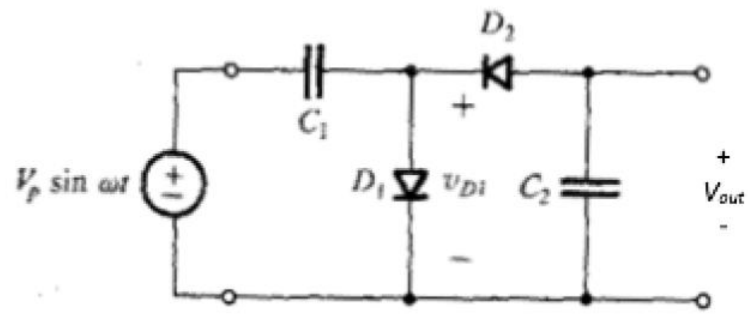
Problem 1

Consider the voltage doubler circuit in Figure 1. Perform the following:



a. A sinusoidal input voltage is applied at t=0. Plot the output waveform of the circuit for the first three periods $T=1/f$ provided that the initial condition across C1 and C2 is zero.

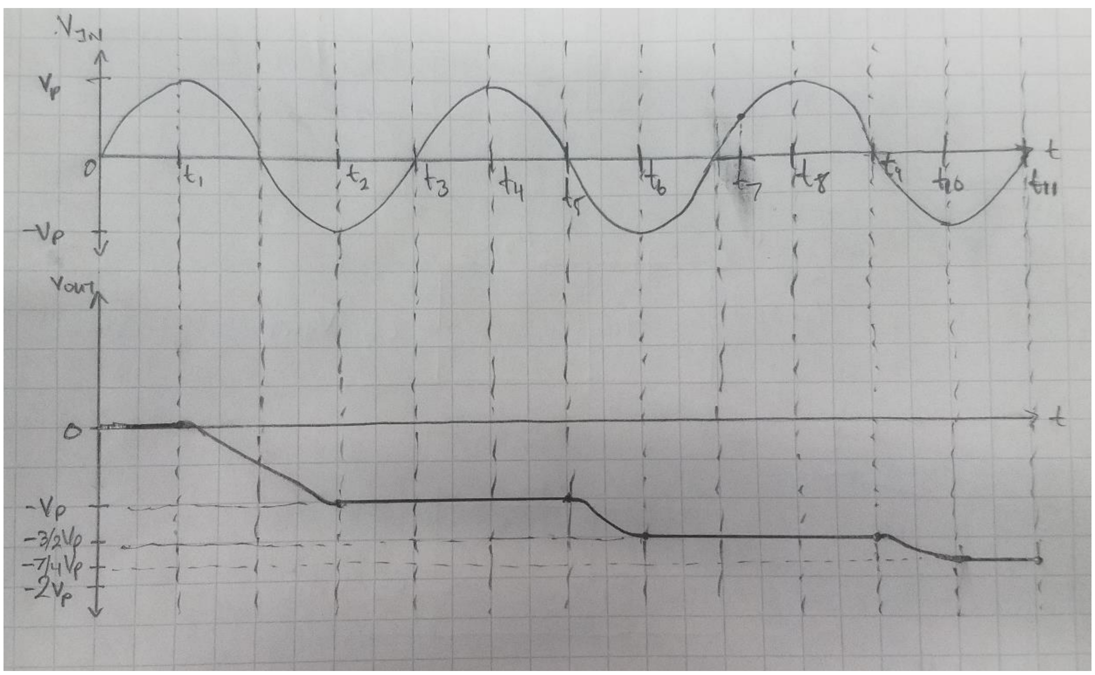


Figure 1: V_{IN} and V_{OUT}, the input and output waveforms.

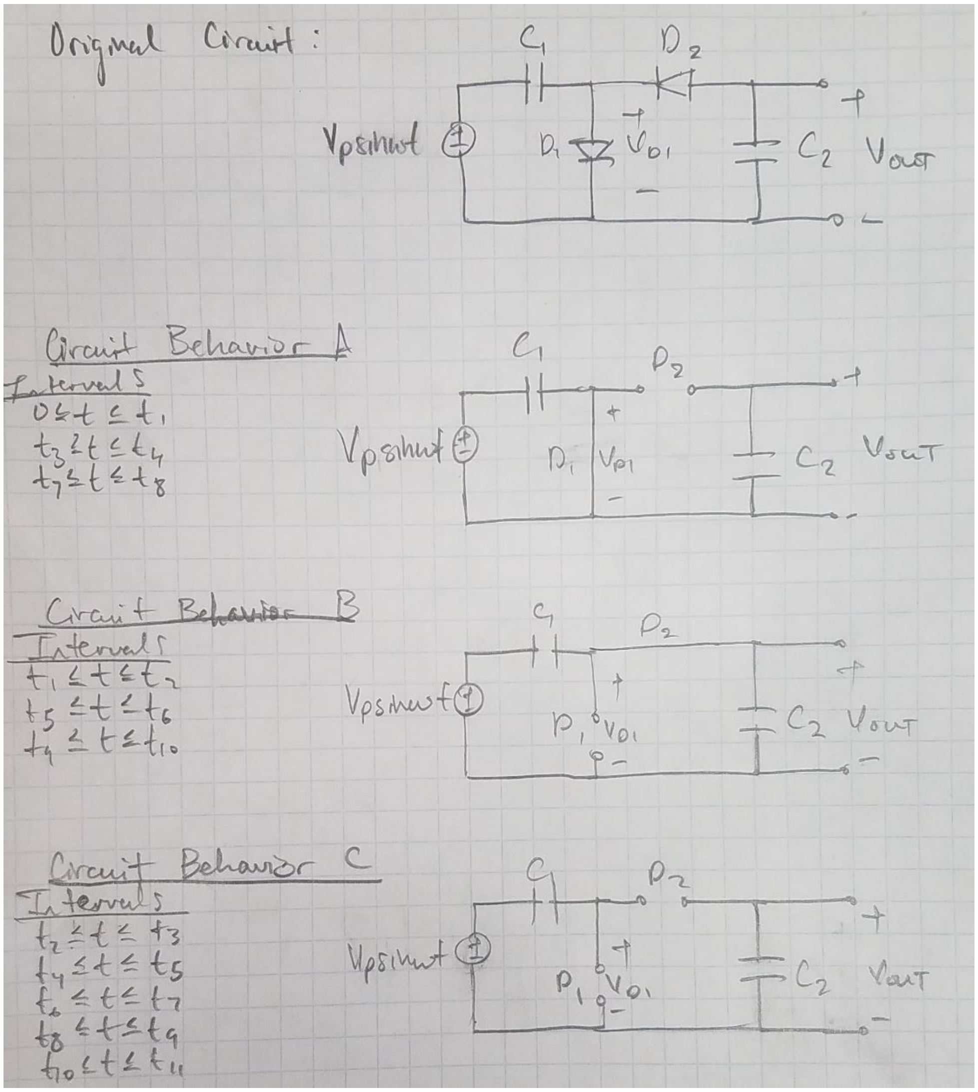


Figure 2: Each representation of the voltage doubler circuit.

Above is each representation of the voltage doubler circuit:

The Original Circuit

Circuit Behavior A (D1 is in forward bias and D2 is in reverse bias)

Circuit Behavior B (D1 is in reverse bias and D2 is in forward bias)

Circuit Behavior C (D1 is in reverse bias and D2 is in reverse bias)

Below is a table that shows the diode behavior for each interval, namely whether the diode is in forward bias or reverse bias, and the capacitor behavior for each interval, namely whether the capacitor is charging, discharging, or idle.

Interval	D1	D2	C1	C2
$0 \le t \le t_1$	Forward Bias	Reverse Bias	Charges to V_P	-
$t_1 \le t \le t_2$	Reverse Bias	Forward Bias	Discharges to 0	Charges to $-V_P$
$t_2 \le t \le t_3$	Reverse Bias	Reverse Bias	-	-
$t_3 \le t \le t_4$	Forward Bias	Reverse Bias	Charges to V_P	-
$t_4 \le t \le t_5$	Reverse Bias	Reverse Bias	-	-
$t_5 \le t \le t_6$	Reverse Bias	Forward Bias	Discharges to $\frac{1}{2}V_P$	Charges to $-\frac{3}{2}V_P$
$t_6 \le t \le t_7$	Reverse Bias	Reverse Bias	-	-
$t_7 \le t \le t_8$	Forward Bias	Reverse Bias	Charges to V_P	-
$t_8 \le t \le t_9$	Reverse Bias	Reverse Bias	-	-
$t_9 \le t \le t_{10}$	Reverse Bias	Forward Bias	Discharges to $\frac{3}{4}V_P$	Charges to $-\frac{7}{4}V_P$
$t_{10} \le t \le t_{11}$	Reverse Bias	Reverse Bias	-	-

b. Use LTspice to plot the transient behavior of the voltages Vin, Vout, and VD1. Provided that *Vp = 10 V, f = 2 kHz, C1 = C2 = 1 uF*, and the diode used is of type 1N4148.

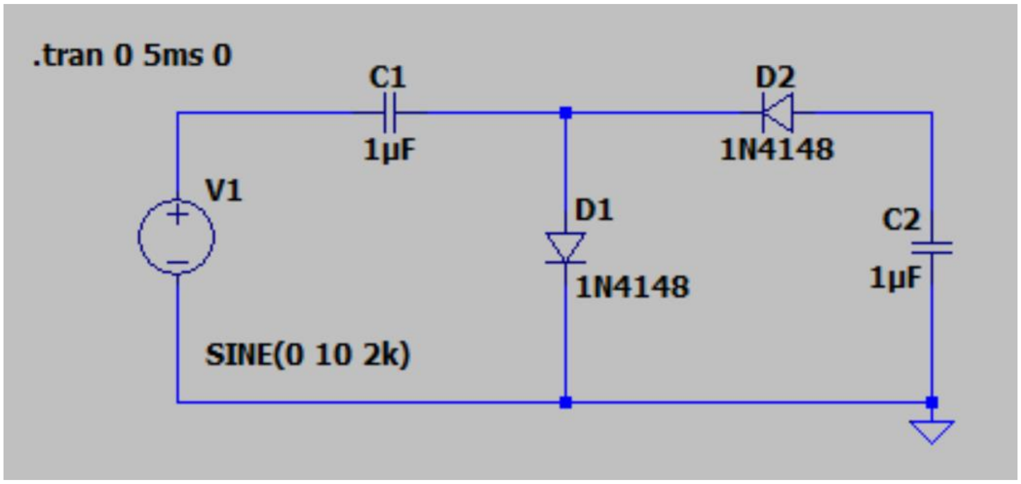


Figure 3: LTspice Circuit

The transient behavior of the circuit matched the predicted behavior. The small difference between the predicted behavior and simulated behavior is due to the nonideality of the diodes used in the simulation.

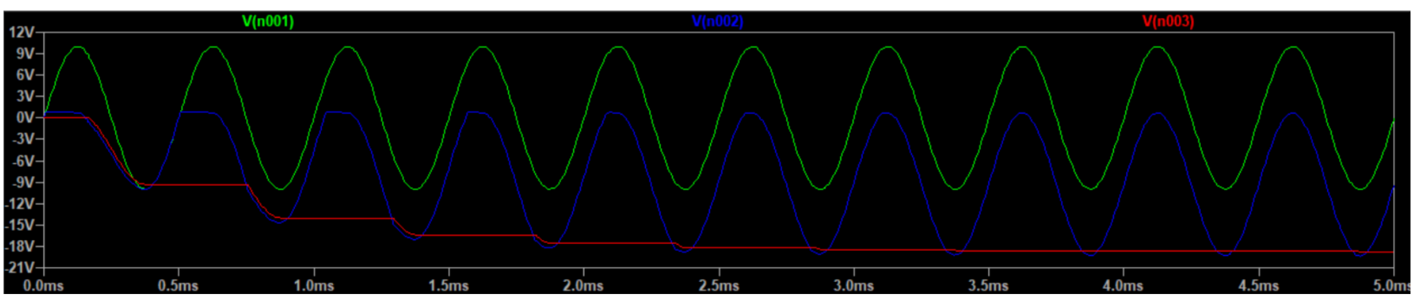


Figure 4: LTspice Simulation. V_{IN}, V_{D1}, and V_{OUT}

Problem 2

Design a dc power supply that operates from a 120 V (rms) 60 Hz household supply through a 10 to 1 step-down transformer having a single secondary winding. The dc supply feeds a resistive load that could be within a 200-1000 Ohm range and requires a nominal voltage of 5 V. You can assume that a 5.1 V Zener diode is available where $R_z = 10$ Ohms at $I_z = 20\ mA$ and $I_{zmin} = 5\ mA$. Perform complete simulations plotting the waveforms at various stages. Determine the line and load regulation of your design.

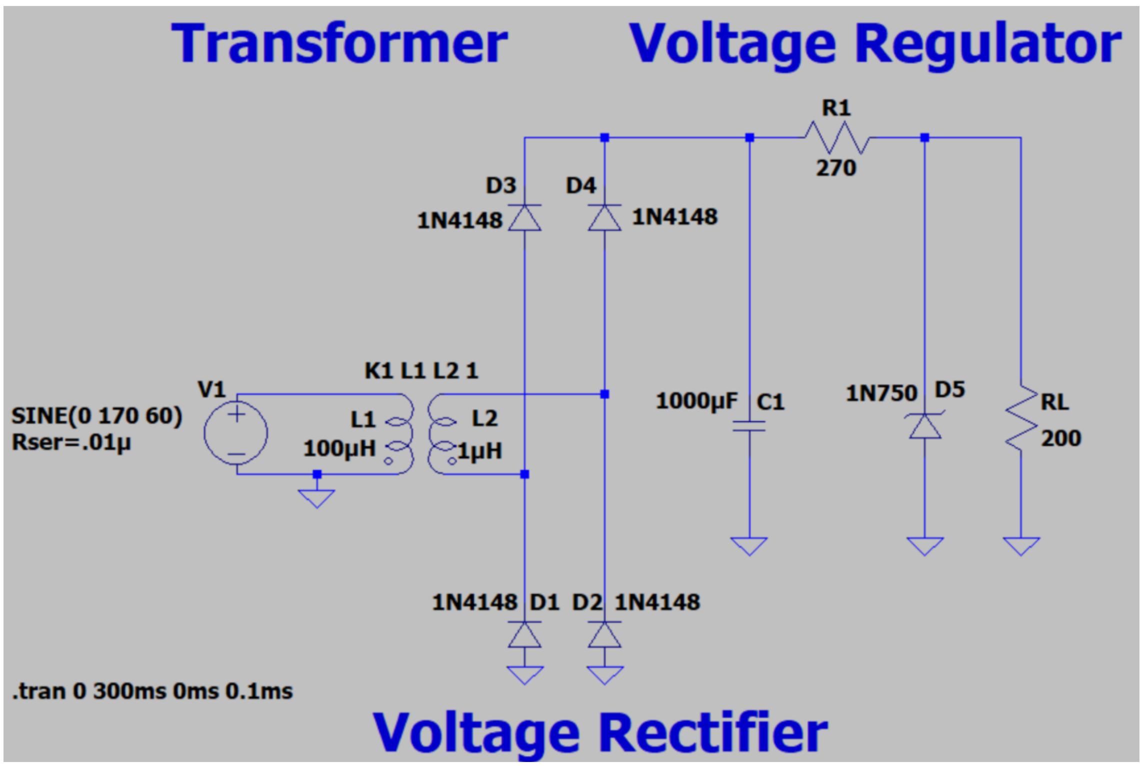


Figure 5: DC Power Supply

The design is divided into the following three parts:

the **transformer**,

the **full wave rectifier**,

and the **voltage regulator**.

PART A – Transformer

The first step was to find the peak voltage from the root means square voltage. The conversion between these two values is shown below. A V_{RMS} of 120V means the peak voltage must be about 170 V.

Equation 1: V_{RMS} to V_{PEAK} Conversion

$$V_{PEAK} = V_{RMS} * \sqrt{2}$$

The next step was to find the appropriate inductors to achieve the desired step-down ratio. The relationship between inductance and voltage is shown below. The desired voltage ratio of 1/10 means the inductance ratio must be 1/100.

Equation 2: Transformer Voltage Ratio

$$\text{Voltage Ratio} = \sqrt{Lsecondary/Lprimary}$$

Note the following in the circuit:

L1 = 100 μH

L2 = 1 μH

Testing the model with LTspice showed the transformer in action. A small resistor in series with the voltage source was added to the circuit so that the inductor was not directly in series with the power supply.

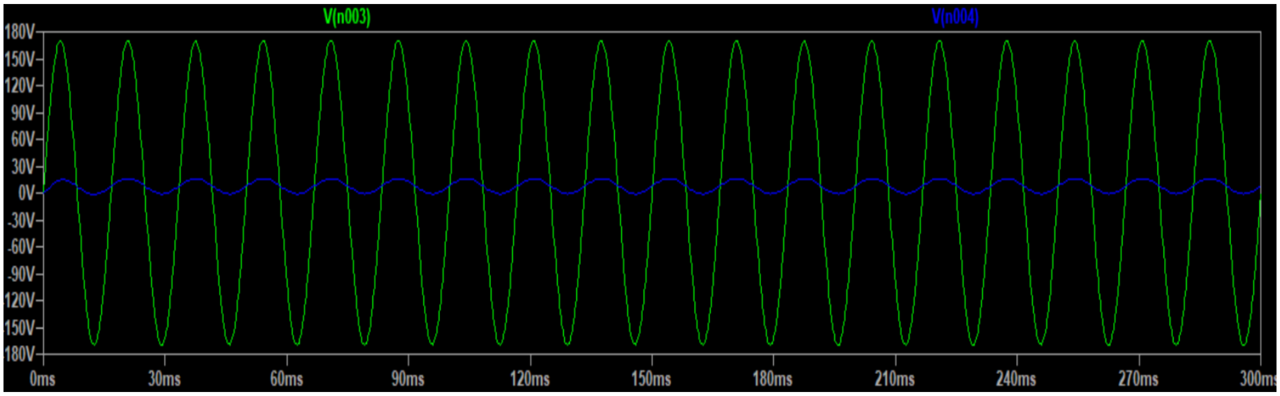


Figure 6: LTspice Simulation. V_{IN} and $V_{STEPDOWN}$

PART B – Full Wave Rectifier

As we discussed in class, the best when to get a DC output from an AC input is by using a full wave rectifier and smoothing capacitor. The transformer provides the second part of the voltage supply with an AC input. This AC input to the full wave rectifier is just a sine wave with an amplitude of 17 V oscillating at 60 Hz. Adding the capacitor, as shown in the figure below, smooths out the waveform, resulting in a small V_{RIPPLE}. As V_{RIPPLE} decreases, the waveform becomes closer and closer to DC.

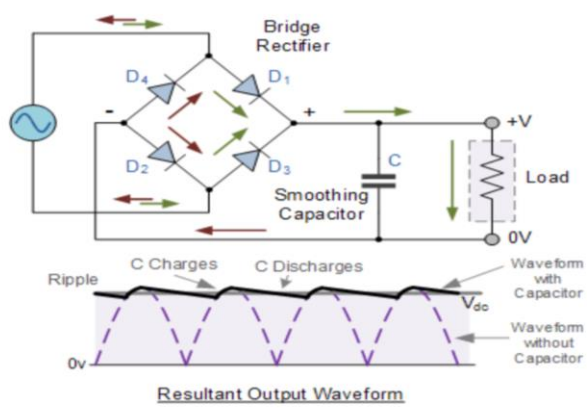


Figure 7: Full Wave Rectifier with and without Smoothing Capacitor

Note the following in the circuit:

C1 = 1000 μF

Equation 3: V_{RIPPLE}

$$V_{RIPPLE} = \frac{V_{PEAK}}{f R_L C}$$

The ripple voltage designed for was 10% of the output DC voltage for the power supply, about 0.5 V. This means that the capacitance would be about 1000 μF.

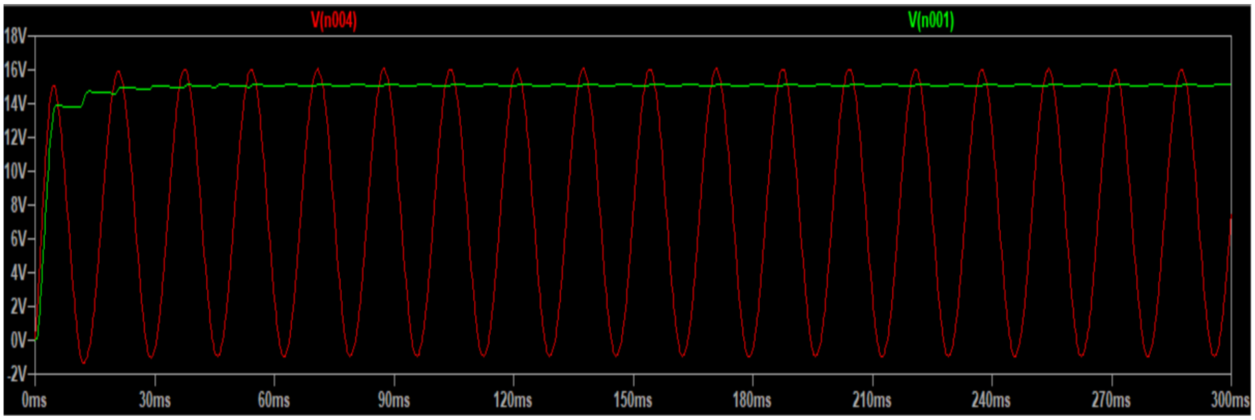


Figure 8: $V_{STEPDOWN}$ and $V_{RECTIFIED+SMOOTHED}$

PART C – Voltage Regulator

***NOTE:** The Zener diode, 1N750, used in the LTspice simulation has a breakdown voltage $V_{BREAKDOWN}$ = 4.7 V. This diode was chosen as it was closest to the provided one in the problem statement.

After the voltage from the transformer is rectified, it must be regulated down to 5 V. To do this, we use a voltage regulator in the form of a resistor and Zener diode.

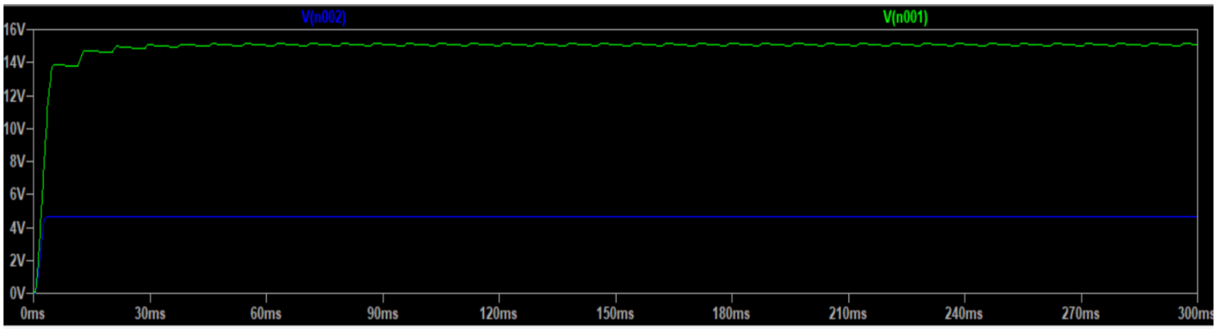


Figure 9: $V_{REGULATOR\text{-}INPUT}$ and $V_{REGULATED}$

Note the following in the circuit:

R1 = 270 Ω (Calcualted with equation 4)

RL = 200 Ω (Worst case ripple)

Equation 4: R1

$$R_Z = \frac{V_{OUT} - V_{IN}}{I_Z}$$

Equation 5: Line Regulation

$$\text{Line Regulation: } \frac{\Delta V_{OUT}}{\Delta V_{IN}} * 100\%$$

Equation 6: Load Regulation

$$\text{Load Regulation: } \frac{\Delta V_{OUT}}{\Delta I_C}$$

By zooming in on the waveforms we can find the change in V_{OUT}, V_{IN}, and I_C. The result is that our line regulation is: $\frac{4.6835\,V - 4.6815\,V}{15.02\,V - 14.74\,V} * 100\% = .71\%$

and our load regulation is: $\frac{4.6835\,V - 4.6815\,V}{24.421\,mA - 24.405\,mA} = 125\ \Omega$