Document Title

A5133 reference code for FIFO extension mode

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Preliminary	Aug. 16 , 2022	
0.1	Add delay time after enable EFSW&EFRE	Mar. 3, 2023	

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RF Chip-A5133
Reference code for FIFO extension mode

1. Introduction

This document describes development of simple example procedures by A5133 Extend FIFO mode. It could support user how to implement two-way radio and how to initial A5133.

2. System summary

The procedure is divided into two parts, one is Master, and another one is Slave.

Master side ：After power on and initial RF chip procedure, Master will deliver 256 bytes data from TX FIFO. After delay 50ms, Master will deliver 256 bytes data again.

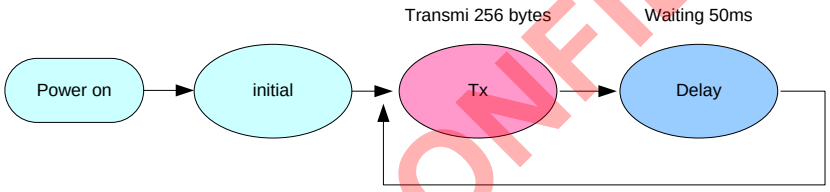

Fig1. The state diagram of master side

Slave side： After power on and initial RF procedure, Slave enters into RX state for receiving data from Master. Slave is set to stay in RX state until it receives the data. If Slave receives the data from Master, it will calculated bit error rate. After delay 30ms, Slave will enter into RX state again.

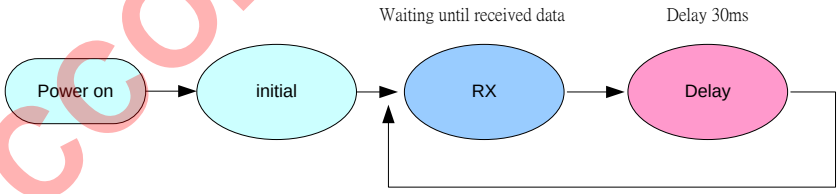

Fig2. The state diagram of Slave side

3. Hardware

3.1 System block diagram

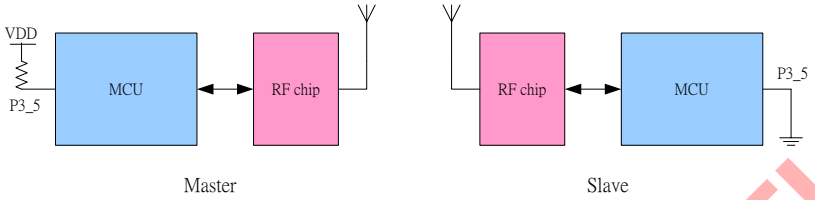

Fig3. System block diagram

MCU I/O Pin Definition:
The example is explanation how to use the I/O:

- SCS, SCK, SDIO - 3 wire serial interface to access A5133 register.
- GIO1 - The control signal that FIFO movements finish, MCU can monitor this pin and convey or receive packet to finish.
- CKO - Monitors signal that under extend FIFO mode, User can see FIFO the Pointer marginal value change, so as to control FIFO data write or FIFO data read motion.

MCU controls A5133 RF chip I/O assign:

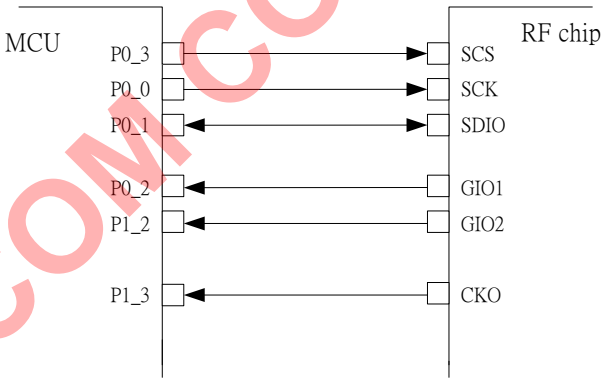

Fig4. Connections between 8051 MCU and A5133

4. Firmware Program

4.1Introduction

After power on reset, MCU do initialization of its Timer0 and Uart0 as well as A5133. Then, MCU check its Port 3_5 to identify Master or Slave. If Port 3_5 = 1, MCU executes Master code in the main program; else, MCU executes Slave code in the main program.

Master code：

1) First, write 64 bytes data to TX FIFO.
2) Enter TX state and transmit packet.
3) Waiting until CKO pin=1, write 48 bytes data to TX FIFO.
4) Return Step 4 and total write 4 x 48 Byte
5) Waiting until GIO1 pin=0, RF chip will automatically exit TX state back to PLL state.
6) After delay 50ms, return Step 2 to next cycle.

Slave code：

1) Enter RX state waiting until received data from Master.
2) IF CKO pin =1, MCU readout RX FIFO 48 Byte data to tmpbuf, and total 5 times.
3) Waiting until GIO1 pin=0, RF chip will automatically exit RX state back to PLL state.
4) Readout data from RX FIFO 16Byte data to tmpbuf.
5) MCU compares received 256 bytes data and calculates BER (Bit Error Rate)
6) After delay 30ms, return Step 2 to next cycle.
7) For each 500 ms, MCU reports BER to personal computer.

4.2 Example State Diagram

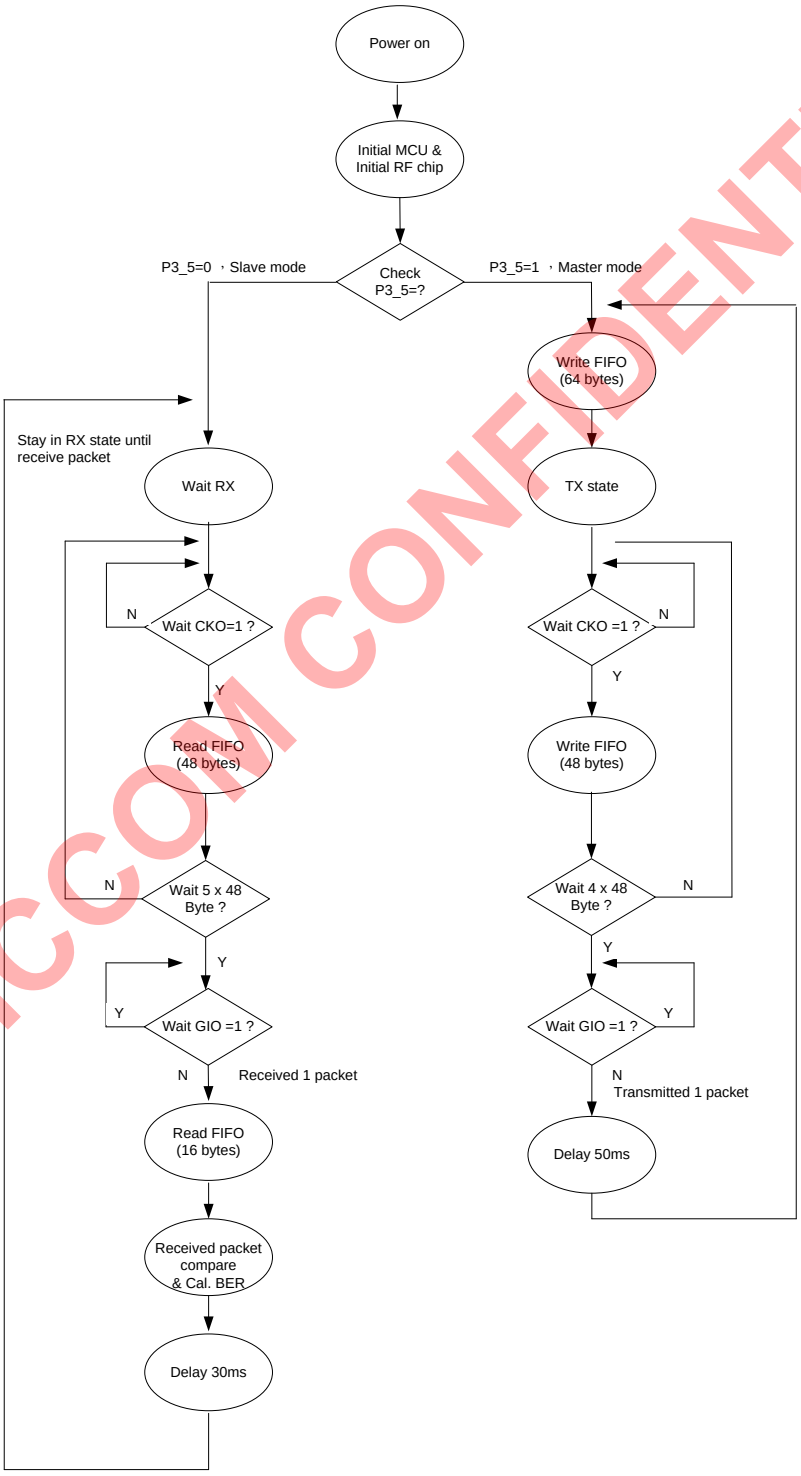

Fig5 Example state diagram

5. Explanation of reference code

1. This program only supplies reference procedure under FIFO extension mode. For FIFO data read/write timing control, User must according to the MCU working speed, processes FIFO data to read/write timing cautiously tightly, avoids the wrong occurrence.