Document Title

A5133 reference code for FIFO mode

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Preliminary	Jan. 20, 2020	
0.1	Merge 4Mbps,2Mbps,1Mbps,500Kbps config file	Apr. 14, 2020	
0.2	Modify DR2Mbps cfg. Addr0x20[], page0 value Modify DR1Mbps cfg. Addr0x20[], page0 value Modify DR500kbps cfg. Addr0x20[], page0 value	Nov. 1, 2021	
0.3	Modify DR4Mbps cfg file Modify DR2Mbps cfg file Modify DR1Mbps cfg file Delete DR500kbps cfg file	Dec. 6, 2021	
0.4	Add DR500kbps cfg file Modify DR 4Mbps cfg, CHGL=40, CHBH=80, Modify DR 2Mbps cfg, CHGL=40, CHBH=80, Modify DR 1Mbps cfg, CHGL=40, CHBH=80, DEVS=3, DMV=1, CHD=3	May. 17, 2022	
0.5	Add RF_TXPower setting procedure	Aug. 16, 2022	
0.6	Add delay time after enable EFSW&EFRE	Mar. 6, 2023	

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RF Chip-A5133
Reference code for FIFO mode

1. Introduction

This document describes development of simple example procedures by A5133 FIFO mode.

2. System summary

The procedure is divided into two parts, one is Master, and another one is Slave.

Master side ：After power on and initial RF chip procedure, Master will deliver 64 bytes data from TX FIFO, then jump into RX state to wait ACK data from Slave. If Master receives the ACK data, it will back to TX state to deliver next 64 byte data. If Master does not receive the ACK data, Master will also back to TX state for next 64 byte data delivery after staying in RX state for 50 ms.

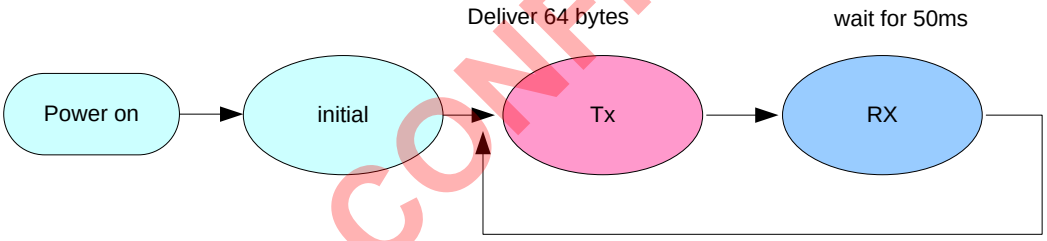

Fig1. The state diagram of master side

Slave side： After power on and initial RF procedure, Slave enters into RX state for receiving data from Master. Slave is set to stay in RX state until it receives the data. If Slave receives the data from Master, it will transit to TX state to deliver 64 bytes ACK data and then back to RX state for receiving next 64 byte data from Master.

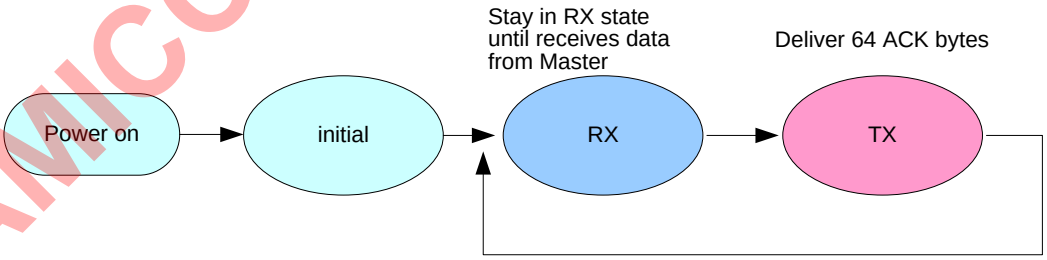

Fig2. The state diagram of Slave side

From Fig3, in Master side, Master enters into RX state to wait 64 byte ACK data once it delivers 64 byte data. If Master does not receive 64 byte ACK data within 50ms, it will back to TX state to deliver next 64 byte data. Once Master receives 64 byte packet, this packet will be authenticated and calculated bit error rate. After 10 ms, Master is set to back TX state for next 64 byte delivery.

From Fig3, in Slave side, Slave stays in RX state until it receives 64 byte data from Master. Once Slave receives 64 byte packet, this packet will be authenticated and calculated bit error rate. Then, Slave is set to enter TX state to deliver 64 byte ACK data to Master.
Based on the sample procedures between Master and Slave, user can learn how to implement two-way radio as well as how to calculate BER (bit error rate).

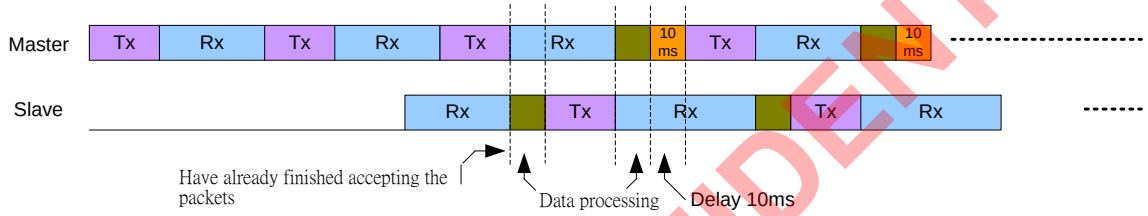

Fig3. Time slot for Master and Slave

3. Hardware

3.1 System block diagram

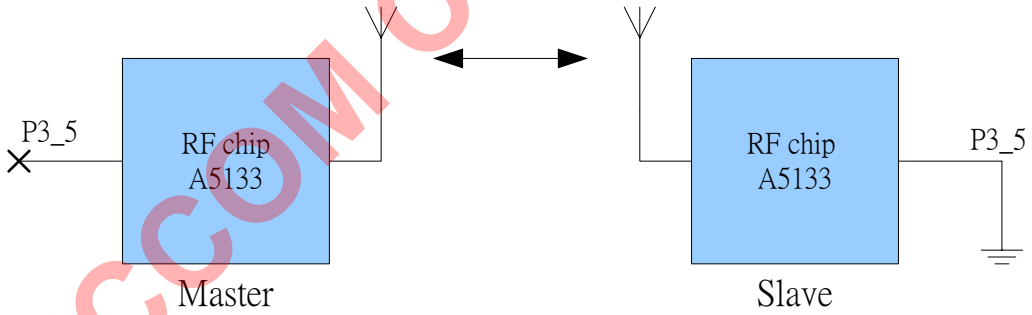

Fig4. System block diagram

**** I/O Pin – P3_5 define Master or Slave device**

MCU I/O Pin Definition:
The example is explanation how to use the I/O:

- SCS, SCK, SDIO - 3 wire serial interface to access A7130 register.
- GIO1 - The control signal that FIFO movements finish, MCU can monitor this pin and convey or receive packet to finish.

MCU controls A7130 RF chip I/O assign:

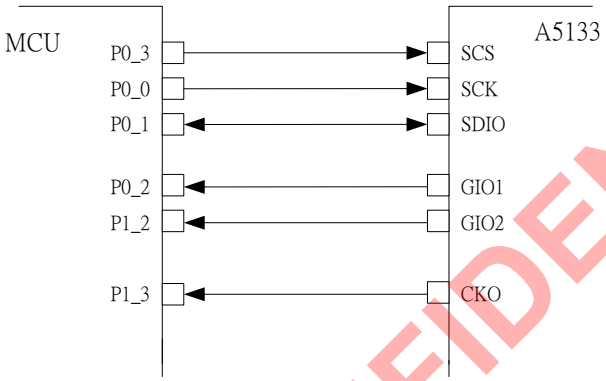

Fig5. Connections between 8051 MCU and A5133

4. Firmware Program

4.1Introduction

After power on reset, MCU do initialization of its Timer0 and Uart0 as well as A5133. Then, MCU check its Port 3_5 to identify Master or Slave. If Port 3_5 = 1, MCU executes Master code in the main program; else, MCU executes Slave code in the main program.

Master code：
1) Writes 64 bytes PN9 code into TX FIFO.
2) MCU asks A5133 to enter TX State to deliver 64 byte PN9 code. After done, A5133 is auto back to PLL state.
3) MCU asks A5133 to enter RX state to wait 64 byte ACK data.
4) Enable Timer 0 and clear TimeoutFlag flag
5) If Flag_Timeout = 1 (timeout = 50ms), back to step (1).
6) Once A5133 receives the packet, A5133 will be auto back to PLL state.
7) MCU compares received 64 bytes data with PN9 code and calculates BER (Bit Error Rate).
8) MCU calls delay loop for 10 ms, then back to step (1).
9) For each 500 ms, MCU reports BER to personal computer.

Slave code：
1) MCU asks A5133 to enter RX state until it receives 64 byte data from Master.
2) Once A5133 receives the packet, A5133 will be auto back to PLL state.
3) MCU compares received 64 bytes data with PN9 code and calculates BER (Bit Error Rate).
4) MCU writes 64 bytes PN9 code into TX FIFO.
5) MCU asks A5133 to enter TX State to deliver 64 byte PN9 code. After done, A5133 is auto back to PLL state.
6) Back to step (1).
7) For each 500 ms, MCU reports BER to personal computer.

4.2 Example State Diagram

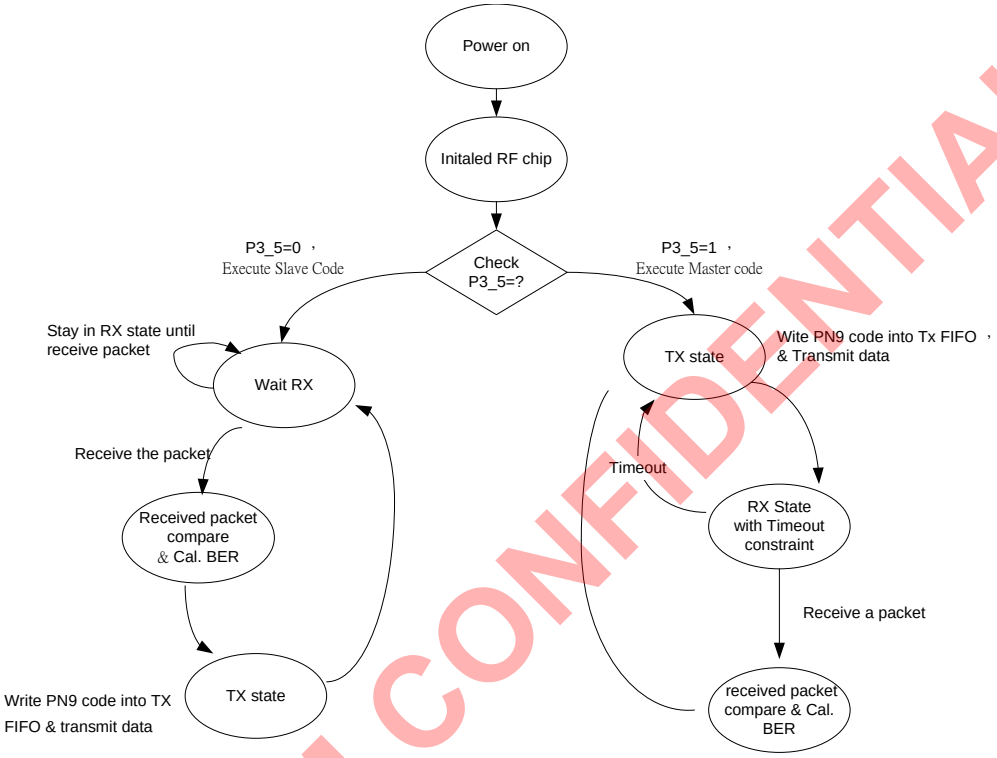

Fig6 Example state diagram