

Preliminary

Application Note AN_A5133_HW_D00

General Information



Document Title

Application Note AN_A5133_HW_D00

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	Jun., 2023	Preliminary



Table of Contents

1. Crystal Selection Guide	3
2. Application Circuit and Layout Guide	4
3. Tx Power Control Setting	8
4. Receiver Sensitivity Flatness	10
5 RSSI	11



1. Crystal Selection Guide

Selecting an appropriate crystal for A5133 is important for RF performance. If users are not familiar with choosing the X'tal, we suggest user to select the one in BOM of MD5133-A03 module spec. The X'tal spec. shown as table 1 is a suitable example. Users can also get more information in "FQA_0001_Xtal Selection". Users can adjust frequency by tuning the external capacitor at A5133 XI and XO pins. Please read A5133 datasheet or contact our FAE for detail.

Quartz Crystal Specification	SMD 2.0x1.6mm			
Center Frequency	16 MHz			
Frequency tolerance at room temperature	±20 ppm			
Frequency stability over operation temperature	±20 ppm			
Load Capacitance	9 pF			
Equivalent Series Resistor (ESR)	≤150Ω			
Shunt Capacitance	5 pF			
External Capacitor at A5133 XI pin	NC			
External Capacitor at A8133 XO pin	NC			
Crystal Setting Time(Typical)	0.6ms			

Table 1 Quartz Crystal Specification

Annotation:

A5133 can work well with a X'tal at ESR $\leq 150~\Omega$. However, the settling time of X'tal will get longer at higher ESR. The X'tal shown in BOM of MD5133-A03 module spec. is fully tested. If users have any problem with X'tal selection, please contact your X'tal supplier or Amiccom's FAE.

3



2. Application Circuit and Layout Guide

2.1 Application Circuit

MD5133-A03-01 is AMICCOM's reference design for 5GHz high power transmission application (please see module spec. for the last update). The schematic is as Fig. 2.1a and the layout is as Fig. 2.1b. This document mainly notifies some key points which should be paid attention while doing PCB layout.

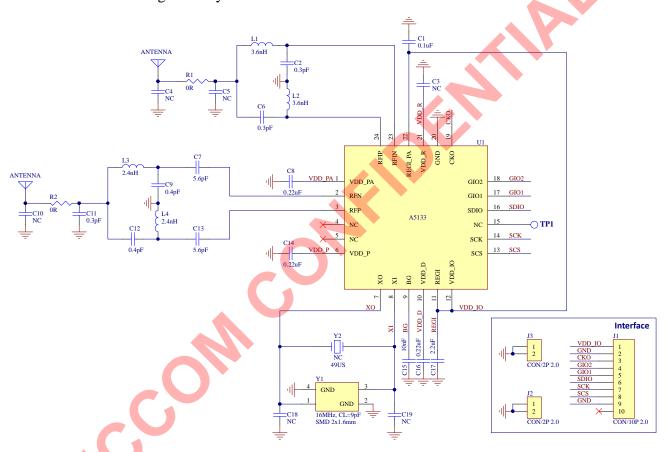
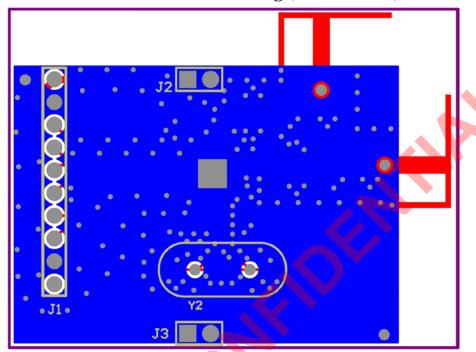


Fig. 2.1a Schematic of MD5133-A03-01



Module dimension drawing (Bottom view)



Module dimension drawing (Top view)

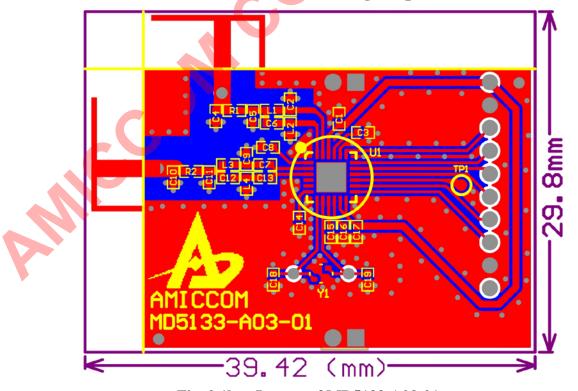


Fig. 2.1b Layout of MD5133-A03-01



2.2 Layout Guide

- 1. Bad ground plane always induce poor RF performance. Hence, a solid ground where it under the IC should be intact and not fragmentary can make the best RF performance of A5133. Please refer to Fig. 2.1b.
- 2. The impedance of RF path should be as close to 50 ohm as possible, and the RF trace should also be as short as possible. The ground plane below all RF traces must be intact and not fragmentary. The matching network (TX : C7, C13, C9, L4, C12, L3, C11, R2, C10; RX : C2, L2, C6, L1, C5, R1, C7) should be placed close to A5130 IC because the matching network affects RF performance (power, and current) heavily. Therefore, we strongly recommend user to follow components placement and layout where shown by green traces in Fig. 2.2a. without any change. (P.S: The Lumped-element Balun is consists of C2, L2, C6, L1, C9, L4, C12, L3.)

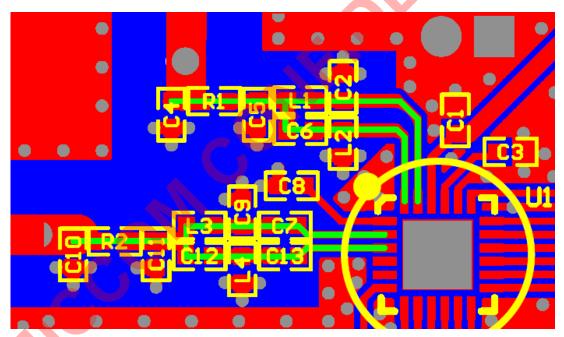


Fig. 2.2a RF matching trace (green)

3. In addition to ground plane, the clean and stable VDD source is also a key factor to impact RF performance. The bypass capacitors (C1, C14, C15, C16 and C17) on this reference design are used for this purpose. To have the clean VDD source to A5133, those capacitors should be placed as close to the IC pins as possible and its ground via should be just nearby the components ground pad. Please refer to Fig. 2.1b.



4. The X'tal traces should be as short as possible and are better to be isolated by ground via. In addition, to minimize cross talk issue, components placement shall be as far away to X'tal trace as possible. Please refer to the green traces in Fig. 2.2b.

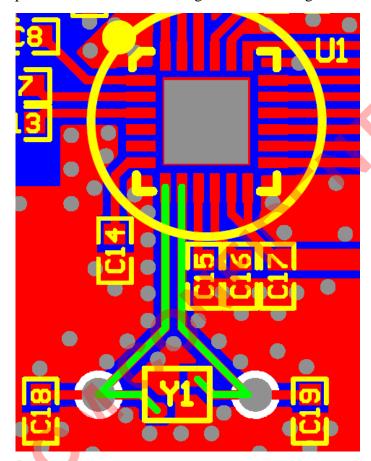


Fig. 2.2b X'tal trace (green)



3. Tx Power Control Setting

Users can get different TX power from Control Register (Fig. 3.1a) as the tables below. The default setting for A5133 is 1 of Fig. 3.1b. The power maybe change between different modules because the variation of components.

Control	Register		
Address Name		Bits	
21h	EXT3_P9	b[2:0]	PGV_PA
22h	EXT7_P1	b[4]	TXLPN
2Dh	TX test	b[5]	TXCS
2011	IN test	b[2:0]	TBF
21h	EXT2_P8	b[6:4]	TPA
21h	EXT5_P11	b[1:0]	CBBF
	DAS_P6	b[2]	TXLO_HC
2Ah		b[1]	PAB_HCS
		b[0]	PA_HCS

Fig. 3.1a Control Register Table

	TX Control Register										
Setting	PGV_PA	TXLPN	TXCS	CBBF	TXLO _HC	PAB _HCS	PA _HCS	TBF	TPA	TX power (dBm)	Current (mA)
1	2.5V	1	1	2	0	1	1	7	2	15.5	93
2	2.5V	1	1	2	0	1	1	2	0	15.1	85
3	2.5V	1	1	2	0	1	0	1	1	14.0	73
4	2.5V	1	1	2	0	0	0	М	0	13.3	68
5	2.5V	1	1	2	0	0	0	1	4	12.3	64
6	2.5V	1	1	2	0	0	0	1	3	12.1	62
7	2.5V	1	1	0	0	0	0	0	6	10.3	55
8	1.6V	1	0	0	0	0	0	5	6	8.9	51
9	1.6V	1	1	3	0	1	0	0	0	8.0	49
10	1.6V	1	0	1	0	0	0	1	7	7.4	46
11	1.6V	1	0	2	0	0	0	0	7	5.9	44
12	1.6V	1	0	0	0	0	0	0	7	5.3	40

Fig. 3.1b Tx Power Control Setting (15 ~ 5dBm) and current consumption

8



Setting	PGV PA	TXLPN	TXCS	CBBF	TXL0 HC	PAB HCS	PA HCS	TBF	TPA	TX power (dBm)	Current (mA)
13	2.4V	0	1	2	0	1	1	4	2	-0.5	36
14	2.5V	0	1	2	0	1	1	4	1	-1.4	32
15	2.5V	0	1	2	0	1	1	4	0	-2.4	30
16	2.5V	0	1	2	0	0	1	7	0	-3.2	30
17	2.5V	0	1	2	0	1	1	3	0	-4.2	29
18	2.5V	0	1	2	0	0	1	5	0	-5.3	29
19	2.5V	0	1	3	0	0	1	3	0	-6.0	30
20	2.4V	0	1	2	0	1	1	2	0	-6.9	28
21	2.5V	0	1	3	0	1	1	0	0	-7.7	29
22	2.4V	0	1	2	0	1	1	1	1	-9.0	30
23	2.4V	0	1	2	0	0	1	1	1	-10.5	30

Fig. 3.1c Tx Power Control Setting (0 ~ -10dBm) and current consumption

Annotation:

The input voltage is 3.3V (REGI).

User can get more information from our FAE.



4. Sensitivity Flatness

Users can set different channel by setting CHN (channel number) in register [0E]. The default setting of register [0E] is 0x41 by 4Mbps data rate. When Tx frequency is in the N*16MHz (X'tal frequency) $\pm 2MHz$, the sensitivity will degrade a little because of the interference from the X'tal. We suggest customers avoid using these channels.

Typical sensitivity flatness is shown in fig. 4.1.

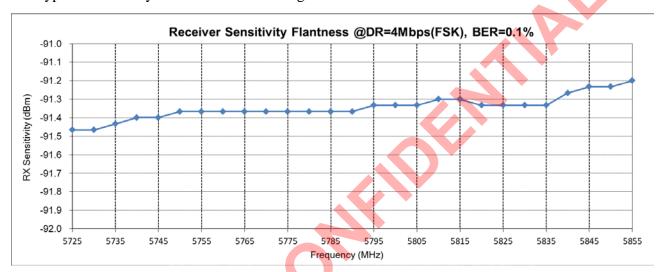


Fig. 4.1 Receiver Sensitivity Flatness



5. RSSI

A5133 has built-in digital RSSI (Received Signal Strength Indicator) which measure the strength of the incoming RF signal. The digital RSSI can be read form ED value and its range is form 0 to 255 (8bits). In the linear range, users can use the formula below to get the rough input power of the module.

$$Pin (dBm) = 12 * [(ADC - RL) / (RH - RL)] - 83$$

ADC value can be read form the register [1E],

RL value can be read from the register [1C],

RH value can be read form the register [1B].

The ADC values of each IC may have slight difference. If customers want to get more accurate RSSI value, they should use the ICs with RSSI tuning. Please contact Amiccom's FAE for detail about the RSSI tuning.

Typical RSSI characteristic is shown in fig. 5.1.



Fig. 5.1 RSSI Curve