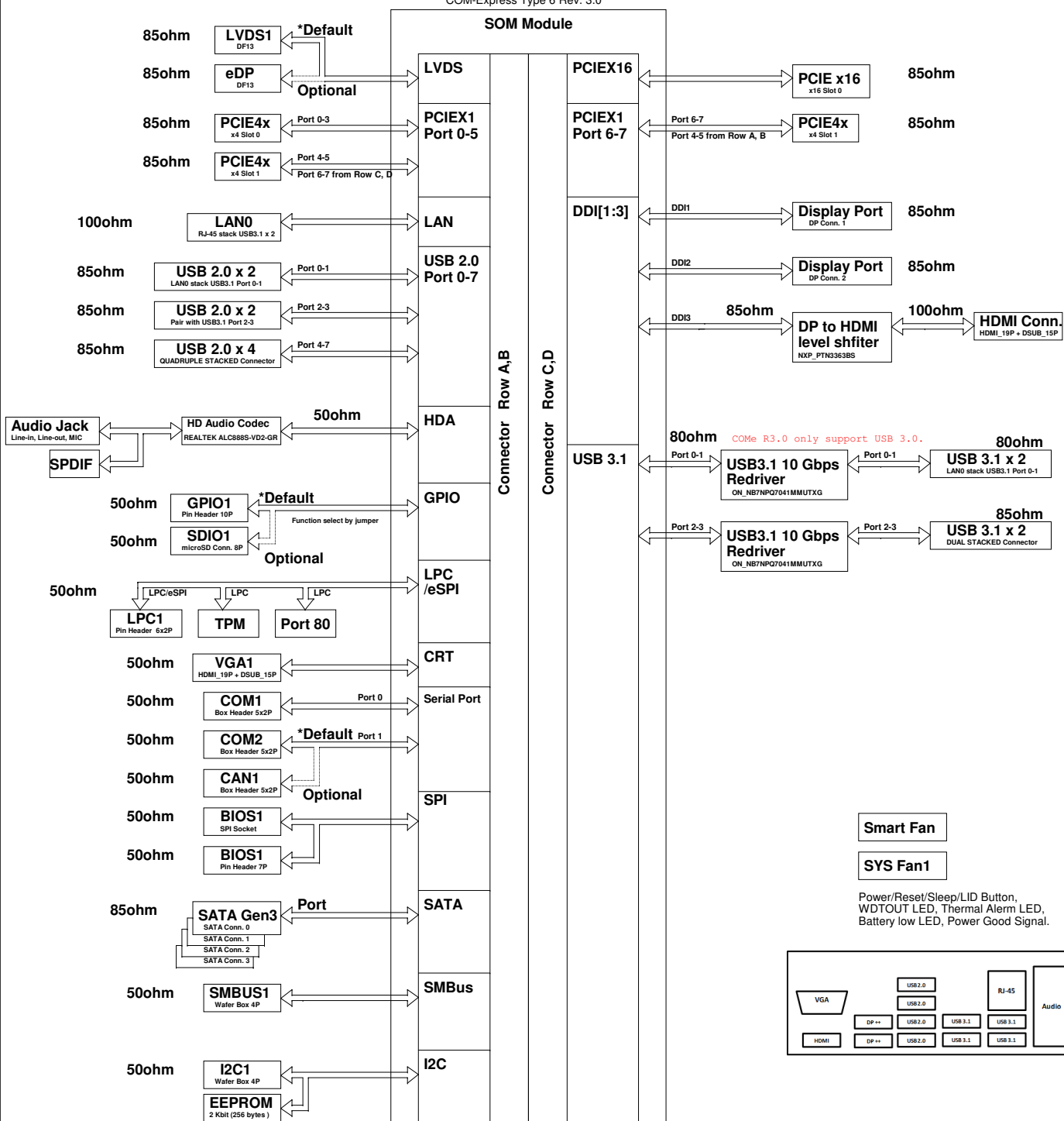


# Model Name: SOM-DB5830

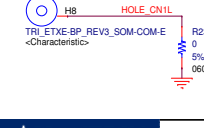
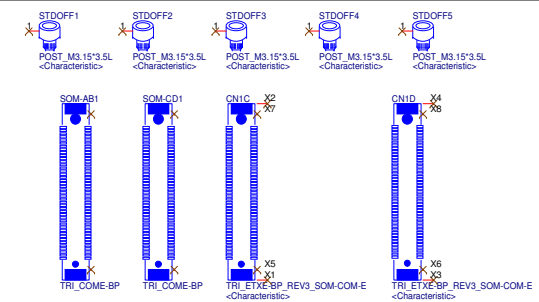
01	COVER
02	Block Diagram
03	Power Map
04	COMe R3.0 Type6 RAW A/B
05	COMe R3.0 Type6 RAW C/D
06	LAN0/USB 3.1 Port 0-1
07	USB3.1 Port 2-3
08	USB3.1 Redriver Port 0-1
09	USB3.1 Redriver Port 2-3
10	USB2.0 Port 4-7
11	BIOS socket/SATA/RTC
12	HD Audio Codec ALC888
13	PCIe X4 Slot 1-2
14	PCI Express X16 Slot
15	Clock Buffer PCI-E/PCI
16	VGA
17	LVDS Connector
18	HDMI Conn. DDI3
19	DP Conn. DDI port 1-2
20	SYS FAN / SMART FAN
21	GPIO/SMBus/I2C/MicroSD/BZ
22	BIOS / eSPI selection
23	Port 80/ LPC PH / TPM


24	COM Port 1-2 / CAN
25	LED/SCREW/PROBE/BTN/PCB
26	ATX power / +V5_DUAL
27	DC IN / +V3.3_DUAL
28	RAPID SHUTDOWN
29	Revision History





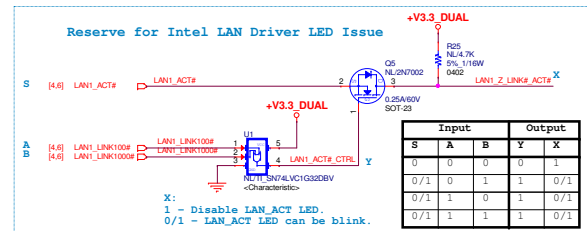
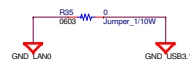
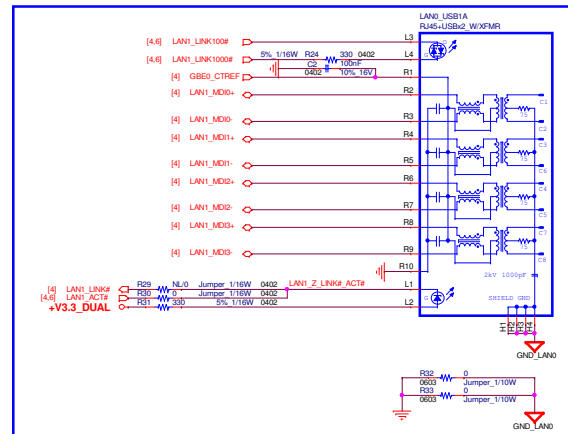
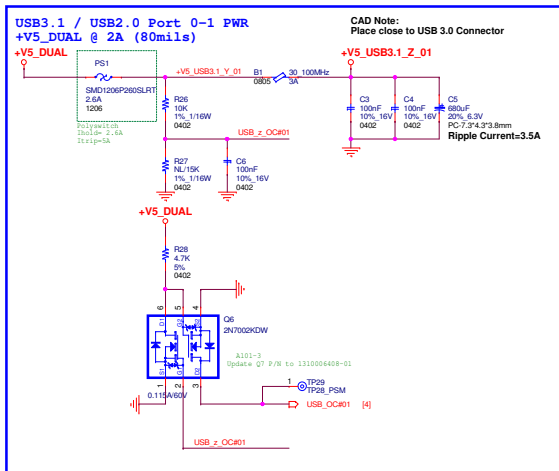




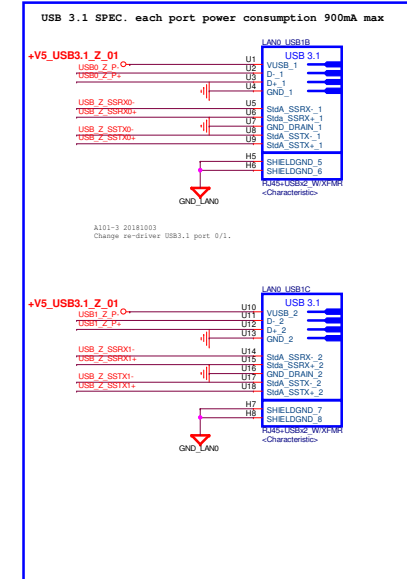
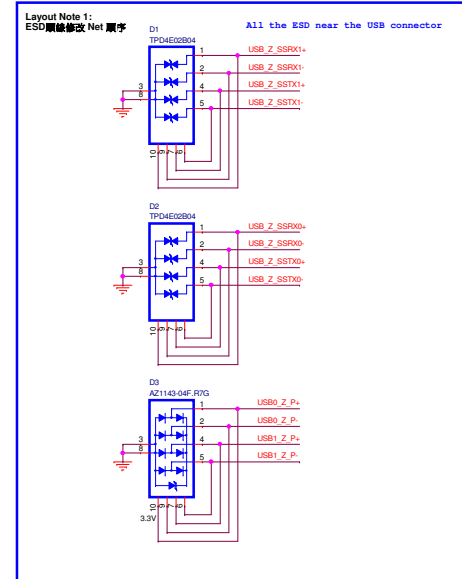
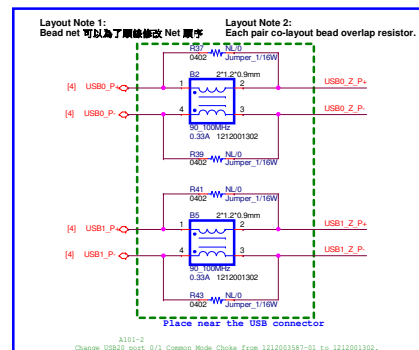
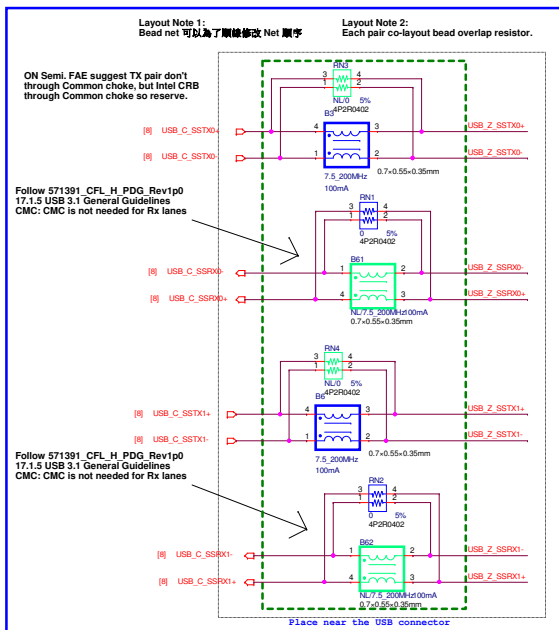
1  TP28 TP28\_PSM

**COM.0 R3.0 Changes from R2.1:**  
**Remove TYPE 2 D97 pin PEG\_ENABLE#.**  
**TYPE 6 is RSVD.**

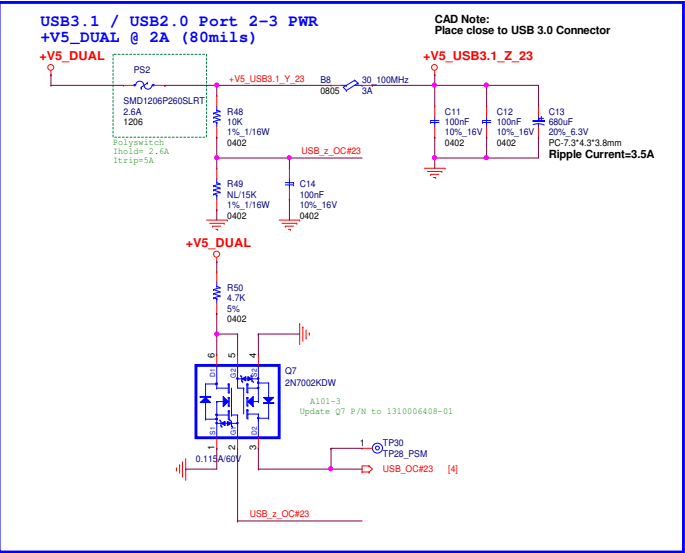
**LAN0**  
**RJ-45 (w/ USB3.1 x2)**



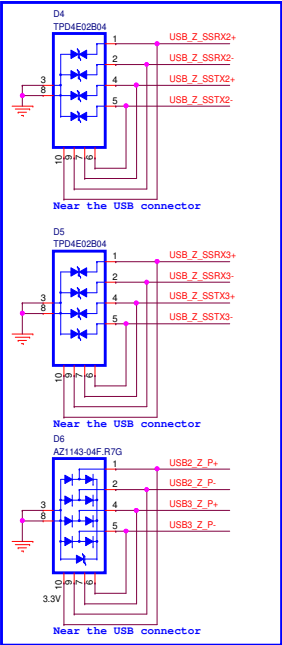
LED-Function	LED Color#	LED State	Description
Link Speed	Green / Orange	Off	10 Mbps link speed
		Green	100 Mbps link speed
		Orange	1000 Mbps link speed
Link Status & Activity	Yellow	Off	No Link
		Steady On	Link established, no activity detected
		Blinking	Link established, activity detected



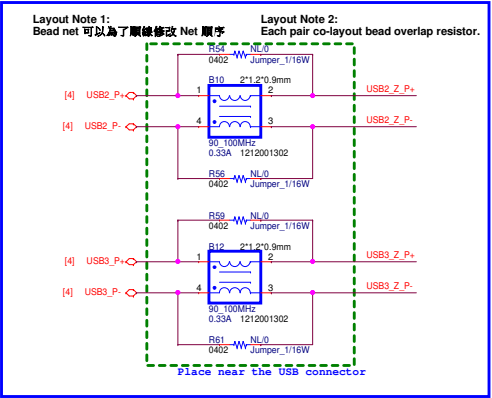
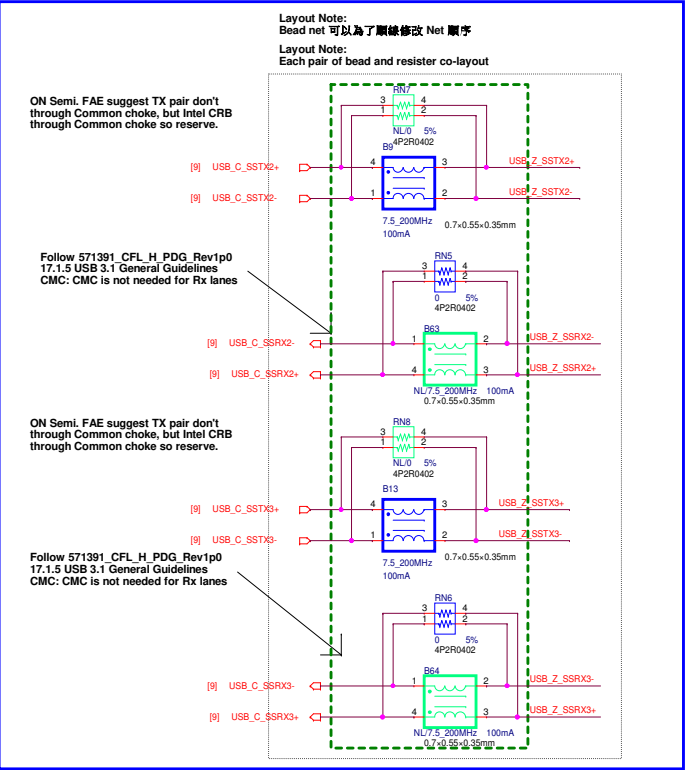
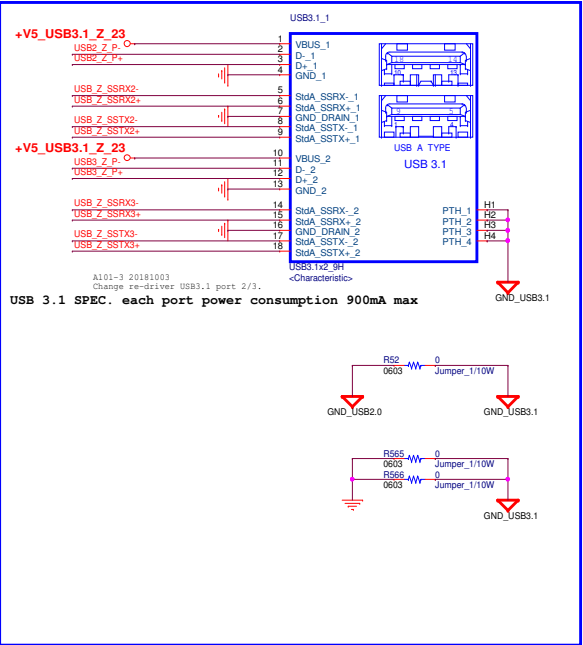
USB3.1 x2



A101-1 170915  
After ON Semi. review, ESD should work OK,  
but will limit bandwidth due to loss.  
Layout Note:  
ESD net 可以為了順線修改 Net 順序

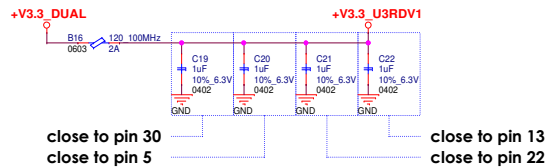


USB3.1 Connector Port 2-3





+V3.3\_U3RDV1 @ 130mA (10.4mils)



## USB3.1 Gen2 Redriver for RJ45 + USB3.1 x2 Port 0-1

From PCH

To PCH

From PCH

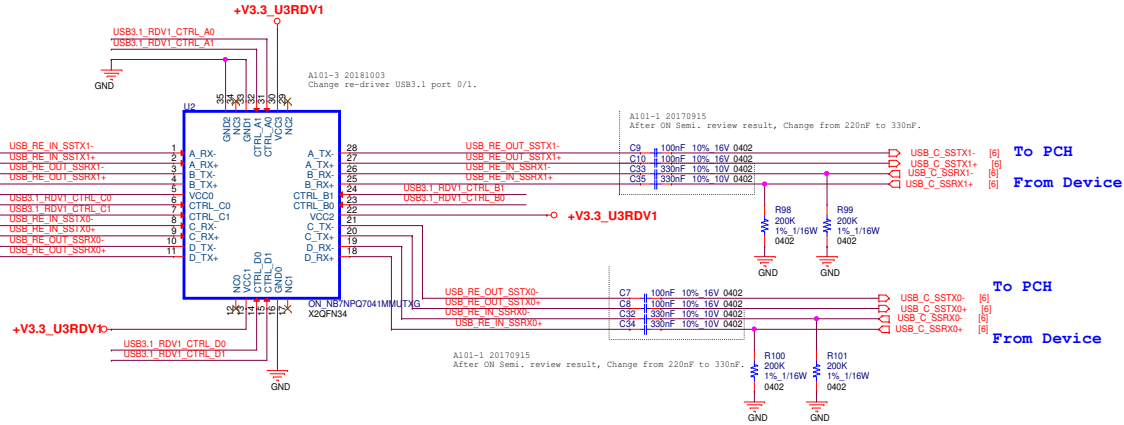
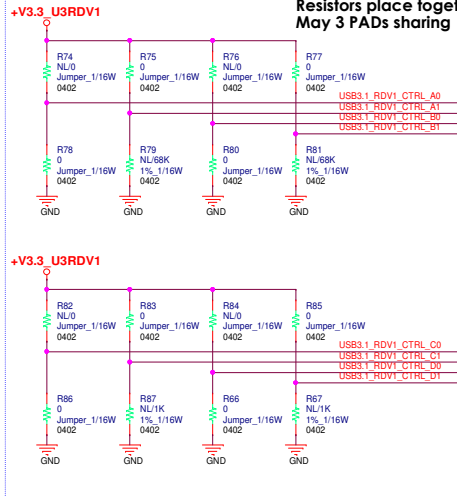
To PCH

### HW Strap table for equalization and flat gain

DC Input Setting "L"	Input pin connected to GND
DC Input Setting "R"	A "68k ohm" must be applied between pin and GND
DC Input Setting "F"	Input pin is left floating
DC Input Setting "H"	Input pin connected to VCC

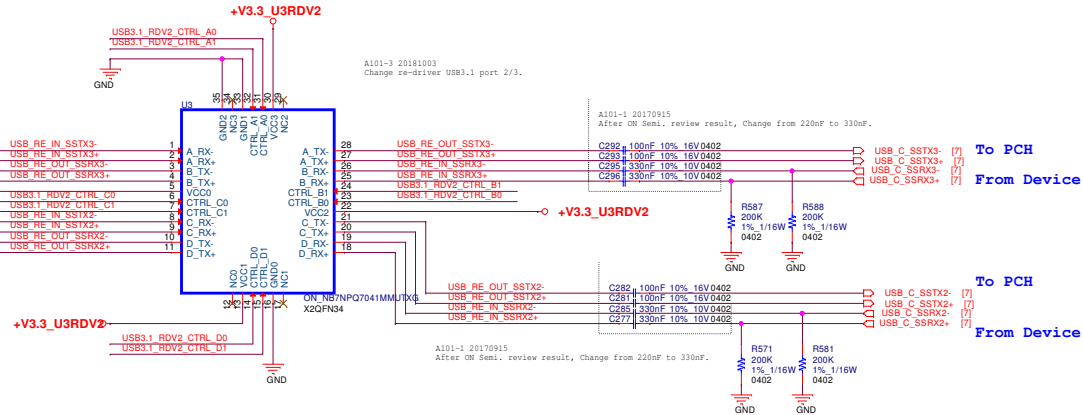
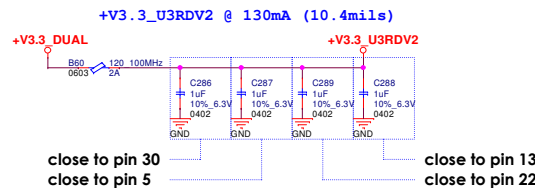
ON\_NB7NPQ7041MMUTXG CAD Note:  
Internal pull-up 100k ohm and pull-down 200k ohm.

Layout note:  
Resistors place together  
May 3 PADs sharing





# USB3.1 Gen2 Redriver for USB3.1 x2 Port 2-3



## HW Strap table for equalization and flat gain

DC Input Setting "L"	Input pin connected to GND
DC Input Setting "R"	A "68k ohm" must be applied between pin and GND
DC Input Setting "F"	Input pin is left floating
DC Input Setting "H"	Input pin connected to VCC

ON\_NB7NPQ7041MMUTXG CAD Note:  
Internal pull-up 100k ohm and pull-down 200k ohm.

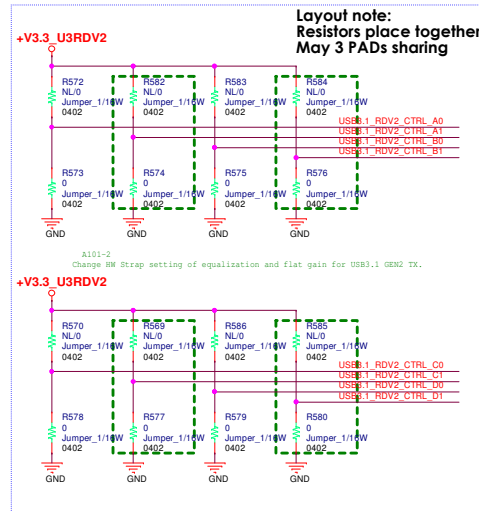


Table 2. CONTROL PIN EFFECTS (Typical Values)

Setting #	Channel A Channel C		Channel B Channel D		EQ Equalize	FG Flat Gain
	CTRL_A1 / C1	CTRL_A0 / C0	CTRL_B1 / D1	CTRL_B0 / D0		
1	L	L	L	L	4 dB	-1 dB
2	L	R	L	R	5 dB	-1 dB
3	L	F	L	F	6 dB	-1 dB
4	L	H	L	H	8 dB	-1 dB
5	R	L	R	L	9 dB	-1 dB
6	R	R	R	R	3 dB	1 dB
7	R	F	R	F	4 dB	1 dB
8	R	H	R	H	5 dB	1 dB
9	F	L	F	L	6 dB	1 dB
10	F	R	F	R	7 dB	1 dB
11 (Default)	F	F	F	F	8 dB	-2 dB
12	F	H	F	H	5 dB	-2 dB
13	H	L	H	L	7 dB	-2 dB
14	H	R	H	R	9 dB	-2 dB
15	H	F	H	F	10 dB	-2 dB
16	H	H	H	H	7 dB	-2 dB

Table 7. LVCMOS CONTROL PIN CHARACTERISTICS 4-State LVCMOS Inputs (CTRL\_A0, CTRL\_A1, CTRL\_B0, CTRL\_B1)

Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	DC Input Setting "L"	Input pin connected to GND			V
V <sub>IR</sub>	DC Input Setting "R"	A specified resistor must be applied between pin and GND	0.33*V <sub>CC</sub>		V
V <sub>IF</sub>	DC Input Setting "F"	Input pin is left floating	0.66*V <sub>CC</sub>		V
V <sub>IH</sub>	DC Input Setting "H"	Input pin connected to V <sub>CC</sub>	V <sub>CC</sub>		V
R <sub>PU</sub>	Internal pull-up resistance	100			kΩ
R <sub>PD</sub>	Internal pull-down resistance	200			kΩ
R <sub>ext</sub>	External Resistor for input setting "R"	68			kΩ

## TYPICAL APPLICATION

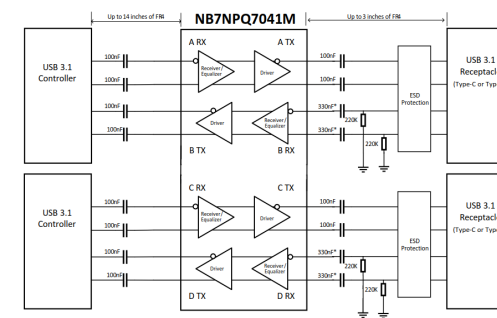


Figure 5. USB 3.1 Host Side NB7NPQ7041M Typical Application  
\*330nF capacitors on B RX and D RX are recommended, but not necessary in all cases.

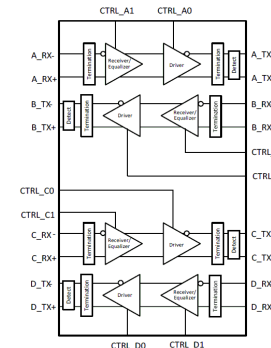
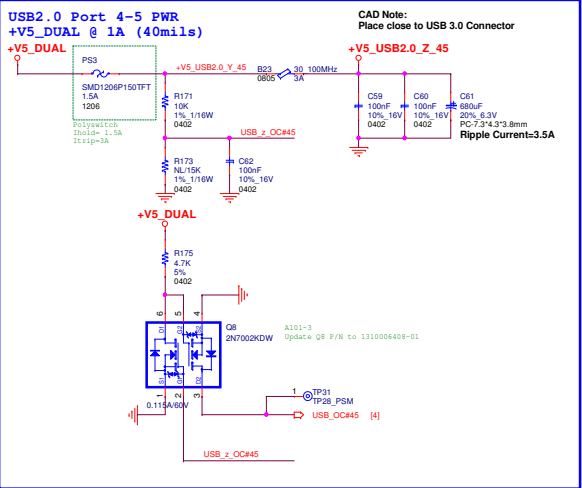
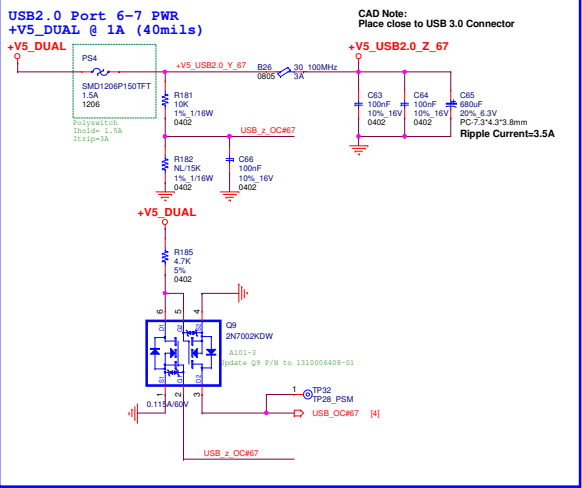


Figure 1. Logic Diagram of NB7NPQ7041M

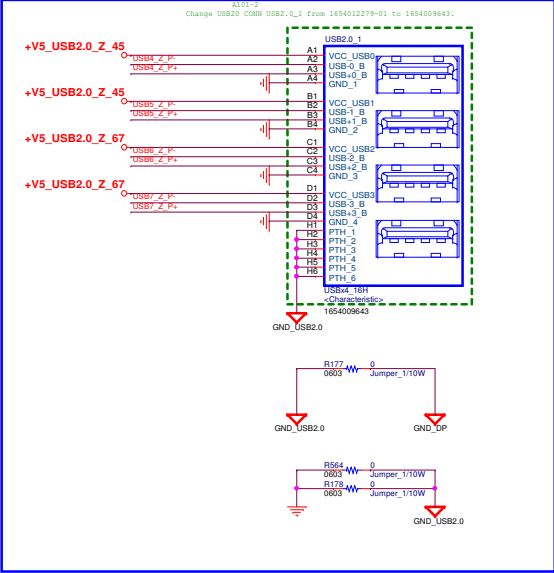
USB2.0 Port 4-5 PWR



USB2.0 Port 6-7 PWR



USB2.0 Port 4-7

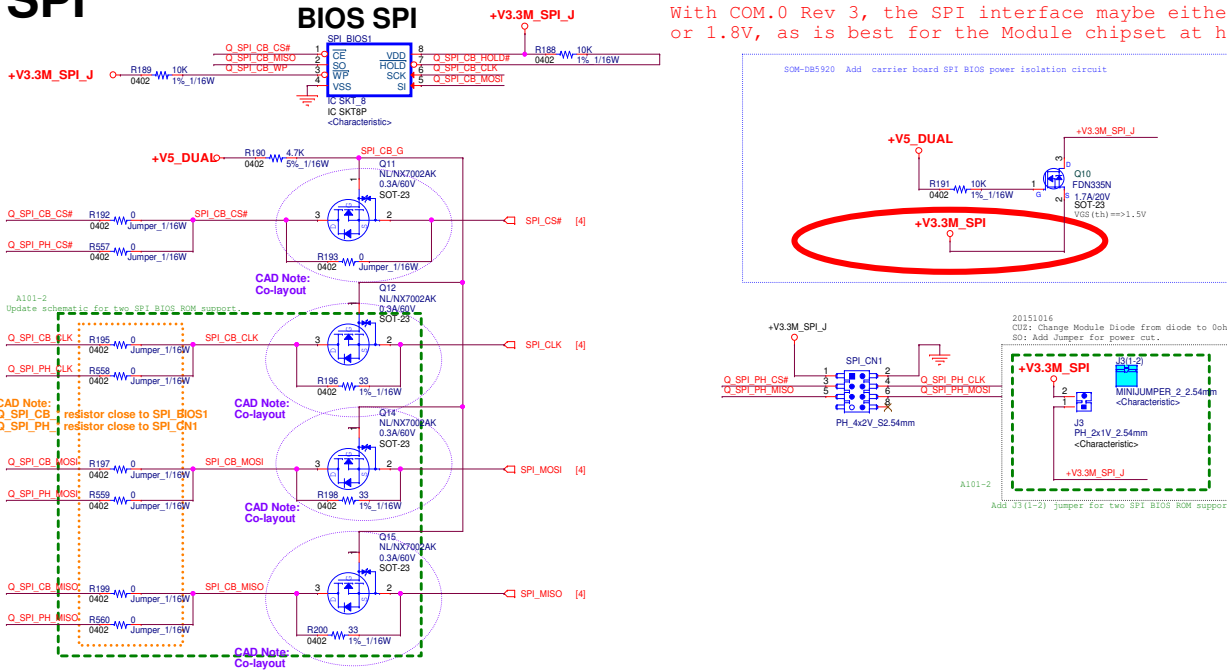


# SPI

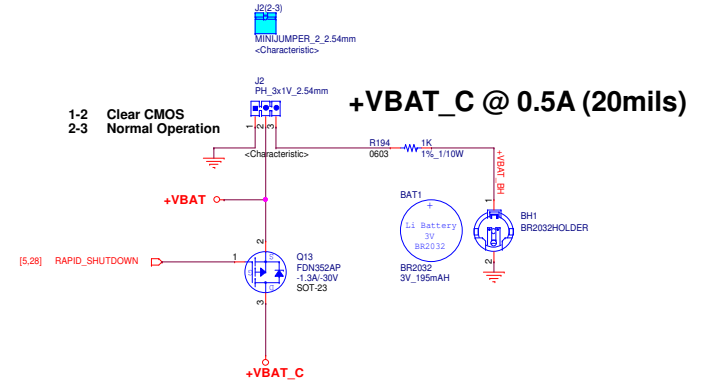
## BIOS SPI

### +V3.3M\_SPI @ 100mA

With COM.0 Rev 3, the SPI interface maybe either 3.3V or 1.8V, as is best for the Module chipset at hand.



## RTC BATTERY



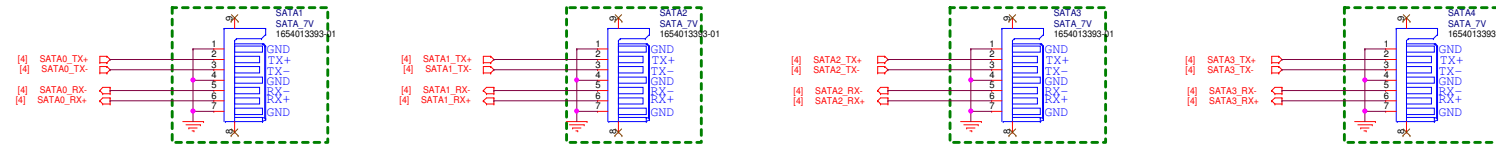
## SATA

P/N: 1654005955  
PIN length 3.3mm

P/N: 1654013393-0  
PIN length 2.1mm

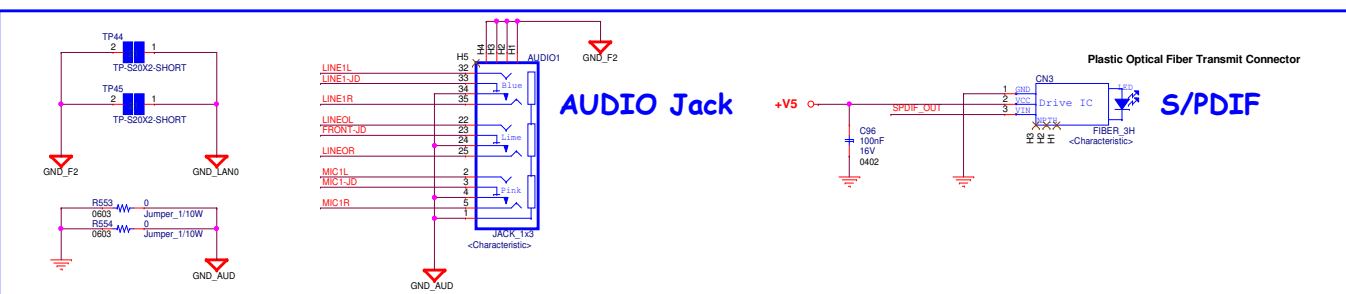
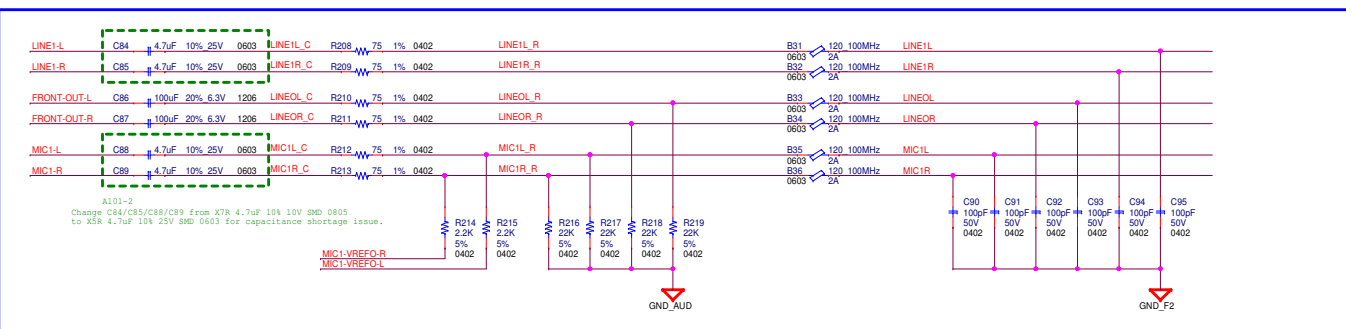
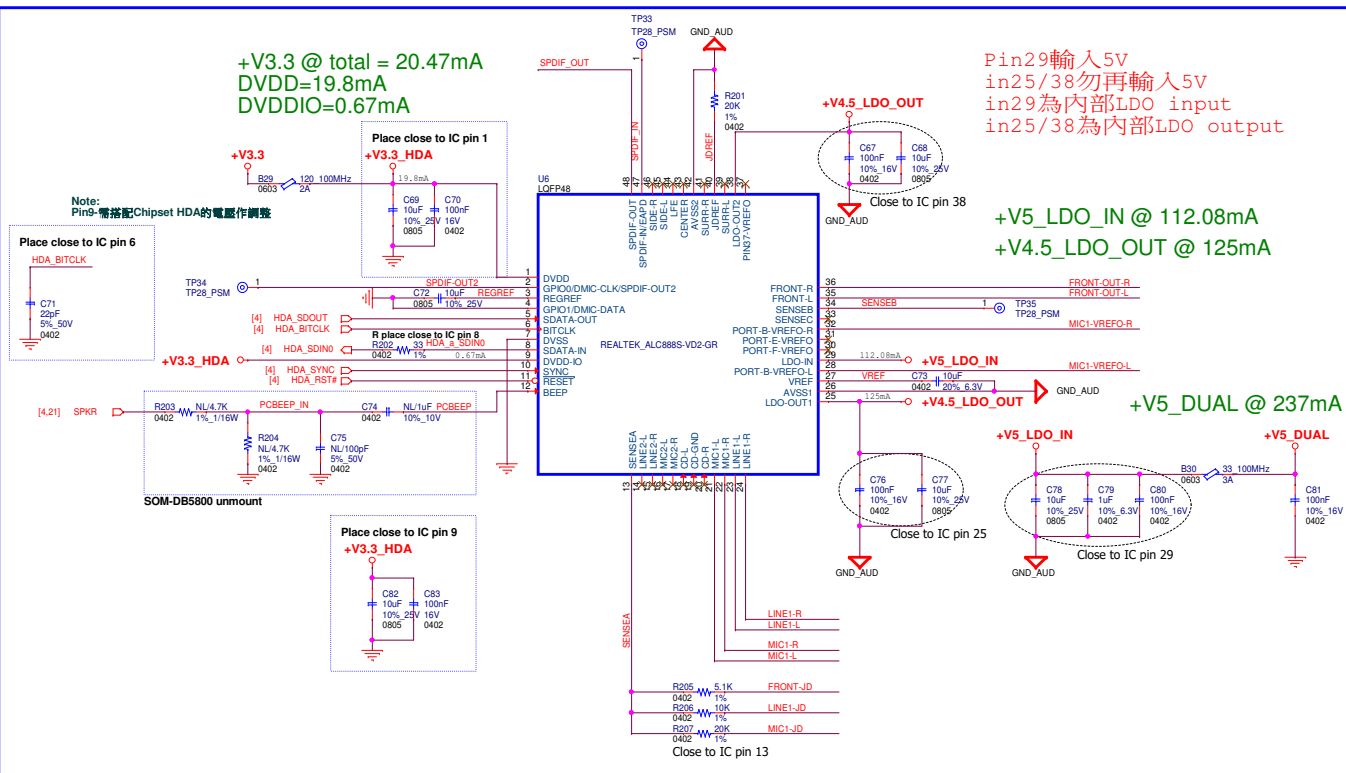
P/N: 1654013393-0  
PIN length 2.1mm

A101-2  
Change SATA1-SATA4 from 1654005955 to 1654013393-01 for DFM request.



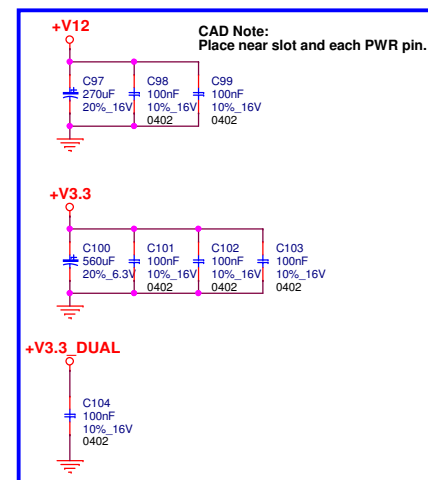
<b>ADVANTECH</b>			
Title		<b>BIOS socket/SATA/RTC</b>	
Size	Document Number	Rev	
	<b>SOM-DB5830</b>		<b>A1</b>
Date: Monday, October 22, 2018			
		Sheet	11 of 34

# HD Audio Codec REALTEK ALC888S-VD2-GR



The diagram shows the pinout for the PCIE4-1 connector, which is a PCIe 4.0 x4 port. The connector is labeled "PCIE4-1\_1" and "PCIEXPRESS 64V". The pins are numbered 1 to 32. The diagram shows the following connections:

- Power:**
  - V12 (12V) is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - V3.3 is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
- Signal:**
  - SMB\_CLK (SMB) is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - SMB\_DAT (SMB) is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_JTAG1 is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_JTAG2 is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_JTAG3 is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_JTAG4 is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_JTAG5 is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_PRSTN is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_RX+ is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_RX- is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_TX+ is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_TX- is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_RX+ is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_RX- is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_TX+ is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.
  - PCIE4\_1\_TX- is connected to pins B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32.



**PCIE4\_2**

**PCIE4\_2\_1#**

**PCIE4\_2\_2#**

**PCIE4\_2\_3#**

**PCIE4\_2\_4#**

**PCIE4\_2\_5#**

**PCIE4\_2\_6#**

**PCIE4\_2\_7#**

**PCIE4\_2\_8#**

**PCIE4\_2\_9#**

**PCIE4\_2\_10#**

**PCIE4\_2\_11#**

**PCIE4\_2\_12#**

**PCIE4\_2\_13#**

**PCIE4\_2\_14#**

**PCIE4\_2\_15#**

**PCIE4\_2\_16#**

**PCIE4\_2\_17#**

**PCIE4\_2\_18#**

**PCIE4\_2\_19#**

**PCIE4\_2\_20#**

**PCIE4\_2\_21#**

**PCIE4\_2\_22#**

**PCIE4\_2\_23#**

**PCIE4\_2\_24#**

**PCIE4\_2\_25#**

**PCIE4\_2\_26#**

**PCIE4\_2\_27#**

**PCIE4\_2\_28#**

**PCIE4\_2\_29#**

**PCIE4\_2\_30#**

**PCIE4\_2\_31#**

**PCIE4\_2\_32#**

**PCIE4\_2\_33#**

**PCIE4\_2\_34#**

**PCIE4\_2\_35#**

**PCIE4\_2\_36#**

**PCIE4\_2\_37#**

**PCIE4\_2\_38#**

**PCIE4\_2\_39#**

**PCIE4\_2\_40#**

**PCIE4\_2\_41#**

**PCIE4\_2\_42#**

**PCIE4\_2\_43#**

**PCIE4\_2\_44#**

**PCIE4\_2\_45#**

**PCIE4\_2\_46#**

**PCIE4\_2\_47#**

**PCIE4\_2\_48#**

**PCIE4\_2\_49#**

**PCIE4\_2\_50#**

**PCIE4\_2\_51#**

**PCIE4\_2\_52#**

**PCIE4\_2\_53#**

**PCIE4\_2\_54#**

**PCIE4\_2\_55#**

**PCIE4\_2\_56#**

**PCIE4\_2\_57#**

**PCIE4\_2\_58#**

**PCIE4\_2\_59#**

**PCIE4\_2\_60#**

**PCIE4\_2\_61#**

**PCIE4\_2\_62#**

**PCIE4\_2\_63#**

**PCIE4\_2\_64#**

**PCIE4\_2\_65#**

**PCIE4\_2\_66#**

**PCIE4\_2\_67#**

**PCIE4\_2\_68#**

**PCIE4\_2\_69#**

**PCIE4\_2\_70#**

**PCIE4\_2\_71#**

**PCIE4\_2\_72#**

**PCIE4\_2\_73#**

**PCIE4\_2\_74#**

**PCIE4\_2\_75#**

**PCIE4\_2\_76#**

**PCIE4\_2\_77#**

**PCIE4\_2\_78#**

**PCIE4\_2\_79#**

**PCIE4\_2\_80#**

**PCIE4\_2\_81#**

**PCIE4\_2\_82#**

**PCIE4\_2\_83#**

**PCIE4\_2\_84#**

**PCIE4\_2\_85#**

**PCIE4\_2\_86#**

**PCIE4\_2\_87#**

**PCIE4\_2\_88#**

**PCIE4\_2\_89#**

**PCIE4\_2\_90#**

**PCIE4\_2\_91#**

**PCIE4\_2\_92#**

**PCIE4\_2\_93#**

**PCIE4\_2\_94#**

**PCIE4\_2\_95#**

**PCIE4\_2\_96#**

**PCIE4\_2\_97#**

**PCIE4\_2\_98#**

**PCIE4\_2\_99#**

**PCIE4\_2\_100#**

**PCIE4\_2\_101#**

**PCIE4\_2\_102#**

**PCIE4\_2\_103#**

**PCIE4\_2\_104#**

**PCIE4\_2\_105#**

**PCIE4\_2\_106#**

**PCIE4\_2\_107#**

**PCIE4\_2\_108#**

**PCIE4\_2\_109#**

**PCIE4\_2\_110#**

**PCIE4\_2\_111#**

**PCIE4\_2\_112#**

**PCIE4\_2\_113#**

**PCIE4\_2\_114#**

**PCIE4\_2\_115#**

**PCIE4\_2\_116#**

**PCIE4\_2\_117#**

**PCIE4\_2\_118#**

**PCIE4\_2\_119#**

**PCIE4\_2\_120#**

**PCIE4\_2\_121#**

**PCIE4\_2\_122#**

**PCIE4\_2\_123#**

**PCIE4\_2\_124#**

**PCIE4\_2\_125#**

**PCIE4\_2\_126#**

**PCIE4\_2\_127#**

**PCIE4\_2\_128#**

**PCIE4\_2\_129#**

**PCIE4\_2\_130#**

**PCIE4\_2\_131#**

**PCIE4\_2\_132#**

**PCIE4\_2\_133#**

**PCIE4\_2\_134#**

**PCIE4\_2\_135#**

**PCIE4\_2\_136#**

**PCIE4\_2\_137#**

**PCIE4\_2\_138#**

**PCIE4\_2\_139#**

**PCIE4\_2\_140#**

**PCIE4\_2\_141#**

**PCIE4\_2\_142#**

**PCIE4\_2\_143#**

**PCIE4\_2\_144#**

**PCIE4\_2\_145#**

**PCIE4\_2\_146#**

**PCIE4\_2\_147#**

**PCIE4\_2\_148#**

**PCIE4\_2\_149#**

**PCIE4\_2\_150#**

**PCIE4\_2\_151#**

**PCIE4\_2\_152#**

**PCIE4\_2\_153#**

**PCIE4\_2\_154#**

**PCIE4\_2\_155#**

**PCIE4\_2\_156#**

**PCIE4\_2\_157#**

**PCIE4\_2\_158#**

**PCIE4\_2\_159#**

**PCIE4\_2\_160#**

**PCIE4\_2\_161#**

**PCIE4\_2\_162#**

**PCIE4\_2\_163#**

**PCIE4\_2\_164#**

**PCIE4\_2\_165#**

**PCIE4\_2\_166#**

**PCIE4\_2\_167#**

**PCIE4\_2\_168#**

**PCIE4\_2\_169#**

**PCIE4\_2\_170#**

**PCIE4\_2\_171#**

**PCIE4\_2\_172#**

**PCIE4\_2\_173#**

**PCIE4\_2\_174#**

**PCIE4\_2\_175#**

**PCIE4\_2\_176#**

**PCIE4\_2\_177#**

**PCIE4\_2\_178#**

**PCIE4\_2\_179#**

**PCIE4\_2\_180#**

**PCIE4\_2\_181#**

**PCIE4\_2\_182#**

**PCIE4\_2\_183#**

**PCIE4\_2\_184#**

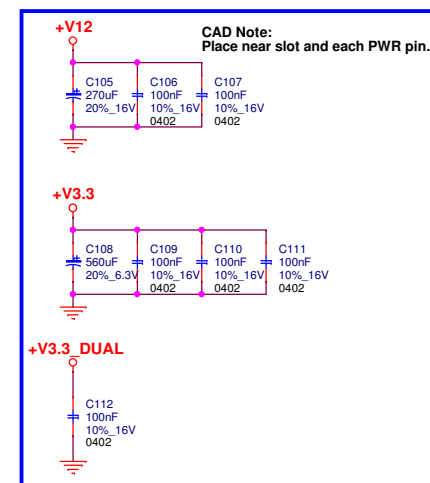
**PCIE4\_2\_185#**

**PCIE4\_2\_186#**

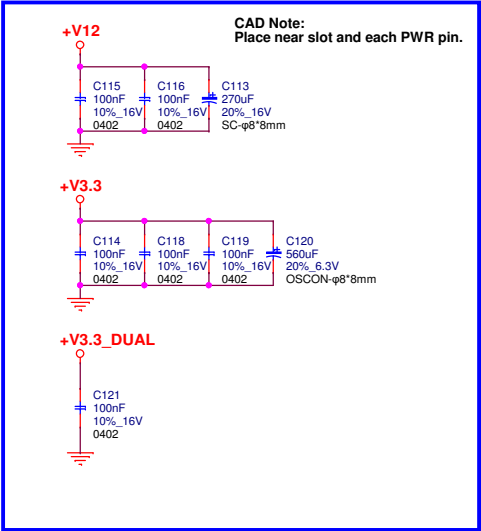
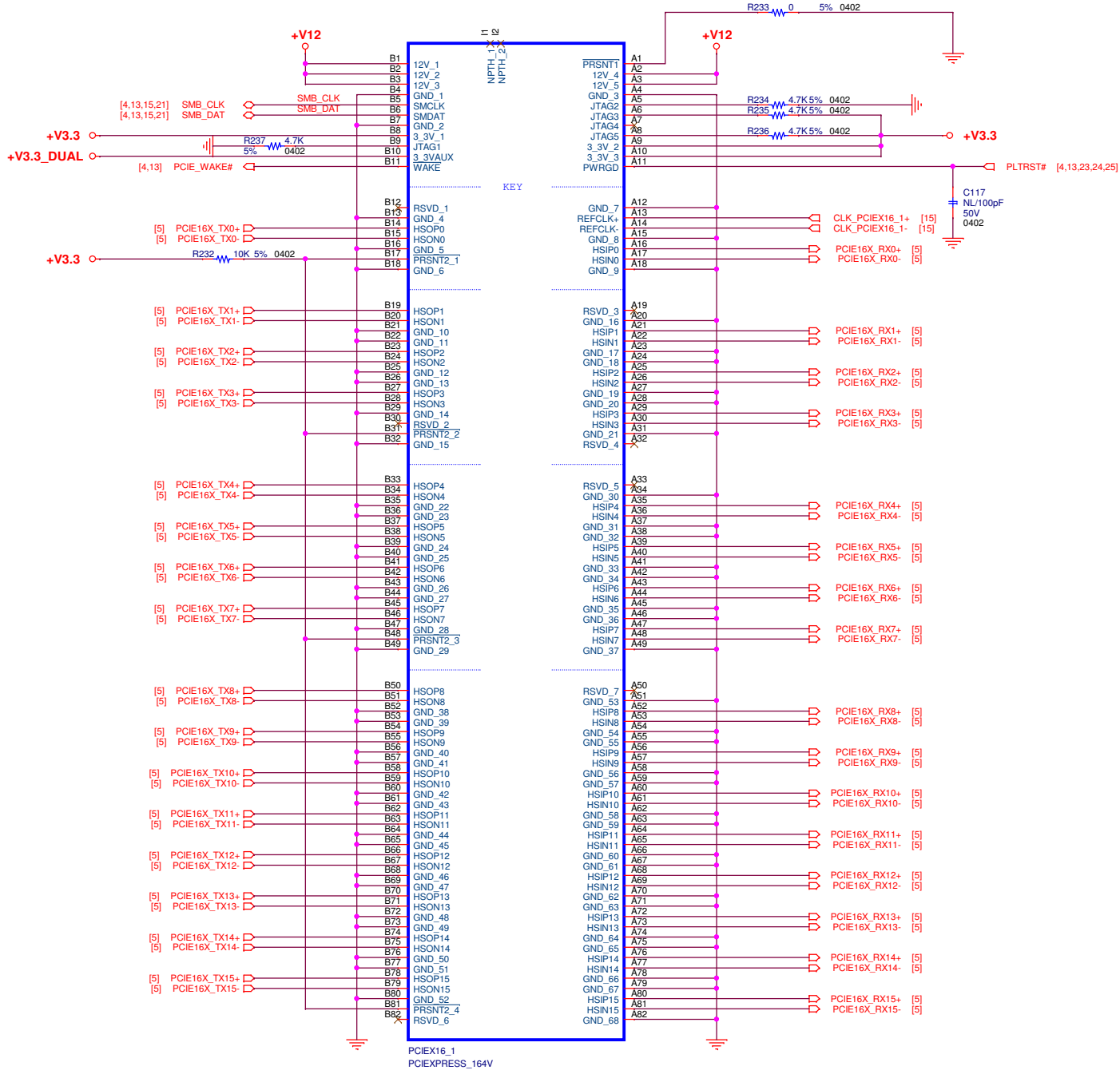
**PCIE4\_2\_187#**

**PCIE4\_2\_188#**

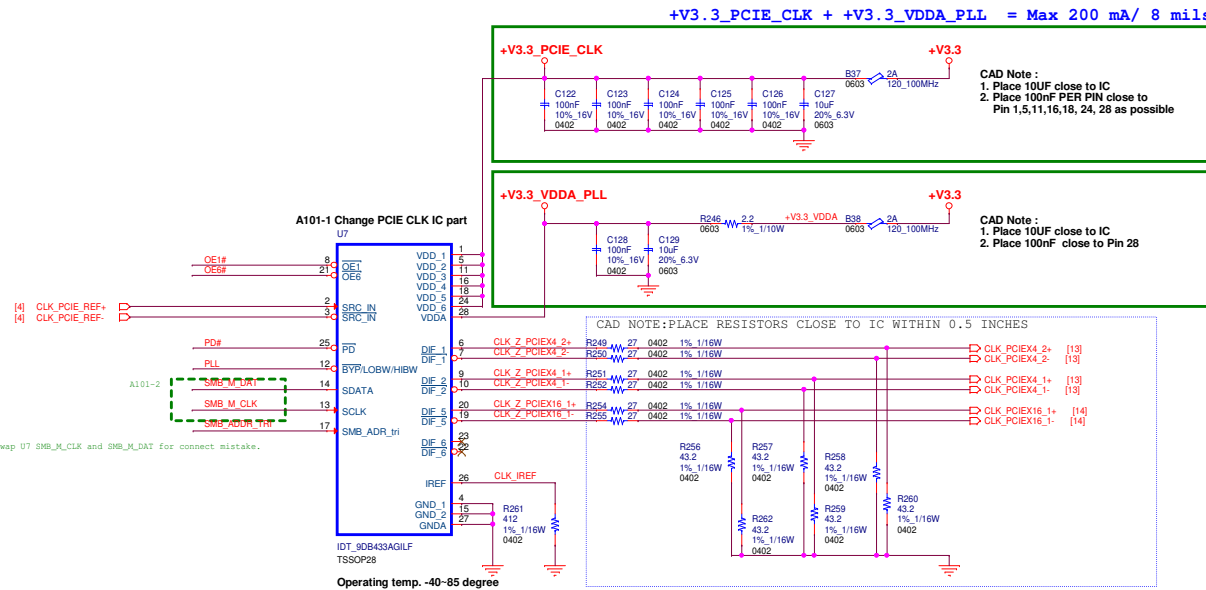
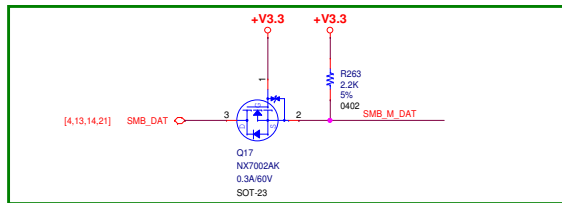
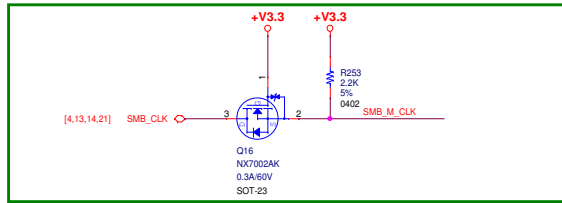
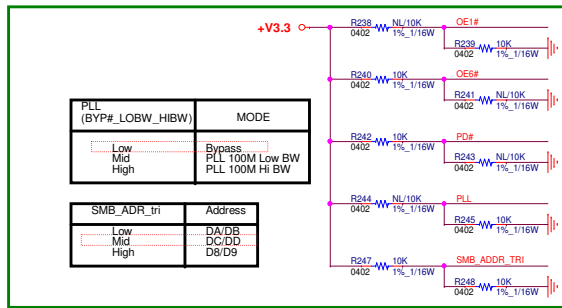
**PCIE4\_2\_**



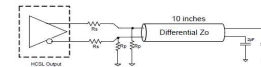
Parameter	PCIe Gen2	PCIe Gen3
Symbol Rate / PCIe Lane	5.0 G Symbols/s	8.0 G Symbols/s
Maximum signal line length (coupled traces) TX and RX	21.0 inches	14.0 inches
Signal length allowance on the COM Express Carrier Board to PCIe device	15.85 inches	10.0 inches
Signal length allowance on the COM Express Carrier Board to PCIe slot	9.00 inches	4.0 inches
PCI-SIG: Differential impedance recommendation	85 $\Omega$ +/-15%	85 $\Omega$ +/-15%
COMCDG Rev. 2.0: Differential impedance recommendation for new Carrier designs	85 $\Omega$ +/-15%	
Single-ended Impedance	50 $\Omega$ +/-15%	50 $\Omega$ +/-15%



## PCIe Clock Buffer



FAE suggestion for diff. impedance 85ohm.



DIF Zo (Ω)	Imp (Ω) (Rd (Ω))	Rd (Ω)
100	475	33
85	412	27

42.2 or 43.2

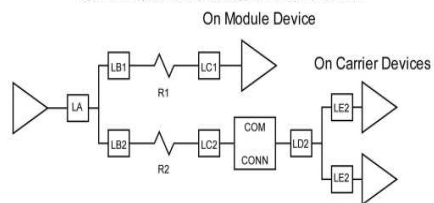
### 5.4.9 Carrier Board LPC Devices

Carrier Board LPC devices **should** be clocked with the LPC clock provided by the Module interface. If the Carrier Board has two loads on the LPC clock these loads **should** be connected to the common clock without a buffer. The Carrier Board **should** not have more than two loads on the LPC clock.

Carrier Board LPC devices **should** be reset with signal CB\_RESET#.

A typical routing topology for a Module LPC device and two Carrier Board LPC devices clock is shown below. This topology is used by Modules that start and stop the LPC clock on the fly. In this case, a buffer cannot be used and all LPC devices must share a common clock.

Figure 5-9: Typical Routing Topology for a Module LPC Device



LA 500 mils max  
LB1 = LB2 = 150 mils max  
LC1 = 8.88" + LC2  
LC2 = .25" max  
LE2 = 1" max  
LD2 + LE2 (note 2 instances of LE2) = 8.88"  
R1 = R2 = 22Ω

Figure 192. LPC\_CLK[0] or LPC\_CLK[1] Routing Topology—2 Branches Using One Clock as Output

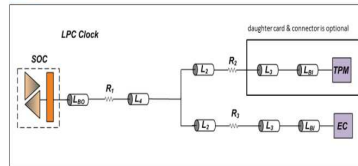
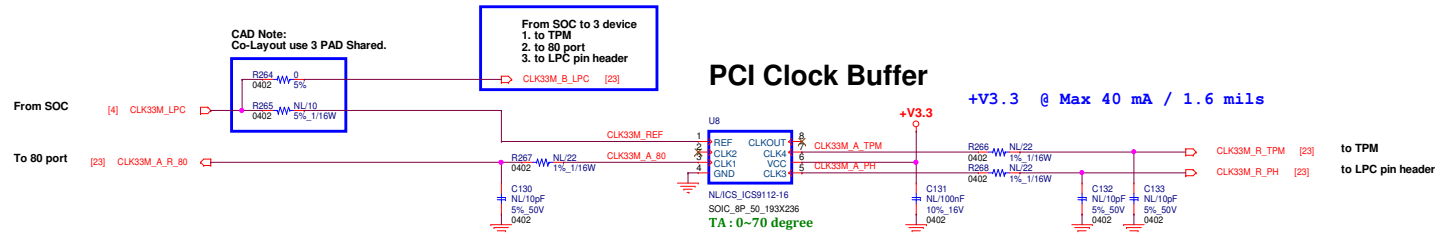


Table 132. LPC\_CLK[1:0] Signals Trace Routing—2 Branches (Sheet 1 of 2)

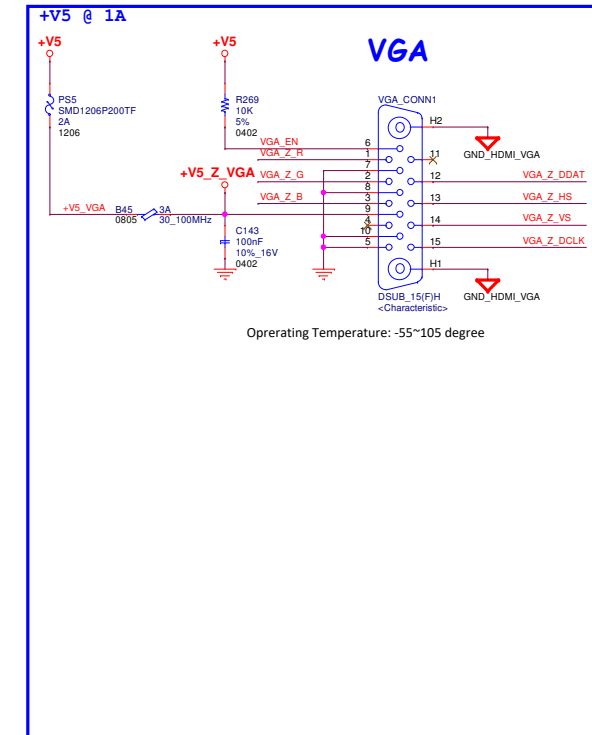
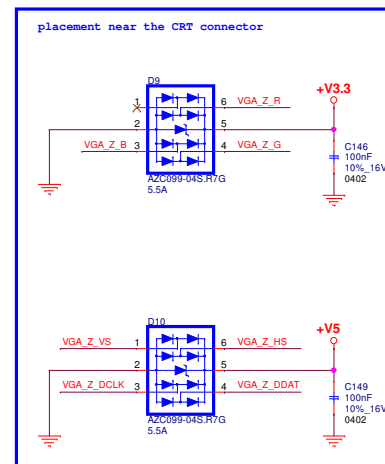
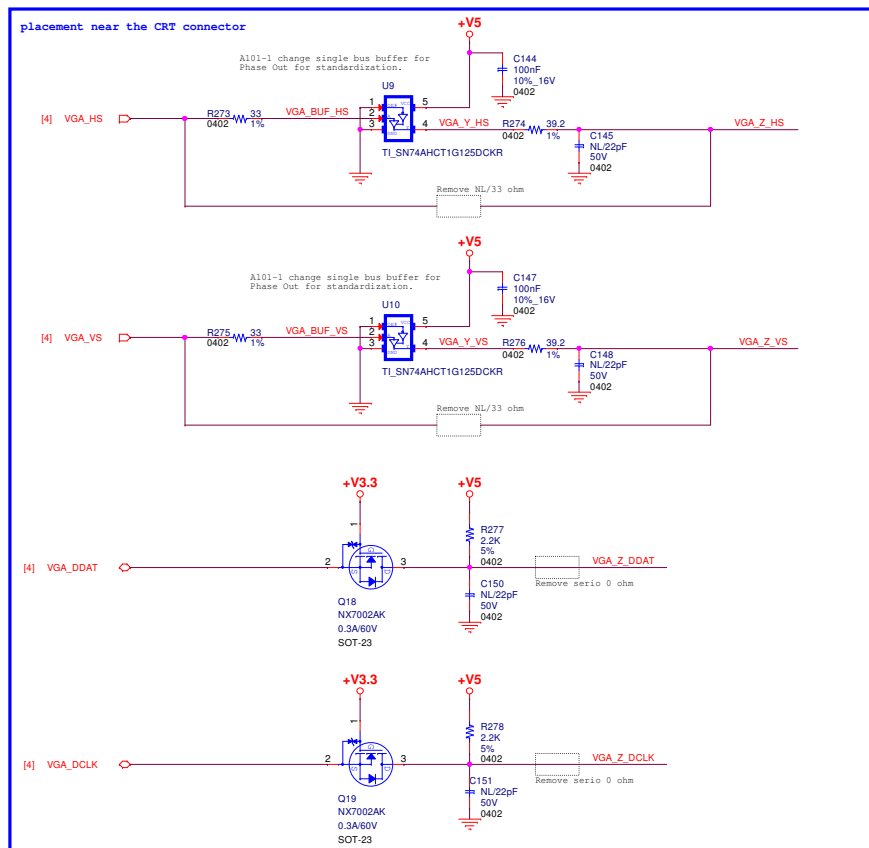
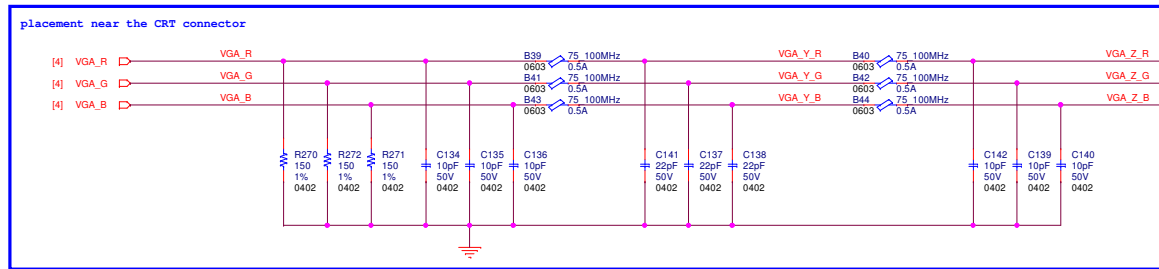
Parameter	Trace Width (mils)	Minimum Trace Spacing (mils)	Trace Length (mils)
Breakout L <sub>40</sub> and Breakin L <sub>41</sub>	3.50	3.50	0-500
L1 Main Route	4mils MS 4.5mils DSL	15	500-7500
L2 Main Route	4mils MS 4.5mils DSL	15	500-2000
L3 Main Route	4mils MS 4.5mils DSL	15	500-2500

## PCI Clock Buffer





# VGA



---



---



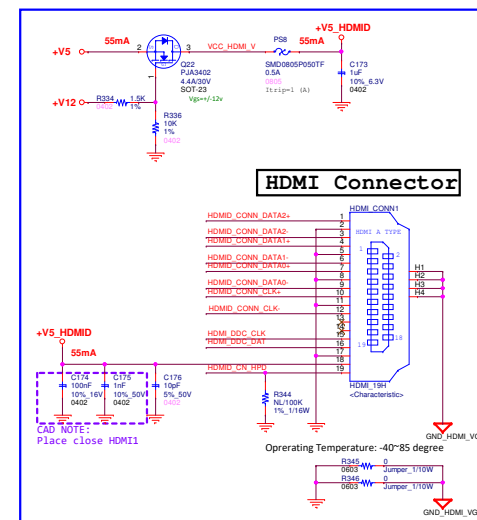
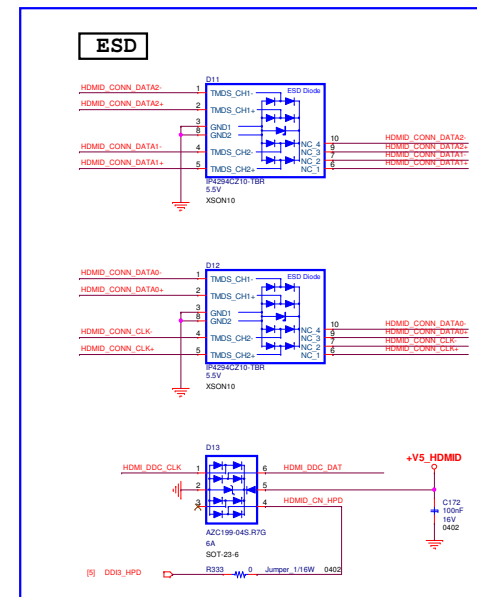
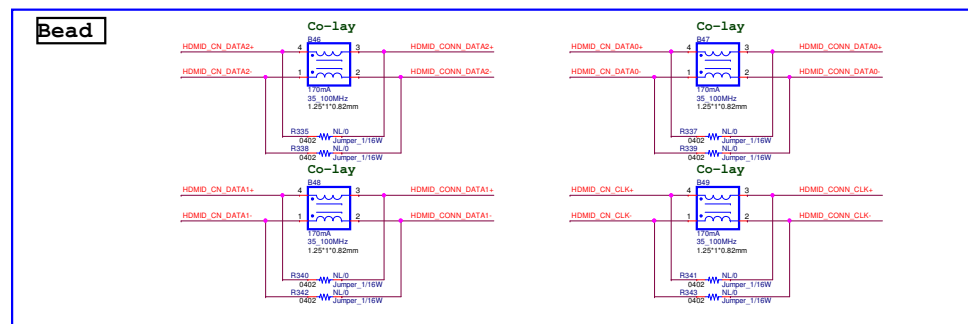
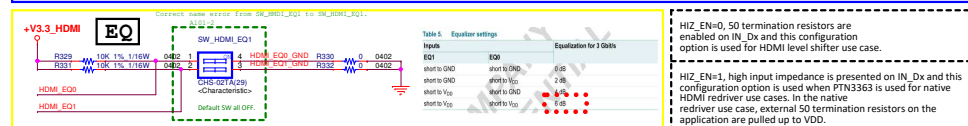
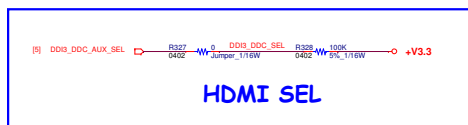
---

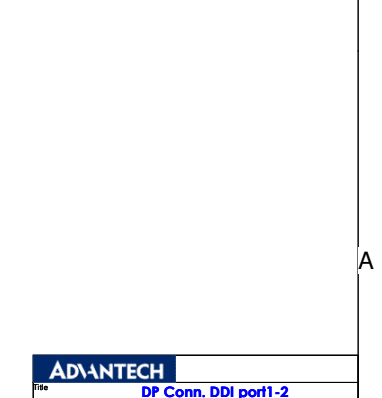
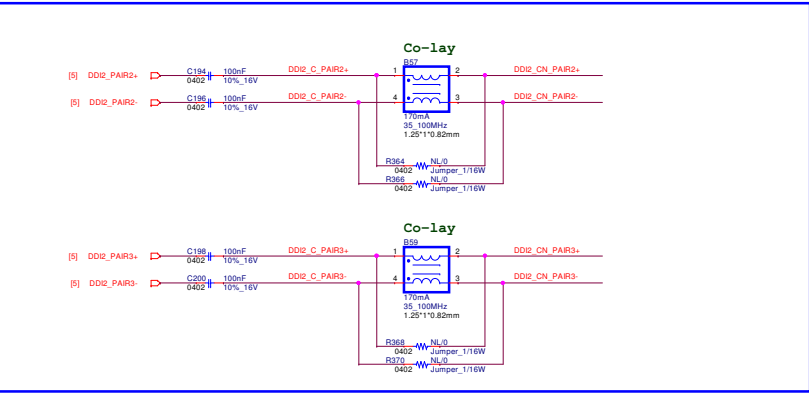
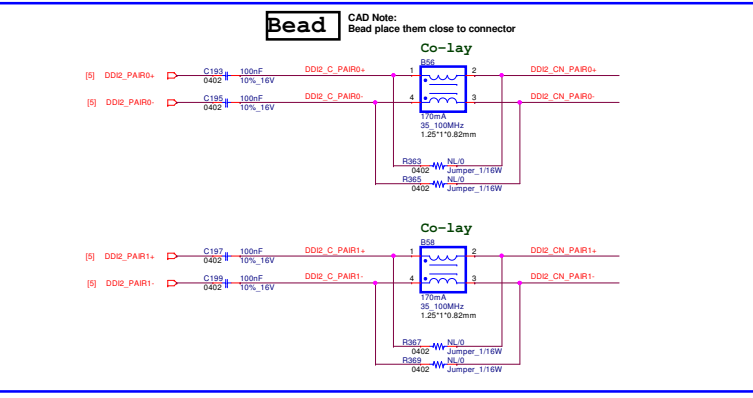
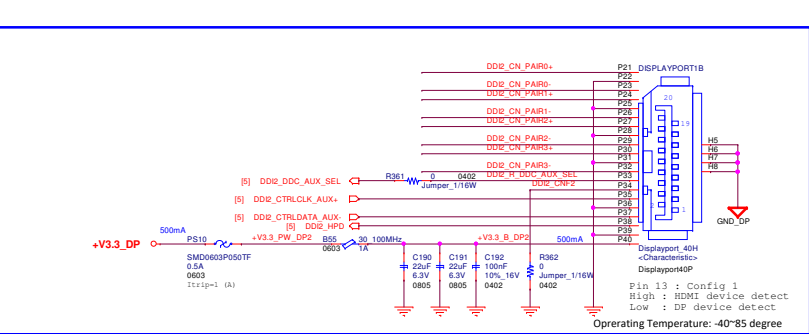
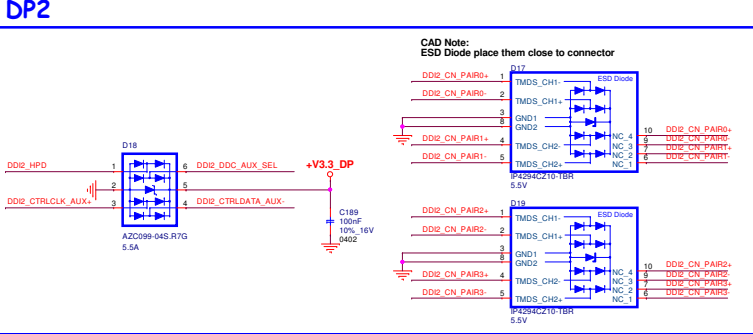
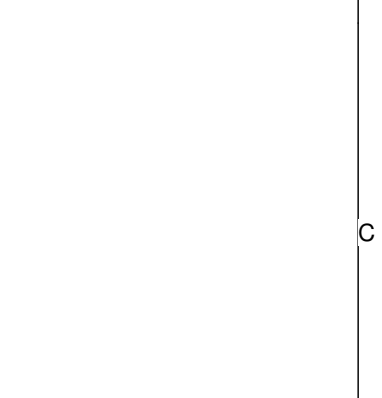
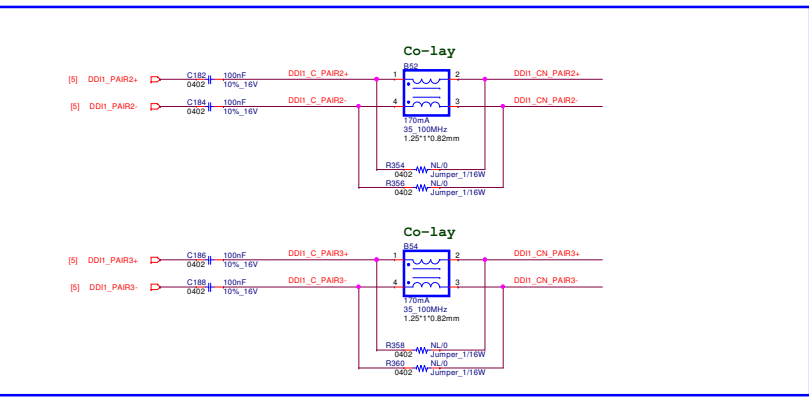
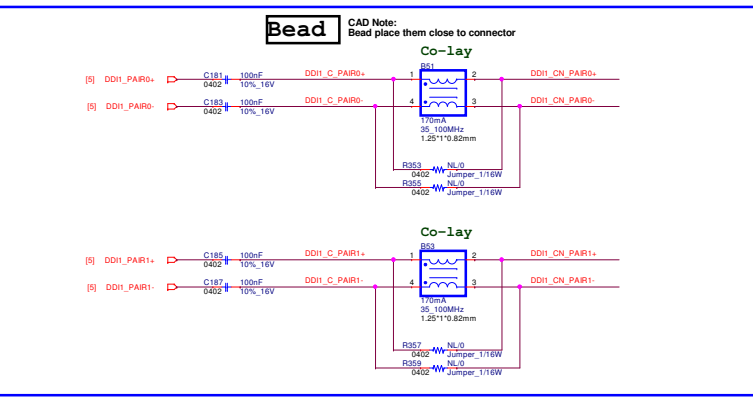
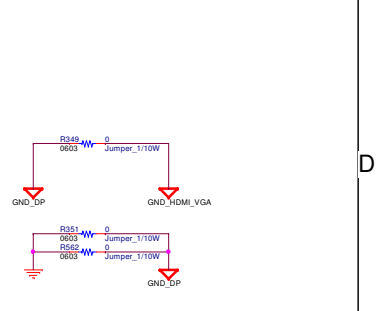
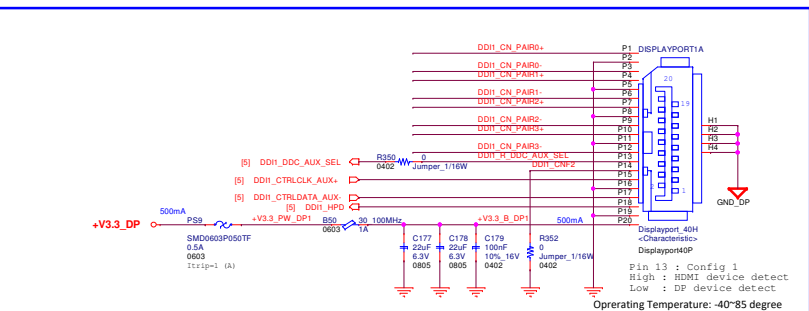
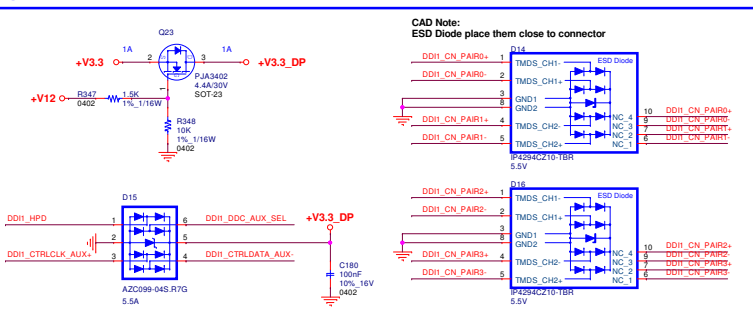


---

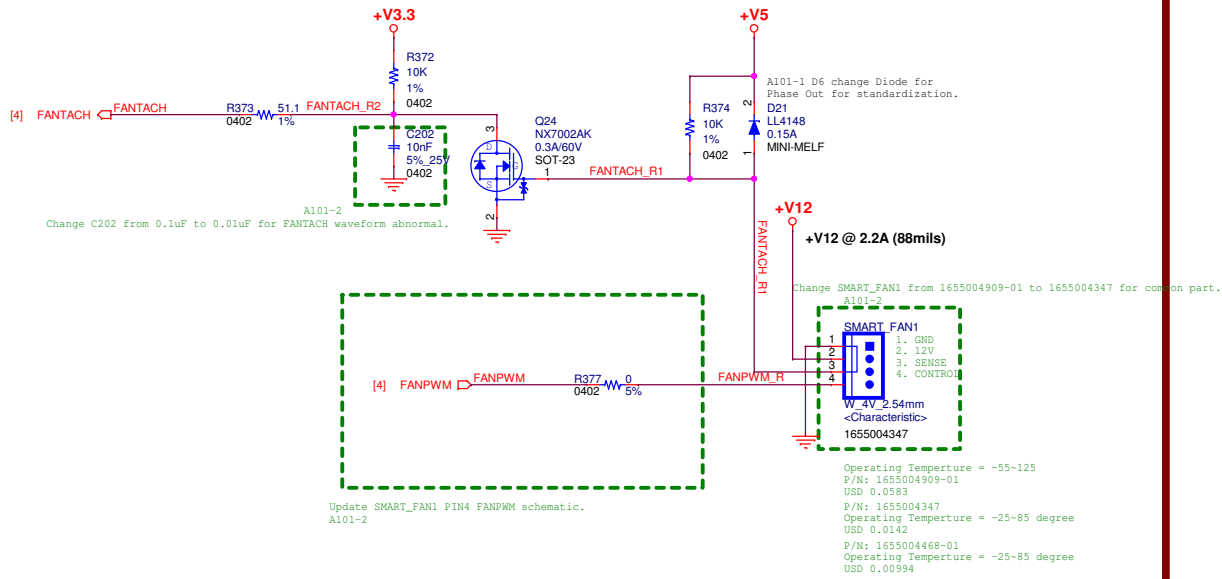


COM Express Pin Name	DDI0 Type 10	DDI1 Type 6	DDI2 Type 6	DDI3 Type 6	Function (DDIX) DisplayPort	Function (DDIX) HDMI / DVI
DDIX_PAIR0+	871	D26	D39	C39	<b>DPX_LANE0+</b>	TMDSX_DATA2+
DDIX_PAIR0-	872	D27	D40	C40	<b>DPX_LANE0-</b>	TMDSX_DATA2-
DDIX_PAIR1+	873	D29	D42	C42	<b>DPX_LANE1+</b>	TMDSX_DATA1+
DDIX_PAIR1-	874	D30	D43	C43	<b>DPX_LANE1-</b>	TMDSX_DATA1-
DDIX_PAIR2+	875	D32	D46	C46	<b>DPX_LANE2+</b>	TMDSX_DATA0+
DDIX_PAIR2-	876	D33	D47	C47	<b>DPX_LANE2-</b>	TMDSX_DATA0-
DDIX_PAIR3+	881	D36	D49	C49	<b>DPX_LANE3+</b>	TMDSX_CLK+
DDIX_PAIR3-	882	D37	D50	C50	<b>DPX_LANE3-</b>	TMDSX_CLK-
DDIX_HPD	889	C24	D44	C44	<b>DPX_HPD</b>	HDIMX_HPD
DDIX_CTRLCLK_AUX+	898	D15	C32	C36	<b>DPX_AUX+</b>	HDIMX_CTRLCLK
DDIX_CTRLDATA_AUX-	899	D16	C33	C37	<b>DPX_AUX-</b>	HDIMX_CTRLDATA
DDIC_DCC_AUX_SEL	895	D34	C34	C38		

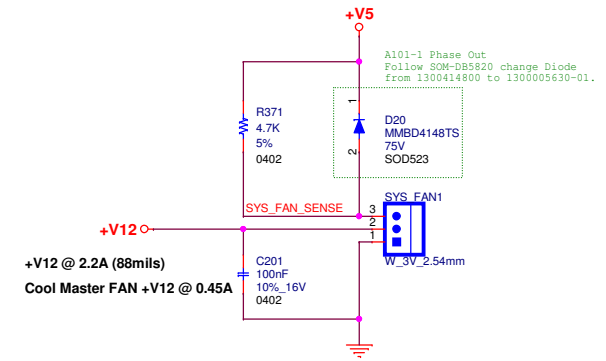




# SMART FAN



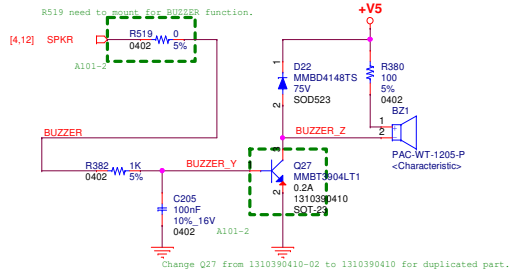
# SYSTEM FAN



ADVANTECH				A
Title		SYS FAN / SMART FAN		
Size	Document Number	SOM-DB5830	Rev	A1
Monday, October 22, 2018				
Date:	Sheet		20	of 34

## BUZZER

+V5 @ 50mA (2mils)



## GPIO CONN

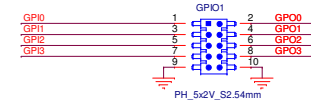
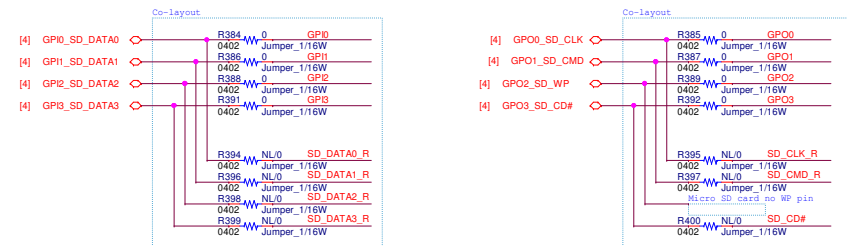


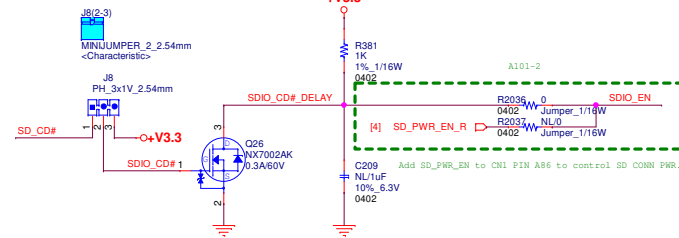
Table 4.30: SD Card Interface Signals

CDM Express Signal	SD card interface signals	Comments
GPIO	SD_DATA0	Bi-directional signal
GPIO1	SD_DATA1	Bi-directional signal
GPIO2	SD_DATA2	Bi-directional signal
GPIO3	SD_DATA3	Bi-directional signal
GPIO0	SD_CLK	Output from CDM Express, input to SD
GPIO1	SD_CMD	Output from CDM Express, input to SD
GPIO2	SD_WP	Input to CDM Express when used as SD_WP
GPIO3	SD_CDM	Input to CDM Express when used as SD_CDM

## GPIO / SD colay

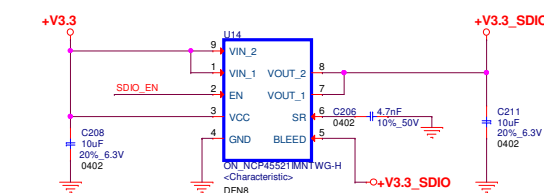


## SD PWR

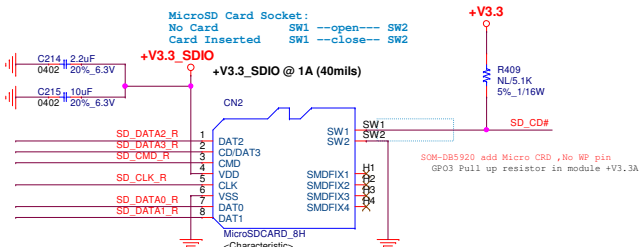


+V3.3

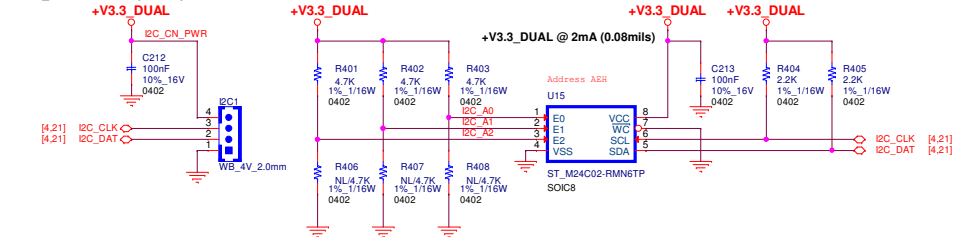
+V3.3\_SDIO @ 1A



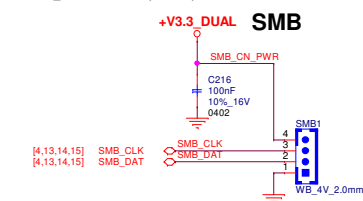
## Micro SD Card



+V3.3\_DUAL @ 80mA (3.2mils)



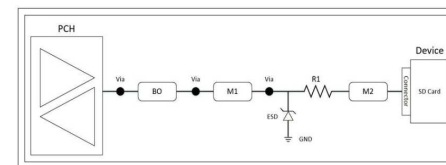
+V3.3\_DUAL @ 80mA (3.2mils)



## 6.3.6 CFL U/S/H SDXC Guidelines Change

Description: CFL-U, S and H PCH SDXC guidelines has changed.

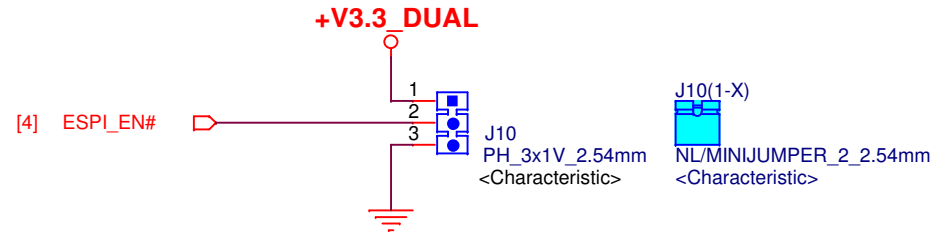
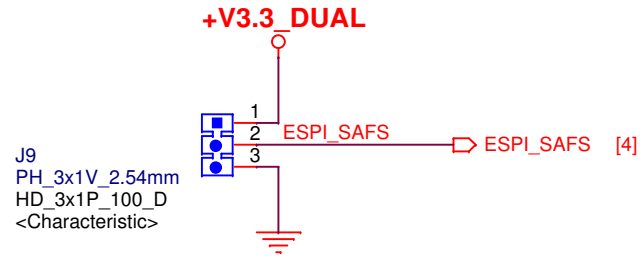
Resistor R1 (22 ohms) is added in the below topology diagram to be placed on SD\_DATA [3:0] and SD\_CMD within 12.7 mm away from the device.



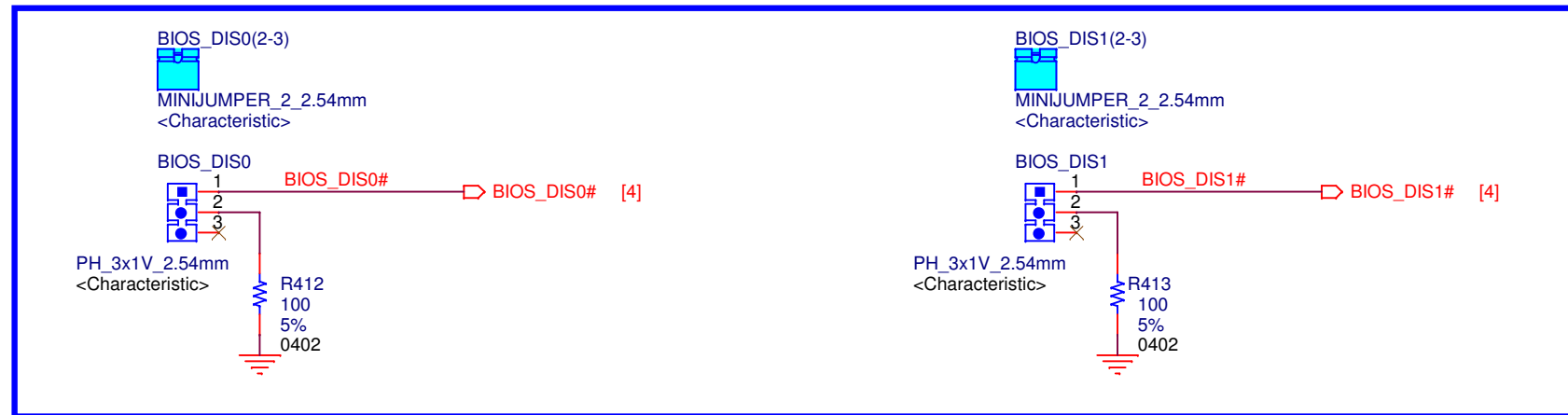
Following PDGs will be updated in the next release.

# ESPI selection / BIOS selection

For COM.0 R3, the Module Carrier based BIOS options have been expanded to support eSPI devices. A third pin that affects the BIOS location, named ESPI\_EN#, works in conjunction with BIOS\_DIS1# and BIOS\_DIS0# to define the BIOS boot path.



1. The Carrier shall leave the ESPI\_EN# unconnected on the Carrier for LPC operation.
2. The Carrier shall tie ESPI\_EN# to GND for eSPI operation.



ADVANTECH

Title BIOS / eSPI selection

Size Document Number SOM-DB5830

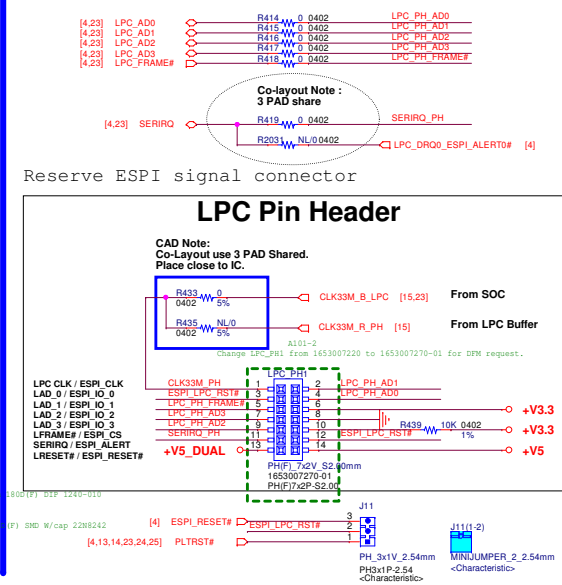
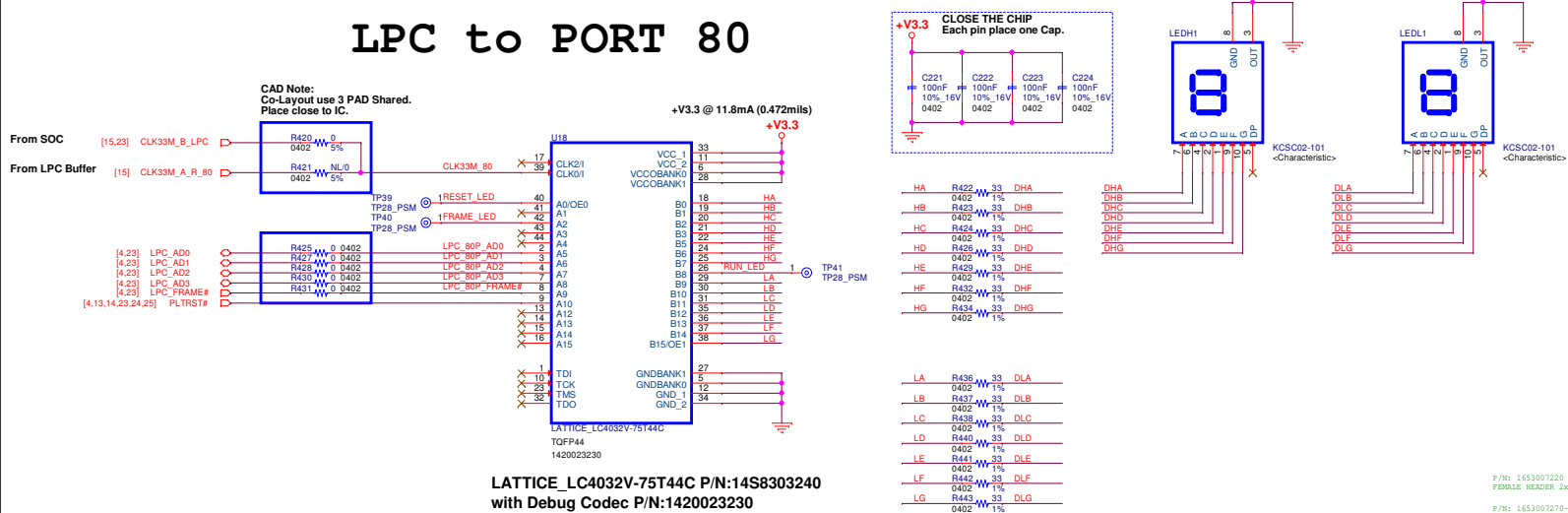
Date: Monday, October 22, 2018

Sheet 22 of 34

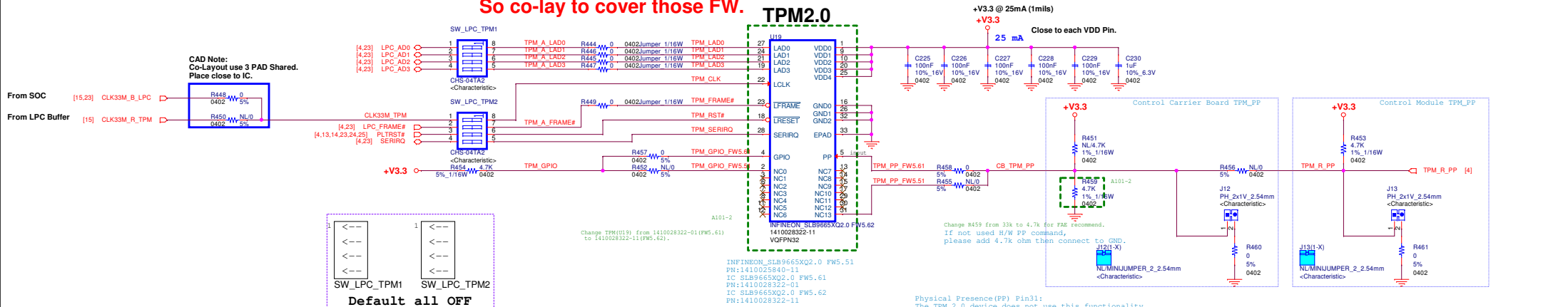
Rev  
A1



## LPC to PORT 80



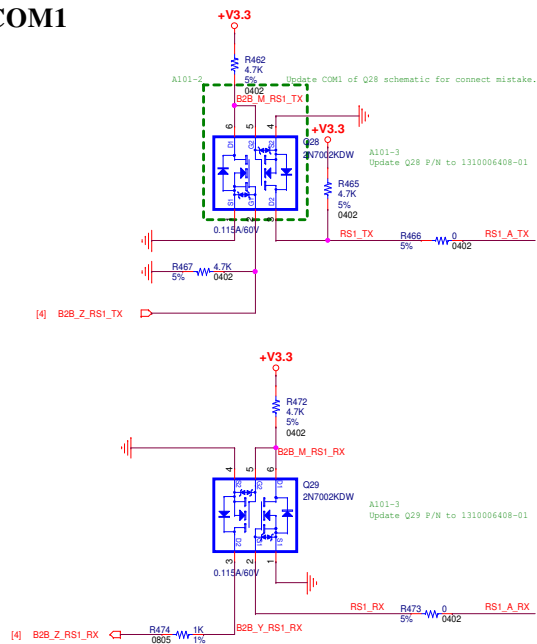
**It's a little bit different between TPM2.0 FW5.51 and FW 5.61.  
So co-lay to cover those FW.**



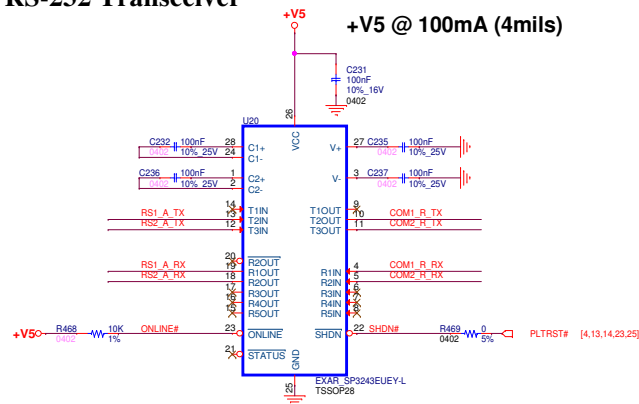
Physical Presence (PP) Pin31:  
The TPM 2.0 device does not use this functionality. For compatibility reasons (downgrade capability to a TPM 1.2), the pin should be connected to a jumper. The standard position of the jumper should connect the pin to GND. If the pin is connected to VDD, some special commands are enabled for a TPM 1.2.  
This pin does not have an internal pull-up or pull-down resistor and must not be left floating.

<b>ADVA-TECH</b>			
Title		<b>Port 80/ LPC PH / TPM</b>	
Size	Document Number		Rev
	<b>SOM-DB5830</b>		<b>A1</b>
Monday, October 22, 2018			
Date:	Sheet	23	of 34

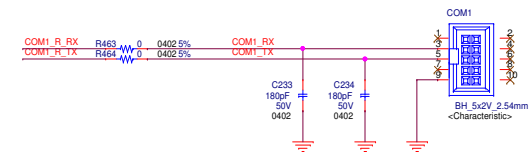
## COM1



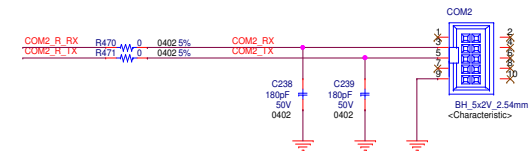
## RS-232 Transceiver



## COM1 BOX HEADER

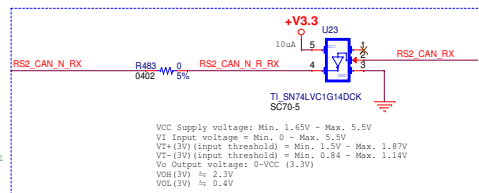
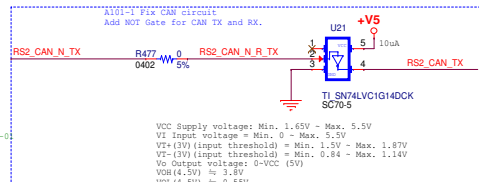
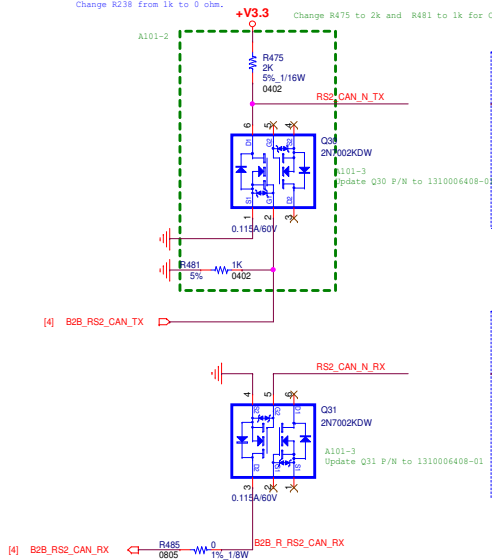


## COM2 BOX HEADER

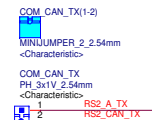


## COM2 (Default) / CAN (OPTIONAL)

A101-1 Fix CAN circuit  
Modify Q18 and Q22 circuit based on CCM Spec.  
Change R238 from 1k to 0 ohm.

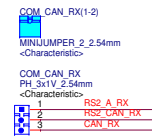


### COM/CAN selection



**COM2 TX (Default)**

**CAN TX (OPTIONAL)**

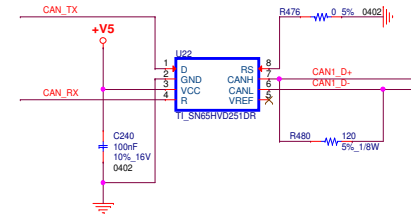


**COM2 RX (Default)**

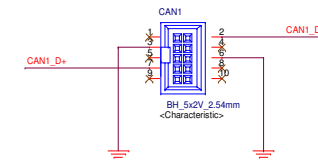
**CAN RX (OPTIONAL)**

## CAN Transceiver

**+V5 @ 65mA (2.6mils)**



## CAN BOX HEADER



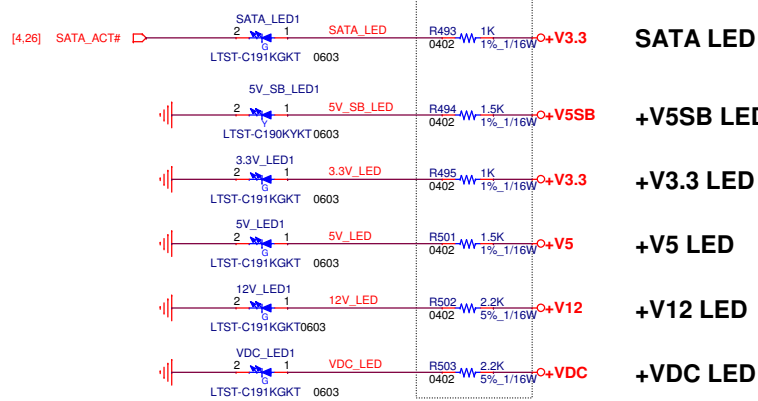
DE-9

### 9 Pin (male) D-Sub CAN Bus PinOut

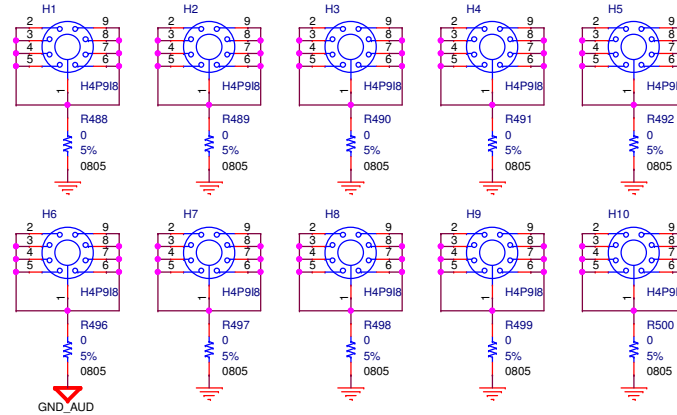
Pin #	Signal names	Signal Description
1	Reserved	Upgrade Path
2	CAN_L	Dominant Low
3	CAN_GND	Ground
4	Reserved	Upgrade Path
5	CAN_SHLD	Shield, Optional
6	GND	Ground, Optional
7	CAN_H	Dominant High
8	Reserved	Upgrade Path
9	CAN_V+	Power, Optional

## LED

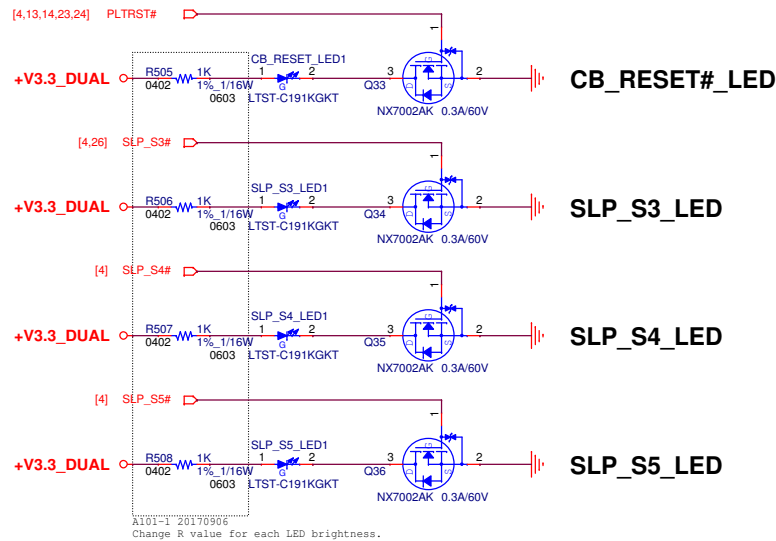
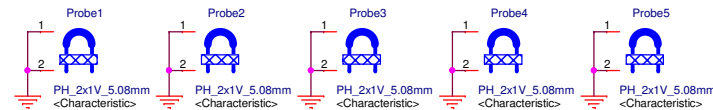
A101-1 20170906  
Change R value for each LED brightness.



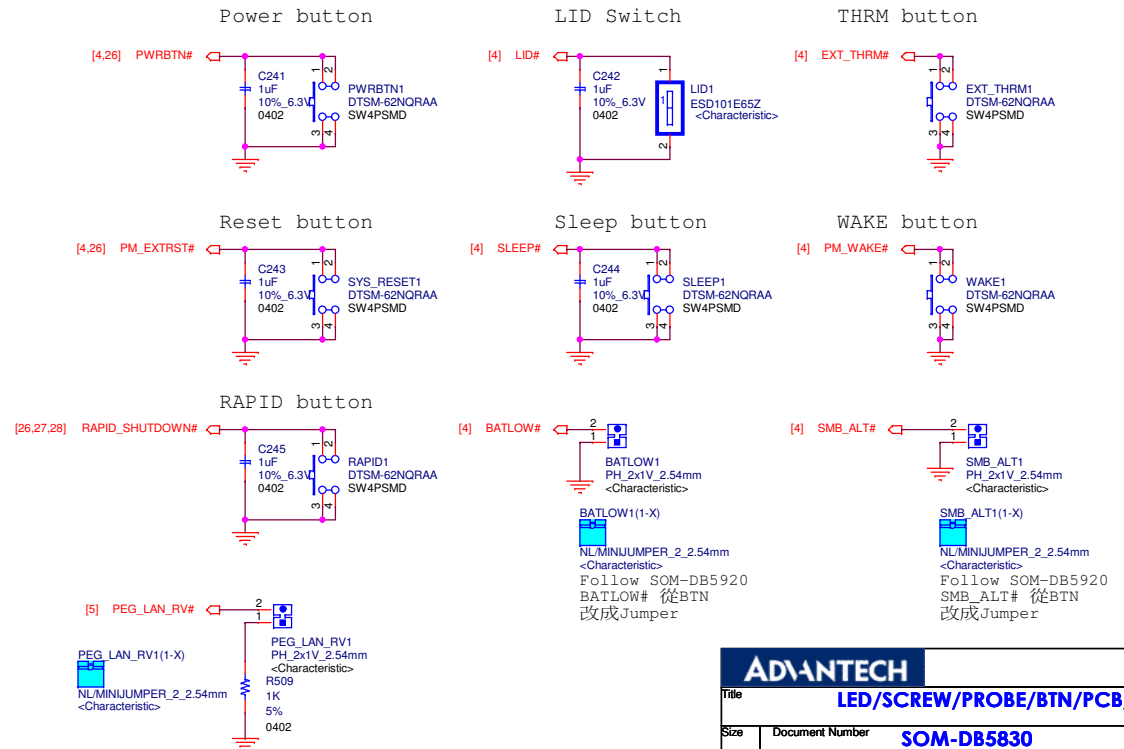
## SCREW HOLE



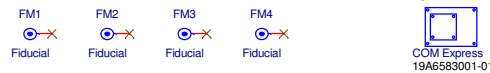
## PROBE



## Button / Pin Header / Switch



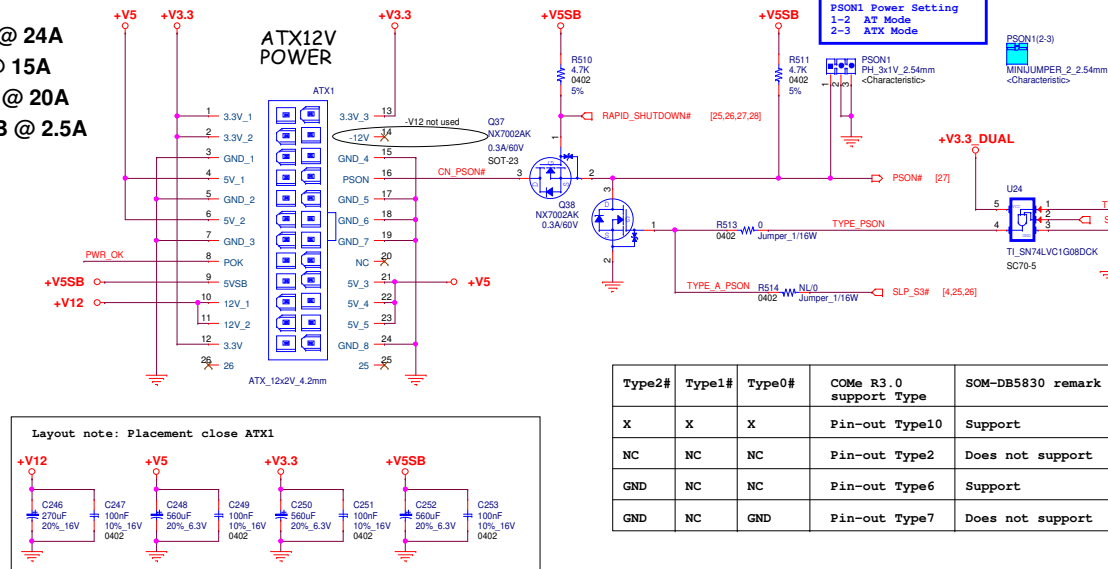
## FM/PCB



**ADVANTECH**

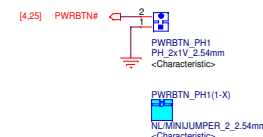
Title			
LED/SCREW/PROBE/BTN/PCB/FM			
Size	Document Number	Rev	
	SOM-DB5830	A1	
Date:	Monday, October 22, 2018	Sheet	25 of 34

**+V12 @ 24A**  
**+V5 @ 15A**  
**+V3.3 @ 20A**  
**+V5SB @ 2.5A**

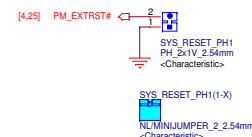


A101-1 20170906  
 Reserve those pin header after RD internal meeting.

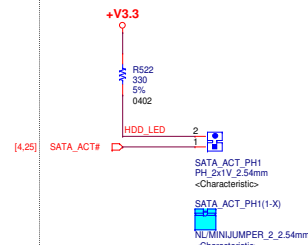
#### PWRBTN Pin Header



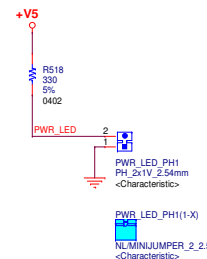
#### SYS RESET Pin Header



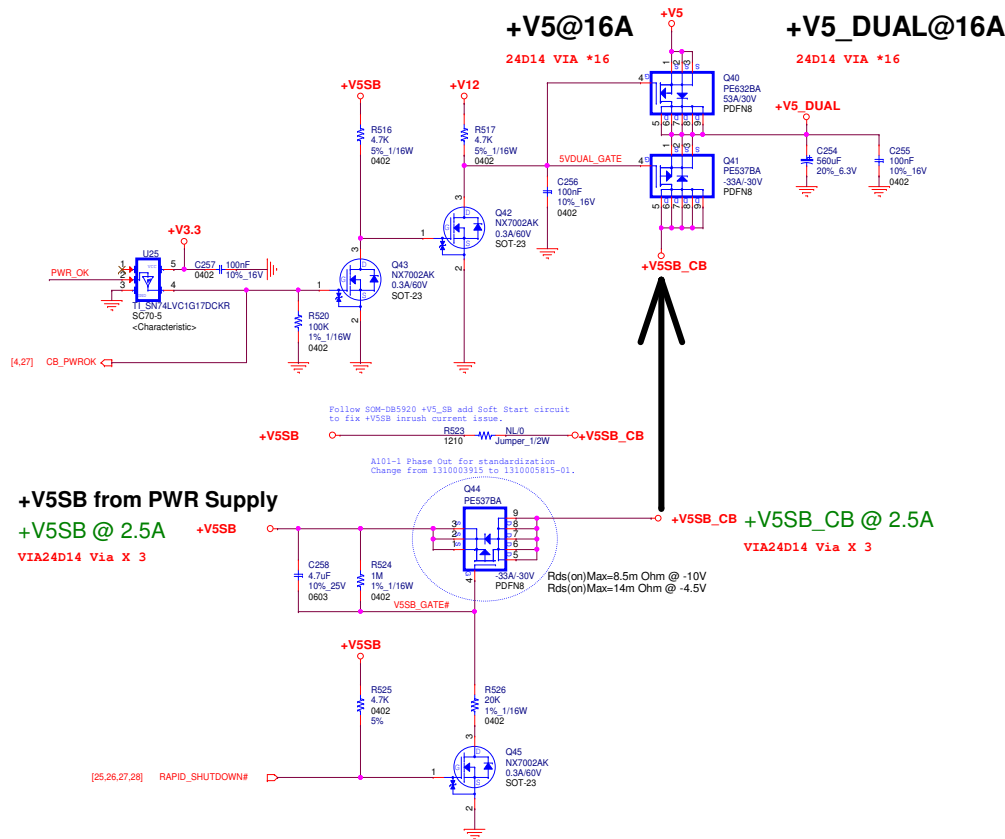
#### SATA ACT# Pin Header



#### Power LED Pin Header



文字面標註正極

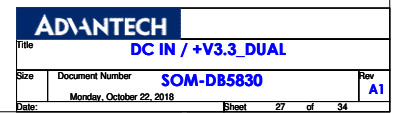


**ADVANTECH**

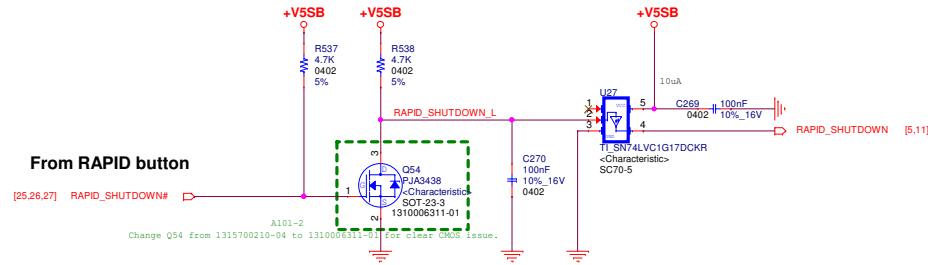
**ATX power / +V5\_DUAL**

Size Document Number **SOM-DB5830** Rev **A1**  
 Date Monday, October 22, 2018 Sheet 26 of 34

**+V3.3\_DUAL@ 1.6A**

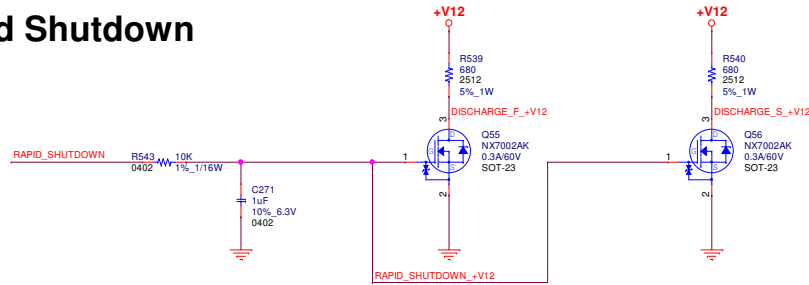


# Rapid Shutdown



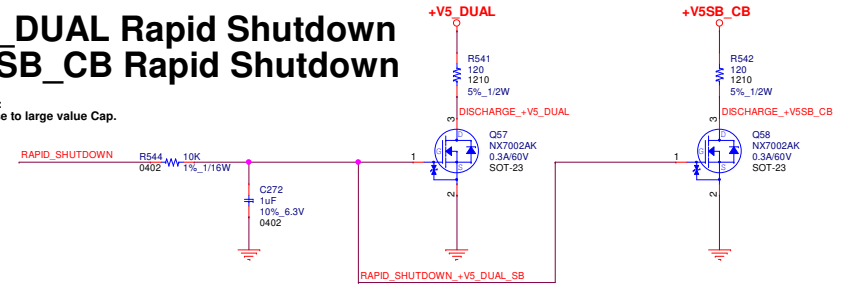
## +V12 Rapid Shutdown

CAD Note:  
Place close to large value Cap.



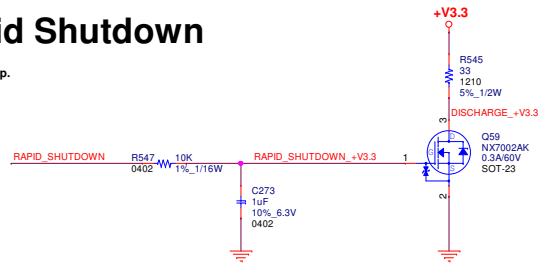
## +V5\_DUAL Rapid Shutdown +V5SB\_CB Rapid Shutdown

CAD Note:  
Place close to large value Cap.



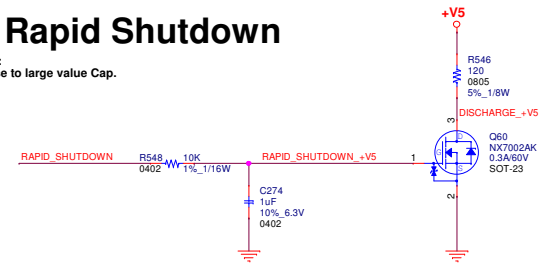
## +V3.3 Rapid Shutdown

CAD Note:  
Place close to large value Cap.



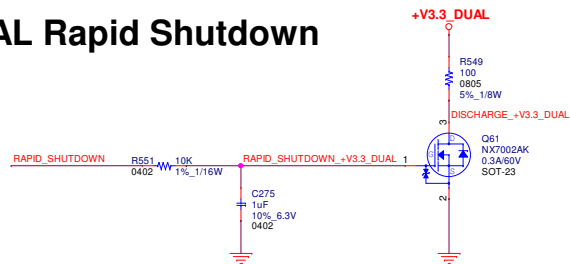
## +V5 Rapid Shutdown

CAD Note:  
Place close to large value Cap.



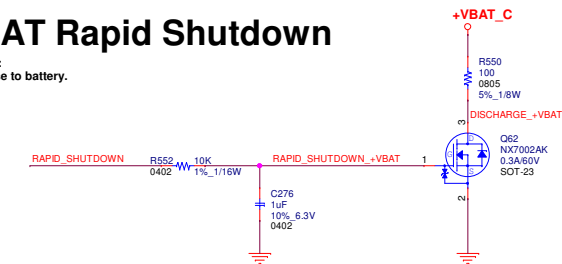
## +V3.3\_DUAL Rapid Shutdown

CAD Note:  
Place close to large value Cap.



## +VBAT Rapid Shutdown

CAD Note:  
Place close to battery.



ADVANTECH			
RAPID SHUTDOWN			
Size	Document Number	SOM-DB5830	Rev A1
Date	Monday, October 22, 2018	Sheet 28	of 34

SOM-DB5830 A1 01-2 PCB:19A6583001-01, 96 BOM:96965830000 Date: 2018/03/26

PG21: R519 need to mount for BUZZER function.

PG20: Change SMART\_FAN1 from 1655004909-01 to 1655004347 for common part.

PG27: Add C1142 & C1165 for +VIN low voltage power ripple.

PG17: Change component at PG17 for LVDS sequence.

PG18: Correct name error from SW\_HMDI\_EQ1 to SW\_HDMI\_EQ1.

PG04: change J1 from 1653006504-01 to 1653002200 for duplicated part.

PG20: Update SMART\_FAN1 PIN4 FANPWM schematic.

PG20: Change C202 from 0.1uF to 0.01uF for FANTACH waveform abnormal.

PG24: Update COM1 of Q28 schematic for connect mistake.

PG24: Change R475 to 2k and R481 to 1k for CAN\_TX waveform abnormal.

PG11: Change SATA1~SATA4 from 1654005955 to 1654013393-01 for DFM request.

PG11: Update schematic for two SPI BIOS ROM support.

PG11: Add J3(1-2) jumper for two SPI BIOS ROM support.

PG21: Add SD\_PWR\_EN to CN1 PIN A86 to control SD CONN PWR.

PG26: Add schematic for TYPE2# & TYPE0# select.

PG15: Swap U7 SMB\_M\_CLK and SMB\_M\_DAT for connect mistake.

PG17: Change R2033 from +V3.3 to +V5\_DUAL for +VLVDS\_PANEL\_PWR discharge.

PG17: Change R2034 from 1.2Kohm to 52.3ohm for +VLVDS\_PANEL\_PWR discharge.

PG23: Change TPM(U19) from 1410028322-01(FW5.61) to 1410028322-11(FW5.62).

PG23: Change R459 from 33k to 4.7k for FAE recommend.

PG23: Change LPC\_PH1 from 1653007220 to 1653007270-01 for DFM request.

PG17: Reserve cap at LVDS signals for SI and remove Common Mode Choke.

PG09: Change HW Strap setting of equalization and flat gain for USB3.1 GEN2 TX.

PG21: Change Q27 from 1310390410-02 to 1310390410 for duplicated part.

PGXX: Change 2N7002 from 1315700214 to 1315700214-01 for part shortage issue.

PG06: Reserve Common Mode Choke co-layout for USB3.1 RX Port 0/1 signal.

PG07: Reserve Common Mode Choke co-layout for USB3.1 RX Port 2/3 signal.

PG10: Change USB20 port 4~7 Common Mode Choke from 1212003587-01 to 1212001302.

PG06: Change USB20 port 0/1 Common Mode Choke from 1212003587-01 to 1212001302.

PG07: Change USB20 port 2/3 Common Mode Choke from 1212003587-01 to 1212001302.

PG10: Change USB20 CONN USB2.0\_1 from 1654012279-01 to 1654009643.

PG29: Change C84/C85/C88/C89 from X7R 4.7uF 10% 10V SMD 0805 to X5R 4.7uF 10% 25V SMD 0603 for capacitance shortage issue.

PG17: Unmount C155 for LVDS sequence.

PG28: Change Q54 from 1315700210-04 to 1310006311-01 for clear CMOS issue.