Kevin Palani

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Education

University of Illinois Urbana Champaign (UIUC) **May 2022**
Bachelor of Science in Computer Engineering *Senior*

Related Coursework:
Computer Architecture — OS — SOC — FPGAs — Robotics — Algorithms — Data Structures

Technical Skills

Programming Languages — SystemVerilog, Verilog, Python, C/C++, Java, php, Javascript, Go
Tools/Frameworks — Vivado, Quartus, AWS, Linux, Docker, SQL, git, LaTeX, Jira, Microsoft Office

Work Experience

Qualcomm **May 2021 - August 2021**
Software Engineering Intern
Created post-linker scripts which extracted information from an embedded image and replaced them with unique hashes. Original information could be recovered by talking to a connected debugging computer. Reduced image size by about 5MB by enhancing how hashes were used and performing assembly level improvements.

Quantum Corp **May 2019 - June 2020**
Software Engineering Intern
Worked on a set of services which allows support personnel to monitor and repair on-premise appliances from the cloud. Used transient Docker containers to facilitate secure connections between support personnel and product through the cloud, along with additions to the web UI and Postgres database to support the changes.

UIUC Staff **January 2020 - Present**
Course Assistant
Working as a course assistant for a FPGA class, where I lead office hours. I answer students questions related to SystemVerilog and digital design, ranging from understanding syntax to design trade-offs.

Nebbiolo Technologies **June - August 2018**
Software Engineering Intern
Extended the data analysis pipeline to allow for distributed analysis and computation, and upgraded the data visualizer to remotely view graphs. Also significantly reduced disk usage by optimizing Dockerfiles.

Projects

RISC-V Processor **October - December 2020**
Designed and implemented a pipelined processor in SystemVerilog that supported the RV32IM instruction set. Features includes pipelined set associative L1 caches, victim caches, stride based prefetching, local branch prediction, a branch target buffer, a return address stack, and a Wallace Tree multiplier.

Operating System from scratch **March - May 2020**
Led a team of 4 students to develop an operating system from the ground up in C. Included dynamic memory support, dynamic processes, a GUI with mouse support and multiple terminals, memory and cpu virtualisation, interrupt support, custom drivers, user programs, and multithreading.

3D Renderer in SystemVerilog on an FPGA **November - December 2019**
Designed and developed a GPU on a CycloneIV FPGA capable of arbitrary texured 3D rendering, and used it within an Avalon SOC along with the Intel NIOS II processor to build a game in which the user could move through and modify a 3D world. Developed with Quartus EDA tool and ModelSim simulator.