NYU Tandon School of Engineering

Fall 2022, ECE 6913 Section INET

Quiz 1

1. Hypersonic Computers, your employer, has just bought a new dual Core processor, and you have been tasked with optimizing your software for this processor - for two applications on this dual Core processor, but the resource requirements are not equal. The first one needs 80% of the resources, and the second only 20%.

(i) Assume that 40% of the first application is parallelizable, how much speedup would you achieve with that application if run in isolation? Assume that 99% of the second application is parallelizable, how much speedup would this application observe if run in isolation?

(iii) Given that 40% of the first application is parallelizable, how much overall system speedup would you observe if you parallelized it? Given that 99% of the second application is parallelizable, how much overall system speedup would you observe if you parallelized it?

2. Implement in RISC V these line of code in C:

(i) `f = g - A[B[C[27]]]`

(ii) `f = g - A[ C[10] + B[11] ]`

(iii) `A[i] = 4B[4i-44] + 3C[32i+32]`

3. Assume a 10-bit floating point representation format where the Exponent Field has 4 bits and the Fraction Field has 5 bits and the sign bit field uses 1 bit

S	**Exponent Field: 4 bits**	**Fraction Field: 5 bits**

a. What is the representation of **-8.80158×10^{-2}** in this Format (in Binary: **-0.00010110100010000011**)
[assume:
bias = 2^{N-1} - 1= 2^{4-1} -1= 7 (where N = number of exponent field bits) for normalized representation, and 1-bias = **-6 = bias for denormalized representation**].
What 10-bit pattern represents the number **−0.125 = −1/8?** What base-10 integer or fraction does this 10-bit floating point representation format of **0101001001** equal to?

b. What is the range of representation for *positive* *normalized* numbers – what is the largest and smallest *normalized* number represented in this format? What is the range of representation for *positive* *denormalized* numbers? – what is the largest and smallest *denormalized* number represented in this format?

4. A fast, energy efficient computer core minimizes (1) *the number of Instructions in the ISA*, (2) the *number of instructions in a Program* from that ISA and (3) *number of cycles per instruction* required to execute that Program. Compilers can actually minimize (2) by *using the least number of registers* leading us to minimize the likelihood of a 'spill' to memory if a program needs more registers than it has available.

Identify the best algorithm to swap 2 registers without using a third register and write a RISC-V program *for swapping the contents of two registers*, x5 and x6. You may not use any other registers.