

Data sheet acquired from Harris Semiconductor SCHS040D – Revised October 2003

CMOS

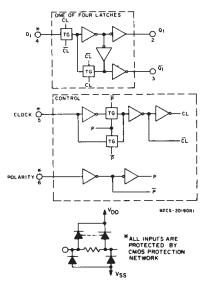
Quad Clocked "D" Latch

High-Voltage Types (20-Volt Rating)

■ CD4042B types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical.

Information present at the data input is transferred to outputs Q and Q during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

The CD4042B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead small-outline packages (D, DR, DT, DW, DWR, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).



CLOCK	POLARITY	Q
0	0	D
	0	LATCH
1	1	D
	1	LATCH

Fig. 1 - Logic block diagram and truth table.

CD4042B Types

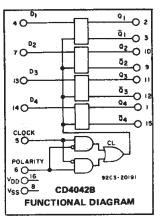
Features:

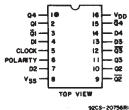
- Clock polarity control

 Q and Q outputs
- Common clock
- Low power TTL compatible
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin (over full package temperature range):
 - 1 V at VDD = 5 V
 - 2 V at V_{DD} = 10 V 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Buffer storage
- Holding register
- General digital logic





TERMINAL ASSIGNMENT

STATIC ELECTRICAL CHARACTERISTICS

CHARAC-								_ -			-
TERISTIC		OITION		LIMI	TS AT	NDICA	TED TE	MPERA	TURES (°C)	UNITS
	ν _ο (۷)	V _{IN} (V)	V _{DD} (V)	-55	40	+85	+125	Min.	Typ.	Max.	
	<u> </u>							141111.			
Quiescent		0,5	5	1	2	30	30 60	- '	0.02	2	
Device		0,10	10 15	4	4	60 120	120		0.02	4	μΑ
Current		0,15	20	20	20	600	600		0.02	20	
I _{DD} Max.		0,20	20	20	20	600	800		0.04	20	
Output Low			_ !								
(Sink)	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1		
Current,	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6		
IOL Min.	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8		mΑ
Output High	4.6	0,5	5	-0.64		-0.42	-0.36	-0.51	-1		
(Source)	2.5	0,5	5	–2	-1.8	-1.3	-1.15	-1.6	-3.2		
Current,	9.5	0,10	10	-1.6	-1.5	-1.1	0.9	-1.3	-2.6	_	
I _{OH} Min.	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	6.8	-	
Output Volt-											
age:	_	0,5	5		0.0)5		_	. 0	0.05	
Low-Level,	-	0,10	10		0.0)5		_	0	0.05	
VOL Max.	_	0,15	15		0.0)5		-	0	0.05	v
Output Volt-		l									ľ
age:	_	0,5	5		4.9	95		4.95	- 5	_	
High-Level,		0,10	10	* 1	9.9	95		9.95	10	_	ŀ
VOH Min.	_	0,15	15		14.	95		14.95	15	- 1	1
Input Low	0.5,4.5	_	5		1.	5		-	_	1.5	
Voltage,	1,9	_	10		.3	3			_	3	
VIL Max.	1.5,13.5		15		4			-	-	4	l v
Input High	0.5,4.5	_	5		3.5			3.5	_		\ \ \
Voltage,	1,9	_	10	7				7			
V _{IH} Min.	1.5,13.5	_	15	11				11	-	-	
Input Current, I _{IN} Max.	_	0,18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μΑ

CD4042B Types

MAXIMUM RATINGS, Absolute-Maximum Values:	
DC SUPPLY-VOLTAGE RANGE, (VDD)	
Voltages referenced to VSS Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	0.5V to Vnn +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (PD):	
For T _A = -55°C to +100°C	500mW
For T _A = +100°C to +125°C	Derate Linearity at 12mW/OC to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	,
FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package	Types)100mW
FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package OPERATING-TEMPERATURE RANGE (TA)	Types)
OPERATING-TEMPERATURE RANGE (TA)	55°C to +125°C
FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package OPERATING-TEMPERATURE RANGE (T _A)	55°C to +125°C

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^{\circ}$ C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V _{DD}	LIN	LIMITS			
	(V)	Min.	Max.	1		
Supply-Voltage Range (For TA=Full Package Temperature Range)	_	3	18	v		
	5	200	_			
Clock Pulse Width, tw	10	100	-	ns		
	15	60	-			
	5	50	-			
Setup Time, t _S	10	30	-	ns		
	15	25		1		
	5	120				
Hold Time, tH	10	60	-	ns		
	15	50	_]]		
Clock Rise or Fall Time: t _r , t _f	5,10 15	Not ris	μS			

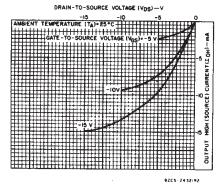


Fig. 5 — Minimum output high (source) current characteristics.

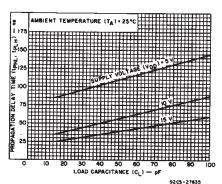


Fig. 6 - Typical propagation delay time vs. load capacitance—data to Q.

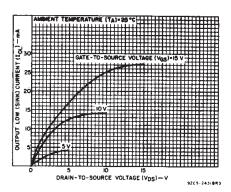


Fig. 2 – Typical output low (sink) current characteristics.

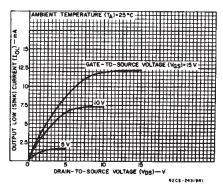


Fig. 3 — Minimum output low (sink) current characteristics.

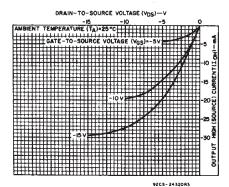


Fig. 4 — Typical output high (source) current characteristics.

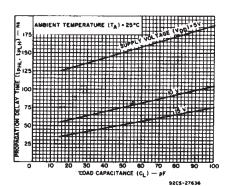


Fig. 7 — Typical propagation delay time vs. load capacitance—data to $\overline{\Omega}$.

CD4042B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r , t_f = 20 ns, C_L = 50 pF, R_L = 200 K Ω

CHARACTERISTIC	V _{DD}	LIM	IITS	UNITS				
	(0)	Тур.	Max.	1				
Propagation Delay	5	110	220					
Time: tpHL , tpLH	10	55	110	ns				
Data In to Q	15	40	80	l .				
	5	150	300					
Data In to Q	10	75	150	ns				
	15	50	100					
	5	225	450					
Clock to Q	10	100	200	ns				
	15	80	160					
	5	250	500	1				
Clock to Q	10	115	230	ns				
	15	90	180					
Transition	5	100	200					
Time: tTHL, tTLH	10	50	100	ns				
· ····································	15	40	80	l				
Minimum Clock	5	100	200					
Pulse Width, tw	10	50	100	ns				
	15	30	60					
	5	60	120					
Minimum Hold Time, tH	10	30	60	ns				
	15	25	50					
Minimum Setup	5	0	50					
Time, ts	10	0	30	ns				
rine, ts	15	0	25					
Clock Input Rise or Fall	5,10	Not rise	or fall					
Time: t _r , t _f	15	time se	nsitive.	μS				
Input Capacitance, CIN		5	7.5	ρF				
Polarity Input		Ŭ	7.5	۳,				
All Other Inputs	-	7.5	15	pF				

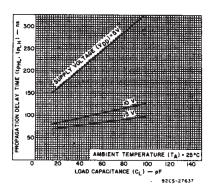


Fig. 8 - Typical propagation delay time vs. load capacitance-clock to Q

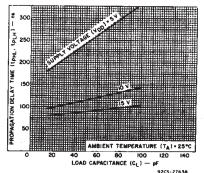
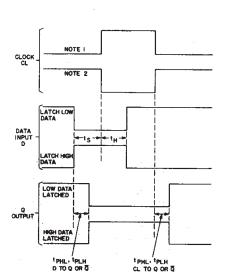


Fig. 9 — Typical propagation delay time vs. load capacitance—clock to $\overline{\mathbf{Q}}$.



NOTES: 1. FOR POSITIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS LOW.

2. FOR NEGATIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS NIGH.

92cs-27630 Fig. 12 - Dynamic test parameters.

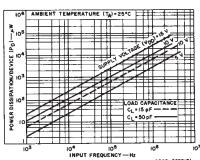


Fig. 10 – Typical power dissipation vs. frequency.

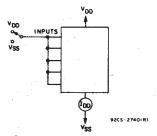


Fig. 13 - Quiescent device current test circuit.

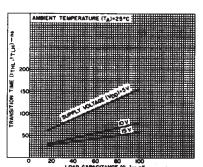


Fig. 11 — Typical transition time vs. load capacitance.

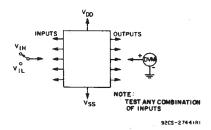


Fig. 14 - Input voltage test circuit.

CD4042B Types

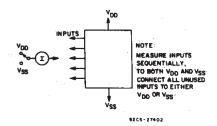
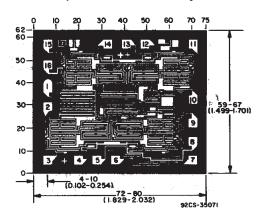


Fig. 15 - Input current test circuit.

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch) .



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4042BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4042BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4042BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4042BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4042BF3AS2329	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
CD4042BF3AS2534	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
CD4042BM	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
CD4042BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.



PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2009

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4042BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4042BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 29-Jul-2009



*All dimensions are nominal

1	Device	Package Type	Package Drawing Pins SPQ		Length (mm)	Width (mm)	Height (mm)	
CD	4042BDR	SOIC	D	16	2500	333.2	345.9	28.6
CD4	1042BNSR	SO	NS	16	2000	346.0	346.0	33.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

D (R-PDS0-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.



D(R-PDSO-G16)



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
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CD4042BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4042BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4042BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4042BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4042BF3AS2329	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
CD4042BF3AS2534	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
CD4042BM	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
CD4042BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BNSRE4	ACTIVE	so	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4042BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs. **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.



PACKAGE OPTION ADDENDUM

www.ti.com 3-May-2010

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

www.ti.com 29-Jul-2009

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4042BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4042BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 29-Jul-2009



*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD	4042BDR	SOIC	D	16	2500	333.2	345.9	28.6
CD4	1042BNSR	SO	NS	16	2000	346.0	346.0	33.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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