ETM10E-02

EPSON TOYOCOM

Application Manual

Real Time Clock Module

RX-8025SA/NB

Model	Product Number
RX-8025SA	Q41802551xxxx00
RX-8025NB	Q41802591xxxx00

EPSON TOYOCOM CORPORATION

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Contents

I²C-Bus Interface Real-time Clock Module

RX - 8025 SA / NB

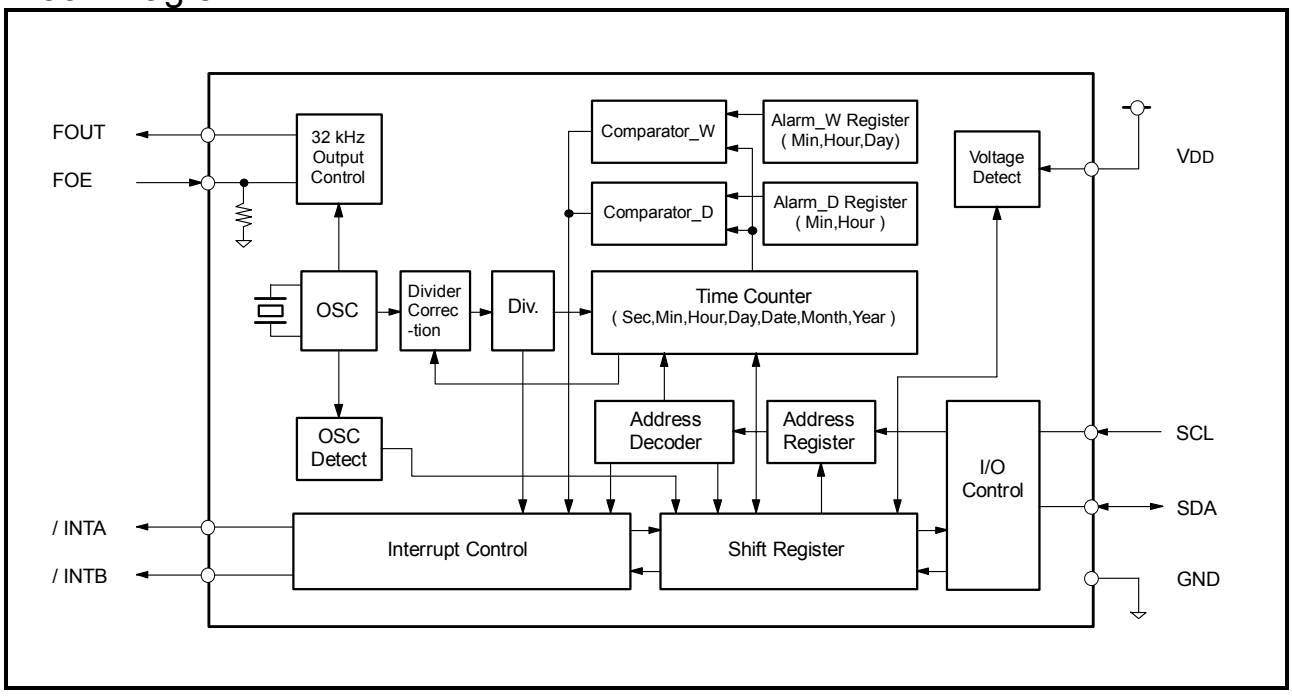
- Features built-in 32.768-kHz quartz oscillator, frequency adjusted for high precision ($\pm 5 \times 10^{-6}$ when Ta = +25°C)
- Supports I²C-Bus's high speed mode (400 kHz)
- Includes time (H/M/S) and calendar (YR/MO/DATE/DAY) counter functions (BCD code)
- Select between 12-hr and 24-hr clock mode.
- Auto calculation of leap years until 2099
- Built-in high-precision clock precision control logic
- CPU interrupt generation function (cycle time range: 1 month to 0.5 seconds, includes interrupt flags and interrupt stop function)
- Dual alarm functions (Alarm_W: Day/Hour/Min, Alarm_D: Hour/Min)
- 32.768-kHz clock output (CMOS output with control pin)
- Oscillation stop detection function (used to determine presence of internal data)
- Power supply voltage monitoring function (with selectable detection threshold)
- Wide clock (retention) voltage range: 1.15 V to 5.5 V
- Wide interface voltage range: 1.7 V to 5.5 V
- Low current consumption: 0.48 μA/3.0 V (Typ.)

1. Overview

This module is an I²C bus interface-compliant real-time clock which includes a 32.768-kHz quartz oscillator that has been adjusted for high precision. In addition to providing a function for generating six types of interrupts, a dual alarm function, an oscillation stop detection function (used to determine presence of valid internal data at power-on), and a power supply voltage monitoring function, this module includes a digital clock precision adjustment function that can be used to set various levels of precision.
Since the internal oscillation circuit is driven at a constant voltage, 32.768-kHz clock output is stable and free of voltage fluctuation effects.

This implementation of multiple functions in one SMT package is ideal for applications ranging from cellular phones to PDAs and other small electronic devices.

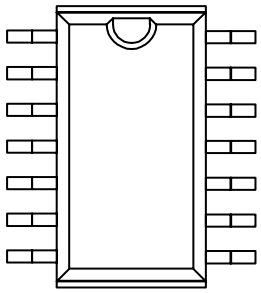
2. Block Diagram



3. Description of Pins

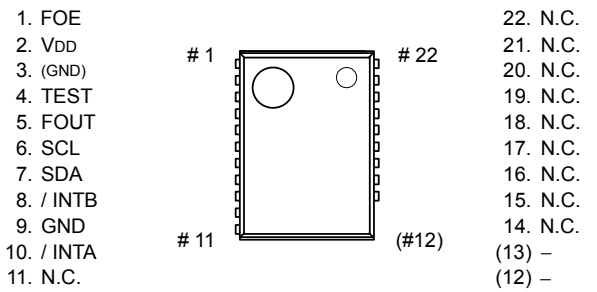
3.1. Pin Layout

RX - 8025 SA



SOP - 14pin

RX - 8025 NB



SON - 22pin

3.2. Pin Functions

Signal name	I / O	Function
SCL	I	This is the serial clock input pin for I^2C communications. Data input and output across the SDA pin is synchronized with this pin's clock signal. Up to 5.5 V can be used for this input, regardless of the power supply voltage.
SDA	I/O	This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for I^2C communications. The SDA pin is an N-ch open drain pin during output. Be sure to connect a suitable pull-up resistance relative to the signal line capacity.
FOUT	O	FOUT terminal is 32.768 kHz clock output terminal (C-MOS) that output control is possible. FOE terminal is the input terminal controlling the output of FOUT pin with /CLEN1 and /CLEN2 bit. The output of FOUT terminal stops when /CLEN1bit and /CLEN2 bit both sets to "1". FOUT output stops when FOE is Low or OPEN. Status of FOUT output stopped is " L ". ∗The logic table.
FOE	I	FOE terminal had pull-down resistor built-in and input voltage is possible regardless of power supply voltage to 5.5 V.
/INTA	O	This interrupt output A pin is an N-ch open drain output. It outputs alarm interrupts (Alarm_D) and periodic interrupts.
/INTB	O	This interrupt output B pin is an N-ch open drain output. It outputs alarm interrupts (Alarm_W).
TEST	–	This pin is used by the manufacturer for testing. Do not connect externally.
VDD	–	This pin is connected to a positive power supply.
GND	–	This pin is connected to a ground.
(GND)	–	This pin has the same voltage level as GND. Do not connect externally.
N.C.	–	This pin is not connected to the internal IC. However, note with caution that the RX-8025NB's N.C. pins (pins 14 to 22) are interconnected via the internal frame. Leave N.C. pins open or connect them to GND or VDD.

FOE input	/CLEN1 bit	/CLEN2 bit	FOUT output
L	X	X	OFF (" L ")
H	0	0	32.768 kHz
	0	1	32.768 kHz
	1	0	32.768 kHz
	1	1	OFF (" L ")

' X ' Don't care.

Note: Be sure to connect a bypass capacitor rated at least 0.1 µF between VDD and GND.

4. Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Between V_{DD} and GND	−0.3 to +6.5	V
Input voltage	V_I	SCL, SDA, FOE pins	GND−0.3 to +6.5	V
Output voltage	V_{O1}	SDA, /INTA, /INTB pins	GND−0.3 to +6.5	V
	V_{O2}	FOUT pin	GND−0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	When stored separately, without packaging	−55 to +125	°C

5. Recommended Operating Conditions

GND = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	−	1.7	3.0	5.5	V
Clock supply voltage	V_{CLK}	−	1.15	3.0	5.5	V
Applied voltage when OFF	V_{PUP}	SCL, SDA, /INTA, /INTB pins	GND−0.3		5.5	°C
Pull-up resistance	R_{PUP}	FOE pin			10	kΩ
Operating temperature	T_{OPR}	No condensation	−40	+25	+85	°C

6. Frequency Characteristics

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Frequency precision	Δ f / f	Ta = +25°C V_{DD} = 3.0 V	AA ; 5 ± 5 (*1) AC ; 0 ± 5 (*1)	× 10^{-6}
Frequency/voltage characteristics	f / V	Ta = +25°C V_{DD} = 2 V to 5 V	± 1 Max.	× 10^{-6} / V
Frequency/temperature characteristics	Top	Ta = −20 °C to +70 °C, V_{DD} = 3.0 V; +25 °C reference	+10 / −120	× 10^{-6}
Oscillation start time	t_{STA}	Ta = +25 °C V_{DD} = 2.0 V	1 Max.	s
Aging	fa	Ta = +25 °C V_{DD}=3.0 V; first year	± 5 Max.	× 10^{-6} / year

*1) AC rank. Precision gap per month: 13 seconds (excluding offset value)

7. Electrical Characteristics

7.1. DC Electrical Characteristics

7.1.1. DC electrical characteristics (1)

* Unless otherwise specified, GND = 0 V, V_{DD} = 3 V, Ta = −40 °C to +85 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD1}	f_{SCL} = 0Hz, FOE = GND /INTA, /INTB = V_{DD} FOUT; output OFF (Output = OPEN)	VDD=5 V		0.60	1.80	µA
			VDD=3 V		0.48	1.20	
Current consumption (2)	I_{DD2}	f_{SCL} = 0Hz V_{DD}, /INTA, /INTB, FOE = 5.5 V FOUT;32.768 kHz output ON (Output = OPEN ; CL= 0 pF)			3.0	6.5	µA
High-level input voltage	V_{IH}	SCL, SDA, FOE pins V_{DD} = 1.7 ~ 5.5 V		0.8 × V_{DD}		5.5	V
Low-level input voltage	V_{IL}			GND − 0.3		0.2 × V_{DD}	V
High-level input current	I_{OH}	FOUT pin, V_{OH} = V_{DD} − 0.5 V				−0.5	mA
Low-level input current	I_{OL1}	FOUT pin, V_{OL} = 0.4 V		0.5			mA
	I_{OL2}	/INTA and /INTB pins, V_{OL} = 0.4 V		1.0			mA
	I_{OL3}	SDA pin, V_{OL} = 0.4 V		4.0			mA
Input leakage current	I_{IL}	SCL pin, V_I = 5.5 V or GND, V_{DD} = 5.5 V		−1		1	µA

7.1.2. DC electrical characteristics (2) * Unless otherwise specified, GND = 0 V, V_{DD} = 3 V, Ta = –40 °C to +85 °C

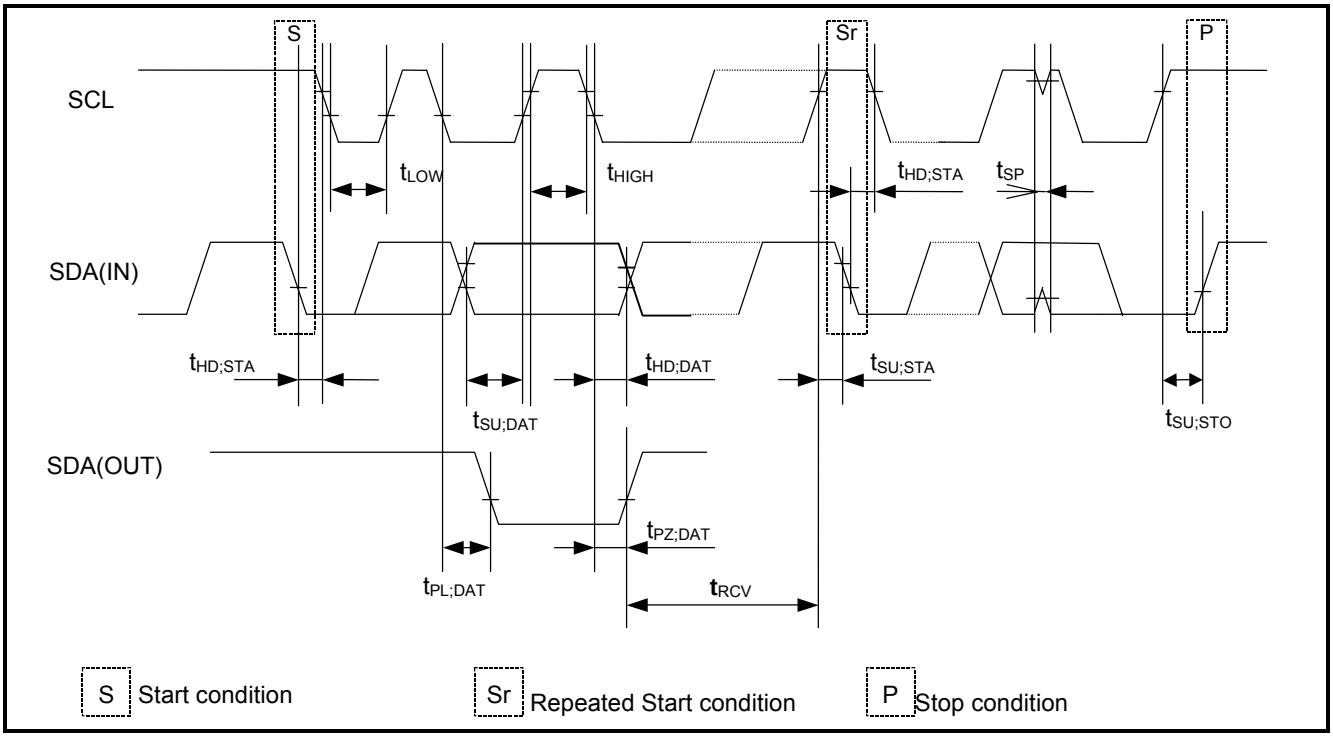
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Input current with pull-down resistance		I_{FOE}	FOE pin, V_I = 5.5 V		0.3	1.0	µA
Output current when OFF		I_{OZ}	SDA, /INTA, and /INTB pins V_O = 5.5 V or GND, V_{DD} = 5.5 V	–1		1	µA
Power supply detection voltage	High-voltage mode	V_{DETH}	V_{DD} pin, Ta = –30 to +70 °C	1.90	2.10	2.30	V
	Low-voltage mode	V_{DETL}	V_{DD} pin, Ta = –30 to +70 °C	1.15	1.30	1.45	V

7.2. AC Electrical Characteristics

∗ Unless otherwise specified: GND = 0 V, V_{DD} = 1.7 V to 5.5 V, Ta = –40 °C to +85 °C

∗ Input conditions: V_{IH} = 0.8 × V_{DD}, V_{IL} = 0.2 × V_{DD}, V_{OH} = 0.8 × V_{DD}, V_{OL} = 0.2 ×V_{DD}, CL = 50 pF

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}				400	kHz
SCL clock low time	t_{LOW}		1.3			µs
SCL clock higt time	t_{HIGH}		0.6			µs
Start condition hold time	$t_{HD;STA}$		0.6			µs
Stop condition setup time	$t_{SU;STO}$		0.6			µs
Start condition setup time	$t_{SU;STA}$		0.6			µs
Recovery time from stop condition to start condition	t_{RCV}		62			µs
Data setup time	tSU:DAT		200			ns
Data hold time	tHD;DAT		0			ns
SDA “L” stable time after falling of SCL	tPL;DAT				0.9	µs
SDA off stable time after falling of SCL	tPZ;DAT				0.9	µs
Rising time of SCL and SDA (input)	tR				300	ns
Falling time of SCL and SDA (input)	tF				300	ns
Spike width that can be removed with input filter	tSP				50	ns



Caution: When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access should be completed within 0.5 seconds.
If such communication requires 0.5 to 1.0 second or longer, the I^2C bus interface is reset by the internal bus timeout function. Please see also 8.8.3. Starting and stopping I^2C bus communications.

8.1. Functional descriptions

8.1. Overview of Functions

1) Clock functions

This function is used to set and read out month, date, day, hour, minute, and second.
Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.

∗ For details, see "8.2. Description of Registers".

2) Clock precision adjustment function

The clock precision can be adjusted forward or back in units of $\pm 3.05 \times 10^{-6}$. This function can be used to implement a higher-precision clock function, such as by:

- enabling higher clock precision throughout the year by taking seasonal clock precision adjustments into account in advance, or
- enabling correction of temperature-related clock precision variation in systems that include a temperature detection function.

Note: Only the clock precision can be adjusted. The adjustments have no effect on the 32.768-kHz output from the FOUT pin.

∗ For details, see "8.3. Clock Precision Adjustment Function".

3) Periodic interrupt function

In addition to the alarm function, Periodic interrupts can be output via the /INTA pin.
Select among five Periodic frequency settings: 2 Hz, 1 Hz, 1/60 Hz, hourly, or monthly.
Select among two output waveforms for periodic interrupts: an ordinary pulse waveform (2 Hz or 1 Hz) or a waveform (every second, minute, hour, or month) for CPU-level interrupts that can support CPU interrupts.
A polling function is also provided to enable monitoring of pin states via registers.

∗ For details, see "8.4. Periodic Interrupt Function".

4) Alarm functions

This module is equipped with two alarm functions (Alarm W and Alarm D) that output interrupt signals to the host at preset times. The Alarm W function can be used for day, hour, and minute-based alarm settings, and it outputs interrupt signals via the /INTB pin. Multiple day settings can be selected (such as Monday, Wednesday, Friday, Saturday, and Sunday). The Alarm D function can be used only for hour or minute-based settings, and it outputs interrupt signals via the /INTA pin.
A polling function is also provided to enable checking of each alarm mode by the host.

∗ For details on the Alarm W function, see "8.5. Alarm W function" and for the Alarm D function, see "8.6. Alarm D Function".

5) Oscillation stop detection function, power drop detection function (voltage monitoring function), and power-on reset detection function

The oscillation stop detection function uses registers to record when oscillation has stopped.
The power drop detection function (supply voltage monitoring function) uses registers to record when the supply voltage drops below a specified voltage threshold value. Use registers to specify either of two voltage threshold values: 2.1 V or 1.3 V. Voltage sampling is performed once per second in consideration of the module's low current consumption.
While the oscillation stop detection function is useful for determining when clock data has become invalid, the supply voltage monitoring function is useful for determining whether or not the clock data is able to become invalid. The supply voltage monitoring function can also be used to monitor a battery's supply voltage.
When these functions are utilized in combination with the power-on reset detection function, they are useful for determining whether clock data is valid or invalid when checking for power-on from 0 V or for back-up.

∗ For details, see "8.7. Detection Functions".

6) Interface with CPU

Data is read and written via the I^2C bus interface using two signal lines: SCL (clock) and SDA (data).
Since neither SCL nor SDA includes a protective diode on the V_{DD} side, a data interface between hosts with differing supply voltages can still be implemented by adding pull-up resistors to the circuit board.
The SCL's maximum clock frequency is 400 kHz (when $V_{DD} \geq 1.7$ V), which supports the I^2C bus's high-speed mode.

∗ For further description of data read/write operations, see "8.8. Reading/Writing Data via the I^2C Bus Interface".

7) 32.768-kHz clock output

The 32.768-kHz clock (with precision equal to that of the built-in quartz oscillator) can be output via the FOUT pin.

Note: The precision of this 32.768-kHz clock output via the FOUT pin cannot be adjusted (even when using the clock precision adjustment function).

8.2. Description of Registers

8.2.1. Register table

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	note
0	Seconds	○	S40	S20	S10	S8	S4	S2	S1	∗5
1	Minutes	○	M40	M20	M10	M8	M4	M2	M1	∗5
2	Hours	○	○	H20 P , /A	H10	H8	H4	H2	H1	∗5
3	Weekdays	○	○	○	○	○	W4	W2	W1	∗5
4	Days	○	○	D20	D10	D8	D4	D2	D1	∗5
5	Months	**0**	○	○	MO10	MO8	MO4	MO2	MO1	∗4, ∗5
6	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	–
7	Digital Offset	**0**	F6	F5	F4	F3	F2	F1	F0	∗4
8	Alarm_W ; Minute	○	WM40	WM20	WM10	WM8	WM4	WM2	WM1	∗5
9	Alarm_W ; Hour	○	○	WH20 WP,/A	WH10	WH8	WH4	WH2	WH1	∗5
A	Alarm_W ; Weekday	○	WW6	WW5	WW4	WW3	WW2	WW1	WW0	∗5
B	Alarm_D ; Minute	○	DM40	DM20	DM10	DM8	DM4	DM2	DM1	∗5
C	Alarm_D ; Hour	○	○	DH20 DP , /A	DH10	DH8	DH4	DH2	DH1	∗5
D	Reserved	Reserved								∗3
E	Control 1	WALE	DALE	/12 , 24	/CLEN2	TEST	CT2	CT1	CT0	∗1, ∗2, ∗6
F	Control 2	VDSL	VDET	/XST	PON	/CLEN1	CTFG	WAFG	DAFG	∗1, ∗6

Caution points:

∗1. The PON bit is a power-on reset flag bit.
The PON bit is set to "1" when a reset occurs, such as during the initial power-up or when recovering from a supply voltage drop. At the same time, all bits in the Control 1 and Control 2 registers except for the PON and / XST bits are reset to "0".
Note: At this point, all other register values are undefined, so be sure to perform a reset before using the module. Also, be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the time data is incorrect.

∗2. The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit.

∗3. Address D (a reserved register) is used for the manufacturer's settings. Do not read from or write to this register.

∗4. All bits marked with a " **0** " in the above table should be set as "0". Their value when read will be "0".

∗5. All bits marked with " ○ " are read-only bits. Their value when read is always "0".

∗6. When PON bit became 1 because power-on reset function worked, /CLEN1 and /CLEN2 bit become 0.
When /CLEN1 and /CLEN2 bit become 1 even if FOE input is "H", FOUT output stops.

FOE input	/CLEN1 bit	/CLEN2 bit	FOUT output
L	X	X	OFF (" L ")
H	0	0	32.768 kHz
	0	1	32.768 kHz
	1	0	32.768 kHz
	1	1	OFF (" L ")

' X ' Don't care.

8.2.2. Time counter (Reg 0 to 2)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	Seconds	○	S40	S20	S10	S8	S4	S2	S1
1	Minutes	○	M40	M20	M10	M8	M4	M2	M1
2	Hours	○	○	H20 P, /A	H10	H8	H4	H2	H1

- The time counter counts seconds, minutes, and hours.
- The data format is BCD format (except during 12-hour mode). For example, when the "seconds" register value is "0101 1001" it indicates 59 seconds.

∗ Note with caution that writing non-existent time data may interfere with normal operation of the time counter.

1) Second counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	Seconds	○	S40	S20	S10	S8	S4	S2	S1

- This second counter counts from "00" to "01," "02," and up to 59 seconds, after which it starts again from 00 seconds.
- When a value is written to the second counter, the internal counter is also reset to zero in less than one second.

2) Minute counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	Minutes	○	M40	M20	M10	M8	M4	M2	M1

- This minute counter counts from "00" to "01," "02," and up to 59 minutes, after which it starts again from 00 minutes.

3) Hour counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
2	Hours	○	○	H20 P , /A	H10	H8	H4	H2	H1

- The hour counter counts hours, and its clock mode differs according to the value of its /12,24 bit.
- During 24-hour clock operation, bit 5 functions as H20 (two-digit hour display). During 12-hour clock operation, bit 5 functions as an AM/PM indicator ("0" indicates AM and "1" indicates PM).

/12,24 bit	Description	Address 2 (Hours register) data [h] during 24-hour and 12-hour clock operation modes
0	12-hour clock	24-hour clock / 12-hour clock: 00 / 12 (AM 12) 01 / 01 (AM 01) 02 / 02 (AM 02) 03 / 03 (AM 03) 04 / 04 (AM 04) 05 / 05 (AM 05) 06 / 06 (AM 06) 07 / 07 (AM 07) 08 / 08 (AM 08) 09 / 09 (AM 09) 10 / 10 (AM 10) 11 / 11 (AM 11) 12 / 32 (PM 12) 13 / 21 (PM 01) 14 / 22 (PM 02) 15 / 23 (PM 03) 16 / 24 (PM 04) 17 / 25 (PM 05) 18 / 26 (PM 06) 19 / 27 (PM 07) 20 / 28 (PM 08) 21 / 29 (PM 09) 22 / 30 (PM 10) 23 / 31 (PM 11)
1	24-hour clock	

8.2.3. Day counter (Reg 3)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
3	Days	○	○	○	○	○	W4	W2	W1

- The day counter is a divide-by-7 counter that counts from 00 to 01 and up 06 before starting again from 01.
- The correspondence between days and count values is shown below.

Days	W4	W2	W1	Day	Remark
Write / Read	0	0	0	Sunday	00 h
	0	0	1	Monday	01 h
	0	1	0	Tuesday	02 h
	0	1	1	Wednesday	03 h
	1	0	0	Thursday	04 h
	1	0	1	Friday	05 h
	1	1	0	Saturday	06 h
Write prohibit	1	1	1	–	Do not enter a setting for this bit.

8.2.4. Calendar counter (Reg 4 to 6)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
4	Days	○	○	D20	D10	D8	D4	D2	D1
5	Months	0	○	○	MO10	MO8	MO4	MO2	MO1
6	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1

- The auto calendar function updates all dates, months, and years from January 1, 2001 to December 31, 2099.
- The data format is BCD format. For example, a date register value of "0011 0001" indicates the 31st.

∗ Note with caution that writing non-existent date data may interfere with normal operation of the calendar counter.

1) Date counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
4	Days	○	○	D20	D10	D8	D4	D2	D1

- The updating of dates by the date counter varies according to the month setting.

∗ A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96).

Days	Month	Date update pattern
Write / Read	1, 3, 5, 7, 8, 10, or 12	01, 02, 03 to 30, 31, 01…
	4, 6, 9, or 11	01, 02, 03 to 30, 01, 02…
	February in leap year	01, 02, 03 to 28, 29, 01…
	February in normal year	01, 02, 03 to 28, 01, 02…

2) Month counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
5	Months	0	○	○	MO10	MO8	MO4	MO2	MO1

- The month counter counts from 01 (January), 02 (February), and up to 12 (December), then starts again at 01 (January).

∗ Be sure to set a "0" for any bit whose value is shown above as "0". A zero is returned when any of these bits is read.

3) Year counter

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
6	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1

- The year counter counts from 00, 01, 02 and up to 99, then starts again at 00.

∗ In any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.), the dates in February are counted from 01, 02, 03 and up to 29 before starting again at 01.

8.2.5. Clock precision adjustment register (Reg 7)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
7	Digital Offset (Default)	0 (0)	F6 (0)	F5 (0)	F4 (0)	F3 (0)	F2 (0)	F1 (0)	F0 (0)

- The binary encoded settings in the seven bits from F6 to F0 are used to set the precision of the clock generated from the 32768-Hz internal oscillator up to $\pm 189 \times 10^{-6}$ in the forward (ahead) or reverse (behind) direction, in units of $\pm 3.05 \times 10^{-6}$. (Only the clock precision can be adjusted. The 32.768-kHz output from the FOUT pin is not affected.)
- When not using this function, be sure to set "0" for bits F6 to F0.

∗ For details, see "8.3. Clock Precision Adjustment Function".

8.2.6. Alarm_W register (Reg 8 to A)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
8	Alarm_W ; Minute	○	WM40	WM20	WM10	WM8	WM4	WM2	WM1
9	Alarm_W ; Hour	○	○	WH20 WP , /A	WH10	WH8	WH4	WH2	WH1
A	Alarm_W ; Day	○	WW6	WW5	WW4	WW3	WW2	WW1	WW0

- The Alarm W function is used, along with the WALE and WAFG bits, to set alarms for specified day, hour, and minute values.
- When the Alarm_W setting matches the current time, /INTB pin is set to "L" and the WALE bit is set to "1".
  Note: If the current date/time is used as the Alarm_W setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).
- During 24-hour clock operation, the "Alarm_W ; Hours" register's bit 5 (WH20, WP, /A) functions as WH20 (two-digit hour display), and during 12-hour clock operation it functions as an AM/PM indicator.
- When the Alarm_W function's day values (WW6 to WW0) are all "0" Alarm W does not occur.

∗ For details, see "8.5. Alarm W Function".

8.2.7. Alarm_ D register (Reg B and C)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
B	Alarm_D ; Minute	○	DM40	DM20	DM10	DM8	DM4	DM2	DM1
C	Alarm_D ; Hour	○	○	DH20 DP , /A	DH10	DH8	DH4	DH2	DH1

- The Alarm D function is used, along with the DALE and DAFG bits, to set alarms for specified hour and minute values.
- When the Alarm_D setting matches the current time, /INTA pin is set to "L" and the DALE bit is set to "1".
  Note: If the current time is used as the Alarm_D setting, the alarm will not occur until the counter counts up to the current time (i.e., an alarm will occur next time, not immediately).
- During 24-hour clock operation, the "Alarm_D ; Hours" register's bit 5 (DH20, DP, /A) functions as DH20 (two-digit hour display), and during 12-hour clock operation it functions as an AM/PM indicator.

∗ For details, see "8.6. Alarm D Function".

8.2.8. Control register 1 (Reg E)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
E	Control 1 (Default)	WALE (0)	DALE (0)	/12 , 24 (0)	/CLEN2 (0)	TEST (0)	CT2 (0)	CT1 (0)	CT0 (0)

∗) The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.

1) WALE bit

This bit is used to set up the Alarm W function (to generate alarms matching day, hour, or minute settings).

WALE	Data	Description
Write / Read	0	Alarm_W, match comparison operation invalid ∗ Default
	1	Alarm_W, match comparison operation valid (/INTB = "L" when match occurs)

∗ For details, see "8.5. Alarm W Function".

2) DALE bit

This bit is used to set up the Alarm D function (to generate alarms matching hour or minute settings).

DALE	Data	Description
Write / Read	0	Alarm_D, match comparison operation invalid ∗ Default
	1	Alarm_D, match comparison operation valid (/INTA = "L" when match occurs)

∗ For details, see "8.6. Alarm D Function".

3) /12,24 bit

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

/12,24	Data	Description
Write / Read	0	12-hour clock ∗ Default
	1	24-hour clock

∗ Be sure to select between 12-hour and 24-hour clock operation before writing the time data.

∗ See also "3) Hour counter" in section 8.2.4.

4) /CLEN2 bit

It combines /CLEN1 bit, and is bit controlling FOUT output.
When /CLEN1 and /CLEN2 bit become 1 even if FOE input is "H", FOUT output stops.
If FOUT output is unnecessary, it functions as RAM-bit and is (FOE="L")
When PON bit became 1 because power-on reset function worked, /CLEN1 and /CLEN2 bit become 0.

5) TEST bit

This bit is used by the manufacturer for testing. Be sure to write "0" to this bit.
Be careful to avoid writing a "1" to this bit when writing to other bits.

TEST	Data	Description
Write / Read	0	Normal operation mode ∗ Default
	1	Setting prohibited (manufacturer's test mode)

6) CT2, CT1, and CT0 bits

These bits are used to set up the operation of the periodic interrupt function that uses the /INTA pin.

CT2	CT1	CT0	/INTA pin's output setting		
			Waveform mode	Cycle/Fall timing	
0	0	0	–	/INTA = Hi-Z (= OFF)	∗ Default
0	0	1	–	/INTA = Fixed low	
0	1	0	Pulse mode ∗1)	2 Hz	(50% duty)
0	1	1	Pulse mode ∗1)	1 Hz	(50% duty)
1	0	0	Level mode ∗2)	Once per second	(Synchronous with per-second count-up)
1	0	1	Level mode ∗2)	Once per minute	(Occurs when seconds reach ":00")
1	1	0	Level mode ∗2)	Once per hour	(Occurs when minutes and seconds reach "00:00")
1	1	1	Level mode ∗2)	Once per month	(Occurs at 00:00:00 on first day of month)

∗ For details, see "8.4. Periodic Interrupt".

8.2.9. Control register 2 (Reg F)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
F	Control 2 (Default)	VDSL (0)	VDET (0)	/ XST (–)	PON (1)	/CLEN1 (0)	CTFG (0)	WAFG (0)	DAFG (0)

∗1) The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.
∗2) "–" indicates undefined status.

1) VDSL bit
This bit is used to set the power drop detection function's threshold voltage value.

VDSL	Data	Description
Write / Read	0	Sets 2.1 V as the power drop detection function's threshold voltage value ∗ Default
	1	Sets 1.3 V as the power drop detection function's threshold voltage value

∗ For details, see "8.7. Detection Functions".

2) VDET bit
This bit indicates the power drop detection function's detection results.
VDET = "1" once a power voltage drop has occurred.

VDET	Data	Description
Write	0	Clears the VDET bit to zero, restarts the power drop detection operation and sets up for next power drop detection operation ∗ Default
	1	Setting prohibited (do not set this bit value, even though it has no effect)
Read	0	Power drop was not detected ∗ Default
	1	Power drop was detected (result is that bit value is held until cleared to zero)

∗ For details, see "8.7. Detection Functions".

3) / XST bit
This bit indicates the oscillation stop detection function's detection results.
If a "1" has already been written to this bit, it is cleared to zero when stopping of internal oscillation is detected.

/ XST	Data	Description
Write	0	Setting prohibited (do not set this bit value, even though it has no effect)
	1	Sets the oscillation stop detection function as use-enabled and sets up for next detection operation
Read	0	Oscillation stop was detected (result is that bit value is held until a "1" is written)
	1	Oscillation stop was not detected

∗ For details, see "8.7. Detection Functions".

4) PON bit
This bit indicates the power-on reset detection function's detection results.
The PON bit is set (= 1) when the internal power-on reset function operates.

PON	Data	Description
Write	0	Clears the PON bit to zero and sets up next detection operation
	1	Setting prohibited (do not set this bit value, even though it has no effect)
Read	0	Power-on reset was not detected
	1	Power-on reset was detected (result is that bit value is held until cleared to zero) ∗ Default

∗ When PON = "1" all bits in the Clock Precision Adjustment register and in the Control 1 and Control 2 registers (except for the PON and / XST bits) are reset to "0". This also causes output from /INTA and /INTB pin to be stopped (= Hi-Z).

∗ For details, see "8.7. Detection Functions".

5) /CLEN1 bit
This bit is controlling FOUT output with /CLEN2 bit.
When /CLEN1 and /CLEN2 bit set to 1 even if FOE input is "H", FOUT output stops.
If FOUT output is unnecessary, it functions as RAM-bit and is (FOE="L")
When PON bit became 1 because power-on reset function worked, /CLEN1 and /CLEN2 bit become 0.

6) CTFG bit
During a read operation, this bit indicates the /INTA pin's priodic interrupt output status.
This status can be set as OFF by writing a "0" to this bit when /INTA = " L".

CTFG	Data	Description
Write	0	A "0" can be written only when the periodic interrupt is in level mode, at which time the /INTA pin is set to OFF (Hi-z) status. (Only when Alarm_D does not match) ∗ After a "0" is written, the value still becomes "1" again at the next cycle. ∗ Default
	1	Setting prohibited (do not set this bit value, even though it has no effect)
Read	0	Periodic interrupt output OFF status; /INTA = OFF (Hi-z) ∗ Default
	1	Periodic interrupt output ON status; /INTA = "L"

∗ For details, see "8.4. Periodic Interrupt Function".

7) WAFG bit
This bit is valid only when the WALE bit value is "1". The WAFG bit value becomes "1" when Alarm W has occurred.
The /INTB = "L" status that is set at this time can be set to OFF by writing a "0" to this bit.

WAFG	Data	Description
Write	0	/INTB pin = OFF (Hi-z) ∗ Default
	1	Setting prohibited (do not set this bit value, even though it has no effect)
Read	0	Alarm_W time setting does not match current time (This bit's value is always "0" when the WALE bit's setting is "0") ∗ Default
	1	Alarm_W setting matches current time (Result is that bit value is held until cleared to zero)

∗ For details, see "8.5. Alarm W Function".

8) DAFG bit
This bit is valid only when the DALE bit value is "1". The DAFG bit value becomes "1" when Alarm D has occurred.
The /INTA = "L" status that is set at this time can be set to OFF by writing a "0" to this bit.

DAFG	Data	Description
Write	0	/INTA pin = OFF (Hi-z) (but only when the periodic interrupt output status is OFF) ∗ Default
	1	Setting prohibited (do not set this bit value, even though it has no effect)
Read	0	Alarm_D time setting does not match current time (This bit's value is always "0" when the DALE bit's setting is "0") ∗ Default
	1	Alarm_D time setting matches current time (result is that bit value is held until cleared to zero)

∗ For details, see "8.6. Alarm D function".

8.3. Clock Precision Adjustment Function

The clock precision can be set ahead or behind.
This function can be used to implement a higher-precision clock function, such as by:

- enabling higher clock precision throughout the year by taking seasonal clock precision adjustments into account in advance, or
- enabling correction of temperature-related clock precision variation in systems that include a temperature detection function.

∗ Note: Only the clock precision can be adjusted. The adjustments have no effect on the 32.768-kHz output from the FOUT pin.

8.3.1. Related register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
7	Digital Offset (Default)	0 (0)	F6 (0)	F5 (0)	F4 (0)	F3 (0)	F2 (0)	F1 (0)	F0 (0)

∗) Be sure to set a "0" for any bit whose value is shown above as "0". A zero is returned when any of these bits is read.

- The binary encoded settings in the seven bits from F6 to F0 are used to set the precision of the clock generated from the 32768-Hz internal oscillator up to $\pm 189.1 \times 10^{-6}$ in the forward (ahead) or reverse (behind) direction, in units of $\pm 3.05 \times 10^{-6}$.

∗1) When not using this function, be sure to set "0" for bits F6 to F0.
∗2) This function operates every twenty seconds (at 00 seconds, 20 seconds, and 40 seconds within each minute), which changes the cycle of the periodic interrupts that occur via this timing. (See "8.4. Periodic Interrupt Function".)

8.3.2. Adjustment capacity

1) Adjustment range and resolution

Adjustment range	Adjustment resolution	Internal timing of adjustment
-189.1×10^{-6} to $+189.1 \times 10^{-6}$	$\pm 3.05 \times 10^{-6}$	Once every 20 seconds (at "00", "20" and "40" seconds)

2) Adjustment amount and adjustment value

Adjustment amount ($\times 10^{-6}$)	Adjustment data Decimal / Hexadecimal	bit 7 0	bit 6 F6	bit 5 F5	bit 4 F4	bit 3 F3	bit 2 F2	bit 1 F1	bit 0 F0
−189.10	+63 / 3F h	0	0	1	1	1	1	1	1
−186.05	+62 / 3E h	0	0	1	1	1	1	1	0
−183.00	+61 / 3D h	0	0	1	1	1	1	0	1
⋮	⋮	⋮							
−9.15	+4 / 04	0	0	0	0	0	1	0	0
−6.10	+3 / 03	0	0	0	0	0	0	1	1
−3.05	+2 / 02 h	0	0	0	0	0	0	1	0
OFF	1 / 01 h	0	0	0	0	0	0	0	1
OFF	0 / 00 h	0	0	0	0	0	0	0	0
+3.05	−1 / 7F h	0	1	1	1	1	1	1	1
+6.10	−2 / 7E h	0	1	1	1	1	1	1	0
+9.15	−3 / 7D h	0	1	1	1	1	1	0	1
⋮	⋮	⋮							
+183.00	−60 / 44 h	0	1	0	0	0	1	0	0
+186.05	−61 / 43 h	0	1	0	0	0	0	1	1
+189.10	−62 / 42 h	0	1	0	0	0	0	1	0
OFF	−63 / 41 h	0	1	0	0	0	0	0	1
OFF	−64 / 40 h	0	1	0	0	0	0	0	0

8.3.3. Adjustment examples

Example 1) Setting time forward

Objective) To adjust (advance) the clock precision when FOUT clock output is 32767.7 Hz

(1) Determine the current amount of variance

32767.7 Hz $\rightarrow$ (32767.7 – 32768) / 32768 ∗ [32768] = Reference values
$\rightarrow -9.16 \times 10^{-6}$

(2) Calculate the optimum adjustment data (decimal value) relative to the current variance.

Adjustment data = variance / adjustment resolution
= –9.16 / 3.05
≈ –3 (decimal values are rounded down from 4 and up from 5)

∗ For adjusting forward from a retarded variance, this formula can be corrected using reciprocal numbers, but since this product inverts the +/- attributes, this formula can be used as it is.

(3) Calculate the setting adjustment data (hexadecimal)

To calculate the setting adjustment data while taking 7-bit binary encoding into account, subtract the adjustment data (decimal) from 128 (80h).

Setting adjustment data = 128 – 3 = 125 (decimal)
= 80h – 03h = 7Dh (hexadecimal)

Example 2) Setting time backward

Objective) To adjust (set back) the clock precision when FOUT clock output is 32768.3 Hz

(1) Determine the current amount of variance

32768.3 Hz $\rightarrow$ (32768.3 – 32768) / 32768 ∗ [32768] = reference values
$\rightarrow +9.16 \times 10^{-6}$

(2) Calculate the optimum adjustment data (decimal value) relative to the current variance.

Adjustment data = (variance / adjustment resolution) + 1
= (+9.16 / 3.05) + 1 ∗ Add 1 since reference value is 01h
≈ +4 (decimal values are rounded down from 4 and up from 5)

∗ For adjusting backward from an advanced variance, this formula can be corrected using reciprocal numbers, but since this product inverts the +/- attributes, this formula can be used as it is.

(3) Calculate the setting adjustment data (hexadecimal)

The value "4" can be used in hexadecimal as it is (04h).

Setting adjustment data = 04 h (hexadecimal)

8.4. Periodic Interrupt Function

Periodic interrupt output can be obtained via the /INTA pin.
Select among five periodic-cycle settings: 2 Hz (once per 0.5 seconds), 1 Hz (once per second), 1/60 Hz (once per minute), 1/3600 Hz (once per hour), or monthly (on the 1st of each month).
Select among two output waveforms for periodic interrupts: an ordinary pulse waveform (2 Hz or 1 Hz) or a waveform (every second, minute, hour, or month) for CPU-level interrupts that can support CPU interrupts.
A polling function is also provided to enable monitoring of pin states via registers.

8.4.1. Related registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
E	Control 1 (Default)	WALE (0)	DALE (0)	/12 , 24 (0)	/CLEN2 (0)	TEST (0)	**CT2 (0)**	**CT1 (0)**	**CT0 (0)**
F	Control 2 (Default)	VDSL (0)	VDET (0)	/ XST (–)	PON (1)	/CLEN1 (0)	**CTFG (0)**	WAFG (0)	DAFG (0)

∗1) The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.
∗2) "–" indicates undefined status.

1) CTFG bit
During a read operation, this bit indicates the /INTA pin's periodic interrupt output status.
This status can be set as OFF by writing a "0" to this bit when /INTA = " L". .

CTFG	Data	Description
Write	0	A "0" can be written only when the periodic interrupt is in level mode, at which time the /INTA pin is set to OFF (Hi-z) status. (Only when Alarm_D does not match) ∗ Default ∗ After a "0" is written, the value still becomes "1" again at the next cycle.
	1	Setting prohibited (do not set this bit value, even though it has no effect)
Read	0	periodic interrupt output OFF status; /INTA = OFF (Hi-z) ∗ Default
	1	Periodic interrupt output ON status; /INTA = "L"

2) CT2, CT1, CT0 bit
Combinations of these three bits are used to change the /INTA pin's output status.

CT2	CT1	CT0	/INTA pin's output setting		
			Waveform mode	Cycle / Fall timing	
0	0	0	–	/INTA = Hi-z (= OFF)	∗ Default
0	0	1	–	/INTA = Fixed low	
0	1	0	Pulse mode ∗1)	2 Hz	(50% duty)
0	1	1	Pulse mode ∗1)	1 Hz	(50% duty)
1	0	0	Level mode ∗2)	Once per second	(Synchronous with per-second count-up)
1	0	1	Level mode ∗2)	Once per minute	(Occurs when seconds reach ":00")
1	1	0	Level mode ∗2)	Once per hour	(Occurs when minutes and seconds reach "00:00")
1	1	1	Level mode ∗2)	Once per month	(Occurs at 00:00:00 on first day of month)

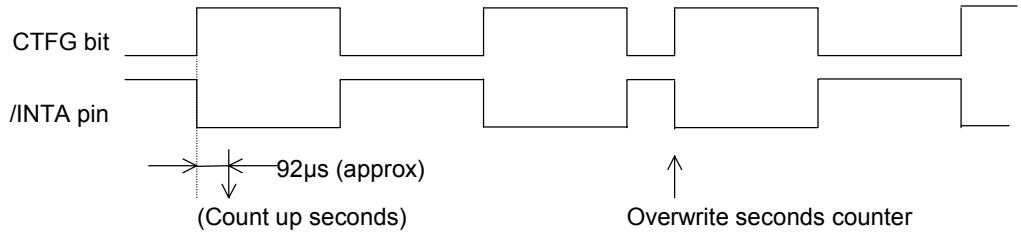
∗ The /INTA pin goes low ("L") when the Alarm_D function operates, but you can prevent that effect by setting "0" for CT2, CT1, and CT0 to stop this function.

∗ See the next page's description of pulse mode/level mode waveforms.

8.4.2. Mode-specific output waveforms

∗1) Pulse mode

A 2-Hz or 1-Hz clock pulse is output.
The relation between the clock pulse and the count operation is shown below.



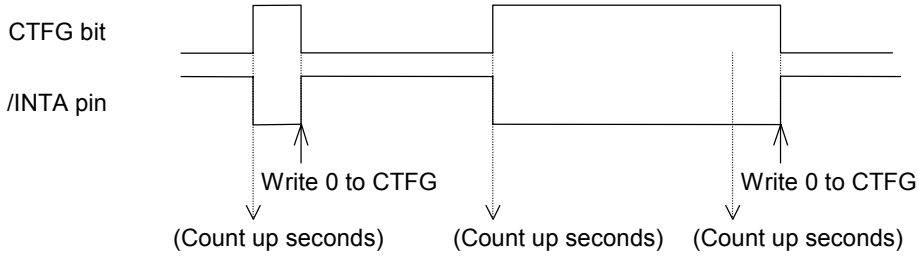
Note 1: As is shown in the above diagram, the seconds register's count up operation occurs approximately 92 µs after the falling edge of the /INTA output. Therefore, if the clock's value is read immediately after the output's falling edge, the read clock value may appear to be about one second slower than the RTC module's clock value.

Note 2: When the seconds counter is overwritten, the counter for time values under one second is also reset, which causes the /INTA level to go low ("L") again.

Note 3: When using the clock precision adjustment function, the periodic interrupt's cycle changes once every 20 seconds.
During pulse mode:
The period during which the output pulse is low can be adjusted backward or forward up to ±3.784 msec.
(For example, the duty for the 1-Hz setting can be adjusted ±0.3784% from 50%.)

∗2) Level mode

Select among four interrupt cycles: one second, one minute, one hour, or one month.
Counting up of seconds occurs in sync with the falling edge of the interrupt output. The following is a timing chart when a one-second interrupt cycle has been set.



Note: When using the clock precision adjustment function, the periodic interrupt's cycle changes once every 20 seconds.
During level mode
A one-second period can be adjusted backward or forward up to ±3.784 msec.

8.5. Alarm W function

The Alarm W function generates interrupt signals (output via the /INTB pin) that correspond to specified days, hours, and minutes.
For description of the Alarm D function, which supports only hour and minute data, see "8.6. Alarm D Function".
Multiple day settings can be selected (such as Monday, Wednesday, Friday, Saturday, and Sunday).
A polling function is also provided to enable checking of each alarm mode by the host.

8.5.1. Related registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	Minutes	○	**M40**	**M20**	**M10**	**M8**	**M4**	**M2**	**M1**
2	Hours	○	○	**H20 P, /A**	**H10**	**H8**	**H4**	**H2**	**H1**
3	Days	○	○	○	○	○	**W4**	**W2**	**W1**
8	Alarm_W ; Minute	○	**WM40**	**WM20**	**WM10**	**WM8**	**WM4**	**WM2**	**WM1**
9	Alarm_W ; Hour	○	○	**WH20 WP, /A**	**WH10**	**WH8**	**WH4**	**WH2**	**WH1**
A	Alarm_W ; Day	○	**WW6**	**WW5**	**WW4**	**WW3**	**WW2**	**WW1**	**WW0**
E	Control 1 (Default)	**WALE (0)**	DALE (0)	**/12, 24 (0)**	/CLEN2 (0)	TEST (0)	CT2 (0)	CT1 (0)	CT0 (0)
F	Control 2 (Default)	VDSL (0)	VDET (0)	/ XST (–)	PON (1)	/CLEN1 (0)	CTFG (0)	**WAFG (0)**	DAFG (0)

∗1) The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.
∗2) "○" indicates write-protected bits. A zero is always read from these bits.
∗3) "–" indicates undefined status.

- When the Alarm_W setting matches the current time, /INTB pin is set to "L" and the WALE bit is set to "1".
  Note: If the current date/time is used as the Alarm_W setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).
- During 24-hour clock operation, the "Alarm_W ; Hours" register's bit 5 (WH20, WP, /A) functions as WH20 (two-digit hour display), and during 12-hour clock operation it functions as an AM/PM indicator.
- When the Alarm_W function's day values (WW6 to WW0) are all "0" Alarm W does not occur.

1) WALE bit
This bit is used to set up the Alarm W function (to generate alarms matching day, hour, or minute settings).

WALE	Data	Description
Write / Read	0	Alarm_W, match comparison operation invalid ∗ Default
	1	Alarm_W, match comparison operation valid (/INTB = "L" when match occurs)

∗ When using the Alarm W function, first set this WALE bit value as "0," then stop the function. Next, set the day, hour, minute, and the WAFG bit. Finally, set "1" to the WALE bit to set the Alarm W function as valid. The reason for first setting the WALE bit value as "0" is to prevent /INTB = "L" output in the event that a match between the current time and alarm setting occurs while the alarm setting is still being made.

2) WAFG bit
This bit is valid only when the WALE bit value is "1". When a match occurs between the Alarm_W setting and the current time, the WAFG bit value becomes "1" approximately 61 μs afterward. (There is no effect when the WALE bit becomes "0".)
The /INTB = "L" status that is set at this time can be set to OFF by writing a "0" to this bit.

WAFG	Data	Description
Write	0	/INTB pin = OFF (Hi-z) ∗ Default
	1	Setting prohibited (do not set this bit value, even though it has no effect)
Read	0	Alarm_W time setting does not match current time ∗ Default (This bit's value is always "0" when the WALE bit's setting is "0")
	1	Alarm_W setting matches current time (Result is that bit value is held until cleared to zero)

∗ When a "0" is written to the WAFG bit, provisionally the WAFG bit value is "0" and the /INTB pin status is OFF (Hi-z). However, as long as the WALE bit value is "1" the Alarm W function continues to operate, and Alarm W occurs again the next time the same specified time arrives. You can stop Alarm W from occurring by writing "0" to the WALE bit to set this function as invalid.

3) /12, 24 bit

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

/12,24	Data	Description	Address 2 (Hours register) data [h] during 24-hour and 12-hour clock operation modes
Write / Read	0	12-hour clock	
	1	24-hour clock	

24-hour clock	12-hour clock	24-hour clock	12-hour clock
00	12 (AM 12)	12	32 (PM 12)
01	01 (AM 01)	13	21 (PM 01)
02	02 (AM 02)	14	22 (PM 02)
03	03 (AM 03)	15	23 (PM 03)
04	04 (AM 04)	16	24 (PM 04)
05	05 (AM 05)	17	25 (PM 05)
06	06 (AM 06)	18	26 (PM 06)
07	07 (AM 07)	19	27 (PM 07)
08	08 (AM 08)	20	28 (PM 08)
09	09 (AM 09)	21	29 (PM 09)
10	10 (AM 10)	22	30 (PM 10)
11	11 (AM 11)	23	31 (PM 11)

∗ Be sure to select between 12-hour and 24-hour clock operation before writing the time data.

4) Day setting

The following table shows the correspondence between the current day (W4, W2, W1) and the Alarm_W day (WW6 to WW0). Be sure to set a "1" to the Alarm_W day when the alarm will occur. (An alarm will not occur for any day that has a "0" setting.)

It is possible to enter settings for several days at the same time, in which case be sure to set a "1" for each day (among WW6 to WW0) in which an alarm will occur.

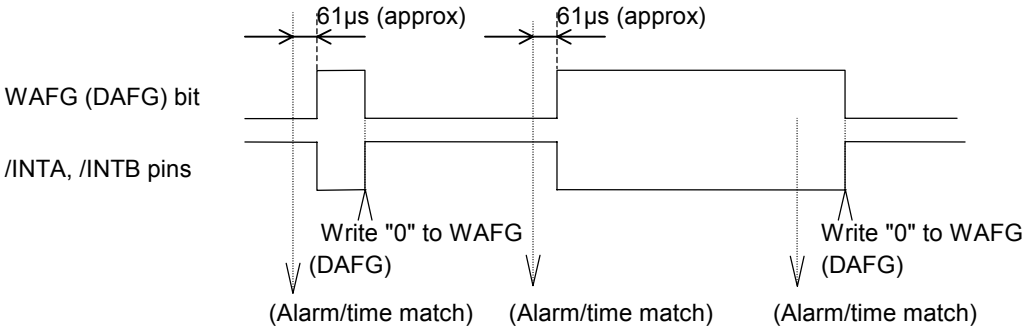
Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Alarm_W ; Day	□	WW6	WW5	WW4	WW3	WW2	WW1	WW0
Target day(s) (W4,W2,W1)	–	Saturday (1, 1, 0)	Friday (1, 0, 1)	Thursday (1, 0, 0)	Wednesday (0, 1, 1)	Tuesday (0, 1, 0)	Monday (0, 0, 1)	Sunday (0, 0, 0)

8.5.2. Alarm setting examples

Examples of settings for alarm usage are shown below.

Alarm setting (example)		Alarm_W ; Day Day setting							Alarm_W ; Hour Hour (hexadecimal)		Alarm_W ; Minute Minute (hexadecimal)
		WW6 Sat	WW5 Fri	WW4 Thu	WW3 Wed	WW2 Tue	WW1 Mon	WW0 Sun	24-hour clock	12-hour clock	12- & 24-hour clock
Every day	at 00:00 AM	1	1	1	1	1	1	1	00h hours	12h hours	00h min
Every day	at 01:30 AM	1	1	1	1	1	1	1	01h hours	01h hours	30h min
Every day	at 11:59 AM	1	1	1	1	1	1	1	11h hours	11h hours	59h min
Mon to Fri	at 12:00 PM	0	1	1	1	1	1	0	12h hours	32h hours	00h min
Sunday	at 01:30 PM	0	0	0	0	0	0	1	13h hours	21h hours	30h min
Mon/Wed/Fri	at 11:59 PM	0	1	0	1	0	1	0	23h hours	31h hours	59h min

8.5.3. WAFG, DAFG and /INTA, /INTB output



8.6. Alarm D function

The Alarm D function generates interrupt signals (output via the /INTA pin) that correspond to specified hours and minutes.
For description of the Alarm W function, which supports only day, hour, and minute data, see "8.5. Alarm W Function".
A polling function is also provided to enable checking of each alarm mode by the host.

8.6.1. Related registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1	Minutes	○	**M40**	**M20**	**M10**	**M8**	**M4**	**M2**	**M1**
2	Hours	○	○	**H20 P , /A**	**H10**	**H8**	**H4**	**H2**	**H1**
B	Alarm_D ; Minute	○	**DM40**	**DM20**	**DM10**	**DM8**	**DM4**	**DM2**	**DM1**
C	Alarm_D ; Hour	○	○	**DH20 DP , /A**	**DH10**	**DH8**	**DH4**	**DH2**	**DH1**
E	Control 1 (Default)	**WALE (0)**	**DALE (0)**	**/12 , 24 (0)**	/CLEN2 (0)	TEST (0)	CT2 (0)	CT1 (0)	CT0 (0)
F	Control 2 (Default)	VDSL (0)	VDET (0)	/ XST (–)	PON (1)	/CLEN1 (0)	CTFG (0)	**WAFG (0)**	**DAFG (0)**

∗1) The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.
∗2) "○" indicates write-protected bits. A zero is always read from these bits.
∗3) "–" indicates undefined status.

- When the Alarm_D setting matches the current time, /INTA pin is set to "L" and the DALE bit is set to "1".
  Note: If the current date/time is used as the Alarm_D setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).
- During 24-hour clock operation, the "Alarm_D ; Hours" register's bit 5 (DH20, DP, /A) functions as DH20 (two-digit hour display), and during 12-hour clock operation it functions as an AM/PM indicator.

1) DALE bit
This bit is used to set up the Alarm D function (to generate alarms matching hour or minute settings).

DALE	Data	Description
Write / Read	0	Alarm_D, match comparison operation invalid ∗ Default
	1	Alarm_D, match comparison operation valid (/INTA = "L" when match occurs)

∗ When using the Alarm D function, first set this DALE bit value as "0," then stop the function. Next, set the hour, minute, and the DAFG bit. Finally, set "1" to the DALE bit to set the Alarm D function as valid.
The reason for first setting the DALE bit value as "0" is to prevent /INTA = "L" output in the event that a match between the current time and alarm setting occurs while the alarm setting is still being made.

2) DAFG bit
This bit is valid only when the DALE bit value is "1". When a match occurs between the Alarm_D setting and the current time, the DAFG bit value becomes "1" approximately 61 μs afterward. (There is no effect when the DALE bit becomes "0".)
The /INTA = "L" status that is set at this time can be set to OFF by writing a "0" to this bit.

DAFG	Data	Description
Write	0	/INTA pin = OFF (Hi-z) (only when periodic interrupt output is OFF) ∗ Default
	1	Setting prohibited (do not set this bit value, even though it has no effect)
Read	0	Alarm_D time setting does not match current time ∗ Default (This bit's value is always "0" when the DALE bit's setting is "0")
	1	Alarm_D time setting matches current time (result is that bit value is held until cleared to zero)

∗ When a "0" is written to the DAFG bit, provisionally the DAFG bit value is "0" and the /INTA pin status is OFF (Hi-z). However, as long as the DALE bit value is "1" the Alarm D function continues to operate, and Alarm D occurs again the next time the same specified time arrives.
You can stop Alarm D from occurring by writing "0" to the DALE bit to set this function as invalid.

3) /12,24 bit
∗ See "/12, 24 bit" in section 8.5.1. 3.

8.6.2. WAFG, DAFG and /INTA, /INTB output
∗ See "WAFG, DAFG and /INTA, /INTB output" in section 8.5.3.

8.7. The various detection Functions

The detection functions include detection of power-on resets, oscillation stops, and supply voltage drops, as well as reporting of detection results in corresponding bits of the address Fh (Control 2) register.
The status of the power supply, oscillation circuit, and clock can be confirmed by checking these results.

∗ Note with caution that detection functions may not operate correctly when power flickers occur.

8.6.1. Related register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
F	Control 2 (Default)	**VDSL** **(0)**	**VDET** **(0)**	**/ XST** **(–)**	**PON** **(1)**	/CLEN1 (0)	CTFG (0)	WAFG (0)	DAFG (0)

∗1) The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.
∗2) '"–" indicates undefined status.

8.7.1. Power-on reset detection

This function detects when a power-on reset occurs. When a power-on reset is detected, the PON bit value becomes "1".
A reset is detected when a power-on from 0 V has occurred, including when the power-on reset from 0 V occurred due to a supply voltage drop.

1) PON bit
This bit indicates the detection results when a power-on reset has occurred.
The power-on reset function operates when a power-on from 0 V has occurred, including when a power-on reset from 0 V occurred due to a supply voltage drop. When this function operates, the PON bit value becomes "1".
The /XST and VDET bits can be used in combination to determine the valid/invalid status of the clock and calendar data.

PON	Data	Description
Write	0	Clears PON bit to zero and sets up for next detection operation
	1	Setting prohibited (do not set this bit value, even though it has no effect)
Read	0	Power-on reset was not detected
	1	Power-on reset was detected ∗ Default (result is that bit value is held until cleared to zero)

∗ When PON = "1" the clock precision adjustment register, Control register 1, and Control register 2 (except for PON and /XST) are reset and cleared to "0". This stops (sets Hi-Z for) output from the /INTA and /INTB pins.

2) Status of other bits when power-on reset is detected

- Internal initialization status during a power-on reset

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
7	Digital Offset (Default)	0 (0)	F6 (0)	F5 (0)	F4 (0)	F3 (0)	F2 (0)	F1 (0)	F0 (0)
E	Control 1 (Default)	WALE (0)	DALE (0)	/12, 24 (0)	/CLEN2 (0)	TEST (0)	CT2 (0)	CT1 (0)	CT0 (0)
F	Control 2 (Default)	VDSL (0)	VDET (0)	/ XST (–)	PON (1)	/CLEN1 (0)	CTFG (0)	WAFG (0)	DAFG (0)

∗1) The default value is the value that is read (or is set internally) after the PON bit has been set to "1," such as after powering up from 0 V or recovering from a supply voltage drop.

∗2) " –" indicates undefined status.

∗3) At this point, all other register bits are undefined, so be sure to perform a reset before using the module. Also, be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the time data is incorrect.

8.7.2. Oscillation stop detection

This function detects when internal oscillation has stopped. When an oscillation stop is detected, the /XST bit value becomes "0".
If a "1" has already been written to the /XST bit, the /XST bit is cleared to zero when stopping of internal oscillation is detected, so this function can be used to determine whether or not an oscillation stop has occurred previously, such as after recovery from a backup.

1) / XST bit
This bit indicates the oscillation stop detection function's detection results.

/ XST	Data	Description
Write	0	Setting prohibited (do not set this bit value, even though it has no effect)
	1	Sets the oscillation stop detection function as use-enabled and sets up for next detection operation
Read	0	Oscillation stop was detected (result is that bit value is held until a "1" is written)
	1	Oscillation stop was not detected

2) Caution points

To prevent detection errors during operation of the oscillation stop detection function, be sure to prevent stops due to V_{DD} power flicker and prevent application of voltage exceeding the maximum rated voltage to any pin.
In particular, fluctuation in the supply voltage may occur as shown in the figure at right, such as when a back-up battery is used. If this occurs, internal data may be lost even when the / XST bit value has not changed from "1" to "0" so be sure to avoid any input that contains large amounts of chattering.

Example of voltage fluctuation that makes oscillation stop hard to detect

8.7.3. Voltage drop detection

This function detects when a voltage drop occurs. Detection of a voltage drop changes the VDET bit value to "1".
The threshold voltage value for detection can be set via the VDSL bit as 2.1 V or 1.3 V.

1) VDSL bit
This bit is used to set the power drop detection function's threshold voltage value.

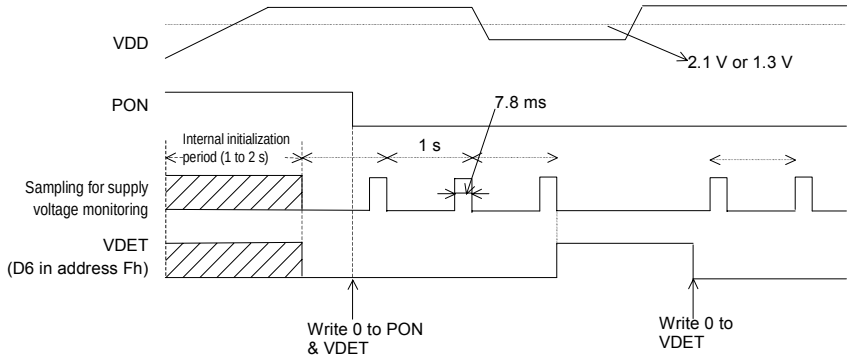
VDSL	Data	Description
Write / Read	0	Sets 2.1 V as the power drop detection function's threshold voltage value ∗ Default
	1	Sets 1.3 V as the power drop detection function's threshold voltage value

2) VDET bit
This bit indicates the power drop detection function's detection results. VDET = "1" once a power voltage drop has occurred. This detection operation is then stopped and the bit value (1) is held.

VDET	Data	Description
Write	0	Clears the VDET bit to zero, restarts the power drop detection operation and sets up for next power drop detection operation ∗ Default
	1	Setting prohibited (do not set this bit value, even though it has no effect)
Read	0	Power drop was not detected ∗ Default
	1	Power drop was detected (result is that bit value is held until cleared to zero)

3) Caution points

To reduce current consumption while monitoring the supply voltage, the supply voltage monitor circuit samples for only 7.8 ms during each second, as shown at right. Sampling is stopped once the VDET bit = "1". (Clear the VDET bit to zero to resume operation of the detection function.)

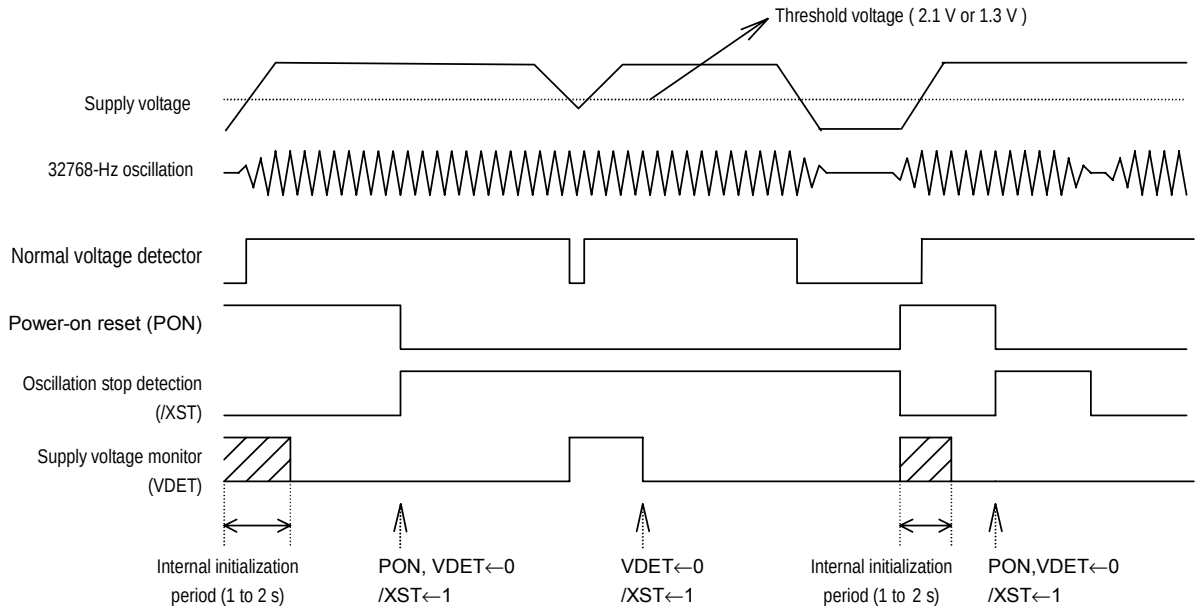


8.7.4. Estimation of status based on detection results

The power supply status and clock status can be confirmed by reading the detection results indicated by the PON, /XST, and VDET bits.
The following are status estimates based on various combinations of detection results.

Address F h Control 2 Register			Estimated status	
bit 4	bit 5	bit 6	Status of power supply and oscillation circuit	Status of clock and backup
PON	/ XST	VDET		
0	0	0	• No supply voltage drop, but oscillation has stopped.	• Clock abnormality has occurred → Initialization is required ∗ Clock has stopped temporarily, possibly due to condensation.
0	0	1	• Supply voltage has dropped and oscillation has stopped.	• Clock abnormality has occurred → Initialization is required ∗ Clock has stopped, perhaps due to drop in backup power supply.
0	1	0	• Normal status.	• Normal status.
0	1	1	• Supply voltage has dropped but oscillation continues.	• Clock is normal, but an abnormality exists in the power supply. ∗ Backup power supply may have dropped to a hazardous level.
1	0	x	• Supply voltage has dropped to 0 V.	• Initialization is required regardless of the clock status and whether or not a voltage drop has occurred. ∗ Initialization is required due to bits that are reset when PON = "1".
1	1	x	• Power supply flickering is likely.	

∗ The example shown above is when a "1" has already been written to /XST.



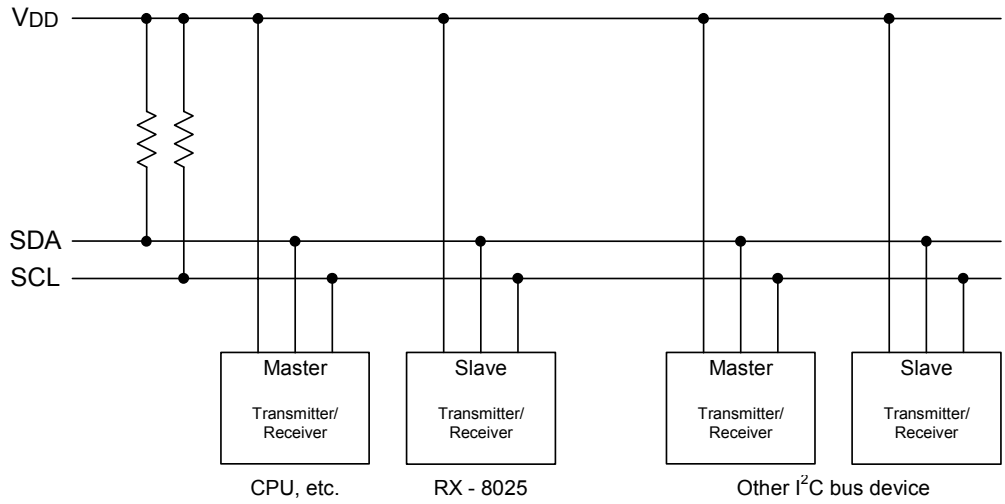
8.8. Reading/Writing Data via the I2C Bus Interface

8.8.1. Overview of I2C-BUS

The I2C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.
Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

8.8.2. System configuration

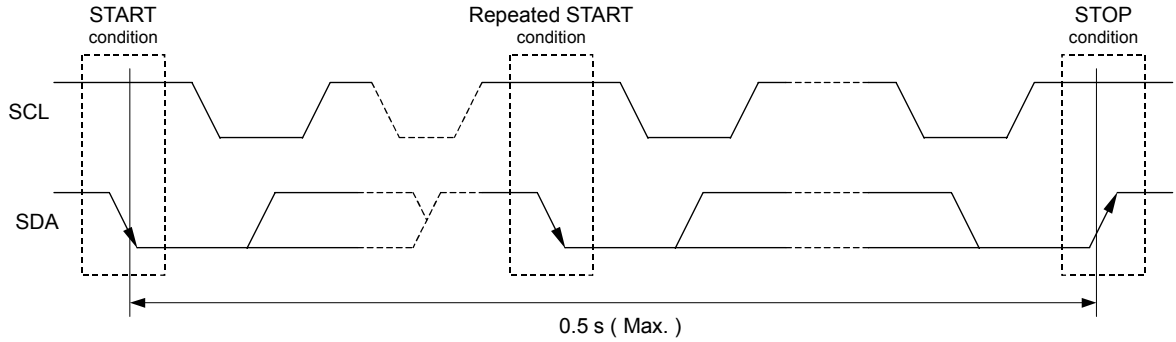
All ports connected to the I2C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.
SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).



Any device that controls the transmission and reception of data is defined as a master device and any device that is controlled by a master device is defined as a slave device.
Also, any device that transmits data is defined as a transmitter and any device that receives data is defined as a receiver.

In the case of this RTC module, controllers such as a CPU are defined as master devices and the RTC module is defined as a slave device. When a device is used for both transmitting and receiving data, it is defined as either a transmitter or receiver depending on these conditions.

8.8.3. Starting and stopping I^2C bus communications



1) START condition, repeated START condition, and STOP condition

(1) START condition

- This condition regulates how communications on the I^2C-BUS are started. SDA level changes from high to low while SCL is at high level

(2) STOP condition

- This condition regulates how communications on the I^2C-BUS are terminated. SDA level changes from low to high while SCL is at high level

(3) Repeated START condition (RESTART condition)

- In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

2) Caution points

∗1) The master device always controls the START, RESTART, and STOP conditions for communications.

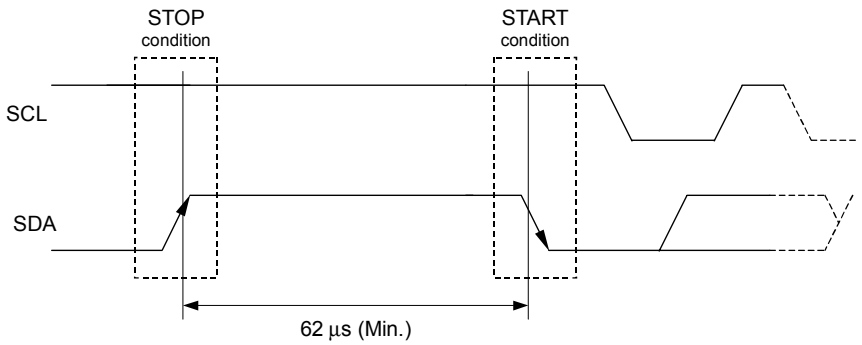
∗2) The master device does not impose any restrictions on the timing by which STOP conditions affect transmissions, so communications can be forcibly stopped at any time while in progress. (However, this is only when this RTC module is in receiver mode (data reception mode = SDA released).

∗3) When communicating with this RTC module, the series of operations from transmitting the START condition to transmitting the STOP condition should occur within 0.5 seconds. (A RESTART condition may be sent between a START condition and STOP condition, but even in such cases the series of operations from transmitting the START condition to transmitting the STOP condition should still occur within 0.5 seconds.)

If this series of operations requires 0.5 to 1.0 seconds or longer, the I^2C bus interface will be automatically cleared and set to standby mode by this RTC module's bus timeout function. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation. (When the read operation is invalid, all data that is read has a value of "1").

Restarting of communications begins with transfer of the START condition again.

∗4) When communicating with this RTC module, wait at least 62 µs between transferring a STOP condition (to stop communications) and transferring the next START condition (to start the next round of communications). (If any carries occur in the time data during this communication period, corrections are made during this period.)



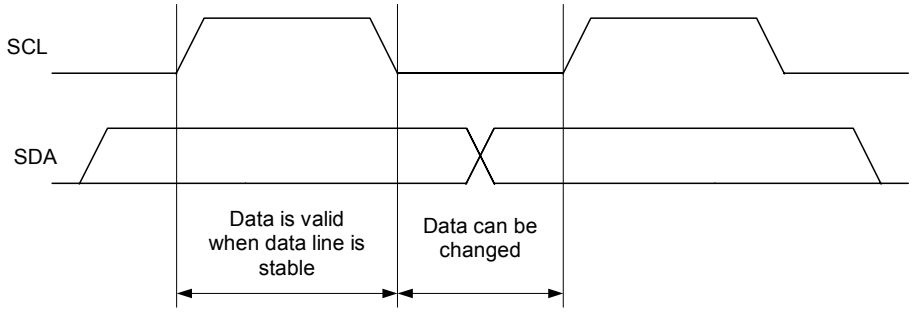
8.8.4. Data transfers and acknowledge responses during I²C-BUS communications

1) Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.
(However, the transfer time must be no longer than 0.5 seconds and access to the Address Dh (Reserved) register is prohibited.)

The address auto increment function operates during both write and read operations.
After address Fh, incrementation goes to address 0h.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level.
The receiver (receiving side) captures data while the SCL line is at high level.

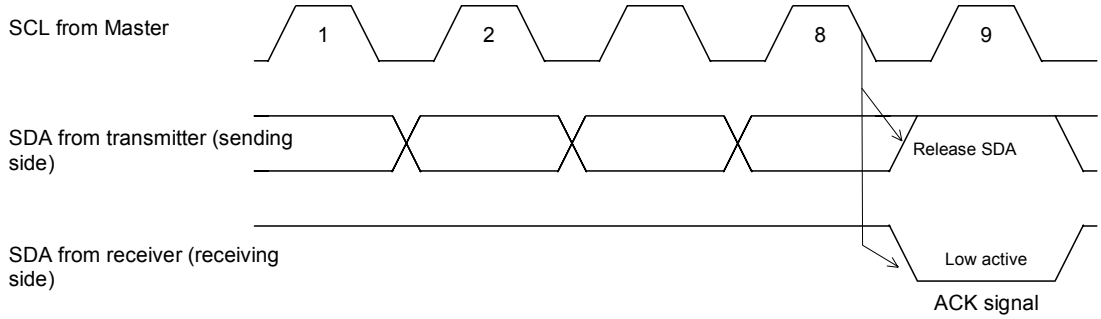


∗ Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

2) Data acknowledge response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.
When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

8.8.5. Slave address

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.
All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

Slave addresses have a fixed length of 7 bits. This RTC's slave address is [0110 010∗].
An R/W bit ("*" above) is added to each 7-bit slave address during 8-bit transfers.

	Transfer data	Slave address							R / W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	65 h	0	1	1	0	0	1	0	1 (= Read)
Write	64 h								0 (= Write)

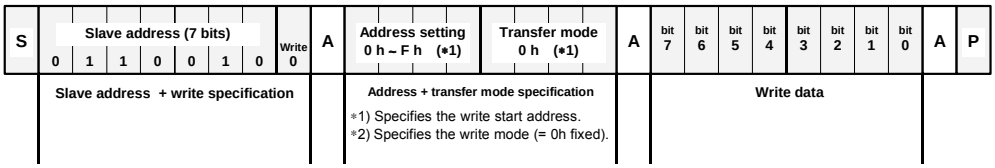
8.8.6. I²C bus's basic transfer format

- The write/read steps are illustrated below.

	Master is transmitter (sending side), RTC is receiver (receiving side)	S	START condition, sent by Master	A	Confirmation response from Master
	Master is receiver (receiving side), RTC is transmitter (sending side)	Sr	RESTART condition, sent by Master	/A	Master does not respond
		P	STOP condition, sent by Master	A	Confirmation response from RTC

1) Write via I²C bus

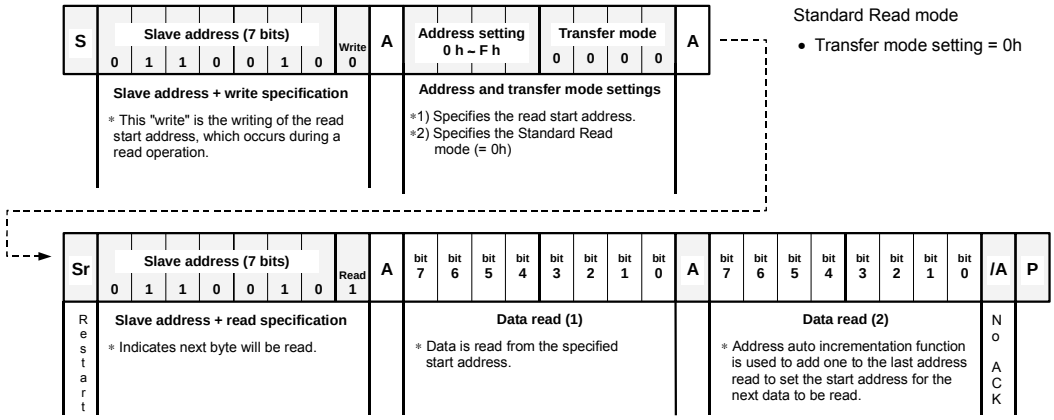
- The steps for writing via the I²C bus are shown below.



2) Read via I²C bus

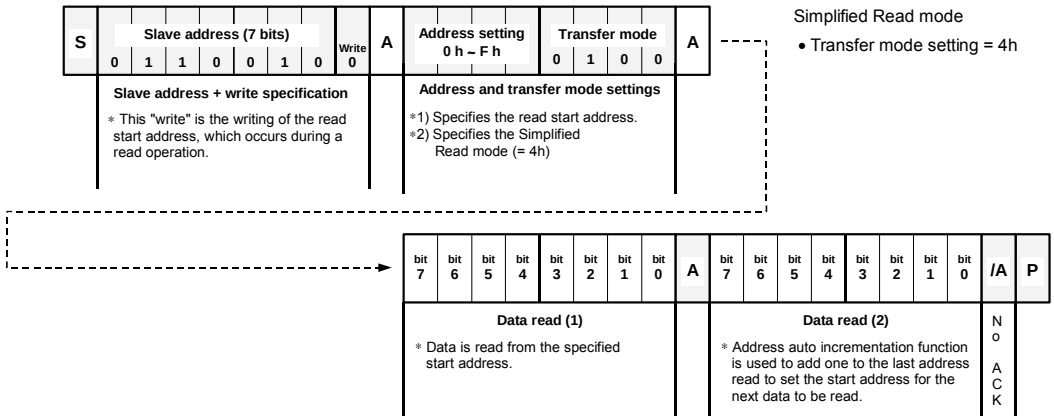
(1) Standard read method for I²C bus

- The steps for standard reading of the I²C bus are shown below.



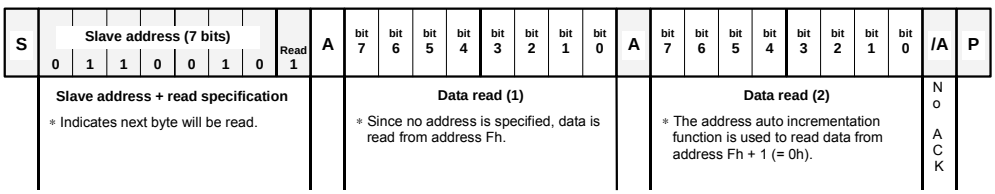
(2) Simplified read method

- This RTC module also provides a special read method that uses fewer read steps.



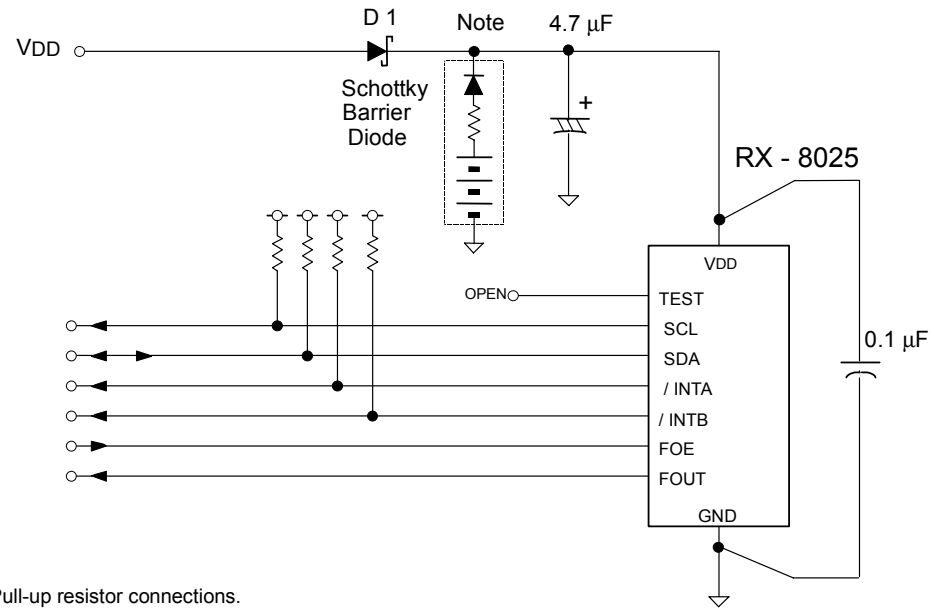
(3) Read method from address Fh, with no specified start address for read operation

- Only when reading from address Fh (Fh → 0h → 1h → 2h, etc.) can a read operation be performed without specifying the read start address or the transfer mode.



* The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications. (However, the transfer time must be no longer than 0.5 seconds and access to the Address Dh (Reserved) register is prohibited.)

8.9. External Connection Example



Note : Pull-up resistor connections.

- SCL and SDA

Connect to the system-power-supply .

- / INTA and / INTB

When , uses these interrupt signals at battery backup, connect these pins to backup power supply.

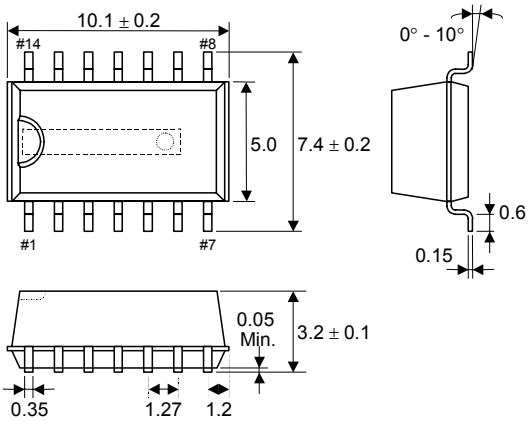
Note : Use a secondary cell or lithium cell. A diode is not required when using a secondary cell. When using a lithium cell, be sure to use a diode. Contact the battery manufacturer for details regarding applied resistance values.

9. External Dimensions / Marking Layout

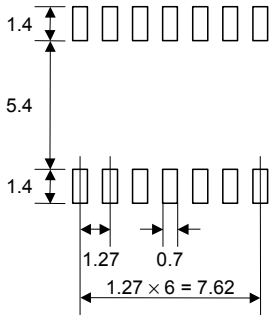
9.1. External Dimensions

RX-8025 SA (SOP-14pin)

• External dimensions



• Recommended soldering

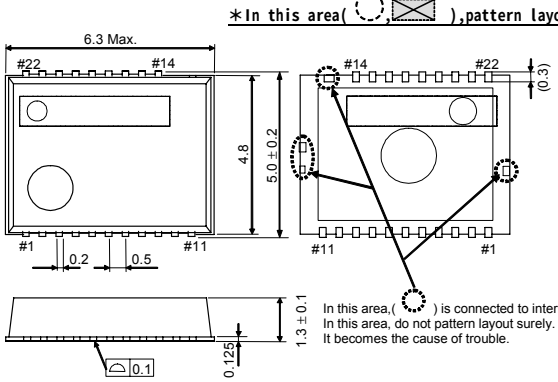


Unit : mm

∗ The cylinder of the crystal oscillator can be seen in this area (back and front), but it has no affect on the performance of the device.

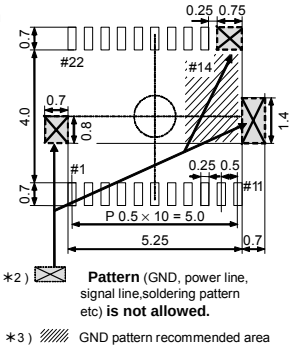
RX-8025 NB (SON-22pin)

• External dimensions



• Soldering pattern

Unit : mm



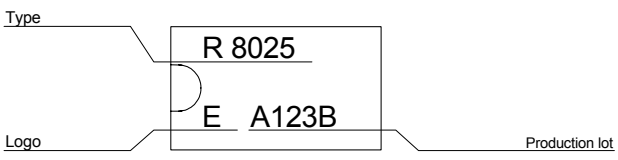
∗1) The cylinder of the crystal oscillator may be exposed in this area (top and bottom), however it has no affect on the performance of the device.

∗2) Pattern (GND, power line, signal line, soldering pattern, etc) is not allowed.
In this area, at a parts side of board, do not pattern layout surely.
∗ In an area ( ) of the product bottom side, a terminal connected to an IC inside is exposed.
When the circuit pattern contacts those terminal, it will cause serious obstruction to the oscillation, function or electronic spec.

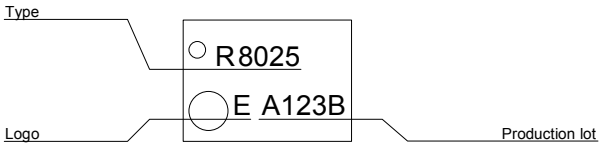
∗3) It is the best design that there is no signal line in this area. Please fill it up with GND pattern if possible.

9.2. Marking Layout

RX - 8025 SA (SOP-14pin)



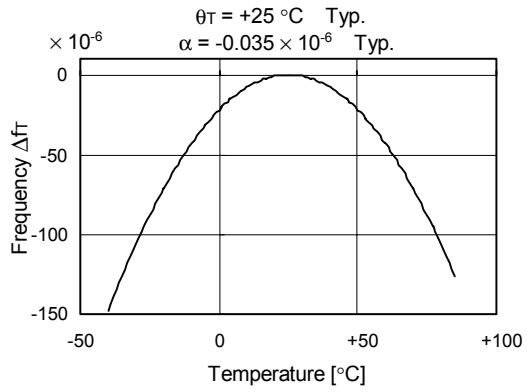
RX - 8025 NB (SON-22pin)



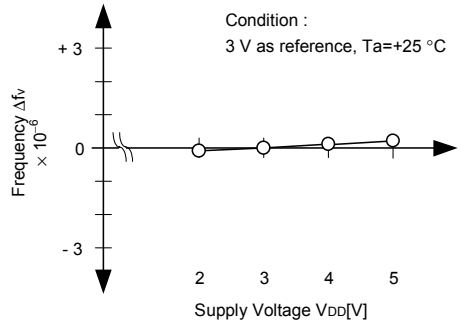
∗ The layout shown above is a simplified drawing of the seal and label. Details such as the fonts, sizes, and positioning of label contents are not necessarily as shown.

10. Reference Data

(1) Example of frequency and temperature characteristics



(2) Example of frequency and voltage characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

$\Delta f_T = \alpha\ (\theta_T - \theta_X)^2$

Δf_T		: Frequency deviation in any temperature
α	(1 / °C^2)	: Coefficient of secondary temperature (–0.035±0.005) × 10^{-6} / °C^2
θ_T	(°C)	: Ultimate temperature (+25±5 °C)
θ_X	(°C)	: Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

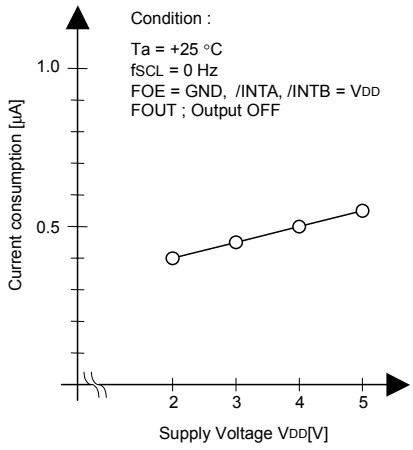
$\Delta f/f = \Delta f/fo + \Delta f_T + \Delta f_V$

$\Delta f/f$	: Clock accuracy (stable frequency) in any temperature and voltage
$\Delta f/fo$	: Frequency precision
Δf_T	: Frequency deviation in any temperature
Δf_V	: Frequency deviation in any voltage

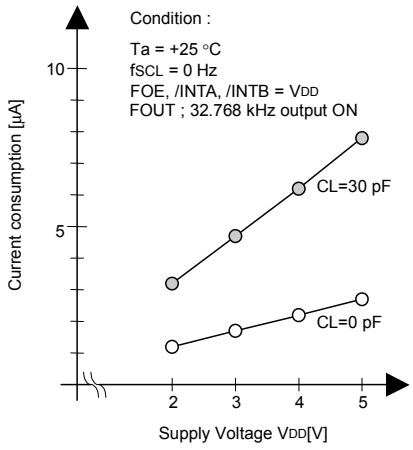
3. How to find the date difference
   Date difference = $\Delta f/f \times 86400$ (seconds)
   * For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

(3) Current and voltage consumption characteristics

(3-1) Current consumption when non-accessed (i) when FOUT=OFF



(3-2) Current consumption when non-accessed (ii) when FOUT=32.768 kHz



11. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1F as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

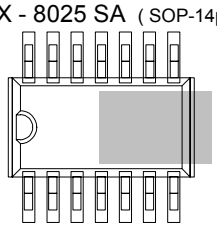
This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Example GND Pattern

RX - 8025 SA (SOP-14pin)



RX - 8025 NB (SON-22pin)

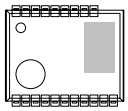
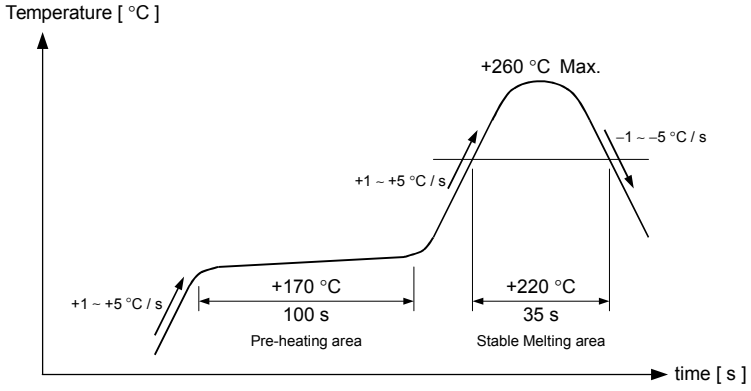


Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.



∗ In addition, please confirm the Notes of an individual specification.

EPSON TOYOCOM

Application Manual

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