UNIVERSITY OF COLOMBO SCHOOL OF COMPUTING

DEGREE OF BACHELOR OF INFORMATION TECHNOLOGY (EXTERNAL)

Academic Year 2011/2012 – 3rd Year Examination – Semester 5

IT5304: Computer Systems II
Structured Question Paper

4th March, 2012
(TWO HOUR)

To be completed by the candidate
BIT Examination Index No: _____

Important Instructions:

- The duration of the paper is **2 (two) hours**.
- The medium of instructions and questions is English.
- This paper has **4 questions** and **14 pages**.
- **Answer all questions.** All questions carry equal marks.
- **Write your answers** in English using the space provided **in this question paper**.
- Do not tear off any part of this answer book.
- Under no circumstances may this book, used or unused, be removed from the examination hall by a candidate.
- Note that questions appear on both sides of the paper.
  If a page is not printed, please inform the supervisor immediately.

Questions Answered

Indicate by a cross (×), (e.g. ☒) the numbers of the questions answered.

To be completed by the candidate by marking a cross (×).	Question numbers				
	1	**2**	**3**	**4**	
To be completed by the examiners:					

01) (a) Write down the truth table for a 4:1 binary multiplexer with inputs D_0-D_3, select lines S_0,S_1, and an output F.

(4 Marks)

ANSWER IN THIS BOX

S_0	S_1	F
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

(b) For error detection in data communications and data storage, the 'parity bit' method is typically used. For example, in a three bit data word, the fourth bit as an odd parity bit is generated in such a way that the total number of 1's in the four bit word is odd. Write down the truth table showing the possible odd parity bit value p for all possible combinations of a 3 bit data words (a, b, c).

(7 Marks)

ANSWER IN THIS BOX

a	b	cin	p
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

(c) Obtain the *most simplified* Boolean expression for p in terms of a, b and c.

(6 Marks)

ANSWER IN THIS BOX

P =ā b c + ā b c + a.b.c + a.b.c

=c (āb-a.b) + c(āb+ ab)

=c (a + b) + c (a + b)

= (a+b) + c

(d) A multiplexer may be effectively used to replace the combinational logic in many instances. Show how the parity bit p can be generated for a 3 bit data word (a b c) using a 4:1 binary multiplexer and a minimum of extra logic.

(8 Marks)

ANSWER IN THIS BOX

```
c ──→ │ D0                │
c ──→ │ D₁  4: 1          │ ──→ p
c ──→ │ D₂                │
c ──→ │ D₃                │
        ↑ s₀    ↑ s₁
        a       b
```
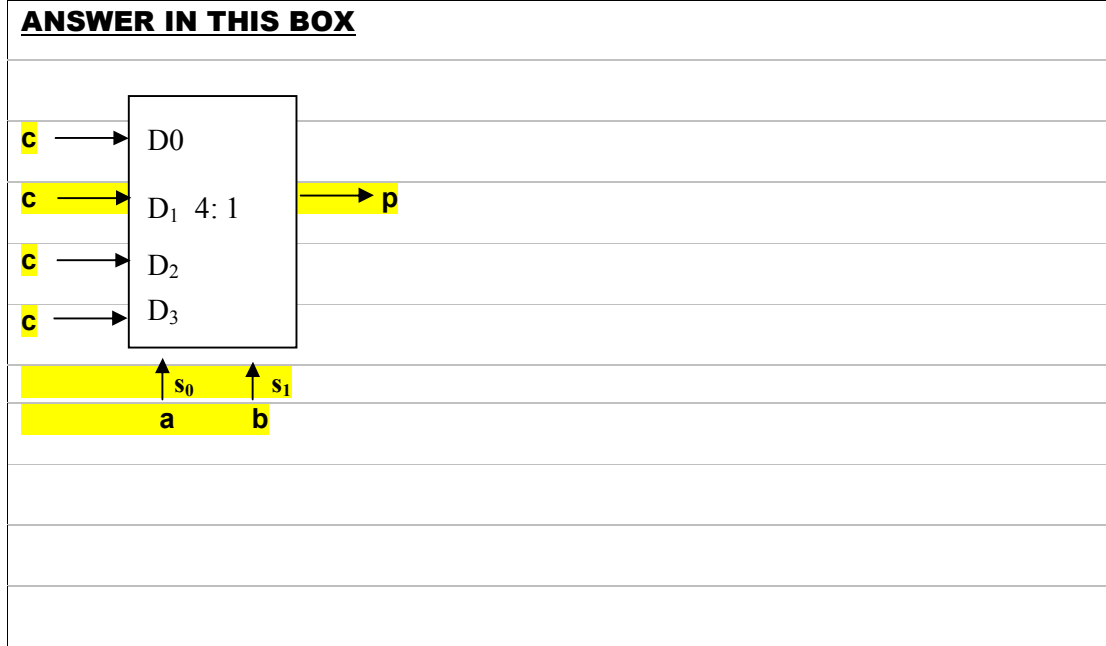
02) (a) State whether each of the following statements is true or false.

(15 Marks)

(i) A 1.2 GHZ processor with a cycles per instruction ratio (CPI) of 0.4 will be able to deliver a maximum throughput of 3000 MIPS.

ANSWER IN THIS BOX

True

(ii) A 64 bit word can be handled by a 32bit processor by assigning a single register or by assigning 4 consecutive (contiguous) memory locations to hold the value.

ANSWER IN THIS BOX

False

(iii) A register-memory (CISC) architecture is characterised by a small CPU register file and a micro programmed control unit.

ANSWER IN THIS BOX

True

(iv) Register-Register (RISC) instructions are of constant length and without complex addressing modes.

ANSWER IN THIS BOX

True

(v) In an instruction pipelined processor, the need for a register argument at the ID stage of a current instruction which has not yet been written to the register file is classified as a structural hazard.

ANSWER IN THIS BOX

False

(vi) Cache hit rates which are usually high around 0.8 may drop if there is frequent context switching by the operating system.

ANSWER IN THIS BOX

True

(vii) The objective of processor multithreading is to achieve reduced overhead in context switching in an instruction pipeline.

ANSWER IN THIS BOX

True

(viii) Shared memory multiprocessors are relatively difficult to program, but highly scalable.

ANSWER IN THIS BOX

False

(ix) There are many similarities between a fully associative hardware cache and a page table which is managed by the operating system: pages (or cache blocks) can be placed any where and page (or block) replacement is done by a LRU/LFU like algorithm.

ANSWER IN THIS BOX

True

(x) According to Amdahl's law, a task with 30% inherent parallelism running on a 16 processor cluster is likely to have a maximum speed-up of around 1.4 against a single processor.

ANSWER IN THIS BOX

True

(b) Write down the following stack instruction in terms of generic RISC instructions.

PUSH 100

where 0x100 is a memory location and the contents of memory location 0x100 is to be pushed on to the stack. Assume stack pointer is referred to by register R31.

(5 Marks)

ANSWER IN THIS BOX

PUSH 100

LD R_1 , 100 [R_0]

ST 0[R31], R_1

SUB I R31, R31, #4

(c) Consider the following RISC code fragment executing on a typical 5-stage RISC instruction pipeline with stages IF, ID, EX, MEM and WB. Identify all the data hazards and by the use of suitable techniques, show a stalling minimised space-time diagram for the code.

```
LD R1, 100[R2]
ADD R4, R1, R3
ST 100[R2], R4
ADDI R2, R2, #4
SUB R5, R5, R2
```

(5 Marks)

ANSWER IN THIS BOX

CD R1, 100[R2]:
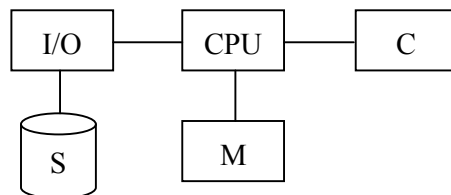
ADD R4, R1, R3:

ST 100[R2], R4:

ADDI R2, R2, #4:

SUB R5, R5, R2:

03) (a) The block diagram below shows the structure of a general purpose computer system emphasizing three levels of storage, namely, the cache (C), the main memory (M) and the secondary storage (S).

(i) Classify the three levels of storage in terms of their relative values of access time, cost per bit and size. Use the one of the terms, low (small), medium and high (large).

(2 Marks)

ANSWER IN THIS BOX

	access time	cost per bit	size
Cache	Low	high	small
M	medium	medium	medium
S	high	low	large

(ii) What is the order of access of the three levels by the CPU for an instruction or data fetch?

(2 Marks)

ANSWER IN THIS BOX

First – cache, second – M, finally - S

(iii) Assuming there is no secondary storage S, calculate the average access time as seen by the CPU for the two level memory system with a cache access time of 10 nsec, and a main memory access time of 100nsec, and a hit ratio of 0.95.

(2 Marks)

ANSWER IN THIS BOX

$t_{avg} = 0.95 \times 10 + (1 - 0.95) \times (10 + 100)$ nsec

(iv) It is possible that a data element can reside simultaneously on cache, on memory and on secondary storage. Suppose the element in cache is updated by the CPU. What possible 'future' problems can occur due to this update?

(2 Marks)

ANSWER IN THIS BOX

The data items on S and M are old values; if a page swap takes place, item the updated value

In C is not in M or S

(v)   Which memory levels are under the operating systems control? What is this mechanism called?

(2 Marks)

ANSWER IN THIS BOX

M & S are under OS; paging is the mechanism

(b)   The processor of a computer system generates a 32 bit virtual address which is translated into a 24 bit real (physical) address. The virtual memory is paged with 16kbyte pages and the cache is 256kbytes and fully associative with a block size (cache line) of 64 bytes. CPU word length is 32bits.

(i)   In the page table, how many bits of the virtual address are mapped to how many bits of the physical address?

(2 marks)

ANSWER IN THIS BOX

18 bits to 10 bits

(ii)   If a 32 bit instruction is located at 0x34AB70, what is the address (in hexadecimal) of the next immediate memory location thereafter?

(2 marks)

ANSWER IN THIS BOX

0×34AB74

(iii)   How many cache blocks are there in the cache?

(2 marks)

ANSWER IN THIS BOX

256 k bytes = 4 × 1024   =4096 cache blocks

64 bytes   64

(iv)   How many bits are there in the tag field of each cache block?

(3 marks)

ANSWER IN THIS BOX

tag field = (24 bit – 6 bits) = 18 bits

(c) (i)   One of the main objectives of computer architects has been to reduce the CPI of the processor thereby increasing the throughput (in MIPS or FLOPS). Given that simple instruction pipelining (ideally) attains a CPI of 1, how would instruction level parallelism help towards this goal?

(2 Marks)

ANSWER IN THIS BOX

1LP → CP1 < 1 by multiple issue pipelines

(ii) State two (2) ways in which a multithreaded processor would differ from a non multithreaded processor.

(2 Marks)

ANSWER IN THIS BOX

Multithreaded	non m/t
Low context switch overhead	high context switch overhead
Higher throughput	lower throughput
More efficient	less efficient

(iii) The emerging multi-core processors are in fact shared memory multiprocessors. Explain this fact.

(2 Marks)

ANSWER IN THIS BOX

Multi core means 2 or more cores sharing caches and may be main memory,

whereas multiprocessors usually share main memory only,

04) (a) Suggest suitable words/phrases for the blanks indicated.

(i) When a computer systems is started, a small piece of code known as the __A__ program locates the __B__, loads it into main memory and starts its execution.

(ii) When a C program invokes the printf() statement, the C library intercepts this call and invokes the operation system's __C__ system call.

(3 Marks)

ANSWER IN THIS BOX

A.

B.

C.

(b) (i) Consider the following code fragment.

```
int pid;

pid = fork();

if (pid<0) {
  fprintf(stderr, "Fork failed");
  return 1;
}
else if (pid==0) {
  printf("Child:\n");
  execlp("/bin/date","date",NULL);
}
else {
  printf("Parent:\n");
  wait(NULL);
  printf("Child complete");
}
```

(Note: The date commands prints the system date.)

Assuming a fork() system call was successful, state a possible output of the above code fragment:

(3 Marks)

ANSWER IN THIS BOX

(ii) Consider the following code fragment.

```
for (i=0;i<2;i++)
pthread_create(&tid, &attr, runner, i);
```

Assuming the code for *runner* is available, state the outcome of the above C code fragment:

(3 Marks)

ANSWER IN THIS BOX

(iii) Suggest suitable words/phrases for the blanks indicated.

Under non-preemptive scheduling, once the CPU has been assigned to a process, the Process uses the CPU until that process ......**A**.....or, the processor is to a ....**B**.... state.

(2 Marks)

ANSWER IN THIS BOX
A.
B.

(iv) State whether each of the following process scheduling algorithms result in starvation?

A. First come, first served   (Yes/No)

B. Shortest job first   (Yes/No)

C. Round robin   (Yes/No)

(3 Marks)

ANSWER IN THIS BOX
A.
B.
C.

(c)   Suggest suitable words/phrases for the blanks indicated.

(i)   A memory address generated by the CPU is commonly referred to as the **A**........ address where an address seen by the main memory unit is commonly referred to as the **B**........ address.

(2 marks)

ANSWER IN THIS BOX
A.
B.

(ii)   When allocating memory to a process, the first fit scheme allocates the first hole that is big enough. In the best fit scheme, the .....**A**..... hole that is big enough is allocated. In the worst fit scheme, the ....**B**.... hole is allocated.

(2 marks)

ANSWER IN THIS BOX
A.
B.

(iii)   Consider the following page reference string:

1,2,3,4,2

Assuming a physical memory that consists of three frames and that all frames are initially empty, how would above pages occupy the memory for an LRU (least recently used) replacement scheme? How many page faults would occur?

(4 marks)

ANSWER IN THIS BOX

13

(d)   Suggest suitable words/phrases for the blanks indicated.

(i)   The mount point is the location within the master file structure where another file system is to be ………**A**

(1 mark)

ANSWER IN THIS BOX
A.

(ii)   The basic hardware interrupt mechanism works as follows. The CPU has a pin called the interrupt-request line that the CPU senses after executing every ….**A**…. When the CPU detects that a controller has asserted a signal on the interrupt request line, the CPU performs a state ……**B**…… and jumps to interrupt handling routine residing at a fixed location in memory. The interrupt handler determines the cause of the interrupt, performs the necessary processing, performs a state restore and executes a return from interrupt instruction to return the CPU to the execution state prior to the interrupt.

(2 marks)

ANSWER IN THIS BOX
A.
B.

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