





## UNIVERSITY OF COLOMBO SCHOOL OF COMPUTING

# **DEGREE OF BACHELOR OF INFORMATION TECHNOLOGY (EXTERNAL)**

Academic Year 2018 – 3<sup>rd</sup> Year Examination – Semester 5

# IT5305: Computer Systems II Structured Question Paper

May 20th, 2018 (TWO HOURS)

To be completed by th	e candida	ate	
BIT Examination	Index 1	No:	

#### Important Instructions:

- The duration of the paper is **2 (two) hours**.
- The medium of instruction and questions is English.
- This paper has 5 questions and 11 pages.
- Answer all questions. Questions do not carry equal marks.
- Write your answers in English using the space provided in this question paper.
- Do not tear off any part of this answer book.
- Under no circumstances may this book, used or unused, be removed from the Examination Hall by a candidate.
- Note that questions appear on both sides of the paper.
   If a page is not printed, please inform the supervisor immediately.
- No calculators are allowed.

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Q	uesti	ons	Answ	rea (

Indicate by a cross (x), (e.g. X) the numbers of the questions answered.

To be completed by the candidate by marking a cross (x).	1	2	3	4	5	
Marks allocated for each question	22	12	26	28	12	
To be completed by the examiners:						

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(a)	A computer system has a CPU with a word length of 64 bits and a clock speed of
	1.5GHz. For a certain task, the measured average CPI (cycles per instruction) of the
	processor is 0.6. What is the MIPS rate of the processor?

1)

[6 marks]

ANSWER IN THIS BOX
Instructions /second = cycles/second x instructions/cycles
$= 1.5 \times 10^{9} \times 1/0.6$
= 2500 MIPS

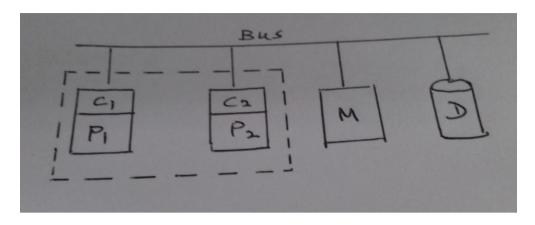
(b) Draw a block diagram of the typical five stage RISC (Load/Store) pipeline and identify the stages where memory access will occur by circling them.

[6 marks]

ANSWER IN THIS BOX
IF -> ID -> EX-> MEM-> WB
Memory access will happen in: IF and MEM stages

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(c) A computer system consisting of a dual core-CPU, main memory, cache, and secondary memory is shown in the block diagram.



(i) According to Flynn's classification of architectures, to which category does this system belong? Explain.

[3 marks]

ANSWER IN THIS BOX
MIMD.
This is a shared memory multiprocessor system. Hence MIMD.

(ii) Identify all the locations in the diagram, where a particular data object can reside as multiple copies. Use labels shown in the diagram.

[3 marks]

ANSWER IN THIS BOX
A particular data object copy can reside in both caches, main memory and the secondary storage at any given time.

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(iii) Compared to a uniprocessor system, state an additional complication that this system would cause with regards to cache and VM page updates?

[4 marks]

ANSWER IN THIS BOX
A cache update should be made consistent with the main memory using a suitable cache coherency protocol. VM paging is under operating systems and any 'dirty page' should be made consistent before being transferred to secondary memory.

Consider the following high level code fragmentwritten to find the maximum of an array of numbers. Here, the array of 4 byte integers a[0], a[1],..a[9] is stored starting at memory location 500 (that is a[0] at 500, a[1] at 504, a[2] at 508 and so on). The maximum of the array should be stored at a pre-defined location. Your code should start at memory location 2000.

2)

Assuming that the processor has only one internal register R, initialized to zero, write down the machine instruction sequence corresponding to a Register/Memory architecture. Your code should have not more than 8 instructions. The typical instruction set for a R/M architecture is given below the code fragment.

[12 marks]

```
max = a[0];
for i=1 to 9
  if (a[i] > max) then
     max = a[i];

LOAD [M] : R is loaded with the content of a memory
location or pointer M

STORE [M]: R is stored at a memory location or pointer M

ADD [M]: adds R to the memory content at M and saves in R

SUB [M]: subtracts R from memory content at M and saves
result in R and raises a flag if result is GT/LT/EQ/GE

MCOMPARE [M1], [M2]: compares memory contents at
```

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locations(or pointer) M1 and M2 and raises a flag if content at M1 GT/LT/EQ/GE to content at M2

COMPARE M1, M2: compares absolute memory addresses(or pointers) M1 and M2 and raises a flag if M1 is GT/LT/EQ/GE to M2

JUMP\_flag M: jumps to memory address(or pointer) M if flag is raised. (flags: GT - greater than 0; EQ - equal to zero; GE - greater than or equal to zero)

JUMP M: jumps to memory address(or pointer) M

SET M<target>: set memory location pointer M to "target" address

INC (or DEC) M: increment (or decrement) memory locationpointer M by 4

#### **ANSWER IN THIS BOX**

(This is not the <u>only</u> acceptable solution)

SET M, 500

Label\_1: LOAD [M]

STORE [1000]: maximum is here

Label 2: INC M

COMPARE M, 536: location of last element

JGT label\_3

LOAD [1000]

SUB [M]

JGT label\_1 : if a new max found

JUMP label\_2

Label\_3: EXIT

3)

In each of the sentences, underline or circle the more suitable term from within the brackets to fill in the blanks.

[26 marks]

- (i) Compared to CISC (Register + Memory) architectures, arithmetic-logic instructions in RISC (Register/Register) architectures never refer to ....(memory/register) operands.
- (ii) A large ..... (<u>register file</u>/cache) is a main feature of all RISC architectures, which are intended to hold ..... (<u>variables</u>/objects) in them for fast access.
- (iii) .....(<u>RISC</u>/CISC) architectures can be efficiently instruction pipelined since their microinstructions can be grouped into independent stages insuch a way that ......(delay/hazards) among them can be minimized.
- (iv) Instruction......(pipelining/super scaling) allows a processor to achieve a CPI (cycles per instruction) of ......(greater than one/equal to one).
- (v) For a process running under a multitasking kernel, a .....(<u>page fault</u>/cache miss) would cause ......................... (<u>acontext switch</u>/some stalling) with missing memory blocks being transferred from the hard disk to main memory via DMA I/O.
- (vi) A memory hierarchy usually works because code execution shows that there are frequently accessed instructions or data that can be kept in a fast but .....(small/large) memory over a slow but .....(smaller/bigger) memory, thereby making an overall performance improvement.
- (vii) A processor which has a word length of 64 bits would have a ...... (virtual/<u>physical</u>) memory width of .....(64/<u>8</u>) bits and a register width of ....(32/<u>64</u>) bits.
- (viii) A processorwhose 48 bit virtual address is translated into a 34 bit physical address, will have a main memory of .....  $(4/\underline{16})$  Gbytes.
- (ix) Assuming Amdhal's Law applies (speed  $up = n/\{f + n(1-f)\}\)$  where f parallelizable fraction of computation, n number of processors), a computing cluster which has 8 homogeneous (identical) nodes, each with 8 processors will provide an approximate speed up of.....(16/6) for a task that has an inherent parallelism of 95%.
- (x) In a multitasking operating system, a running process will be moved to the .....(blocked/ready to run) state when a .....(page fault/time slice expiry) occurs.
- (xi) A thread is a.....(<u>light weight</u>/heavy weight) process where multiple 'threads

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of execution' share the same code and ......(stack/data) but not ......(stack/data).

- (xii) When two or more processes access a shared variable or an object, mutual exclusion has to be imposed by a semaphore or a spin lock to ensure not more than ....(one/two) process(es) is/are inside the critical region at any given time and....(one/all) process(es) is/are given a fair chance to enter a critical region.
- (xiii) A hypervisor like Xen or VMWare enables multiple .....

  (homogeneous/<u>heterogeneous</u>) guest operating systems to be run on the same piece of processor hardware.
- (xiv) Graphics processing units (gpu) are now widely used not only for rendering graphics but also for scientific computing. The main reason they are used for scientific computing is that gpu's are mainly ....(MISD/<u>SIMD</u>) architectures that efficiently process ....(<u>vectors</u>/scalars).
  - (a) Four descriptions and four terms are shown in boxes below. Draw lines to connect each description to its corresponding term.

[6 marks]

Description Term A program in execution context switch Shifting the work of the CPU (central processing unit) from page table one process to another A memory reclamation method wherein memory contents not currently in use are process copied to a disk to make the memory available for other processes The data structure used by a virtual memory system in a computer operating system to store the swapping mapping between virtual and physical addresses

4)

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- (b) Briefly define the following terms as applied to operating system functionality:
  - (i) Demand paging

ANSWER IN THIS BOX	
Demand paging: pages required by processes are brought to memory on demand	

(ii) Disk fragmentation

## **ANSWER IN THIS BOX**

Disk defragmentation: Files are likely to be stored non-contiguously on disks. To increase performance, the operating system can move them to contiguous locations. This work is termed *disk defragmentation*.

(c) The process id is a unique number that identifies each of the running processes in an operating system. The system calls <code>getpid()</code> and <code>getppid()</code> can be used to get a processes' and its parent's process ids respectively. Assuming suitable values for relevant process ids, write down the outcome of the following code. Assume that the <code>fork()</code> call is successful.

[8 marks]

```
#include <stdio.h>
#include <unistd.h>
int main()
{
int id;
printf("Hello, World!\n");

id=fork();
if(id>0) {
/*parent process*/
    printf("This is the parent. [Process id: %d].\n",getpid());
}
else if(id==0)
{
/*child process*/
```

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```
printf("Child created. [Process id: %d].\n",getpid());
printf("Parent process id: %d.\n",getppid());
}
return 0;
}
```

ANSWER IN THIS BOX
Hello, World!
This is the parent. [Process id: 4337].
Child created. [Process id: 4338].
Parent process id: 4337
(Note: The process ids in student answers could be different.)

(d) Pthreads help one to easily create a multi-threaded application. Assume that you plan to use pthreads to compute the **largest** of the numbers in an array. Your program is to run on a quad-core computer. Following is a part of the C codethat could be used for the purpose. Assume the function *inputArray()* is available.

```
// Number of threads
#define THREADS 2

// Array
int A[1000];

// Array to store the maximum found by each thread
intmax_num[THREADS];

void main() {
  int max = 0;
  inti;
  pthread_t threads[THREADS];

// input array
inputArray();

// creating threads
for (i = 0; i < THREADS; i++)</pre>
```

```
pthread_create(&threads[i], NULL,
maximum, (void*) i );

// waiting for all threads to complete
for (i = 0; i < THREADS; i++)
pthread_join(threads[i], NULL);

// final work
for (i = 0; i < THREADS; i++) {
  if (max_num[i] > max)
  max = max_num[i];
}

printf("Maximum is : %d", max);
}
```

Answer the following questions based on the above code.

i. Explain the expected functionality of the *maximum* function in the pthread create call.

[6 marks]

## **ANSWER IN THIS BOX**

Each newly created thread is asked to run the maximum function. The parameter passed to it is i.

Then based on the passed i, each thread would find the maximum of some portion in the A array and put the found value in max\_num[i].

(When the threads are finished, the main thread would compare all max\_num[] elements to find the global maximum to print.)

ii. What would have been a better choice for the constant THREADS instead of the current 2? Why?

[4 marks]

# **ANSWER IN THIS BOX**

Four would have been a better choice as on a quad-core there are four cores and then each thread could run on one core.

(5 threads could also be accepted.)

(a) Give one (1) benefit of operating system	virtualization for portability testing of
applications.	[4:
ANSWER IN THIS BOX	
Portability testing is testing whether applicate environments. Operating system virtualizatinstead of searching and spending for many be done on the same physical machine with	ion helps in this regard, because with it different OS environments, the tesing of
(b) Why is <i>cloud computing</i> said to be cost earnd infrastructure?	
1 0	ffective for organisations requiring serv
and infrastructure?	oney on acquiring hardware and software, upgrading and maintaining them astainable alternative as then the burde
and infrastructure?  ANSWER IN THIS BOX  Instead of organizations spending a lot of n then spending the effort and money in prote computing provides a cheaper and a more sacquiring, protecting, upgrading and maintains.	oney on acquiring hardware and softw cting, upgrading and maintaining them ustainable alternative as then the burdeing the said resources fall on the services giving one practical example of each.
and infrastructure?  ANSWER IN THIS BOX  Instead of organizations spending a lot of n then spending the effort and money in protecomputing provides a cheaper and a more sacquiring, protecting, upgrading and maintaprovider.	oney on acquiring hardware and softw cting, upgrading and maintaining them astainable alternative as then the burde ing the said resources fall on the service

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Infrastructure as a service: Example for servers or storage available over the

via the Internet (for example, a database server)

Internet