UNIVERSITY OF COLOMBO, SRI LANKA

UNIVERSITY OF COLOMBO SCHOOL OF COMPUTING

DEGREE OF BACHELOR OF INFORMATION TECHNOLOGY (EXTERNAL)

Academic Year 2022 – 3rd Year Examination – Semester 5

IT5305: Computer Systems II

Structured Question Paper

March, 2022

TWO HOURS

To be completed by the candidate

BIT Examination Index No: .....

Important Instructions:

- The duration of the paper is **2 (two) hours**.
- The medium of instruction and questions is English.
- This paper has **4 questions** on **12 pages**.
- **Answer all questions.** Questions **do not** carry equal marks.
- **Write your answers** in English using the space provided **in this question paper**.
- Do not tear off any part of this answer book.
- Under no circumstances may this book, used or unused, be removed from the Examination Hall by a candidate.
- Note that questions appear on both sides of the paper.
  If a page is not printed, please inform the supervisor immediately.
- **No** calculators are allowed.

Questions Answered

Indicate by a cross (✖), (e.g. [✖]) the numbers of the questions answered.

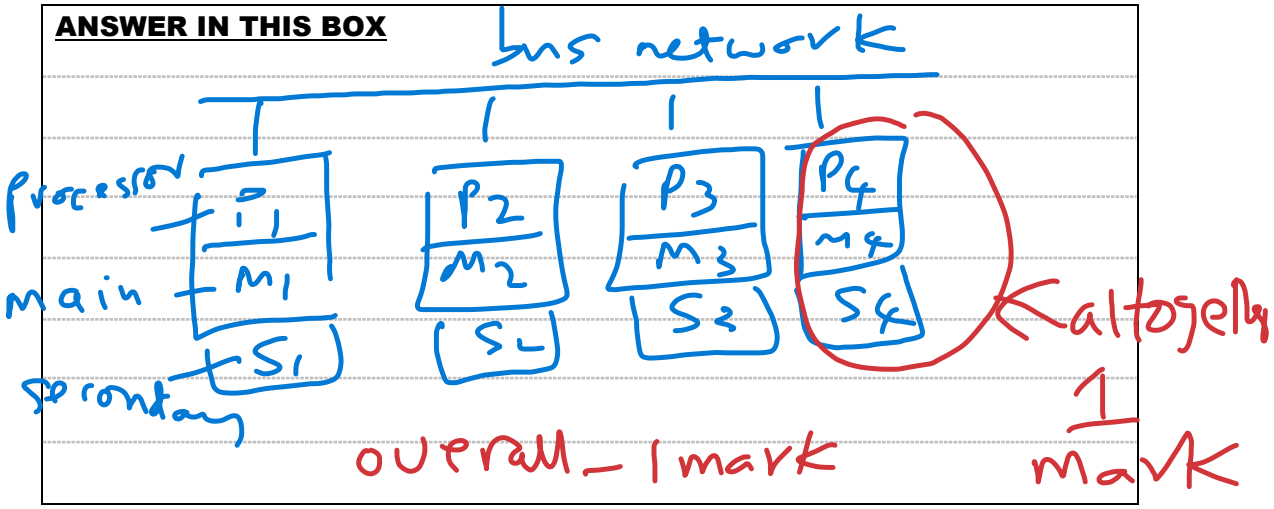
To be completed by the candidate by marking a cross (✖).	1	2	3	4	
Marks allocated for each question	20	10	30	40	
To be completed by the examiners:					

Index No …….

1) (a) In the Flynn's classification the MIMD category can refer to both distributed memory multiprocessors (computing cluster) and shared memory multiprocessors (multi-core architectures).

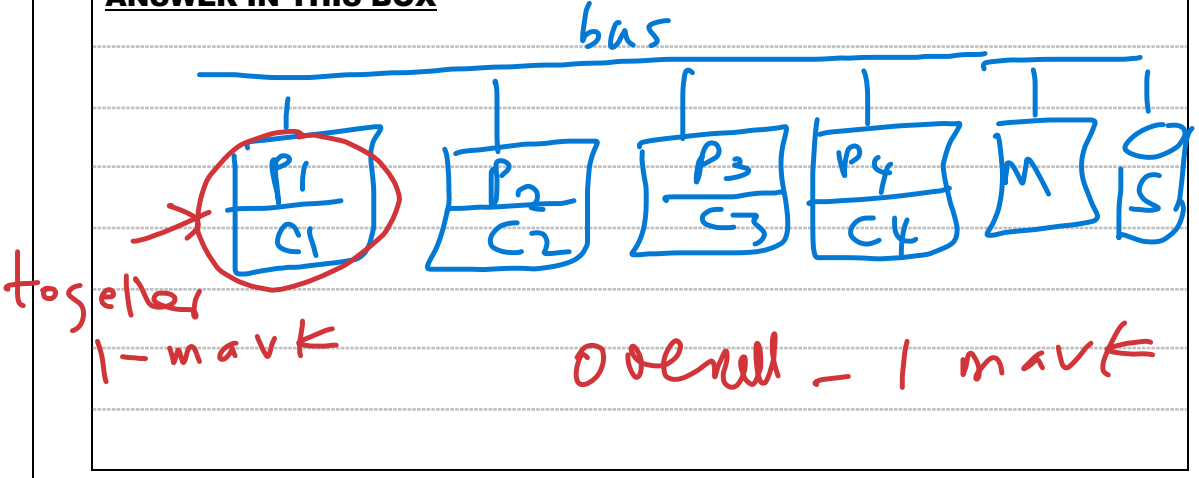
(i) Draw the block diagram of a computing cluster having 4 processing nodes, each with its own main and secondary memory, connected over a bus type of network. **[2 marks]**

ANSWER IN THIS BOX



(ii) Draw the block diagram of a quad core processor, each core having its own cache, but both cores sharing the main and the secondary memory. **[2 marks]**

ANSWER IN THIS BOX



(iii) A processor core has a word length of 64 bits and a clock speed of 1.5GHz. For a certain task, the measured average CPI (cycles per instruction) of the

processor is 0.8. What is the MIPS rate of the processor?

[2 marks]

ANSWER IN THIS BOX

1 mark → [Instructions/second = Cycles/sec ÷ CPI]

∴ IPS = $1.5 \times 10^9 / 0.8$

1 mark → MIPS ≃ 2000

(b) In a stack processor architecture two of the key operations are *PUSH* and *POP*. PUSH moves the content of a main memory location to the top of the stack. POP removes the contents of the top of stack and moves it to a main memory location. Suppose we need to emulate a stack instruction using a RISC (Load/Store) instructions. Let the stack pointer which typically points to the non-empty contents of the top of stack, be given by the register R31 in the RISC architecture. Write down a piece of RISC code (three instructions to be precise) that will emulate the stack instruction *PUSH [M]* where [M] indicates the contents of main memory location M. Assume R0=0.

[4 marks]

ANSWER IN THIS BOX

Emulating PUSH [M]:

(1) — LD R_1, M[R_0] : $R_1 \leftarrow$ Memory($M + R_0$)

(1) — ST 0[R_{31}], R_1 : Memory($0 + R_{31}$) $\leftarrow R_1$

(1) — SUB R_{31}, R_{31}, #4 : $R_{31} \leftarrow R_{31} - 4$ assuming a 4 byte word

overall — 1 mark

(c) Consider the following RISC code fragment. Assume R0=0.

```
        ADD R1, R0, #40 : add 40 to R0 and save it in
                          R1
loop:   LD R2, 100[R1] : load contents of memory
                         location(100+R1) to R2
        MUL R3,R2,R1: multiply R2 and R1 and save it in
                      R3
        ST 100[R1], R3 : save R3 at memory location
                         (100+R1)
        SUB R1, R1, #4
        BGT R1, loop: if R1 >0 then branch off to loop
```

(i) If a memory referencing instruction takes 3 clock cycles, an arithmetic instruction takes 1 clock cycle and a branch takes 2 clock cycles, what is the average CPI for the above piece of code if the code is executed on a non-pipelined processor?

[3 marks]

ANSWER IN THIS BOX

mem. ref instructions — 2 nos
arithmetic " — 3 nos
branch " — 1 no

∴ CPI = (2×3 + 3×1 + 1×2)/6
= 11/6 ≈ 1.8 cycles/instr

1 mark

(ii) How many rounds would the loop run? **[2 marks]**

ANSWER IN THIS BOX

rounds ≈ 40/4 = 10 — 1

#40 ← 40/4 → #4

(iii) At the end of execution of the loop, what would be the contents of memory location 100?

[2 marks]

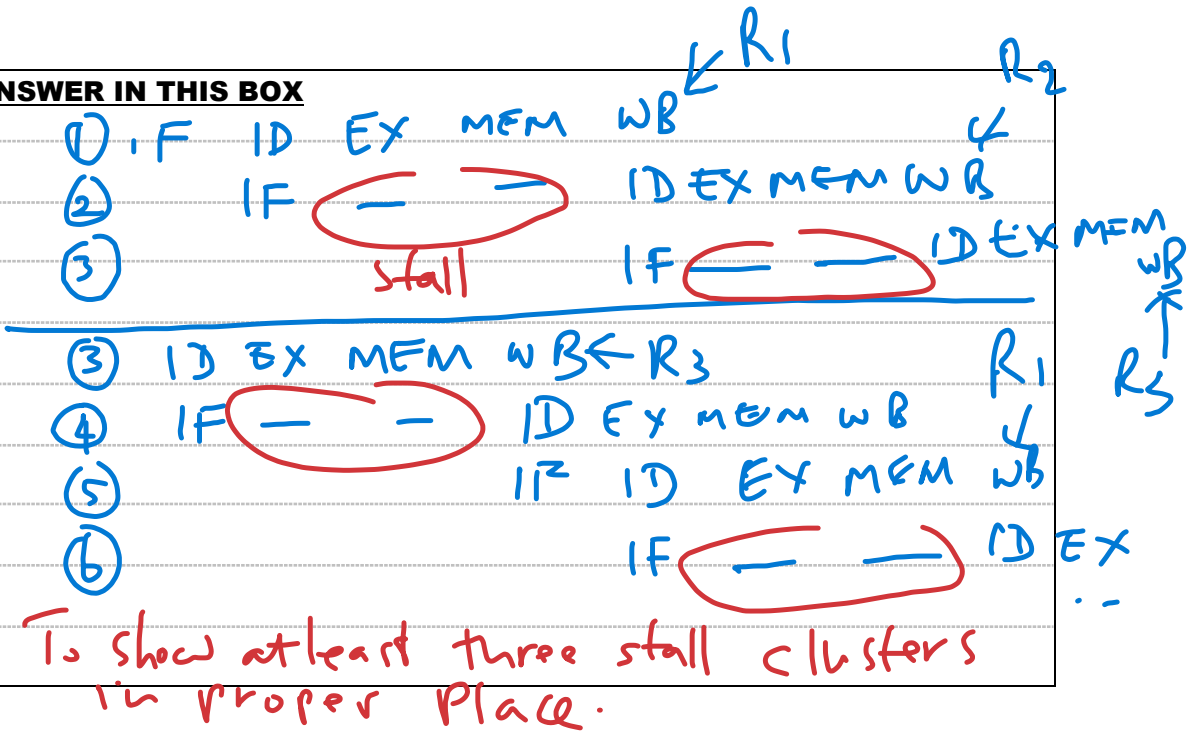
ANSWER IN THIS BOX

Remains unchanged.

Since, when $R_1=0$, it exits the loop.

(iv) If the above RISC code is to be executed on a 5 stage RISC instruction pipeline, draw a space-time diagram to show the code with all data hazards resolved using stalls only. **[3 marks]**

ANSWER IN THIS BOX



2) An array *a[1..100]* of 4 byte numbers consisting of positive integers and zeros is stored starting at memory location 1000. The following high level language code snippet counts the number of positive integers in the array and store the total count at memory

location 3000. Write down the machine instruction sequence for a Register/Memory architecture. Content of memory location 3000 is initialised to 0, the content of memory location 2000 initialised to 1 and the processor has only one internal register R, initialized to zero. Your code should have a minimum number of instructions. The typical instruction set for a R/M architecture is given below. Your code should start at memory location 5000.

[8 marks]

```
for i=1 to 100

    if (a[i]>0)then b=b+1;
```

LOAD [M] : [R is loaded the content of memory location pointed to by M (or an absolute address) and raises a flag if R is GT/LT/EQ/GE to zero]

STORE [M]: [R is stored at memory location pointed to by M (or an absolute address)]

ADD [M]: [adds R to memory content at location pointed to by M (or an absolute address), and saves in R and raises a flag if result is GT/LT/EQ/GE to zero]

SUB [M]: [subtracts R from memory content at location M (or an absolute address) and saves result in R and raises a flag if result is GT/LT/EQ/GE to zero]

COMPARE [M1], [M2]: [compares memory contents at locations pointed to by M1 (or an address) and M2 (or an address) and raises a flag if M1 GT/LT/EQ/GE to M2]

COMPARE M1, M2: [compares absolute memory addresses or pointers M1 and M2 and raises a flag if M1 GT/LT/EQ/GE to M2]

JUMP_flag M: [jumps to memory address (absolute address) or that pointed to by M if flag is raised] (flags: GT - greater than 0; EQ – equal to zero; LT – less than zero)

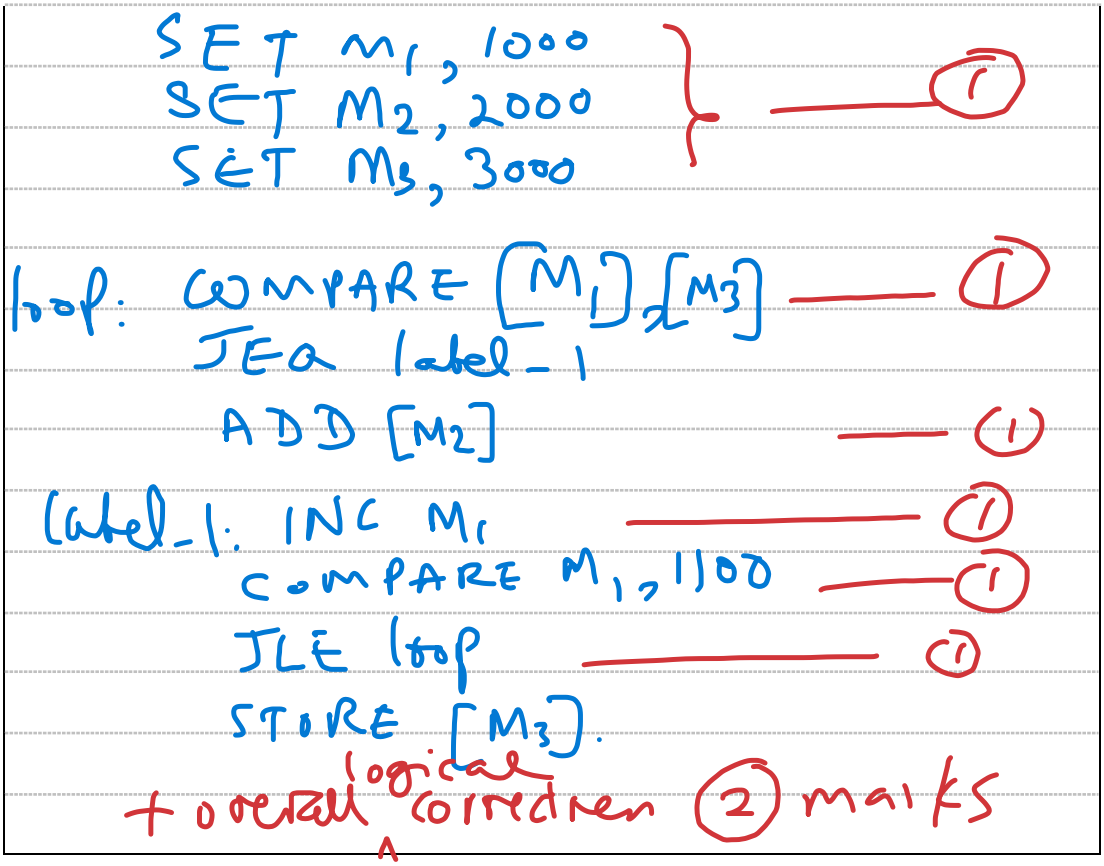
JUMP M: [jumps to memory address (absolute address) or that pointed to by M]

SET M, <target>: set memory location pointer M to "target" address

INC (or DEC) M: increment (or decrement) memory location pointer M (or absolute address) by 4

Note: Pointer M can represent any number of memory pointers M1, M2, M3 etc.,

ANSWER IN THIS BOX



3)

In each of the following sentences, underline or circle the more applicable term from within the brackets to fill in the blanks. **[30 marks]**

1 mark each selection

(i) In RISC or Load-Store architectures, all instructions are of …….(variable/constant) length compared to CISC or Register-Memory architectures, whose instructions are of ……..(variable/constant) length, in order that in RISC the program counter can be auto incremented…..(after/prior to) decoding of the instruction.

(ii) ……..(CISC/RISC) architectural style would be more efficient than a ……..(CISC/RISC) style in a situation where frequent context switching is dominant as is the case in a virtual machine environment.

(iii) In order to achieve an ideal CPI [cycles per instruction] of …… (1.0, <1.0) simple instruction pipelining requires that each stage carries out its micro-instructions within a single clock cycle by both restricting its arithmetic/logic instructions be fully ……. (register based/memory referenced) and by

having ……. (registers/caches) at memory access stages.

(iv) In a simple RISC instruction pipeline, a read-after-write (RAW) data hazard is caused by the …….(source/destination) register operand being not stable at the time of execution of an instruction.

(v) A RAW hazard can be eliminated by simply …… (stalling/halting) the instruction until the required operand is ready or, by using additional hardware for ……. (duplicating resources/arithmetic by pass).

(vi) Two other events that could disrupt the flow of an instruction pipeline are arithmetic exceptions, e.g., divide by zero, or context switching in a multitasking environment. An arithmetic exception could only occur in the ……..(EX/MEM) stage, whereas a context switch due to a page fault can happen in ……(ID or MEM/ID or WB) stages.

(vii) ……..(Multithreading/Superscaling) allows an instruction pipeline to overcome stalls due to frequent context switching.

(viii) The principle of *locality of reference*, can be seen to be working in the physical memory hierarchy of a computer system through its operation of …… (paging/caching) in the management of the virtual memory.

(ix) The memory hierarchy of a computer systems spans from the lowest access time ……. (caches/registers) which has the …….. (lowest/highest) cost per bit to highest access time …… (main memory/secondary storage) which has the …….. (lowest/highest) cost per bit.

(x) A computer system which has a single core CPU with 256 nos. 32 bit general purpose registers, a 48 bit virtual address, a 4GB of RAM and an internal cache of 512kbytes, where the virtual memory (VM) is paged with 4Mbyte pages and with a system disk size of 100Gbytes will have a virtual memory of ……. (256 Gbytes/256 TBytes) and with the main memory having ……(1024/512) pages, and an overall register memory size of …….. (512/1024) bytes.

(xi) In specifying the MIPS rate of a processor it should be noted that it is dependent on the type of code it executes as the …… (cycles per second/ cycles per instruction) parameter can change from code to code.

(xii) According to Amdhal's Law (*speed up = n/{f + n(1-f)} where f – parallelizable fraction of computation, n – number of processors)*, a computing cluster which has 8 homogeneous (identical) nodes will provide an approximate theoretical maximum speed up of……. (1.8/2.0) over its serial computation, for a task that has an inherent parallelism of 50%.

(xiii) In a multitasking operating system, a blocked process will be moved to the …….(running/ready to run) state when the ……..(IO activity has completed/time slice has expired).

(xiv) The mutual exclusion problem applies to a scenario in which two or more processes that compete to read from or write to a memory location simultaneously are controlled in such a way that *safety,* which means ……..(all processes are given a fair chance to enter the critical region /at any time, only one process can be inside critical region) is satisfied.

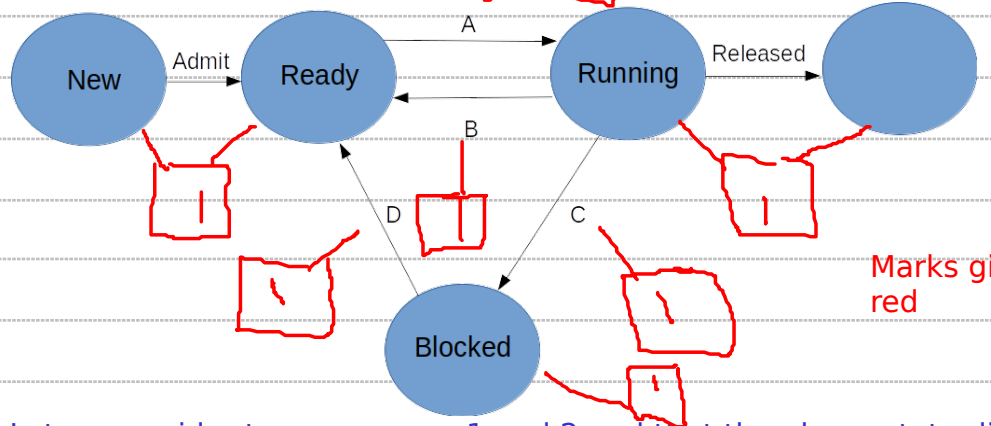
(xv) Graphics processing units (gpu) are now widely used not only for rendering graphics but also for scientific computing. The main reason they are very efficient for scientific computing is that gpu's are primarily ……(improved SISD / a combined SIMD and MIMD) architecture that can exploit ……..(single threaded/multithreaded) applications which operate on …(vectors/scalars).

4) (a) During the lifetime of a process, the process status will change a number of times.

Its status at any point in time is referred to as a *state*. Considering **two** processes that are running on a single processor computer, describe using a diagram, the process states and the transitions between states.

[7 marks]

ANSWER IN THIS BOX



Marks given in red

Let us consider two processes 1 and 2 and that the above state diagram indicates the states and transitions of Process 1.

Once admitted, the state of the process is "Ready" which means it is ready to run on the processor. When the OS selects Process 1 to run, it moves to the "Running" state (indicated by Transition A). From "Running" state it can move back to "Ready" state (Transition B) due to OS deciding that it has run enough on the processor and should give the chance for Process 2 to run. Or else if it has to do some input/output then OS would put the process into "Blocked" state (Transition C). Once the i/o is done, the process is put back into the "Ready" state (Transition D).

(b) Define *pre-emptive process scheduling*. **[4 marks]**

ANSWER IN THIS BOX

Here, the CPU is given to each process for a limited time period only. When that time period has passed and if the process has still not finished with its work then that process is moved to the "Ready" state and the CPU is given to another "Ready" process in order for it to run for a time period. The first process will be given time again later for another period and so on.

(c) Most computers today are equipped with multiple processors. Explain how these processors can be utilized for example by the use of pthreads.

[7 marks]

ANSWER IN THIS BOX

We can create multiple threads through the use of the pthread_create function.

We can specify a work function for each thread to run via the third argument in the above pthread_create function. Any parameter for the work function can also be passed.

Once such threads are created, the OS could run them on different processors of the computer thus effectively utilizing them.

Thus complicated tasks that could execute in parallel can be run through the use of ptheads speeding things up as they will run on multiple processors.

(d) What is meant by a *page table?* **[5 marks]**

ANSWER IN THIS BOX

A page table is a data structure used by the operating system per each process to keep the mapping between virtual and physical memory addresses of that process.

(e) Assume that the physical memory of a computer system contains three frames that are initially empty. Now consider the following page reference string made by the memory management system:

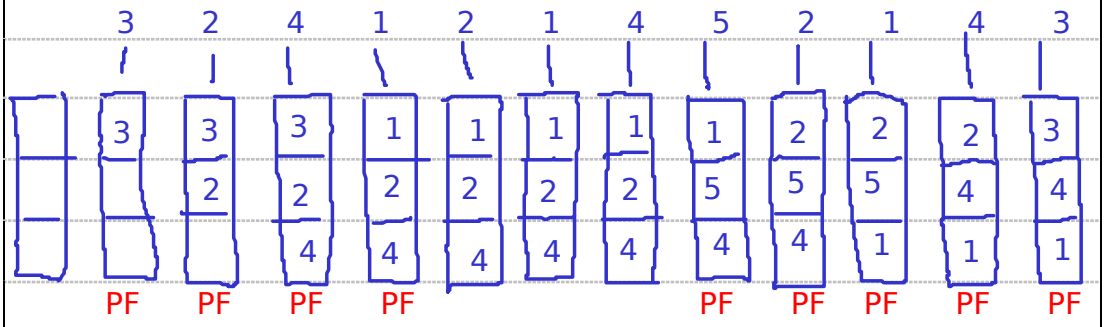
3, 2, 4, 1, 2, 1, 4, 5, 2, 1, 4, 3

Draw the frames showing the page numbers when the above string is referenced with a *least recently used* page replacement policy. Indicate any page faults.

[7 marks]

ANSWER IN THIS BOX

Correctly drawn frames = 5 marks
Page fault indications = 2 marks



Total page faults = 9

(f) What is meant by "Software-as-a-Service (SaaS)? Explain with respect to its definition, benefits, types of software and other important details.

[10 marks]

ANSWER IN THIS BOX

Definition: A method of software delivery in which software is accessed online rather than bought and installed on individual computers.

Benefits: 1 Frees users from complex software installations
2 Reduces time spent on installing software
3. Reduced initial costs due to usually comparatively low licensing fees
4. Reduced maintenance costs as it is provider's burden
5. Easier to scale up
6. No need to buy special servers to install software
7. No need to worry about upgrades as the provider does it

Types of software: There is a very wide variety ranging from office applications, collaboration tools, database tools, business applications, machine learning tools, robotics, security, email etc.

Popular examples: Microsoft Office 365, Google Docs, Gmail, Google Drive, Forms etc.

Other information: It is one cloud computing category. i.e., the software is installed in the cloud.

Many organizations are moving to SasS usage.

Index No …….

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