UNIVERSITY OF COLOMBO, SRI LANKA

UNIVERSITY OF COLOMBO SCHOOL OF COMPUTING

DEGREE OF BACHELOR OF INFORMATION TECHNOLOGY (EXTERNAL)

Academic Year 2022 – 3rd Year Examination – Semester 5

IT5305 (R): Computer Systems II

Structured Question Paper

January 2023.
(TWO HOURS)

To be completed by the candidate

BIT Examination Index No: .....

Important Instructions:

- The duration of the paper is **2 (two) hours**.
- The medium of instruction and questions is English.
- This paper has **4 questions** on **11 pages**.
- **Answer all questions.** Questions **do not** carry equal marks.
- **Write your answers** in English using the space provided **in this question paper**.
- Do not tear off any part of this answer book.
- Under no circumstances may this book, used or unused, be removed from the Examination Hall by a candidate.
- Note that questions appear on both sides of the paper.
  If a page is not printed, please inform the supervisor immediately.
- **Non** programmable calculators are allowed.

Questions Answered

Indicate by a cross (×), (e.g. [X]) the numbers of the questions answered.

To be completed by the candidate by marking a cross (×).	1	2	3	4	
Marks allocated for each question	20	10	30	40	
To be completed by the examiners:					

1) (a) A computer system has a CPU which has 256 nos. 64 bit general purpose registers. It has a 48 bit virtual addresses. The system has 2GB of RAM. Virtual memory (VM) is paged with 4Mbyte pages and the external cache is 1Mbytes. The system disk size is 100Gbytes.

(i) What is the total size of register memory in bytes? **[2 marks]**

ANSWER IN THIS BOX

$= \frac{64\ bit \times 256}{8} = 2048\ byte$

(ii) What fraction of VM pages can be there in the physical memory at any given time? **[3 marks]**

ANSWER IN THIS BOX

$= \frac{2 \times 10^9}{2^{48}} = \frac{2 \times 2^{30}}{2^{48}} = \left(\frac{1}{2^{17}}\right)$

(iii) How many CPU words can occupy a page block? **[2 marks]**

ANSWER IN THIS BOX

$= \frac{4 \times 10^6\ bytes}{8\ bytes} = \frac{4 \times 2^{20}}{8} = 2^{19}$

(b) Consider the following three RISC instructions in a thread that is running on a processor.

(1) `LD R1, 200[R0] : load content of memory location (200+R0) to register R1`

(2) `SUB R3,R1,R2: subtract R2 from R1 and save on R3`

(3) `ST 300[R0], R3: store R3 contents at memory location (300+R0)`

(i) If a memory referencing instruction takes 3 clock cycles and an arithmetic instruction takes 1 clock cycle, what is the average CPI (cycles per instruction) for the above piece of code if the code is executed on a non-pipelined processor? **[2 marks]**

ANSWER IN THIS BOX

$= (3+1+3) \div 3$

$= 2.3$

(ii) If R0=0, and R2=20 and the content of memory location 200 is 40, what would be the content of memory location 300 after the execution of the code?

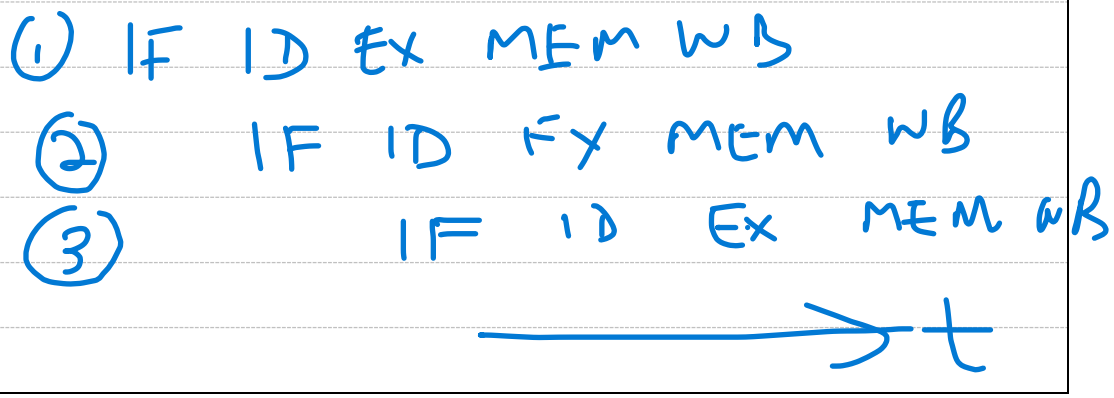
[2 marks]

ANSWER IN THIS BOX

20

(iii) Suppose now, the above code is to be executed on a typical 5 stage RISC pipeline with stages IF, ID, EX, MEM and WB. Draw a space-time diagram to show the overlapped execution of the three instructions. **[3 marks]**

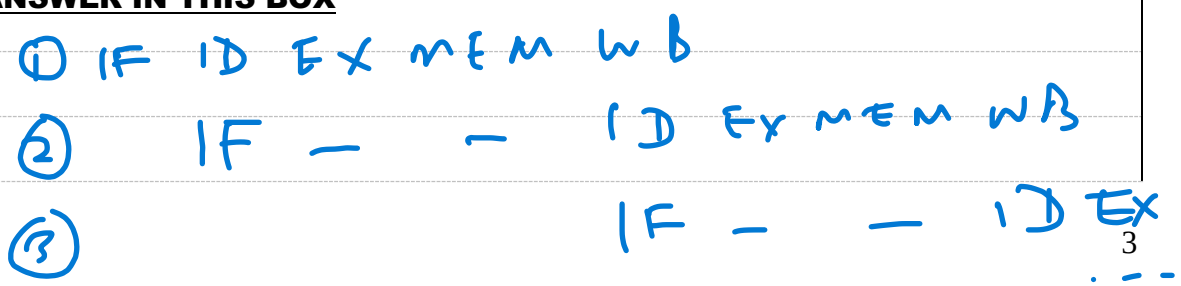
ANSWER IN THIS BOX



(iv) Redraw the space-time diagram for the code with stalls introduced to rectify all data hazards. Assume there are no arithmetic bypass mechanisms.

[3 marks]

ANSWER IN THIS BOX



(v) If each stage takes only 1 clock cycle, compare the average CPI (cycles per instruction) for the code when executing over the ideal pipelined case of (iii) above, with that of (iv) above.

[3 marks]

ANSWER IN THIS BOX

ideal (iii) case → CPI = 1.0 (except for 1st instruction)
case (iv) → CPI = (3+4)/3 = 2.3

2) An array *a[1..100]* of 4 byte numbers consisting of positive integers and zeros is stored starting at memory location 1000. The following high level language code snippet counts the number of zeroes in the array and stores the total count at memory location 3000. Write down the machine instruction sequence for a Register/Memory architecture. Content of memory location 3000 is initialised to 0, the content of memory location 2000 initialised to 1 and the processor has only one internal register R, initialized to zero. Your code should have a minimum number of instructions. The typical instruction set for a R/M architecture is given below.

```
for i=1 to 100

    if (a[i]==0) then b=b+1;
```

[10 marks]

LOAD [M] : [R is loaded the content of memory location pointed to by M (or an absolute address)]

STORE [M]: [R is stored at memory location pointed to by M (or an absolute address)]

ADD [M]: [adds R to memory content at location pointed to by M (or an absolute address), and saves in R]

SUB [M]: [subtracts R from memory content at location M (or an absolute address) and saves result in R and raises a flag if result is GT/LT/EQ/GE]

MCOMPARE [M1], [M2]: [compares memory contents at locations pointed to by M1 (or an address) and M2 (or an address) and raises a flag if M1 GT/LT/EQ/GE to M2]

COMPARE M1, M2: [compares absolute memory addresses or pointers M1 and M2 and raises a flag if M1 GT/LT/EQ/GE to M2]

JUMP_flag M (or Label): [jumps to memory address (absolute address) or that pointed to by M or Label, if flag is raised] (flags: GT - greater than 0; EQ – equal to zero; GE – greater than or equal to zero)

JUMP M (or Label): [jumps to memory address (absolute address) or that pointed to by M or a Label]

SET M <target>: set memory location pointer M to "target" address

INC (or DEC) M: increment (or decrement) memory location pointer M (or absolute address) by 4

Note: Pointer **M** can be used to identify any number of memory pointers **M1, M2, M3** etc.,

ANSWER IN THIS BOX

```
SET M1, 1000
label_1: MCOMPARE [M1], [3000]
         JUMP NE Label_2
         ADD [2000]
label_2: INC M1
         COMPARE M1, 1400
         JUMP LT label_1
         STORE [3000]
         exit
```

3) In each of the following sentences, underline or circle the more suitable term from within the brackets to fill in the blanks. **[30 marks]**

(i) In RISC Instruction Set Architectures, all instructions are of …….(variable/constant) length compared to CISC, whose instructions are of ….(variable/constant) length, in order that RISC CPU program counter can auto advance …..(after/prior to) decoding of the instruction.

(ii) ……(RISC/CISC) architectures can be efficiently instruction pipelined since their machine instructions can be represented by independent blocks of microinstructions which can be executed on replicated hardware.

(iii) In a simple RISC instruction pipeline, a read-after-write (RAW) data hazard could occur if the ……..(source/destination) register operand for an arithmetic instruction or a store instruction is not ready due to the register being a ……(source/destination) operand of a previous instruction, and has to be resolved either by stalling or arithmetic by-pass.

(iv) Instruction……..(pipelining/super scaling) allows a processor to achieve a CPI (cycles per instruction) of ……..(greater than one/equal to one).

(v) For a process running under a multitasking kernel, a …..(page fault/cache miss) for a ….. (instruction fetch/arithmetic operation) would cause ……. (a context switch/stalling of instructions).

(vi) A computer memory hierarchy usually works because it upholds the principle of *locality of reference*, which says that a reference to a memory location will most likely be referenced …….(again/frequently) and a ……..(nearby/furthest) location be also likely to be referenced.

(vii) The memory hierarchy of a computer systems spans from the lowest access time ……. (caches/registers) which has the …….. (lowest/highest) cost

per bit to the highest access time …… (main memory/secondary storage) which has the …….. (lowest/highest) cost per bit.

(viii) A processor which has a clock rate of 1.8GHz and a CPI of 0.9 for a certain type of task, would have a MIPS rate of …….(2000/200).

(ix) In a multitasking operating system, a blocked process will be moved to the …..(running/ready to run) state when the …..(IO activity has completed/time slice has expired).

(x) In demand paging as applied to…….(virtual memory/physical memory), the most frequently accessed set of page blocks by …… (a thread/all threads) is kept in a table, and this functionality can be equally if not better performed by a …… (page table/translation look aside buffer).

(xi) Any acceptable solution to the mutual exclusion problem, that is multiple process access resolution to ……(shared memory/distributed memory) needs to satisfy two conditions, which is *liveness*, ……..(all processes are given a fair chance to enter critical region/at any time, only one process can be inside critical region), and *safety*, ……..(all processes are given a fair chance to enter the critical region/at any time, only one process can be inside the critical region).

(xii) Operating systems virtualization allows the use of multiple ……(hardware/virtual machines) on top of a ……. (hypervisor/kernel) itself running on a piece of processor hardware.

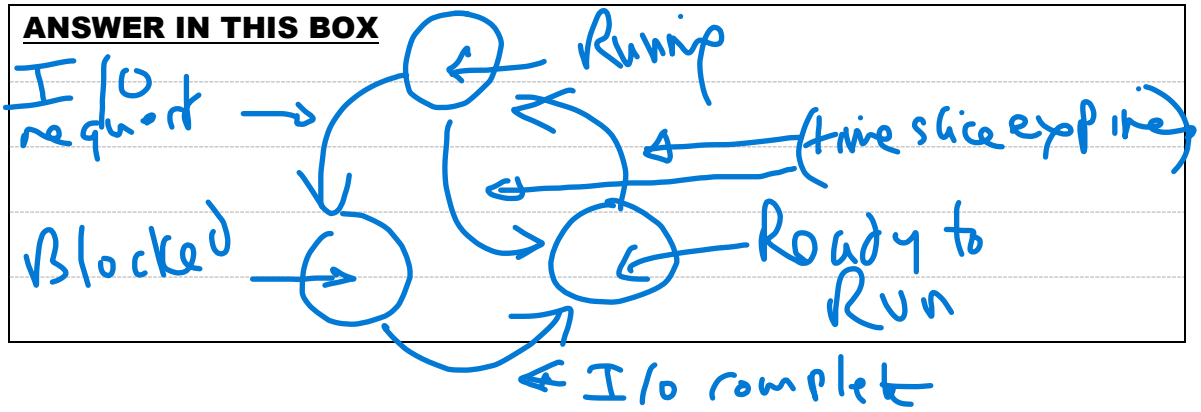
(xiii) Graphics processing units (gpu) are now widely used not only for rendering graphics but also for scientific computing. The main reason they are efficient for scientific computing is that gpu's are primarily….(MISD/SIMD) architectures that are designed to process ….(vectors/scalars).

4) (a)

(i) A multitasking OS would continuously context switch between the processes such that each of them would get a fair share of the resources of the hardware platform on which it runs. Draw a state transition system to show a typical context switch. It should clearly show the three states: *running, ready to run* and *blocked*, as well as state transitions and associated events that cause the transitions.

[8 marks]

ANSWER IN THIS BOX



(ii) The *context* of a process is identified by three components: *user, register and system*. Given the entities, PCB (process control block), CPU register set, executable code, data and stack, associate each of these entities with the corresponding three components of the context.

[4 marks]

ANSWER IN THIS BOX

User context = code + data + stack per process

register context = CPU register set values

system context = PCB entries

(b) The process id is a unique number that identifies each of the running processes in an operating system. The system calls *getpid()* and *getppid()* can be used to get a processes' and its parent's process ids respectively. Assuming suitable values for relevant process ids, write down the outcome of the following code. Assume that the *fork()* call is successful. **[8 marks]**

```
#include <stdio.h>
#include <unistd.h>
int main()
  {
    int id;
    printf("Hello, World!\n");

    id=fork();
    if(id>0) {
          /*parent process*/
     printf("This is the parent. [Process id:
     %d].\n",getpid());
```

```
    }
    else if(id==0)
                {
 /*child process*/
 printf("Child created. [Process id: %d].\n",getpid());
 printf("Parent process id: %d.\n",getppid());
    }
 return 0;
}
```

"**ANSWER IN THIS BOX**

After printing of 'hello world,' depending on synchronisation of child & parent threads, it will print (a) followed by (b) or vice versa:

(a) This is Parent [process id: 10]

(b) [Child created [process id: 0]
[Parent process id: 10

← Example only

(c) Indicate whether each of the statements below is true (**T**) or false (**F**). If false, justify.

[9 marks]

(i) A typical hard-disk is made up of *sectors*, which are divided into *tracks.*

ANSWER IN THIS BOX

F ; should be vice-versa

(ii) Booting begins by running code that is resident in a computer system's ROM.

ANSWER IN THIS BOX

T

(iii) The Windows system places its boot code in the first sector on the hard-disk, which it terms the *master boot record*.

ANSWER IN THIS BOX T

(iv) A device communicates with a computer via a *port.*

ANSWER IN THIS BOX

(v) When devices share a common set of wires for communication, the connection is called a *bus*.

ANSWER IN THIS BOX

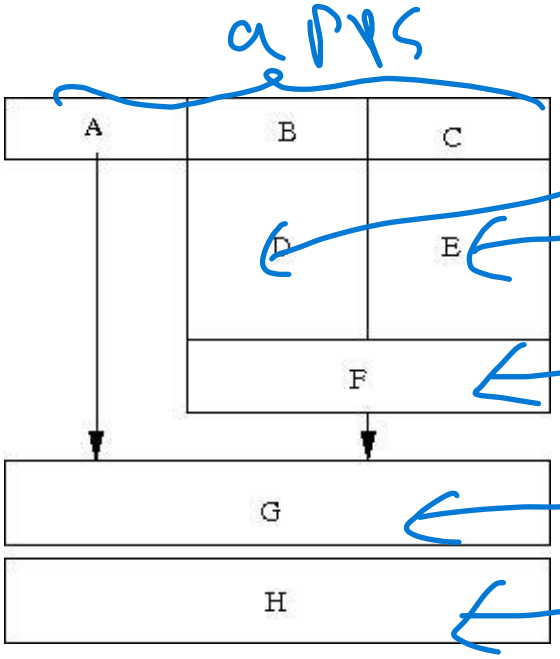
(vi) Physical disks may be segmented into partitions to control media use and to allow multiple, possibly varying, file systems on a single spindle.

ANSWER IN THIS BOX

(d)

(i) A **VMware Workstation** architecture with *Linux* as the host operating system is shown in the diagram below. Indicate what is meant by the labels A to H choosing from the given list. Note that an item may be used for more than one label.

[8 marks]



List: {application, hardware, Linux, Virtualization layer, Windows XP, Windows 10***}***

"**ANSWER IN THIS BOX**

(ii) State **one (1)** advantage in the above setup compared to a single OS running on a host. **[3 marks]**

"**ANSWER IN THIS BOX**

① multi environment on same h/w
② Application isolation

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