UNIVERSITY OF COLOMBO, SRI LANKA

UNIVERSITY OF COLOMBO SCHOOL OF COMPUTING

DEGREE OF BACHELOR OF INFORMATION TECHNOLOGY (EXTERNAL)
Academic Year 2012/2013 – 3rd Year Examination – Semester 5

IT5304: Computer Systems II

Structured Question Paper
17th March, 2013
(TWO HOURS)

To be completed by the candidate

BIT Examination Index No: ....

Important Instructions:

- The duration of the paper is **2 (Two) hours**.
- The medium of instruction and questions is English.
- This paper has **4 questions** and **15 pages**.
- **Answer all 4 questions**. (All questions **do not** carry equal marks).
- **Write your answers** in English using the space provided **in this question paper**.
- Do not tear off any part of this answer book.
- Under no circumstances may this book, used or unused, be removed from the Examination Hall by a candidate.
- Note that questions appear on both sides of the paper.
  If a page is not printed, please inform the supervisor immediately.
- **Non-programmable Calculators may be used.**

Questions Answered

Indicate by a cross (×), (e.g. ☒) the numbers of the questions answered.

	Question numbers				
To be completed by the candidate by marking a cross (×).	1	2	3	4	
To be completed by the examiners:					

Index No: ………………...

1) (a) Write down the truth table for a 1 bit full adder with inputs a, b and C_{in}, and outputs Sum and C_{out}, where C_{in} is carry in and C_{out} is carry out.

(4 marks)

ANSWER IN THIS BOX

a	b	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(b) Obtain the simplified Boolean expression for Sum in terms of a, b, C_{in}.

(3 marks)

ANSWER IN THIS BOX

$Sum = \bar{a}.\,\bar{b}\,.C_{in} + \bar{a}\,.b\,.\,\overline{C}_{in} + a.\bar{b}\,.\overline{C}_{in} + a.b.C_{in}$

$= C_{in}\left(\overline{a \oplus b}\right) + \overline{C}_{in}\,(a \oplus b)$

$= (a \oplus b) \oplus C_{in}$

(c) Obtain the simplified Boolean expression for C_{out} in terms of a, b, C_{in}.

(3 marks)

ANSWER IN THIS BOX

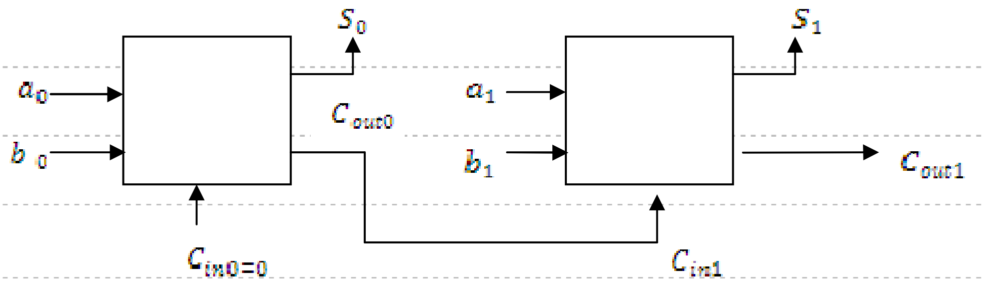
$C_{out} = \bar{a}.b.C_{in} + a.\bar{b}\,.C_{in} + a.b.\overline{C}_{in} + a.b.C_{in}$

$= a.b + C_{in}\,(a \oplus b)$

(d) Now consider a 2 bit full adder with inputs (a_1a_0) and (b_1b_0) where a_0 and b_0 are least significant bits in each 2-bit word. Initial carry in is ($C_{in0}=0$), overall carry out is C_{out1} and the intermediate carries are C_{out0} and C_{in1}. Draw a block diagram for the 2 bit adder consisting of two interconnected 1 bit adders. Clearly show all the inputs, outputs and their interconnections.

(5 marks)

ANSWER IN THIS BOX



(e) Considering all of the above, express the 2 bit adder overall carry out, C_{out1} as a function of (a_1a_0) and (b_1b_0) only.

(7 marks)

ANSWER IN THIS BOX

$C_{out1} = a_1.b_1 + C_{in1}(a_1 \oplus b_1)$

$= a_1.b_1 + C_{out0}(a_1 \oplus b_1)$

Where $C_{out0} = a_0.b_0 + C_{in0}(a_0 \oplus b_0)$

$= a_0\, b_0$

$\therefore C_{out1} = a_1.b_1 + (a_1 \oplus b_1).a_0.b_0$

(f) Which one of the implementations of the two bit full adder, (d) or (e) would be more efficient when adding two n-bit numbers? Explain.

(3 marks)

ANSWER IN THIS BOX

(e) is more efficient.

Ripple carry effect is not present in (e) unlike in (d), and hence instantaneous addition of n-bit number possible in (e)

2) (a) Write down a simple routine in generic high level language constructs to find the maximum element *max*, in an array of integers *array*[1..10].

(6 marks)

ANSWER IN THIS BOX

```
Max = array [1];
for ( i=2; i ≤10; i++)
        If (array [i] > max) then max = array [i];
```

(b) Now, assuming a standard RISC instruction set (chosen from instructions given below), encode the routine of (a) and write down the most compact RISC machine language code that corresponds to (a). Assume, that the array *array*[1..10] of 4 byte integers is stored starting at memory location 5000, and *max* is to be stored at memory location 8000. Assume R_0=0 always.

Typical RISC instructions: `load - LD, store - ST, add - ADD, add immediate - ADDI, subtract immediate - SUBI, subtract - SUB, branch if less than zero - BLE, branch if greater than zero- BGT, branch if not equal to zero – BNE`

(12 marks)

ANSWER IN THIS BOX

LD R_1 , 5000 [R_0]

ADDI R_2 , R_0 , #10

ADD R_3 , R_0 , R_0

Label 1 : LD R_4 , 5004 [R_3]

SUB R5 , R_4 , R_1

BLE label 2

ADD R_1 , R_4 , R_0

Label 2 : ADDI R_3, R_3, # 4

SUBI R_2 , R_2, # 1

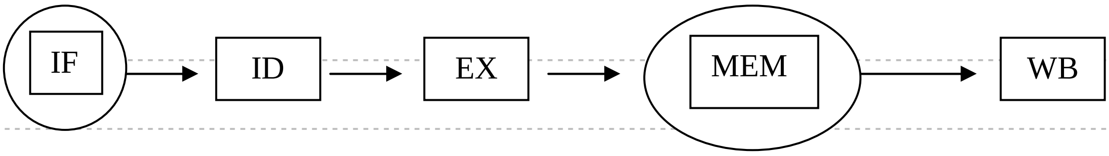
BGT label 1

ST 8000 [R_0] , R_1

(c) Draw a typical 5-stage RISC instruction pipeline, clearly identifying all stages. Circle all stages that refer to memory.

(3 marks)

ANSWER IN THIS BOX



(d) The processor of a computer system generates a 48 bit virtual address which is translated into a 32 bit physical address. The virtual memory is paged with 512kbyte pages and the cache is 1Mbyte and fully associative with a block size (cache line) of 256 bytes. CPU word length is 32 bits.

(9 marks)

(i) In the page table how many bits of the virtual address are mapped into how many bits of the physical address?

ANSWER IN THIS BOX

In page table, (48 – 19)=29 most significant virtual address are mapped to (32 -19)=13 most

Significant bits of physical address

(ii) How many cache blocks are there in the cache?

ANSWER IN THIS BOX

$$\frac{1024 * 1024}{256} = 4096 \ cache \ blocks$$

(iii) How many bits are there in the tag field of each cache block?

ANSWER IN THIS BOX

tag = (32 – 8) bits
= 24 bits

Since 32 bit physical address & 8 bits for block identification.

3) State whether each of the following statements is/are true. If false, explain in at most one sentence, the true position.

(20 marks)

(i) Processor architects can attempt to improve the Instructions per Second (IPS) rate of the processor by increasing the Cycles per Instruction (CPI) while keeping the clock rate fixed.

ANSWER IN THIS BOX

False

IPS can be improved by lowering CPI, while keeping clock rate fixed.

(ii) The emergence of multicore architectures is fuelled by as much as the developments in VLSI densities as much to the limitations of instruction level parallelism.

ANSWER IN THIS BOX

True

(iii) A pure CISC architecture based processor will have a lower overall performance compared to a RISC architecture if it were to run in a context switching intensive scenario such as Xen hypervisor.

ANSWER IN THIS BOX

False

CISC will have a better performance since there is less number of requests to save in context switch and memory transfers are efficient.

(iv) An ideal single instruction pipeline aims at a CPI of less than 1.

ANSWER IN THIS BOX

False

Single instruction Pipeline attempts a CPI $\longrightarrow$ 1

(v) An arithmetic exception occurring in an instruction pipeline is likely to cause a context switch.

ANSWER IN THIS BOX

False

It will cause a trap instruction to be executed by the OS kernel

(vi) A branch target buffer's (BTB) sole purpose is to predict the most likely jump address that helps resolve control hazards in an instruction pipeline.

ANSWER IN THIS BOX

True

(vii) Registers and internal caches are the fast memories found within a processor; but whereas caches can contain both instructions and data, registers can only contain data that corresponds to variables.

ANSWER IN THIS BOX

True

(viii) In case of a cache miss, the main memory is referred, which in turn could cause a page fault.

ANSWER IN THIS BOX

True

(ix) Under certain program behaviours, a fully associative cache organization would cause frequent swapping of blocks compared to direct mapped caches.

ANSWER IN THIS BOX

False

A direct mapped organization could cause frequent swapping of block.

(x) According to Amdahl's law, only tasks with 50% or higher inherent parallelism can achieve a speed up of 2.0 or above when running on a 32 processor cluster.

ANSWER IN THIS BOX

True

(xi) Simultaneous multithreading (SMT) or hyperthreading (HT) attempts to minimize context switching overhead while at the same time maximizing the instruction throughput.

ANSWER IN THIS BOX

True

(xii) Structural hazards in instruction pipelines can be minimized by arithmetic bypassing.

ANSWER IN THIS BOX

False

Data hazards can be minimized by arithmetic bypassing

(xiii) Constant length instructions characteristic of RISC instructions enable the pre-fetching of multiple instructions without the need for waiting for decoding of each instruction.

ANSWER IN THIS BOX

True

(xiv) A 2.4GHz processor with a CPI ratio of 0.3 will be able to deliver a maximum throughput of 8000 MIPS.

ANSWER IN THIS BOX

True

(xv) CISC arithmetic and logic instructions do not have arguments that refer to memory locations.

ANSWER IN THIS BOX

False

They (CISC) do have arithmetic /logic instructions that refer to memory

4) (a) Draw a three state, state transition diagram for a multi-tasking kernel showing the process states and the transitions suitably labelled.

(3 marks)

ANSWER IN THIS BOX

(b) State giving reasons the possible outcomes of the following C code fragment.

```
#include <stdio.h>
main()
{
  int x;
  x = fork();

  if (x==0)
    execlp(“/bin/date”, “date”, NULL);
  else
    if (x>0) {
      wait(NULL);
       printf(“Child complete\n”);
    }
    else
      printf("Fork returned error code; no child\n");
}
```

(7 marks)

ANSWER IN THIS BOX

Countinue

(c) P1 and P2 are two concurrent processes interacting over shared data as shown below. Discuss whether the property of mutual exclusion is satisfied for the given codes or if not, provide a corrected version that satisfies the mutual exclusion property.

Code for P1:

```
do {
   signal(mutex);
   // critical section
   wait(mutex);
   // remainder section
} while (TRUE);
```

Code for P2:

```
do {
   wait(mutex);
   // critical section
   signal(mutex);
   // remainder section
} while (TRUE);
```

Note:

The definition of wait() is as follows:

```
wait(S) {
   while S <= 0
        ;  // no-op
   S- - ;
}
```

The definition of signal() is as follows:

```
signal(S) {
   S++;
}
```

(5 marks)

<u>ANSWER IN THIS BOX</u>

(d) State whether the following statements are true or false. If false, explain why.

(10 marks)

(i) The effect of frequent page movement is called thrashing.

ANSWER IN THIS BOX

(ii) A process deadlock occurs due to lack of swap memory.

ANSWER IN THIS BOX

(iii)Unlike processes, threads can share data, but code, stack and registers are not shared.

ANSWER IN THIS BOX

(iv) In the event of a page fault, the executing process is moved to the "blocked process queue" and a process from the "ready to run process queue" is fetched.

ANSWER IN THIS BOX

(v) When tasks have strict time bounds, non-preemptive process scheduling is preferred.

ANSWER IN THIS BOX

(vi) In the event of a context switch, the page table of the running process is saved on the Process Control Block (PCB).

ANSWER IN THIS BOX

(vii) The maximum file size that can be represented by a FAT32 system with a 512 byte block size is 2 TB.

ANSWER IN THIS BOX

(viii) Index-based file block allocation allows less efficient use of disk space compared to the FAT system.

ANSWER IN THIS BOX

(ix) A Least Recently Used (LRU) page replacement algorithm does not require hardware assistance.

ANSWER IN THIS BOX

(x) At boot time, the operating system probes the hardware buses to determine the active devices and installs the corresponding interrupt handlers into the interrupt vector.

ANSWER IN THIS BOX

******