



UNIVERSITY OF COLOMBO, SRI LANKA



UNIVERSITY OF COLOMBO SCHOOL OF COMPUTING

DEGREE OF BACHELOR OF INFORMATION TECHNOLOGY (EXTERNAL)

Academic Year 2019 – 1st Year Examination – Semester 1

IT1205 – Computer Systems I Multiple Choice Question Paper

22nd June, 2019 (TWO HOURS)

Important Instructions:

- The duration of the paper is 2 (two) hours.
- The medium of instruction and questions is English.
- The paper has 50 questions and 12 pages.
- All questions are of the **MCQ** (Multiple Choice Questions) type.
- All questions should be answered.
- Each question will have 5 (five) choices with **one or more** correct answers.
- All guestions will carry **equal** marks.
- There will be a penalty for incorrect responses to discourage guessing.
- The mark given for a question will vary from 0 (All the incorrect choices are marked & no correct choices are marked) to +1 (All the correct choices are marked & no incorrect choices are marked).
- Answers should be marked on the special answer sheet provided.
- Note that questions appear on both sides of the paper.
 If a page is not printed, please inform the supervisor immediately.
- Mark the correct choices on the question paper first and then transfer them to the given answer sheet which will be machine marked. Please completely read and follow the instructions given on the other side of the answer sheet before you shade your correct choices.
- Calculators are not allowed.
- All Rights Reserved.

	In 1980s a card readers that recorded data using a	utomated his weaving factory using a series of punch	
	What is the suitable option to fill the blank above?		
	(a) Charles Babbage	(b) Herman Hollerith	
	(c) Joseph-Marie Jacquard(e) Howard Aiken	(d) John Von Neuman	
) \	Which of the following statements is/a	are true ?	
	(a) Ada Lovelace is considered to l	be the first computer programmer.	
	(b) The Pascaline developed by Bla	aise Pascal read data from punch cards.	
	(c) Joseph-Marie Jacquard develop and subtraction.	ped by Blaise Pascal could perform addition with carry	
	(d) John Von Neuman designed the		
	(e) The Differential Engine was de	eveloped by Blaise Pascal.	
) 1	Which of the following devices can be	used to read the answers marked as shaded circles in a	
´	multiple-choice question paper? (a) Digitizer (b) Plotter	(c) Light Pen ic Ink Character Reader	
r	multiple-choice question paper? (a) Digitizer (b) Plotter	(c) Light Pen ic Ink Character Reader	
r	multiple-choice question paper? (a) Digitizer (b) Plotter (d) Scanner (e) Magneti	(c) Light Pen ic Ink Character Reader	
r	multiple-choice question paper? (a) Digitizer (b) Plotter (d) Scanner (e) Magneti Which of the following devices is/are p	(c) Light Pen ic Ink Character Reader part of a microprocessor?	
r	multiple-choice question paper? (a) Digitizer (b) Plotter (d) Scanner (e) Magneti Which of the following devices is/are p	(c) Light Pen ic Ink Character Reader part of a microprocessor? (b) Program Counter	
	multiple-choice question paper? (a) Digitizer (b) Plotter (d) Scanner (e) Magneti Which of the following devices is/are p (a) Instruction Register (c) Main Memory (e) Control Unit	(c) Light Pen ic Ink Character Reader part of a microprocessor? (b) Program Counter	
	multiple-choice question paper? (a) Digitizer (b) Plotter (d) Scanner (e) Magneti Which of the following devices is/are p (a) Instruction Register (b) Magneti Which of the following devices is/are p (a) Instruction Register (b) Magneti (c) Magneti (c) Main Memory (e) Control Unit Which of the following statements is/ar (CPU)?	(c) Light Pen ic Ink Character Reader part of a microprocessor? (b) Program Counter (d) Cache Memory	
	multiple-choice question paper? (a) Digitizer (b) Plotter (d) Scanner (e) Magneti Which of the following devices is/are p (a) Instruction Register (c) Main Memory (e) Control Unit Which of the following statements is/ar (CPU)? (a) Cache memory holds data that (b) Arithmetic-Logic-Unit (ALU) CPU. (c) Control Unit sends signals to the state of the paper of the property of the paper of the property of the pro	(c) Light Pen ic Ink Character Reader part of a microprocessor? (b) Program Counter (d) Cache Memory re false with respect to the Central Processing Unit t can be readily accessed by the CPU. and Control Unit (CU) are two principal parts of the the CPU components to perform sequenced operations.	
	multiple-choice question paper? (a) Digitizer (b) Plotter (d) Scanner (e) Magneti Which of the following devices is/are p (a) Instruction Register (c) Main Memory (e) Control Unit Which of the following statements is/ar (CPU)? (a) Cache memory holds data that (b) Arithmetic-Logic-Unit (ALU) CPU. (c) Control Unit sends signals to the state of the paper of the property of the paper of the property of the pro	(c) Light Pen ic Ink Character Reader out of a microprocessor? (b) Program Counter (d) Cache Memory re false with respect to the Central Processing Unit at can be readily accessed by the CPU. and Control Unit (CU) are two principal parts of the the CPU components to perform sequenced operations. s are to be carried out according to the values in a	

(d) 2019	(b) 1991 (e) 2021	(c) 2011
(d) 2019	(e) 2021	
hat is the binary va	lue of decimal numb	er ¹¹ / ₆₄ ?
(a) 0.010111	(b) 0.001101	(c) 0.001110
(d) 0.001011	(e) 0.000111	
hat is the decimal v	value of the binary nu	amber 0.010101 ?
(a) $\frac{5}{64}$	(b) ¹³ / ₆₄	(c) ¹⁷ / ₆₄
$\frac{(a)^{-7.04}}{(d)^{-21}/_{64}}$	(e) $\frac{31}{64}$	(0) / 04
wo's Complement b	(b) OR	(c) AND
(a) NOI	(b) OK	(c) AND
(d) NAND	(e) XOR	· ·
		· ·
That is the IEEE star 1999.328125?	ndard 32-bit floating	point representation for the decimal number
That is the IEEE star 1999.328125?		point representation for the decimal number 00000000
That is the IEEE star 1999.328125? (a) 0 10001001 (b) 0 10000011	ndard 32-bit floating	point representation for the decimal number 0000000 0000000
That is the IEEE star 1999.328125? (a) 0 10001001 (b) 0 10000011 (c) 0 10001011	ndard 32-bit floating 11110011110101010 11110011110101010	point representation for the decimal number 0000000 0000000 0000000
(a) 0 10001001 (b) 0 10001011 (c) 0 10010011 (d) 0 10010011	ndard 32-bit floating 11110011110101010 11110011110101010	point representation for the decimal number 0000000 0000000 0000000 0000000 000000
That is the IEEE star 1999.328125? (a) 0 10001001 (b) 0 10000011 (c) 0 10001011 (d) 0 10010011 (e) 0 10001101	ndard 32-bit floating 11110011110101010 11110011110101010 11110011110101010 11110011110101010	point representation for the decimal number 0000000 0000000 0000000 0000000 000000
That is the IEEE star 1999.328125? (a) 0 10001001 (b) 0 10000011 (c) 0 10001011 (d) 0 10010011 (e) 0 10001101 That is the 16-bit flo	ndard 32-bit floating 11110011110101010 11110011110101010 11110011110101010 11110011110101010 ating point number of	point representation for the decimal number 0000000 0000000 0000000 0000000 000000
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That is the IEEE star 1999.328125? (a) 0 10001001 (b) 0 10000011 (c) 0 10001011 (d) 0 10010011 (e) 0 10001101 That is the 16-bit flo	11110011110101010 11110011110101010 11110011110101010 11110011110101010 11110011110101010 ating point number of the presentation is with	point representation for the decimal number 0000000 0000000 0000000 0000000 00f the decimal number +1999.3125? Assume that a sign bit, 5-bit exponent and 10-bit mantissa.
(a) 0 10001001 (b) 0 10000011 (c) 0 10001011 (d) 0 10010011 (e) 0 10001101 What is the 16-bit flows the flow of t	11110011110101010 11110011110101010 11110011110101010 11110011110101010 11110011110101010 ating point number of the presentation is with	point representation for the decimal number 0000000 0000000 0000000 0000000 of the decimal number +1999.3125? Assume that a sign bit, 5-bit exponent and 10-bit mantissa. (b) 0 11001 1111001111

6) What is the decimal value of the hexadecimal number 7E3?

What is the loss of accuracy (round-off-error) when converting the decimal value +1999.3125 to a 16-bit floating point representation with a sign bit, 5-bit exponent and 10-bit mantissa?

(a) 0.3125

(b) 0.25

(c) 0.1875

(d) 0.125

(e) 0.0625

(a) +1365.75

(b) +1365.5

(c) + 1365.25

(d) + 1365.125

(e) + 1365

14) Consider the following Boolean function

$$F(x,y) = (\overline{x} + y).(x + y)$$

Which of the following Boolean functions provide(s) a simplified form of F?

(a) *x*

(b) \overline{y}

(c) x

(d) y

(e) **X. y**

15) Consider the following Boolean function

$$F(x,y) = (x.y).(\overline{x} + y).(y + \overline{y})$$

Which of the following Boolean functions provide(s) a simplified form of F?

(a) x

 $\overline{(b)} \overline{y}$

(c) x

(d) y

(e) **x.y**

16) Consider the following Boolean function

$$F = (A + B)C + A\overline{B} + (A + B)\overline{C} + (\overline{A}B)$$

Which of the following Boolean functions provide(s) a simplified form of F?

(a) A+C

(b) B+C

(c) A+B+C

(d) (A+B)C

(e) A+B

17) Consider the following Boolean function

$$F(A, B, C) = (A.B) + (A.C) + (B.C)$$

What is the minimum number of NAND gates required for the above Boolean function, if it is to be implemented only using NAND gates?

(a) 3

(b) 4

(c) 5

(d) 6

18)

(e) 7

The output of the Boolean function $F(a, b, c) = (\overline{a.b}) + (\overline{b.c}) + (\overline{a.c})$ is 0 when

- (a) a=1, b=1, c=0
- (b) a=1, b=0, c=1
- (c) a=0, b=0, c=1

- (d) a=0, b=1, c=0
- (e) a=1, b=1, c=1

19) If any word of size 128 bit in a memory space can be addressed by using 33-bit memory address and each location holds one word, what should be the size of the memory space?

(a) 8GB

(b) 16GB

(c) 32GB

- (d) 64GB
- (e) 128GB

Suppose, a particular memory space can be addressed by using a 16-bit memory address and each location can hold a word of size 64 bits. If a 16-byte variable is stored starting at location 1110 0011 0010 0101, what is the address of next available storage location?

- (a) 1110 0011 0010 0110
- (b) 1110 0011 0010 0111
- (c) 1110 0011 0010 1001
- (d) 1110 0011 0010 1011
- (e) 1110 0011 0010 1011

Questions 21, 22 and 23 based on the following:

Consider a machine with an instruction format of the form **opcode R**# **R**# **M** where **R**# is a register address to specify one of 30 registers and **M** is a memory address. Instructions are 32 bits long and each of the instruction formats provides 5 bits for the op-code.

21) How large must the register address field be?

(a) 4 bits

(b) 5 bits

(c) 6 bits

(d) 7 bits

(e) 8 bits

(a) 8 bits	(b) 12 bits	(c) 15 bits
(d) 17 bits	(e) 20 bits	
	achine, each memory location caity of this machine's memory?	n hold a word of size 128 bits. Wha
(a) 1 MB	(b) 2 MB	(c) 4 MB
(d) 8 MB	(e) 16MB	, ,
irst level cache, 10% on nano seconds (nsec) for	n the second level cache, and 109	the memory references hit on the 6 misses. The access times are 10 the second level and 60 nsecfor the ve access time?
(a) 8 nsec	(b) 10 nsec	(c) 14 nsec
(d) 16 nsec A non-pipelined system	(e) 18 nsec n A takes on average 80 nano sec	conds (to process an instruction). A
(d) 16 nsec A non-pipelined system bipelined system B has he "Speed-Up Ratio" f	(e) 18 nsec n A takes on average 80 nano sec a 4-stage pipeline, where each so for system B for a 200 instruction	conds (to process an instruction). A tage takes 20 nano seconds. What is a program?
(d) 16 nsec A non-pipelined system bipelined system B has the "Speed-Up Ratio" f (a) 3.6	(e) 18 nsec n A takes on average 80 nano sec a 4-stage pipeline, where each so for system B for a 200 instruction (b) 3.92	conds (to process an instruction). A tage takes 20 nano seconds. What is
(d) 16 nsec A non-pipelined system bipelined system B has he "Speed-Up Ratio" f	(e) 18 nsec n A takes on average 80 nano sec a 4-stage pipeline, where each so for system B for a 200 instruction	conds (to process an instruction). A tage takes 20 nano seconds. What is a program?
(d) 16 nsec A non-pipelined system B has he "Speed-Up Ratio" f (a) 3.6 (d) 3.96 Which of the following where the next instruction Register (b) Status Register (c) General Purpose	(e) 18 nsec n A takes on average 80 nano sec a 4-stage pipeline, where each so or system B for a 200 instruction (b) 3.92 (e) 3.98 registers is used to keep track or on is located?	conds (to process an instruction). A tage takes 20 nano seconds. What is a program?
(d) 16 nsec A non-pipelined system B has he "Speed-Up Ratio" f (a) 3.6 (d) 3.96 Which of the following where the next instruction Region (b) Status Register	(e) 18 nsec n A takes on average 80 nano sec a 4-stage pipeline, where each so for system B for a 200 instruction (b) 3.92 (e) 3.98 registers is used to keep track or on is located? ester es Register ss Register	conds (to process an instruction). A tage takes 20 nano seconds. What is program? (c) 3.94

22) How large must the memory address field be?

7)	is loaded with the contents of the memory address pointed to by the Program Counter (PC) before fetching the instruction during the CPU Cycle.
	Select the most suitable answer for the black
	(a) Status Register
	(b) Transition Lookaside Buffer (TLB)
	(c) Instruction Register
	(d) Cache Memory
	(e) General Purpose Registers
	Which of the following devices is/are loaded with the contents of the data, instruction or memory address during the execution of the CPU Cycle.
	(a) Program Counter (PC)
	(b) Control Unit
	(c) Instruction Register
	(c) Instruction Register(d) Cache Memory
	(d) Cache Memory
	(d) Cache Memory (e) General Purpose Registers Which of the following devices is/are partially visible to users and loaded with the contents
	(d) Cache Memory (e) General Purpose Registers Which of the following devices is/are partially visible to users and loaded with the contents of the data pointed to the Arithmetic Logic Unit (ALU)?
	(d) Cache Memory (e) General Purpose Registers Which of the following devices is/are partially visible to users and loaded with the contents of the data pointed to the Arithmetic Logic Unit (ALU)? (a) Status Register
	(d) Cache Memory (e) General Purpose Registers Which of the following devices is/are partially visible to users and loaded with the contents of the data pointed to the Arithmetic Logic Unit (ALU)? (a) Status Register (b) Transition Lookaside Buffer (TLB)
	(d) Cache Memory (e) General Purpose Registers Which of the following devices is/are partially visible to users and loaded with the contents of the data pointed to the Arithmetic Logic Unit (ALU)? (a) Status Register (b) Transition Lookaside Buffer (TLB) (c) Instruction Register
0)	(d) Cache Memory (e) General Purpose Registers Which of the following devices is/are partially visible to users and loaded with the contents of the data pointed to the Arithmetic Logic Unit (ALU)? (a) Status Register (b) Transition Lookaside Buffer (TLB) (c) Instruction Register (d) Cache Memory
0)	(d) Cache Memory (e) General Purpose Registers Which of the following devices is/are partially visible to users and loaded with the contents of the data pointed to the Arithmetic Logic Unit (ALU)? (a) Status Register (b) Transition Lookaside Buffer (TLB) (c) Instruction Register (d) Cache Memory (e) General Purpose Registers What type of control pins are needed in a microprocessor to regulate traffic on the bus, in
0)	(d) Cache Memory (e) General Purpose Registers Which of the following devices is/are partially visible to users and loaded with the contents of the data pointed to the Arithmetic Logic Unit (ALU)? (a) Status Register (b) Transition Lookaside Buffer (TLB) (c) Instruction Register (d) Cache Memory (e) General Purpose Registers What type of control pins are needed in a microprocessor to regulate traffic on the bus, in order to prevent two devices from trying to use it at the same time?
0)	(d) Cache Memory (e) General Purpose Registers Which of the following devices is/are partially visible to users and loaded with the contents of the data pointed to the Arithmetic Logic Unit (ALU)? (a) Status Register (b) Transition Lookaside Buffer (TLB) (c) Instruction Register (d) Cache Memory (e) General Purpose Registers What type of control pins are needed in a microprocessor to regulate traffic on the bus, in order to prevent two devices from trying to use it at the same time?
0)	(d) Cache Memory (e) General Purpose Registers Which of the following devices is/are partially visible to users and loaded with the contents of the data pointed to the Arithmetic Logic Unit (ALU)? (a) Status Register (b) Transition Lookaside Buffer (TLB) (c) Instruction Register (d) Cache Memory (e) General Purpose Registers What type of control pins are needed in a microprocessor to regulate traffic on the bus, in order to prevent two devices from trying to use it at the same time? (a) Control Unit (b) Status Register

31)	A data storage used to store data to compensate for the difference in the speed at which the different units can handle data is the
	(a) Cache Memory
	(b) Memory
	(c) Virtual Memory
	(d) Memory Management Unit (MMU)
	(e) Buffer
32)	Which of the following is an/are Optical Storage Device/s?
	(a) Memory Stick
	(b) Magnetic Tape
	(c) Zip Disk
	(d) Super Disk
	(e) CD-ROM
33)	Which of the following devices is a/are biometric device/s?
	(a) Barcode Readers
	(b) Smart Card Readers
	(c) Credit Card Readers
	(d) ePassport
	(e) IRIS Scanners
34)	Which of the following devices is/are used to produce a 3-Dimensional display?
	(a) Compressive Light Field Displays
	(b) Volumetric Displays
	(c) Integral Imaging
	(d) Movie Projectors
	(e) Holographic Displays

1		
	(a) InkJet Printers	
	(b) Label Printer	
	(c) Dot Matrix Printers	
	(d) Game Boy Printer	
	(e) Solid Ink Printers	
1	Which of the following falls into the category of both an input and output device?	
	(a) Scanner	
	(b) Disk Drive	
	(c) Network Card	
	(d) Punch Card	
	(e) Serial Management Interface (SMI)	
	Which of the following technologies is/are used to set up short-range point-to-point communication? (a) IrDA (b) Radio Frequency	
	communication?	
V	(a) IrDA (b) Radio Frequency (c) Bluetooth (d) Microwave	оа
V	(a) IrDA (b) Radio Frequency (c) Bluetooth (d) Microwave (e) HiperLAN Which of the following wireless technologies can be used to connect external devices to	o a
V	(a) IrDA (b) Radio Frequency (c) Bluetooth (d) Microwave (e) HiperLAN Which of the following wireless technologies can be used to connect external devices technologies?	о а
V	(a) IrDA (b) Radio Frequency (c) Bluetooth (d) Microwave (e) HiperLAN Which of the following wireless technologies can be used to connect external devices technologies? (a) IrDA (b) Radio Frequency	эа
	(a) IrDA (b) Radio Frequency (c) Bluetooth (d) Microwave (e) HiperLAN Which of the following wireless technologies can be used to connect external devices technologies? (a) IrDA (b) Radio Frequency (c) Bluetooth (d) Microwave	
	(a) IrDA (b) Radio Frequency (c) Bluetooth (d) Microwave (e) HiperLAN Which of the following wireless technologies can be used to connect external devices temputer? (a) IrDA (b) Radio Frequency (c) Bluetooth (d) Microwave (e) Wi-Fi Which of the following transmission media can be considered as unguided data transmission.	
	(a) IrDA (b) Radio Frequency (c) Bluetooth (d) Microwave (e) HiperLAN Which of the following wireless technologies can be used to connect external devices temputer? (a) IrDA (b) Radio Frequency (c) Bluetooth (d) Microwave (e) Wi-Fi Which of the following transmission media can be considered as unguided data transminedia?	

(a) Laser	(b) Mircowave
(c) Flash Light	(d) Ultra Violet
(e) Infrared	
Which of the following software programs?	e is/are designed be able to modify the source code of the
(a) Compilers	(b) Freeware
(c) Open Source	(d) Assemblers
(e) Interpreters	
(e) User Interfaces	
Which of the following Operation	ng Systems is/are used in a typical embedded system?
(a) OpenZaumia	(b) Mobilinux
(a) OpenZaurus	(d) Amoeba
(c) MotoMagx	
_	
(c) MotoMagx	e is/are utility type of software?
(c) MotoMagx (e) OPhone	e is/are utility type of software?
(c) MotoMagx (e) OPhone Which of the following software	e is/are utility type of software?
(c) MotoMagx (e) OPhone Which of the following software (a) Disk Compression	e is/are utility type of software?
(c) MotoMagx (e) OPhone Which of the following software (a) Disk Compression (b) File Synchronization	e is/are utility type of software?

	() M 1' D	1	
	(a) Machine Deper	ndence	
	(b) Efficiency (c) Accuracy		
	(d) Versatility		
	(e) Reliability		
	(e) Kenaonity		
An it?	error in software or	hardware is called a bug. Wha	t is the alternative computer jargon f
	(a) Leech	(b) Squid	(c) Slug
	(d) Rough	(e) Glitch	
hur	(a) Accuracy	is feature is known as (b) Reliability	(c) Automatic
	(a) Λ courses	(b) Reliability	(a) Automotic
	(a) Accuracy	(b) Renability	(c) Automatic
	(d) Versatility	(e) Efficiency	(c) Automatic
The	(d) Versatility	•	(c) Automatic
The	(d) Versatility	(e) Efficiency	(c) Reproducing
The	(d) Versatility e arranging of data in	(e) Efficiency a a logical sequence is called	
	(d) Versatility e arranging of data in (a) Sorting (d) Summarizing	(e) Efficiency a a logical sequence is called (b) Classifying	(c) Reproducing
	(d) Versatility e arranging of data in (a) Sorting (d) Summarizing	(e) Efficiency a a logical sequence is called (b) Classifying (e) Clustering	(c) Reproducing
	(d) Versatility e arranging of data in (a) Sorting (d) Summarizing e ability of a compute	(e) Efficiency a a logical sequence is called (b) Classifying (e) Clustering er system to remain operational	(c) Reproducing
The Wh	(d) Versatility e arranging of data in (a) Sorting (d) Summarizing e ability of a compute (a) Relation (d) Versatility nich of the following	(e) Efficiency a a logical sequence is called (b) Classifying (e) Clustering er system to remain operationa (b) Schema (e) Diligence will frequently produce obfus code, and is also useful in some	(c) Reproducing al despite various failures is (c) Resilience
The Wh	(d) Versatility e arranging of data in (a) Sorting (d) Summarizing e ability of a compute (a) Relation (d) Versatility which of the following every of lost source of	(e) Efficiency a a logical sequence is called (b) Classifying (e) Clustering er system to remain operationa (b) Schema (e) Diligence will frequently produce obfus code, and is also useful in some	(c) Reproducing al despite various failures is (c) Resilience cated code which can be used for the