UNIVERSITY OF COLOMBO, SRI LANKA

UNIVERSITY OF COLOMBO SCHOOL OF COMPUTING

DEGREE OF BACHELOR OF INFORMATION TECHNOLOGY (EXTERNAL)

Academic Year 2019 – 3rd Year Examination – Semester 5

IT5305: Computer Systems II

Structured Question Paper

July 7, 2019
(TWO HOURS)

To be completed by the candidate

BIT Examination Index No: .....

Important Instructions:

- The duration of the paper is **2 (two) hours**.
- The medium of instruction and questions is English.
- This paper has **5 questions** and **13 pages**.
- **Answer all questions.** Questions **do not** carry equal marks.
- **Write your answers** in English using the space provided **in this question paper**.
- Do not tear off any part of this answer book.
- Under no circumstances may this book, used or unused, be removed from the Examination Hall by a candidate.
- Note that questions appear on both sides of the paper.
  If a page is not printed, please inform the supervisor immediately.
- **No** calculators are allowed.

Questions Answered

Indicate by a cross (×), (e.g. [X]) the numbers of the questions answered.

To be completed by the candidate by marking a cross (×).	1	2	3	4	5	
Marks allocated for each question	20	10	30	25	15	
To be completed by the examiners:						

1) (a) A computer system has a CPU which has 256 nos. 64 bit general purpose registers. It has a 48 bit virtual address. The system has 2GB of RAM. Virtual memory (VM) is paged with 4Mbyte pages and the external cache is 1Mbytes. The system disk size is 100Gbytes.

(i) What is the total size of register memory in bytes? **[2 marks]**

ANSWER IN THIS BOX

= 64x256/8

= 2048 bytes

(ii) What fraction of VM pages can be there in the physical memory at any given time? **[3 marks]**

ANSWER IN THIS BOX

=(2 x 10^9)/2^48

= 2^(-17)

(iii) How many CPU words can occupy a page block? **[3 marks]**

ANSWER IN THIS BOX

=4x10^6/8

= 2^19

(b) Consider the following three RISC instructions contained in a thread that is running on a processor.

```
LD R1, 200[R0] : load content of memory location (200+R0)
to register R1
SUB R3,R2,R1: subtract R2 from R1 and save on R3
ST 300[R0], R3: store R3 contents at memory location
(300+R3)
```

(i) If a memory referencing instruction takes 3 clock cycles and an arithmetic instruction takes 1 clock cycle, what is the average CPI for the above piece of code if the code is executed on a non-pipelined processor?

[3 marks]

ANSWER IN THIS BOX

Total cycles= 3+1+3; total instructions = 3

CPI = 2.3

(ii) If R0=0, and R2=20 and the content of memory location 200 is 40, what would be the content of memory location 300 after the execution of the code?

[3 marks]

ANSWER IN THIS BOX

R1=40, R2=20, R3 = R2 + R1

= 60

(iii) Suppose now, the above code is to be executed on a typical 5 stage RISC pipeline with stages IF, ID, EX, MEM and WB. Draw a space-time diagram to show the overlapped execution of the three instructions. State any assumptions.

[3 marks]

ANSWER IN THIS BOX

(1) IF ID EX MEM WB

(2) IF ID EX MEM WB

(3) IF ID EX MEM WB

(iv) If each stage takes only 1 clock cycle, what is the CPI of the above code executing on the pipelined processor if the data hazards are assumed to be eliminated?

[3 marks]

ANSWER IN THIS BOX

CPI = 1.0 by implication.

2) Consider the following high level code fragment. Here, the source array of 4 byte integers a[0], a[1],..a[9] is stored starting at memory location 1000 (that is a[0] at 1000, a[1] at 1004 and so on). The destination array of 4 byte integers are stored starting at memory location 2000 (that is b[0] is at 2000, b[1] is at 2004 etc.,). Your code should start at memory location 5000. The processor has only one internal register R, initialized to zero. Write down the machine instruction sequence corresponding to a Register/Memory architecture. Your code should have a minimum number of instructions. The typical instruction set for a R/M architecture is given below.

[10 marks]

```
b[0] = a[0];
for i=1 to 9
     b[i] = b[i-1] + a[i];
```

LOAD [M] : [R is loaded the content of memory location pointed to by M (or an absolute address)]

STORE [M]: [R is stored at memory location pointed to by M (or an absolute address)]

ADD [M]: [adds R to memory content at location pointed to by M (or an absolute address), and saves in R]

SUB [M]: [subtracts R from memory content at location M (or an absolute address) and saves result in R and raises a flag if result is GT/LT/EQ/GE]

MCOMPARE [M1], [M2]: [compares memory contents at locations pointed to by M1 (or an address) and M2 (or an address) and raises a flag if M1 GT/LT/EQ/GE to M2]

COMPARE M1, M2: [compares absolute memory addresses or pointers M1 and M2 and raises a flag if M1 GT/LT/EQ/GE to M2]

JUMP_flag M: [jumps to memory address (absolute address) or that pointed to by M if flag is raised] (flags: GT - greater than 0; EQ – equal to zero; GE – greater than or equal to zero)

JUMP M: [jumps to memory address (absolute address) or that pointed to by M]

SET M <target>: set memory location pointer M to “target” address

INC (or DEC) M: increment (or decrement) memory location pointer M (or absolute address) by 4

Note: Pointer M can mean any number of memory pointers M1, M2, M3 etc.,

ANSWER IN THIS BOX

5000		SET M1, 1000
5001		SET M2, 2000 (1 mark for these two statements)
5002		LD [M1]
5003		ST [M2] (2 marks for these two statements)
5004	loop:	INC M1
5005		INC M2
5006		ADD [M1]
5007		ST [M2]
5008		COMPARE M1, 1040 (5 marks for this loop logic, order of statements and their existence)
5009		JLT loop

2 bonus marks for overall efficiency and correctness. Note that there may be other correct but longer answers, for which marks can be given.

3) In each of the following sentences, underline or circle the more suitable term from within the brackets to fill in the blanks. **[30 marks]**

(i) In RISC (Load/Store) Instruction Set Architectures, all instructions are of …….(variable/constant) length compared to CISC (Register/Memory) whose instructions are of ….(variable/constant) length, in order that RISC CPU program counter can auto advance …..(after/prior to) decoding of the instruction.

(ii) In CISC architectures which have a ….. (small/large) register file, a procedure call will make the operating system save the current register file on the stack, whereas in a RISC architecture with a …… (small/ large) register file, current variables in the registers will not be saved on stack.

(iii) ……(RISC/CISC) architectures can be efficiently instruction pipelined since their microinstructions can be grouped into independent blocks in such a way that …….(delay variations/hazards) among them can be minimized.

(iv) Instruction……..(pipelining/super scaling) allows a processor to achieve a CPI (cycles per instruction) of ……..(greater than one/less than one).

(v) For a process running under a multitasking kernel, a …..(page fault/cache miss) for a ….. (instruction fetch/arithmetic operation) would cause ……. (a context switch/stalling of instructions).

(vi) A computer memory hierarchy usually works because it upholds the principle of *locality of reference*, which says that a reference to a memory location will most likely be referenced …….(again/frequently) and a ……..(nearby/furthest) location be also likely to be referenced.

(vii) A processor which has a word length of 64 bits would have a …… (virtual/physical) memory width of …..(64/8) bits and a register width of ….(32/64) bits.

(viii) A processor which has a clock rate of 1.5GHz and a CPI of 0.7 for a certain type of task, would have a MIPS rate of …….2000??

(ix) In a multitasking operating system, a blocked process will be moved to the …..(running/ready to run) state when the …..(IO activity has completed/time slice has expired).

(x) In demand paging as applied to…….(virtual memory/physical memory), the most frequently accessed set of page blocks by …… (a thread/all threads) is kept in a table, and this functionality can be equally if not better performed by a …… (page table/translation look aside buffer).

(xi) Any acceptable solution to the mutual exclusion problem, that is multiple process access resolution to ……(shared memory/distributed memory) needs to satisfy two conditions, which is *liveness*, ……..(all processes are given a fair chance to enter critical region/at any time, only one process can be inside critical region), and *safety*, ……..(all processes are given a fair chance to enter critical region/at any time, only one process can be inside critical region).

(xii) Operating systems virtualization allows the use of multiple ……(hardware/virtual machines) on top of a ……. (hypervisor/kernel) itself running on a piece of processor hardware.

(xiii) Graphics processing units (gpu) are now widely used not only for rendering graphics but also for scientific computing. The main reason they are efficient for scientific computing is that gpu's are primarily….(MISD/SIMD) architectures that are designed to process ….(vectors/scalars).

4) (a)

(i) What is the parameter that is maintained in a process' *process control block (PCB)* by the operating system to help it uniquely identify that process? **[2 marks]**

ANSWER IN THIS BOX

Process id

(ii) What happens at a *context switch* between processes?

[2 marks]

ANSWER IN THIS BOX

The context (eg: values of registers, program counters etc) of the old process is saved in the PCB and the context of the new process scheduled to run is loaded.

(iii) Write down the outcome of the following C code statement labelled (**A)** if it is successfully executed on a dual core computer:

```
int i;
pthread_t tid[2];

for (i=0; i<2; i++)
     pthread_create(&tid[i],NULL,slave,(void ) i);   /* A */
```

[**Note:** Assume that the *mywork()* function is available in the code.]

[2 marks]

ANSWER IN THIS BOX

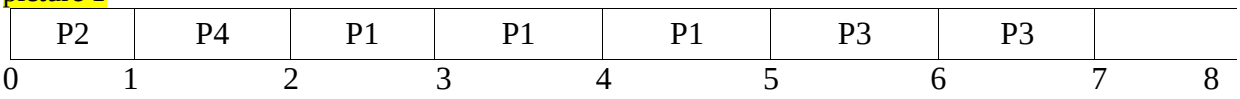
This will create 2 threads (1 mark)
The first thread will run function slave(0) while the second thread will run function slave(1)
OR
The two threads will run on two cores. (1 mark)

(iv) Consider the following set of processes arrive at time 0 in the order P 1 , P 2 , · · ·, P 4 , with CPU bursts and priorities as given in the table:

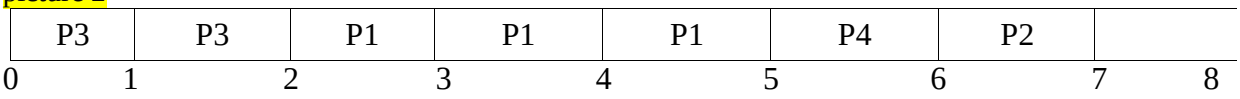
Process	Burst time (ms)	Priority
P1	3	3
P2	1	1
P3	2	4
P4	1	2

Indicate on the *Gantt Chart* below the schedule of the above processes if *priority scheduling* is performed by the operating system. What is the *average turnaround time* of the processes?

picture 1



picture 2



ANSWER IN THIS BOX

If low number represented high priority then picture 1.
avg turnaround time = 15/2 = 7.5ms

If high number represent high priority then picture 2.
Avg turnaround time = 20/2 = 10ms

[3 marks]

(b)

(i) State one difference between a logical and a physical memory address.

[1 mark]

ANSWER IN THIS BOX

Physical address is limited by the actual physical memory size whereas a logical address is not.

(ii) What is meant by "swapping" with regard to memory management?

[2 marks]

ANSWER IN THIS BOX

Process being taken out of memory to the backing store (to free the memory) and bring them again to memory for continued execution.

(iii) Write down the suitable terms to fill the blanks labeled (A) to (C) in the following "paging" related statements:

ANSWER IN THIS BOX

Every address generated by the CPU is divided into two parts: a page ….(A)number…. and a page ….(B)…offset.

The first of the above is used to index into a page ….(C)table…. which contains the base address of each page in physical memory. This base address is combined with the page ….(B)offset…. to define the physical memory address that is sent to the memory unit.

[2 marks]

(iv) Assume that the physical memory of a computer system contains three frames that are initially empty.

Now consider the following page reference string made by the memory management system:

1, 2, 3, 5, 2, 1, 4, 6, 2, 1, 2, 3

Draw the frames showing the page numbers when the above string is referenced with the *least recently used* page replacement policy. Indicate any page faults that may occur.

[3 marks]

ANSWER IN THIS BOX

	1	2	3	5	2	1	4	6	2	1	2	3
	1	1	1	5	5	5	4	4	4	1	1	1
		2	2	2	2	2	2	6	6	6	6	3
			3	3	3	1	1	1	2	2	2	2
	PF	PF	PF	PF		PF	PF	PF	PF	PF		PF

(c) Indicate whether each of the statements below is true (**T**) or false (**F**). If false, justify.

[1 mark X 6 = 6 marks]

(i) Each hard-disk is made up of *sectors*, which are divided into *tracks.*

ANSWER IN THIS BOX

F Each hard disk is made up of tracks which are divided into sectors

(ii) Booting begins by running code that is resident in a computer system's ROM.

ANSWER IN THIS BOX

T

(iii) The Windows system places its boot code in the first sector on the hard-disk, which it terms the *master boot record*.

ANSWER IN THIS BOX

T

(iv) A device communicates with a computer via a *port.*

ANSWER IN THIS BOX

T

(v) When devices share a common set of wires for communication, the connection is called a *bus*.

ANSWER IN THIS BOX

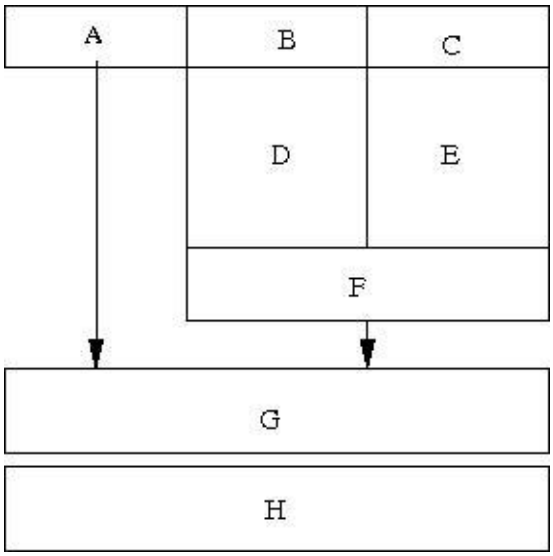
T

(vi) Physical disks may be segmented into partitions to control media use and to allow multiple, possibly varying, file systems on a single spindle.

ANSWER IN THIS BOX

T

5) (a) A **VMware Workstation** architecture with *Linux* as the host operating system is shown in the diagram below. Indicate what is meant by the labels A to H choosing from the given list. Note that an item may be used for more than one label.



List:

{application, hardware, Linux, Virtualization layer, Windows NT, Windows XP***}***

Write down **one (1)** advantage in the above setup.

[8 + 1 = 9 marks]

ANSWER IN THIS BOX

A,B,C : - Application, D/E :- Windows NT, Windows XP, F:- Visualization Layer, G:- Linux, H:- Hardware

One need not have different machines with different operating systems. Everything can be on the same machine.

(b) Define briefly, the following cloud computing services:

[2 marks X 3 = 6 marks]

(i) software as a service (SaaS)

ANSWER IN THIS BOX

A method of software delivering and licensing in which software is accessed online rather than bought and installed on individual computers.

(ii) infrastructure as a service (IaaS)

ANSWER IN THIS BOX

Provides infrastructure (hardware, storage, servers, data centre space) through the Internet.

(iii) platform as a service (PaaS)

ANSWER IN THIS BOX

Provides hardware and software tools (usually needed for application development) to users over the Internet.