Computer Architecture–Homework VIII

107 Fall semester, Chapter 12 ∼ 14

12.4 Many processors provide logic for performing arithmetic on packed decimal numbers. Although the rules for decimal arithmetic are similar to those for binary operations, the decimal results may require some corrections to the individual digits if binary logic is used.

Consider the decimal addition of two unsigned numbers. If each number consists of N digits, then there are $4N$ bits in each number. The two numbers are to be added using a binary adder. Suggest a simple rule for correcting the result. Perform addition in this fashion on the numbers 1698 and 1786.

Sol:
Perform binary addition four bits (one digit) at a time. If the result is greater then 1001 (decimal 9), then add 0110 (decimal 6) to get the correct result. If there is a carry bit, it should be add to the next digit.

$$\begin{array}{rrrrr}
 & \boxed{1} & \boxed{1} & \boxed{1} & \\
 & 0001 & 0110 & 1001 & 1000 \\
+ & 0001 & 0111 & 1000 & 0110 \\
\hline
 & 0011 & 1110 & 10010 & 1110 \\
 & & +0110 & +0110 & +0110 \\
\cline{3-5}
 & & \boxed{1}0100 & \boxed{1}1000 & \boxed{1}0100
\end{array}$$

13.4 Consider a 16-bit processor in which the following appears in main memory, starting at location 200:

200	Load to AC	Mode
201	500	
202	Next instruction	

The first part of the first word indicates that this instruction loads a value into an accumulator. The Mode field specifies an addressing mode and, if appropriate, indicates a source register; assume that when used, the source register is R1, which has a value of 400. There is also a base register that contains the value 100. The value of 500 in location 201 may be part of the address calculation. Assume that location 399 contains the value 999, location 400 contains the value 1000, and so on. Determine the effective address and the operand to be loaded for the following address modes:

(a) Direct
(b) Immediate
(c) Indirect
(d) PC relative
(e) Displacement
(f) Register
(g) Register indirect
(h) Autoindexing with increment, using R1

Sol:

		effective address	operand loaded
(a)	Direct	500	1100
(b)	Immediate	201/x	500
(c)	Indirect	1100	1700
(d)	PC relative	202+500=702	1302
(e)	Displacement	100+500=600	1200
(f)	Register	R1/x	400
(g)	Register indirect	400	1000
(h)	Autoindexing	400+500=900	1500

14.9 A pipelined processor has a clock rate of 2.5GHz and executes a program with 1.5 million instructions. The pipeline has five stages, and instructions are issued at a rate of one per clock cycle. Ignore penalties due to branch instructions and out-of-sequence executions.

(a) What is the speedup of this processor for this program compared to a non-pipelined processor, making the same assumptions used in Section 14.4?

(b) What is throughput (in MIPS) of the pipelined processor?

Sol:

(a) $\frac{1.5\times10^6\times5}{(5-1)+1.5\times10^6} \approx 5$. We can ignore the initial filling up of the pipeline and the final emptying of the pipeline, because this involves only a few instructions out of 1.5 million instructions. Therefore the speedup is a factor of 5.

(b) One instruction is completed per clock cycle, the throughput is $\frac{2.5\times10^9}{10^6} = 2500\text{MIPS}$.