Computer Architecture–Homework II

107 Fall semester, Chapter 3

3.1 The hypothetical machine of Figure 3.4 also has two I/O instructions:

- 0011 = Load AC from I/O
- 0111 = Store AC to I/O

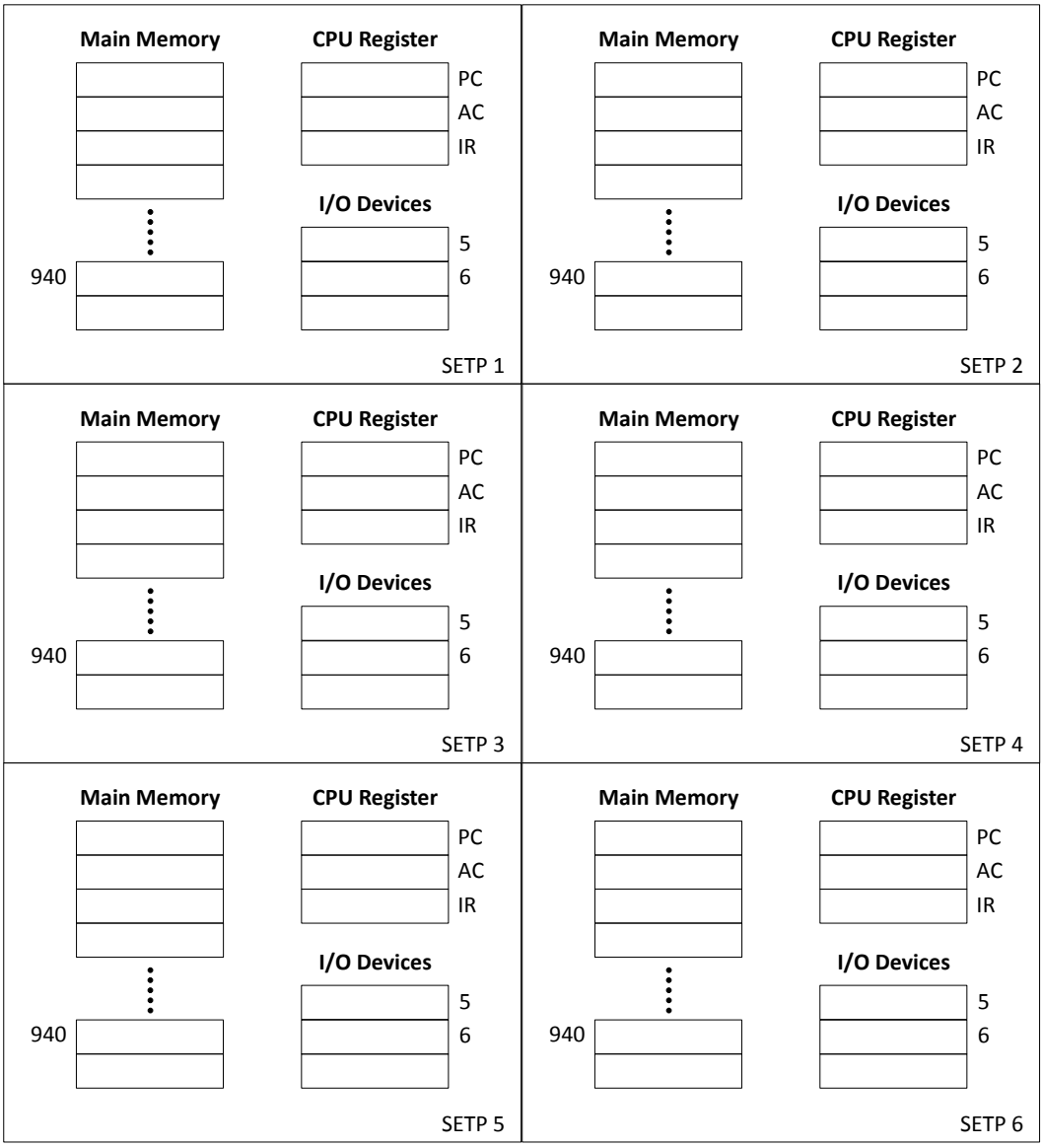
In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 3.5) for the following program:

(a) Load AC from device 5.

(b) Add contents of memory location 940.

(c) Store AC to device 6.

Assume that the next value retrieved from device 5 is 3 and that location 940 contains a value of 2.



3.5 Consider a 16-bit microprocessor, with a 8-bit external data bus, driven by a 4MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/s? To increase its performance, would it be better to make its external data bus 16 bits or to double the external clock frequency supplied to the microprocessor? State any other assumptions you make, and explain. *Hint: Determine the number of bytes that can be transferred per bus cycle.*

3.17 Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 40% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor.