考試科目	計算機結構	■大學日間 □大學進學 □碩士班 □碩士在職班 資訊工程學系 三年級B班	命題老師	林熙中
考試日期	11月2日(星期五) 第2~4節	附答案紙□是 ■否 / 列印大小■A4□B4	試卷別■單一□A卷□B卷	印刷份數 65
姓名		學號		序號	

1. A program spends 30ms to execute on a processor which has a clock cycle time of 4ns. The program consists of four major types of instructions, with the following instruction mix: (16%)

Instruction Type	Instruction Mix	Cycle per Instruction
Integer arithmetic	25%	1
Data transfer	30%	2
Control transfer	30%	3
Floating point	15%	5

(a) What is the clock rate of the processor?

(b) Determine the effective CPI value for this program?

(c) Compute the MIPS rate for this program?

(d) How many instructions are there in the program?

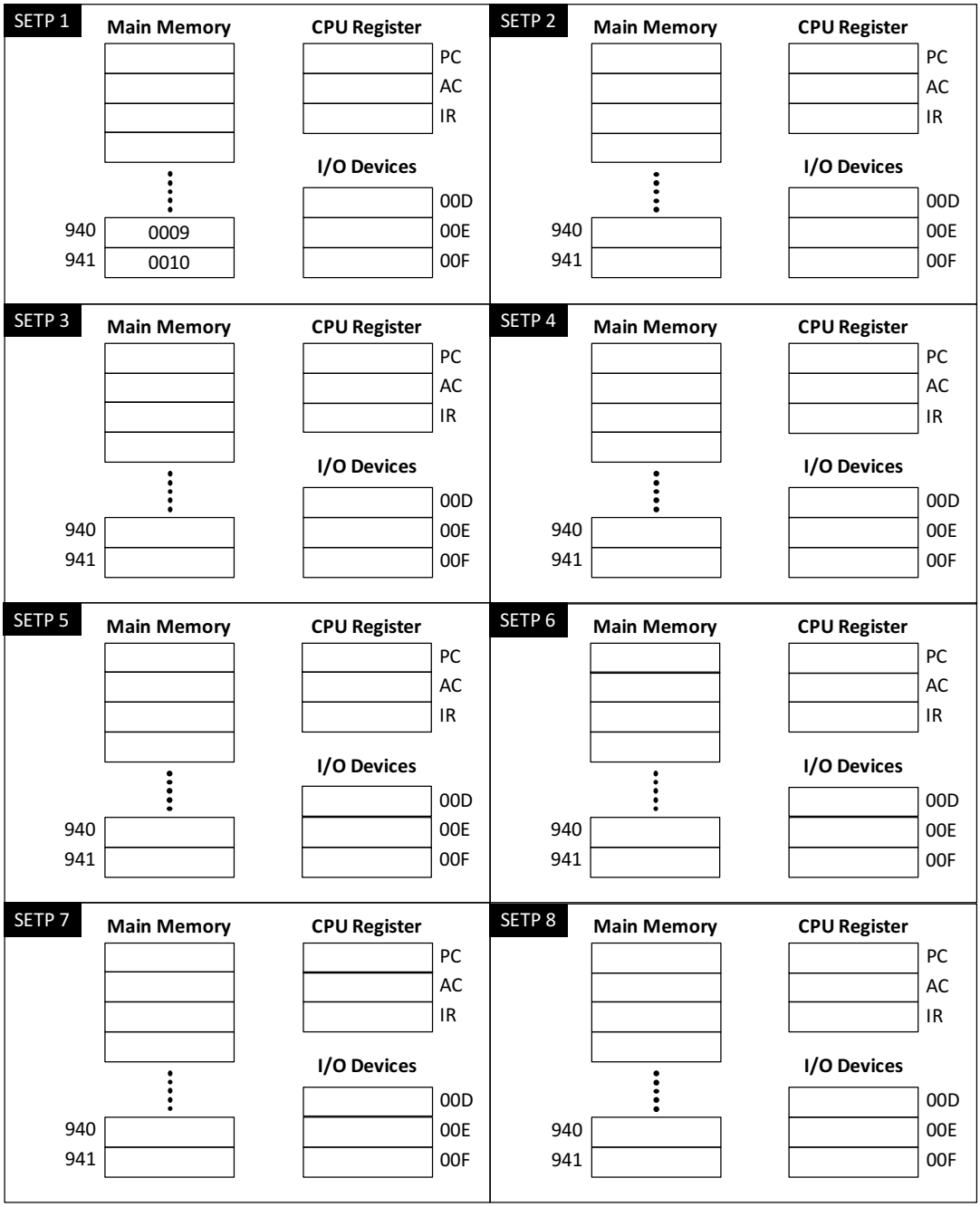
2. (a) Explain "Amdahl's law" and give a concrete example to demonstrate its operation. (8%)

(b) Explain "Little's law" and give a concrete example to demonstrate its operation. (8%)

3. Consider the hypothetical machine described below. (12%)

- An instruction is 16-bit in length where the 4 left-most bits encode the opcode and the following 12 bits represent either a memory address or an I/O device number. Below is a partial list of opcodes:
  - $(0001)_2$ = Load AC from memory
  - $(1001)_2$ = Load AC from I/O
  - $(0010)_2$ = Store AC to memory
  - $(1010)_2$ = Store AC to I/O
  - $(0101)_2$ = Add to AC from memory
- Data are 16-bit in length.
- There are three registers in the processor, which are the program counter (PC), an accumulator (AC), and the instruction register (IR).

Now please explain how the high-level instruction "double the content of memory location 940" is executed by using the following figure. For the sake of simplicity, answer this question with hexadecimal notations. You may extend or modify the figure if it is necessary.



4. Answer the following questions concisely and precisely. (16%)

   (a) What is the main purpose of "interrupts"?

   (b) How to handle multiple interrupts?

   (c) What is the "locality of reference" principle?

   (d) Explain the phenomenon of cache thrashing.

5. Consider a memory system with a cache access time of 60ns and a memory access time of 2μs. If the effective access time is 100ns, what is the cache hit ratio? (8%)

6. Consider a memory system with 4GB byte-addressable main memory and 16MB direct-mapped cache where the cache line size is 4Kbytes. (12%)

   (a) Show the address format.

   (b) Determine the number of blocks in main memory.

   (c) List two different addresses that will map to the same cache line. (You may use hexadecimal notations.)

7. Consider a memory system where the main memory address is 28 bits in length and the cache memory mapping function is fully associative. The capacity of the main memory is 2GB while the capacity of the cache is 2MB; the size of one single cache line is 2KB. (12%)

   (a) Show the address format.

   (b) Determine the word size of this system.

   (c) Determine the number of lines in cache memory.

8. Consider a byte-addressable memory system where the main memory has 2M blocks. The system is equipped with a eight-way set-associative cache memory with 128 bytes line size and 8 bits tag length. (12%)

   (a) Show the address format.

   (b) Determine the capacity of main memory.

   (c) Determine the capacity of cache memory.

9. (a) When do we need a "cache replacement algorithm"?

   (b) List typical cache replacement algorithms and briefly explain how they are implemented. (16%)