Computer Architecture–Homework III

107 Fall semester, Chapter 4

4.5 Consider a 32-bit microprocessor that has an on-chip 16-KByte four-way set-associative cache. Assume that the cache has a line size of 32-bit words. Draw a block diagram of this cache showing its organization and how the different address fields are used to determine a cache hit/miss. Where in the cache is the word from memory location ABCDE8F8 mapped?

4.8 Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

(a) How is a 16-bit memory address divided into tag, line number, and byte number?

(b) In what line would bytes with each of the following addresses be stored?

0001 0001 1001 1011
1100 0011 0010 0100
1101 0000 0111 1101
1010 1010 0110 1010

(c) Suppose the byte with address 0101 1010 0010 1110 is stored in the cache. What are the addresses of the other bytes stored along with it?

(d) How many total bytes of the memory can be stored in the cache?

(e) Why is the tag also stored in the cache?

4.11 Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size.

(a) Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

(b) Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

(c) Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

4.12 Consider a computer with the following characteristics: total of 1 Mbyte of main memory; word size of 1 byte; block size of 16 bytes; and cache size of 64 Kbytes.

(a) For the main memory addresses of C101E, 01234, and F0B30, give the corresponding tag, cache line address, and word offsets for a direct-mapped cache.

(b) Give any two memory addresses with different tags that map to the same cache slot for a direct-mapped cache.

(c) For the main memory addresses of C101E and F0B30, give the corresponding tag and offset values for a fully-associatve cache.

(d) For the main memory addresses of C101E and F0B30, give the corresponding tag, cache set, and offset values for a two-way set-associative cache.