EE580 Discussion -- STA

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Static Timing Analysis (STA)

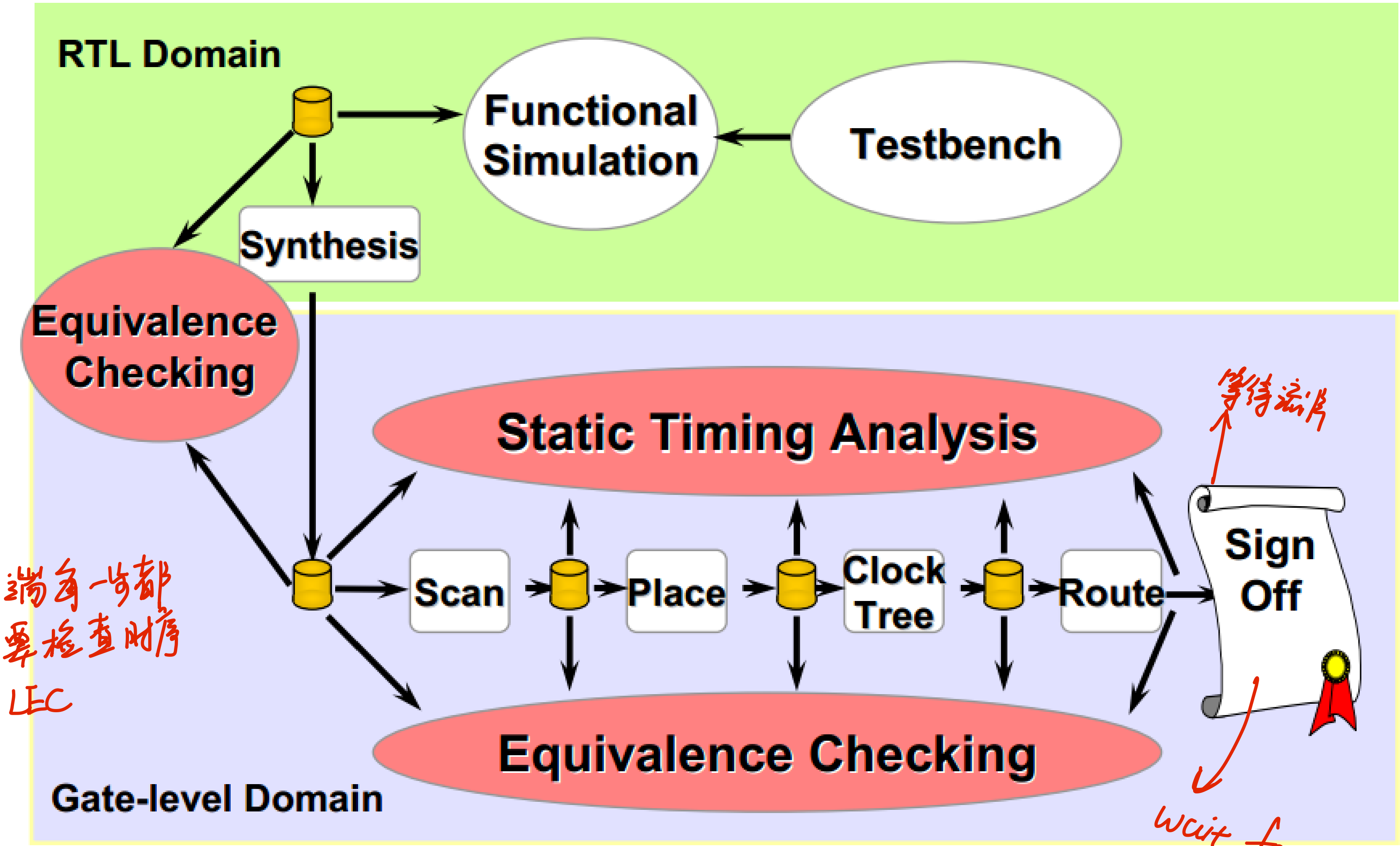
- **What's STA**
  - STA is a method of validating the timing performance of a design by checking all possible paths for timing violations.

- **Different with dynamical timing analysis**
  - **Full coverage:** removes the possibility that not all critical paths are identified

    穷举出所有的时序路径
  - **Higher speed:** especially for large complex designs
  - **Slightly pessimistic estimation:** e.g., wire load model
  - STA does not verify the functionality of a design. Also, certain design styles are not well suited for static approach. For instance, dynamic simulation may be required for asynchronous parts of a design and certainly for any mixed-signal portions.

why?

Static Verification Flow



后端每一步都
需要检查时序
和LEC

等待流片

wait for
fabrication

PrimeTime –overview

- PrimeTime is the Synopsys stand-alone full chip, gate-level static timing analyzer

并不依赖其他的工具

- Widely-adopted in industry and academia, sign-off tools

- Controlled by Tool command language (TCL) compatible with DC

Using Tcl scripts for running STA for huge project.

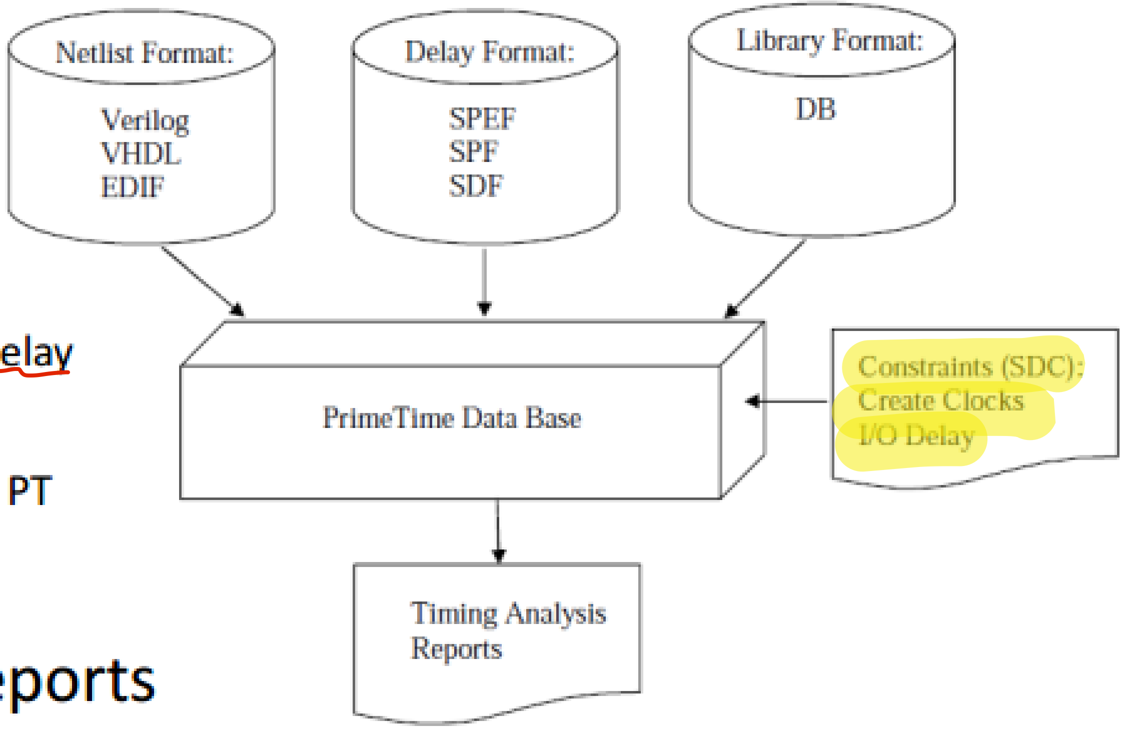
PrimeTime - Input/Output

what is the difference between .sdf and .db

- Inputs:
  - Netlist file
    - Verilog/VHDL/EDIF
  - Delay format:
    - SPEF/SPF/SDF
  - Database file (DB):
    - Determine the cell delay

?

  - SDC file:
    - Define the design to PT
- Outputs:
  - Timing Analysis Reports



Netlist Format:
Verilog
VHDL
EDIF

Delay Format:
SPEF
SPF
SDF

Library Format:
DB

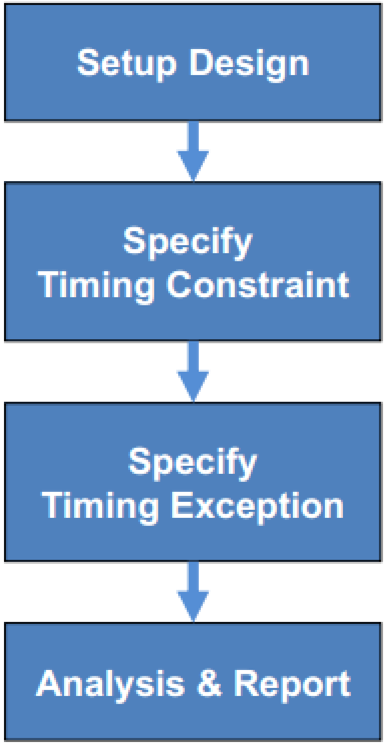
PrimeTime Data Base

Constraints (SDC):
Create Clocks
I/O Delay

Timing Analysis Reports

PrimeTime - STA Flow

Tcl 语法：set 用于创建变量并赋初值



Setup Design

Specify Timing Constraint

Specify Timing Exception

Analysis & Report

Setup Design:

- Set the search path and the link path

```
set search_path “lib path”
set link_library “* design.db”
set target_library “design.db”
```

- Read the design and the libraries

```
read_verilog top_level.v
current_design “top_level“
```

- Link the top design

```
link_design
```

PrimeTime - Specify timing constraints

- **Clock period Constraint**
  - create_clock

  # define the clock frequency

  - set_clock_uncertainty

  we should consider the worst-case of clock

  skew
  jitter
  duty cycle restoration

  # define delay between the clock branches (skew). For pre-layout.

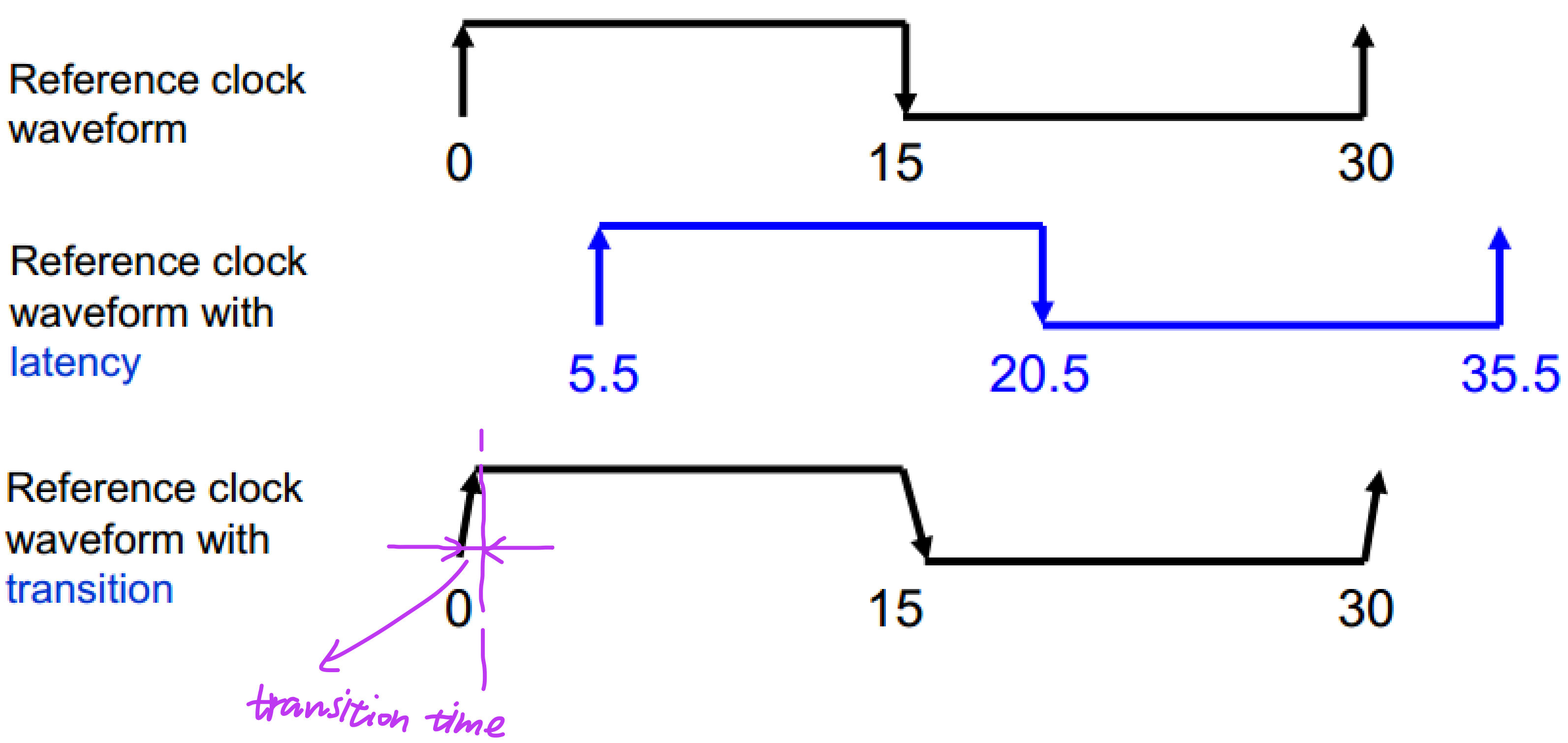
  - set_propagated_clock [all_clocks]

  # specifies that PrimeTime realized the latency for each clock path. This command should be used during post route analysis.

  - set_clock_latency
  - set_clock_transistion
  - set_input_delay
  - set_output_delay

  deal with the edge between two modules

PrimeTime - Specify timing constraints



Reference clock waveform

0

15

30

Reference clock waveform with latency

5.5

20.5

35.5

Reference clock waveform with transition

0

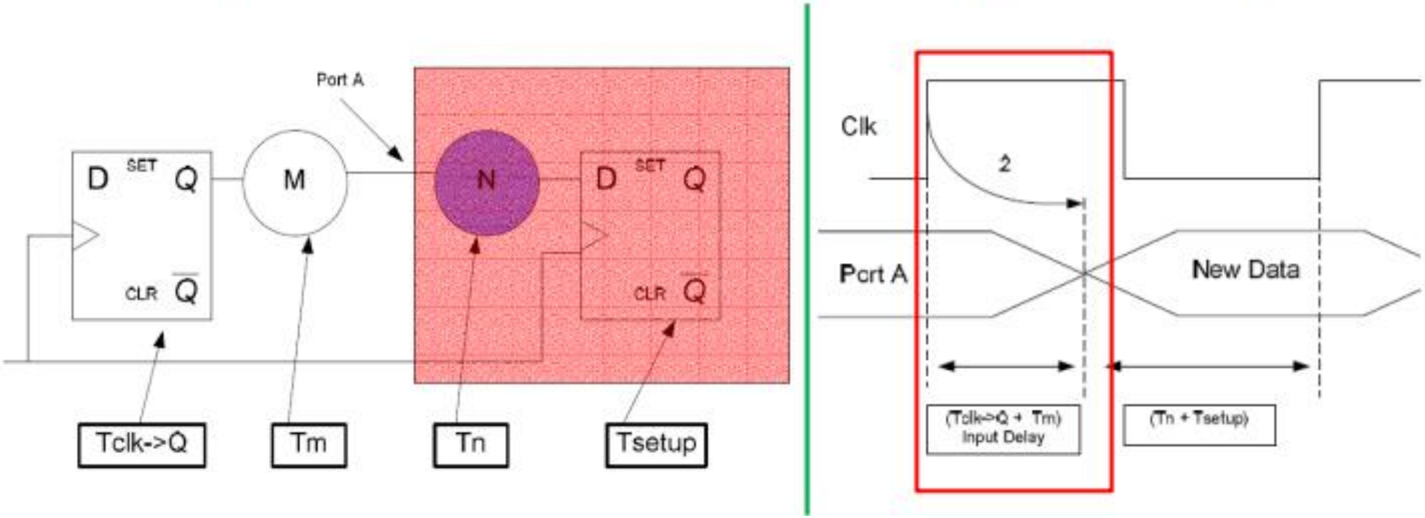
15

30

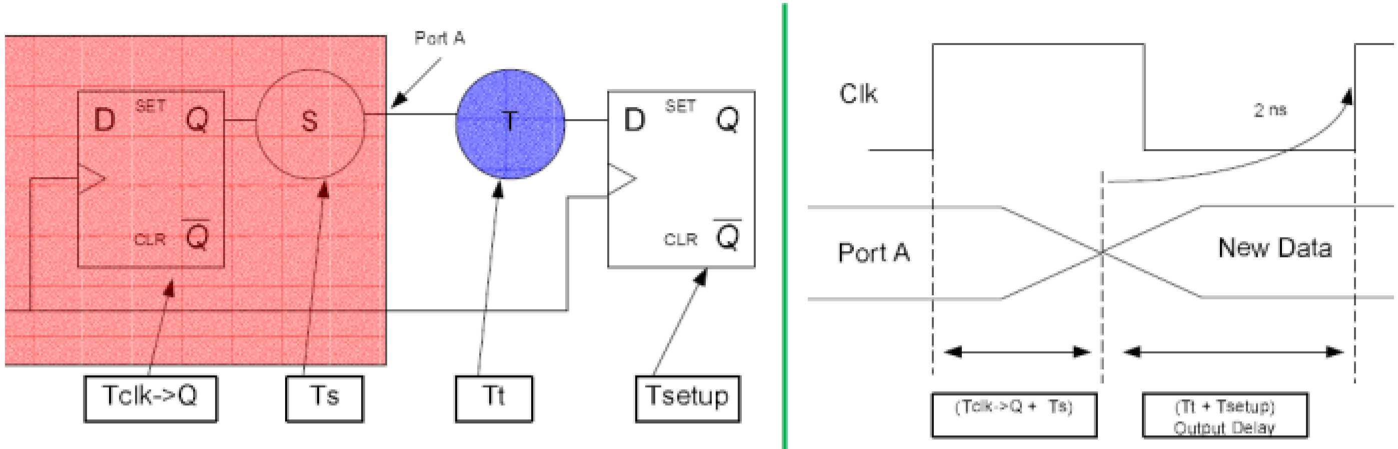
transition time

PrimeTime - Specify timing constraints

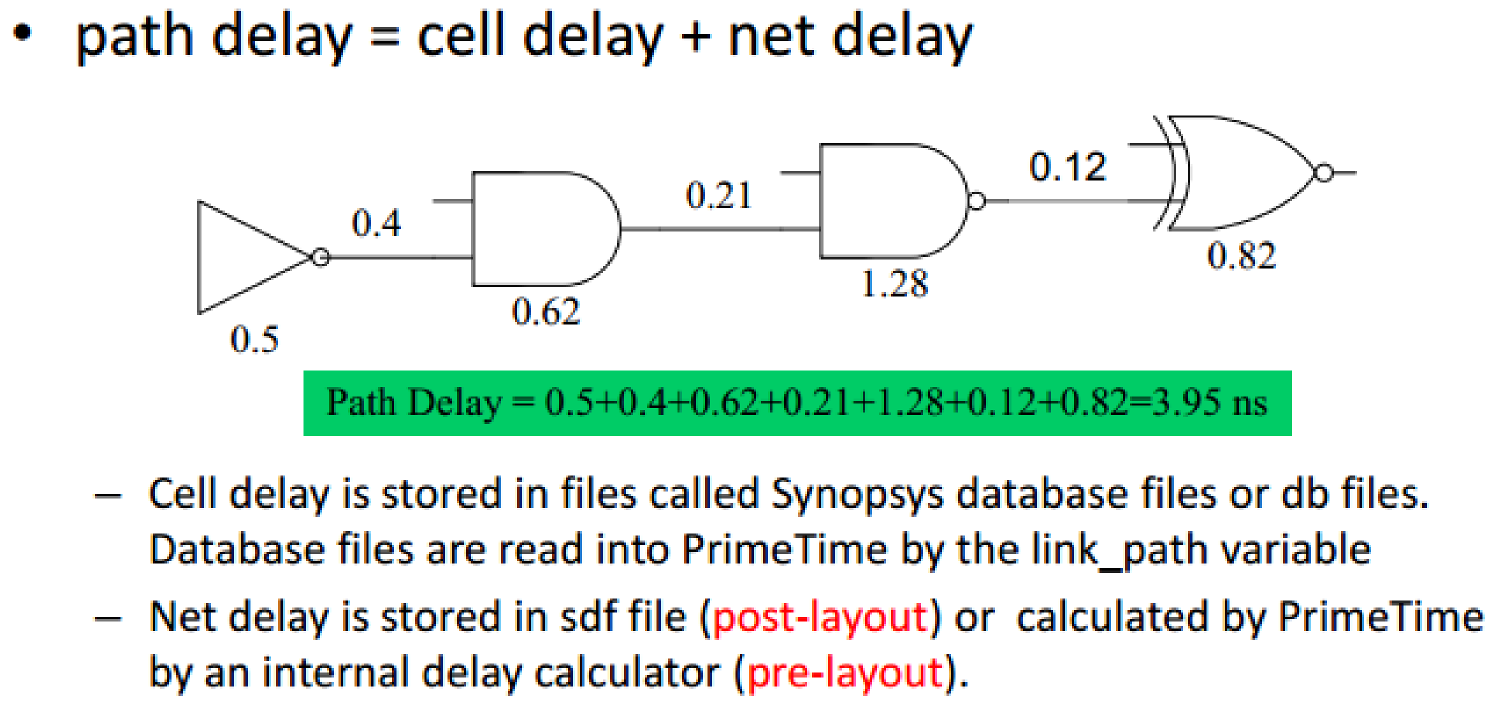
- Input Delay
  - Specify the delay of external logic driving current design



- Output Delay
  - Specify the delay of external logic driven by current design



PrimeTime - Path Delay Calculation



- path delay = cell delay + net delay

Path Delay = 0.5+0.4+0.62+0.21+1.28+0.12+0.82=3.95 ns

- Cell delay is stored in files called Synopsys database files or db files. Database files are read into PrimeTime by the link_path variable
- Net delay is stored in sdf file (post-layout) or calculated by PrimeTime by an internal delay calculator (pre-layout).

- **Script:**

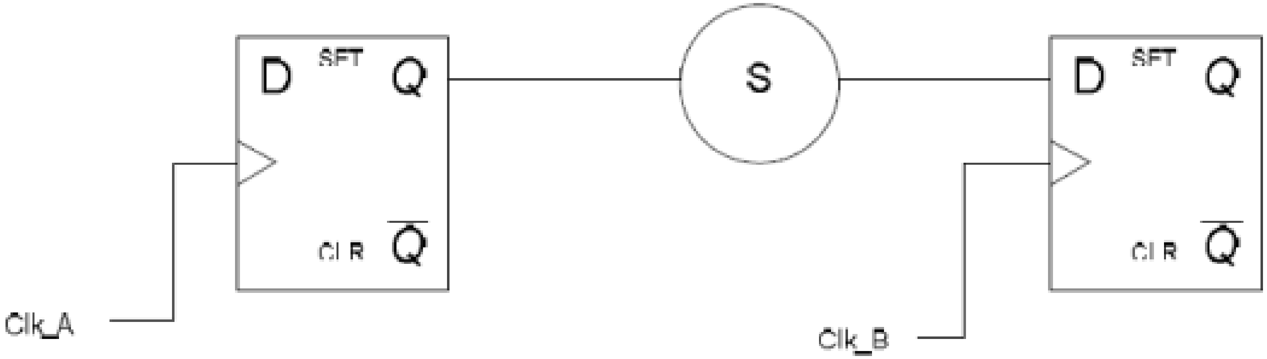
  set link_library “*.db”

  read_parasitics –format SPEF mult.spef

  read_sdf mult.sdf

PrimeTime - Timing Exception

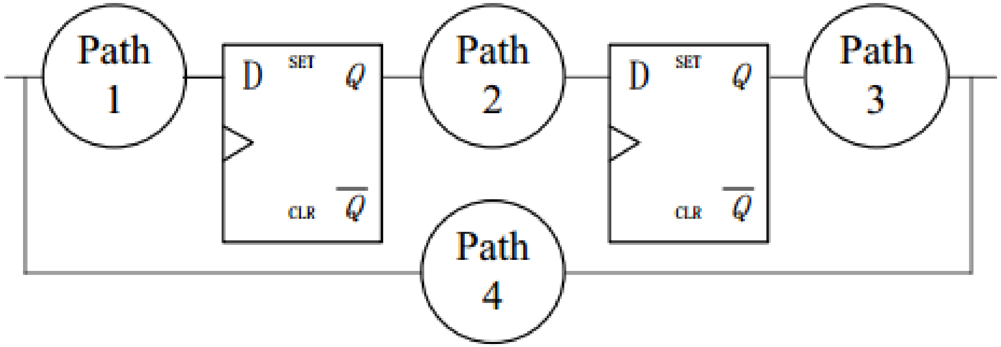
- False Path
  - paths in a design were a designer would not want the timing arcs to be calculated
    - Paths not relevant to functional operation of the circuit
    - paths which are impossible to exercise
    - Paths cross different clock domains



```
set_false_path -from clk_a -to clk_b
set_false_path -from clk_b -to clk_a
```

PrimeTime - Generating Reports

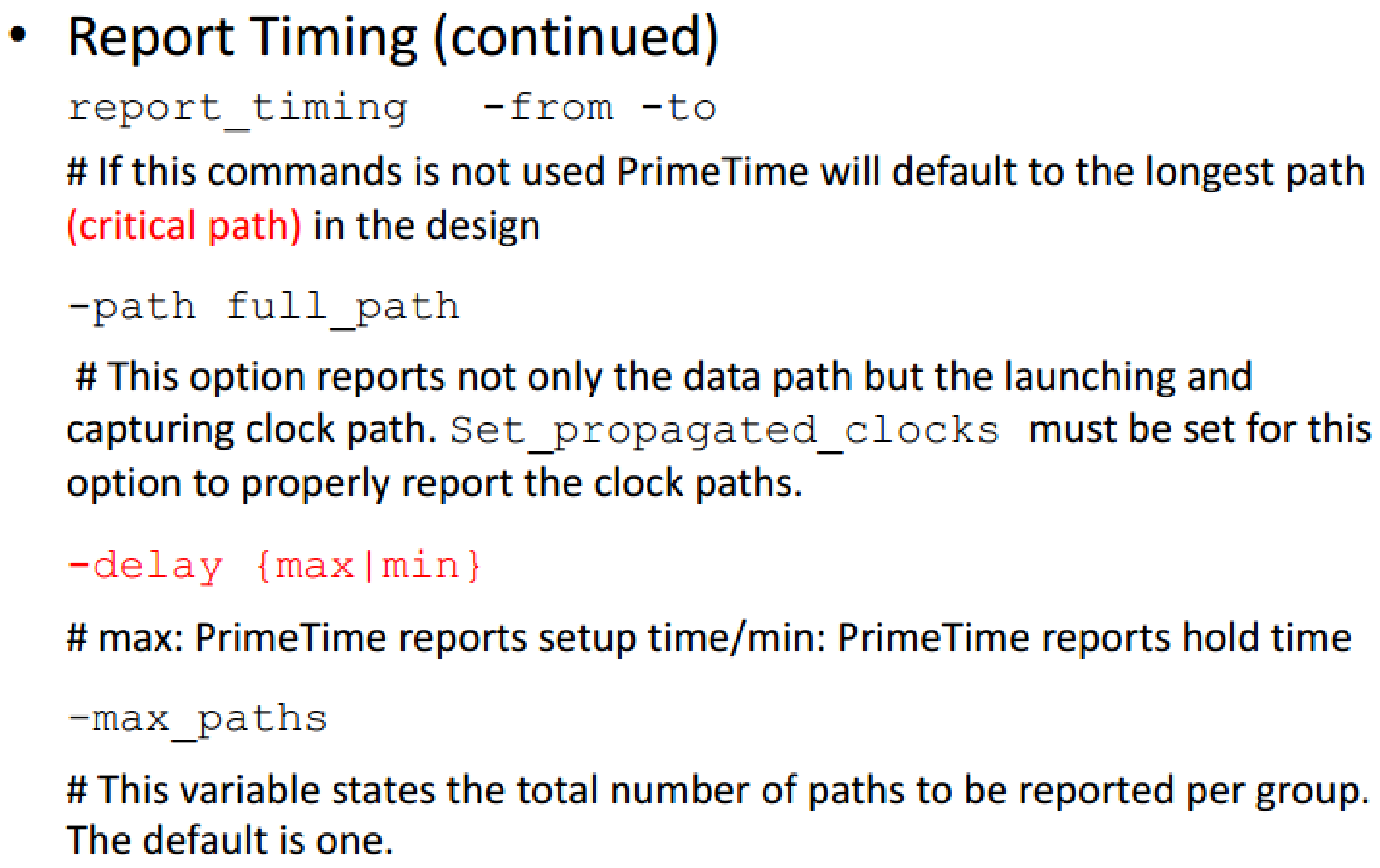
- Report Timing
  - To reduce the size and complexity of the PrimeTime reports, it is recommended to break the design into groups



P1: input to reg
P2: reg to reg
P3: reg to output
P4: input to output

```
report_timing   -from [all_registers -clock_pins]
                      [all_inputs]
                -to   [all_registers -data_pins]
                      [all_outputs]
```

PrimeTime - Generating Reports



- Report Timing (continued)

```
report_timing   -from -to
```

If this commands is not used PrimeTime will default to the longest path (critical path) in the design

```
-path full_path
```

This option reports not only the data path but the launching and capturing clock path. `Set_propagated_clocks` must be set for this option to properly report the clock paths.

```
-delay {max|min}
```

max: PrimeTime reports setup time/min: PrimeTime reports hold time

```
-max_paths
```

This variable states the total number of paths to be reported per group. The default is one.

PrimeTime - Generating Reports

- **Report Violation**

```
report_constraints -all_violators
# This command generates a summary of all paths that are violation setup
and hold times as well as and any cells that violation a design rule such as
fanout, capacitance, and transition. Viewing this one report will tell you if
changes will need to be made to your design.
```

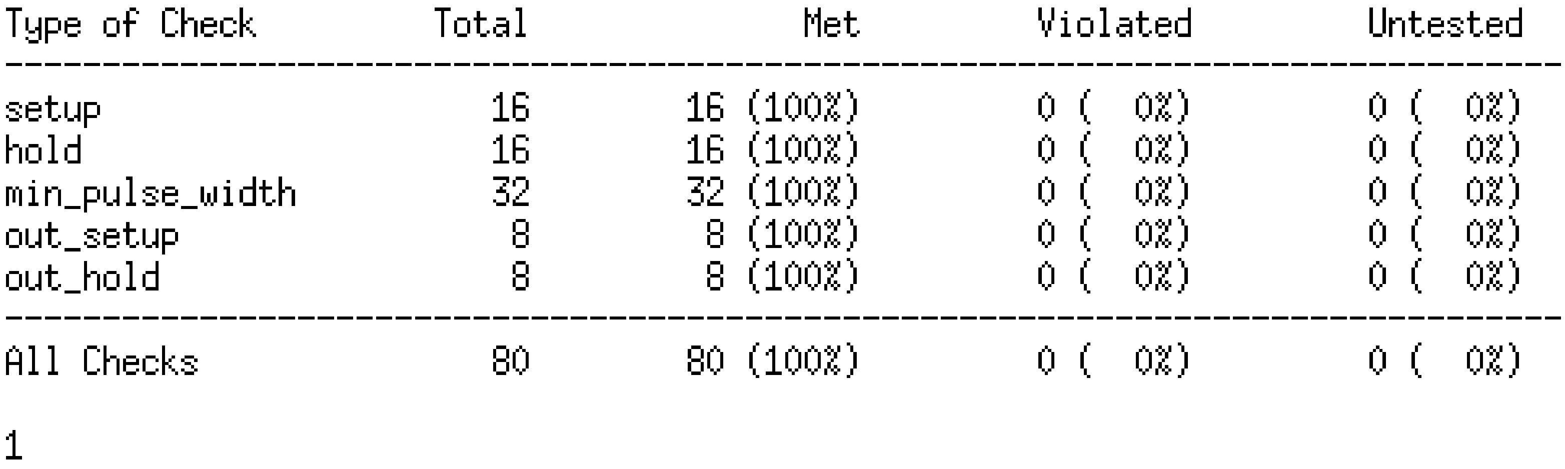
- **Report Clock Timing**

```
report_clock_timing -type skew -verbose
# This command will report clock skew, the difference between the longest
and shortest clock insertion time, and allow the design to evaluate whether
or not the clock tree must be re-synthesized. This is a powerful command
can save the designer from numerous timing closure spins.
```

PrimeTime - Generating Reports

report_analysis_coverage

# Generates a report about coverage of timing checks.



```
Type of Check          Total              Met         Violated         Untested
--------------------------------------------------------------------------------
setup                     16        16 (100%)          0 (   0%)       0 (   0%)
hold                      16        16 (100%)          0 (   0%)       0 (   0%)
min_pulse_width           32        32 (100%)          0 (   0%)       0 (   0%)
out_setup                  8         8 (100%)          0 (   0%)       0 (   0%)
out_hold                   8         8 (100%)          0 (   0%)       0 (   0%)
--------------------------------------------------------------------------------
All Checks                80        80 (100%)          0 (   0%)       0 (   0%)

1
```

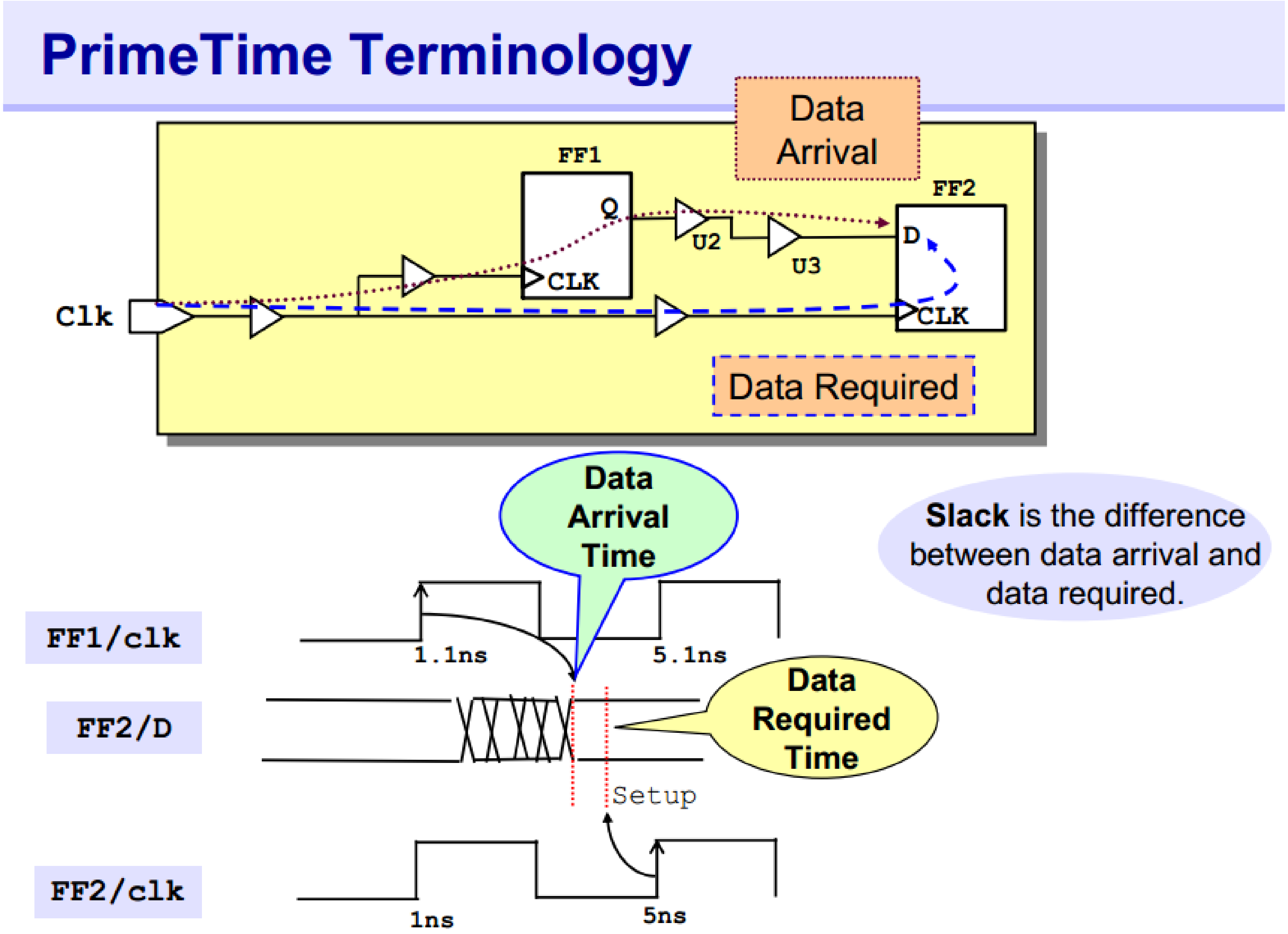
PrimeTime – timing report

Four Sections in a Timing Report

```
report_timing
```

```
                Startpoint: FF1 (rising edge-triggered flip-flop clocked by Clk)
                Endpoint: FF2 (rising edge-triggered flip-flop clocked by Clk)
Header          Path Group: Clk
                Path Type: max

                Point                                    Incr        Path
                ------------------------------------------------------------
                clock Clk (rise edge)                    0.00        0.00
                clock network delay (propagated)         1.10 *      1.10
                FF1/CLK (fdef1a15)                       0.00        1.10 r
Data            FF1/Q (fdef1a15)                         0.50 *      1.60 r
arrival         U2/Y  (buf1a27)                          0.11 *      1.71 r
                U3/Y  (buf1a27)                          0.11 *      1.82 r
                FF2/D (fdef1a15)                         0.05 *      1.87 r
                data arrival time                                    1.87

                clock Clk (rise edge)                    4.00        4.00
Data            clock network delay (propagated)         1.00 *      5.00
required        FF2/CLK (fdef1a15)                                   5.00 r
                library setup time                      -0.21 *      4.79
                data required time                                   4.79
                -------------------------------------------------------------
                data required time                                   4.79
Slack           data arrival time                                   -1.87
                -------------------------------------------------------------
                slack (MET)                                          2.92
```

PrimeTime – timing report



PrimeTime Terminology

Slack is the difference between data arrival and data required.

PrimeTime – timing report

The typical symbols shown in a PrimeTime report are defined as follows:

- “&” after an incremental delay number shows that the delay number is calculated with Resistor-Capacitor (RC) network back-annotation.
- “*” for Standard Delay Format (SDF) back-annotation
- “+” for lumped RC
- “H” for hybrid annotation
- “r” in the path column for the rising edge of the signal
- “f” in the path column for the falling edge of the signal

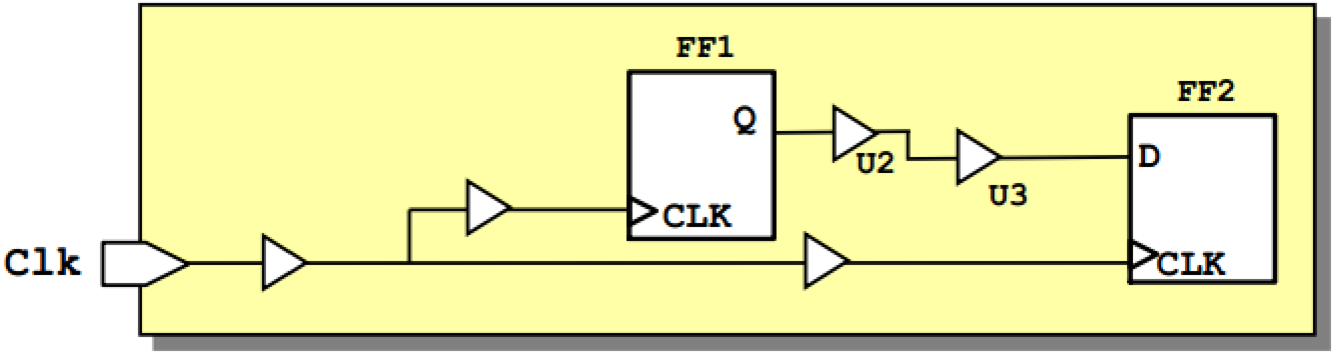
PrimeTime – timing report

Header

```
Startpoint: FF1 (rising edge-triggered flip-flop clocked by Clk)
Endpoint: FF2 (rising edge-triggered flip-flop clocked by Clk)
Path Group: Clk
Path Type: max
```

Capture clock

Report is for setup



PrimeTime – timing report

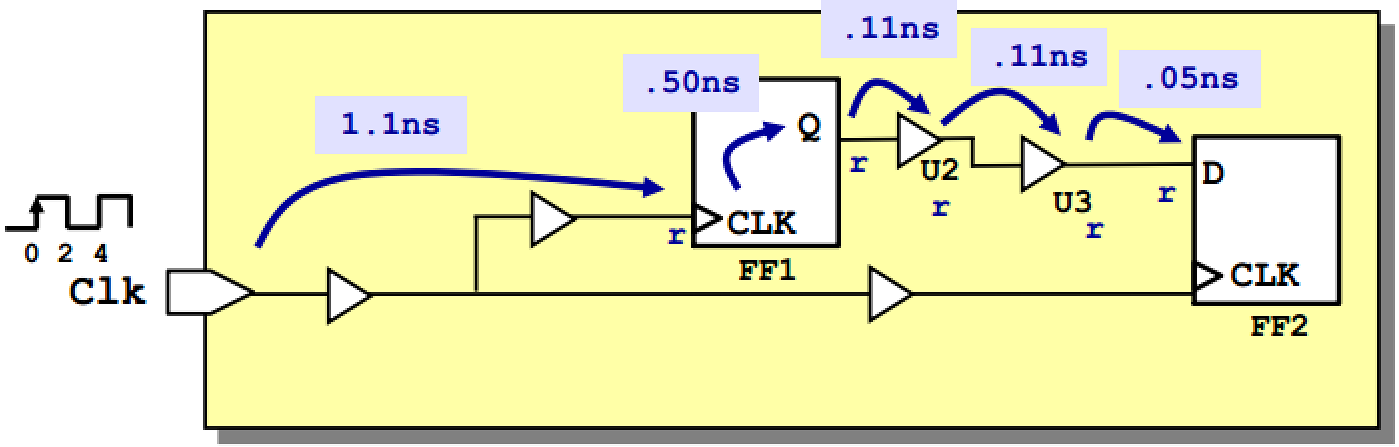
Calculated latency

SDF

```
Point                                        Incr        Path
-----------------------------------------------------------------
clock Clk (rise edge)                        0.00        0.00
clock network delay (propagated)             1.10 *      1.10
FF1/CLK (fdef1a15)                           0.00        1.10 r
FF1/Q (fdef1a15)                             0.50 *      1.60 r
U2/Y   (buf1a27)                             0.11 *      1.71 r
U3/Y   (buf1a27)                             0.11 *      1.82 r
FF2/D (fdef1a15)                             0.05 *      1.87 r
data arrival time                                        1.87
```

Data arrival

Library reference names

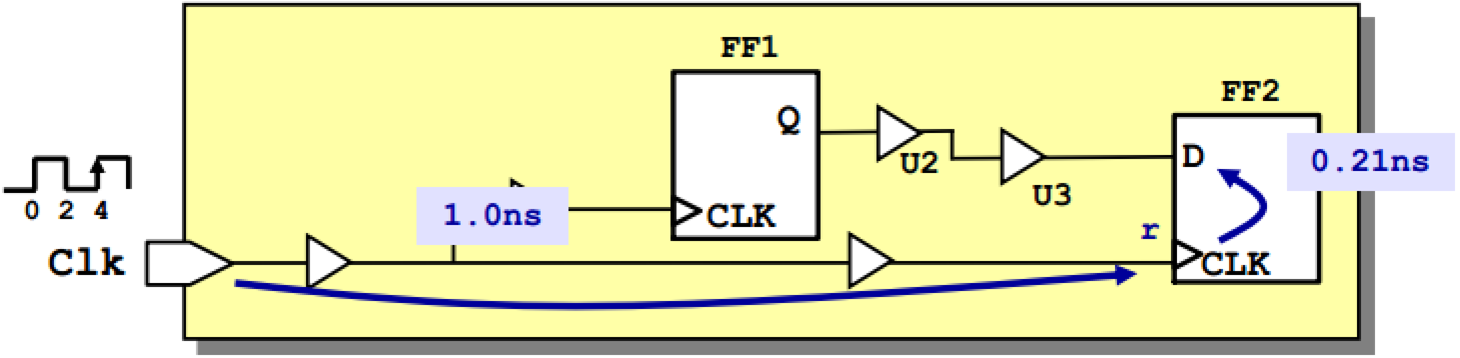


PrimeTime – timing report

```
Point                                     Incr        Path
------------------------------------------------------------
clock Clk (rise edge)                     0.00        0.00
clock network delay (propagated)          1.10 *      1.10
FF1/CLK (fdef1a15)                        0.00        1.10 r
FF1/Q (fdef1a15)                          0.50 *      1.60 r
U2/Y   (buf1a27)                          0.11 *      1.71 r
U3/Y   (buf1a27)                          0.11 *      1.82 r
FF2/D (fdef1a15)                          0.05 *      1.87 r
data arrival time                                     1.87

clock Clk (rise edge)                     4.00        4.00
clock network delay (propagated)          1.00 *      5.00
FF2/CLK (fdef1a15)                                    5.00 r
library setup time                       -0.21 *      4.79
data required time                                    4.79
```

Data required

SDF



PrimeTime – timing report

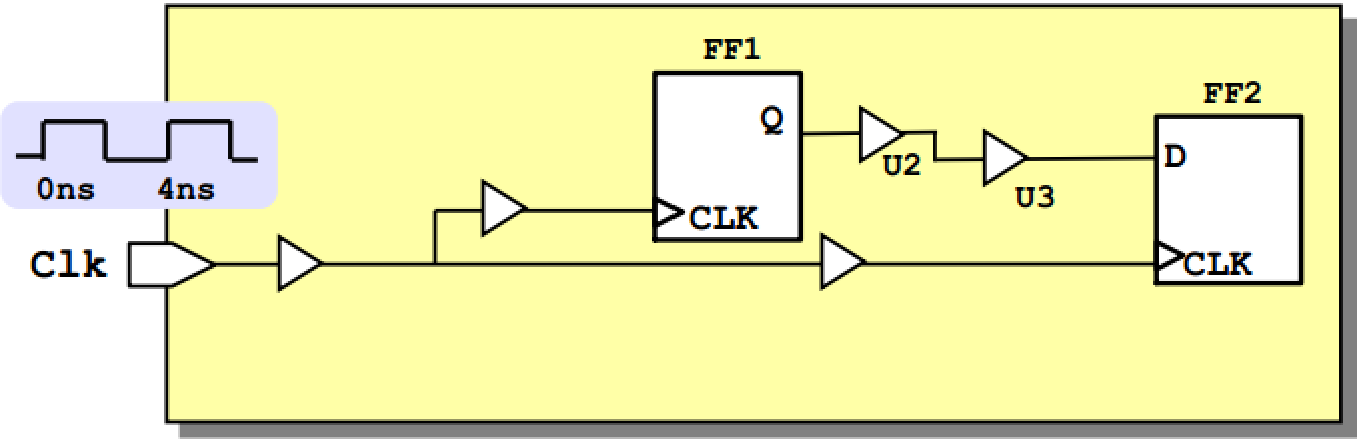
`report_timing`

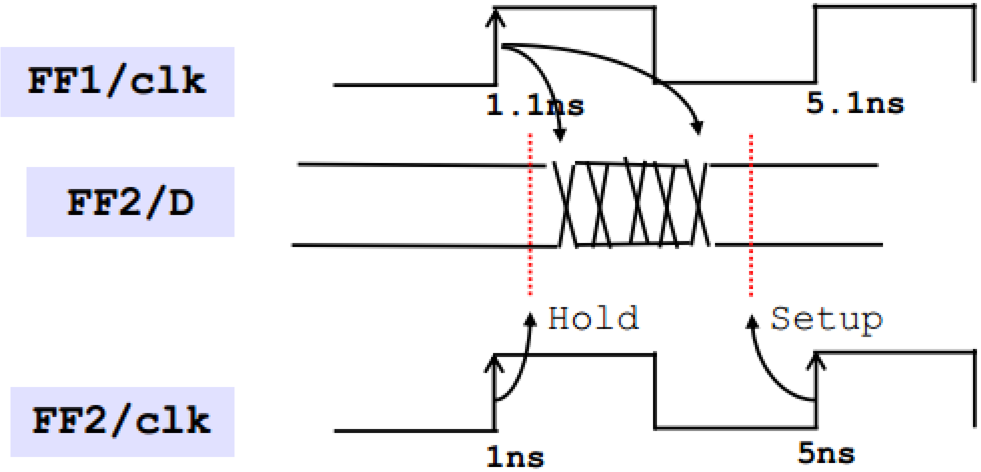
```
Startpoint: FF1 (rising edge-triggered flip-flop clocked by Clk)
Endpoint: FF2 (rising edge-triggered flip-flop clocked by Clk)
Path Group: Clk
Path Type: max

Point                                      Incr       Path
-----------------------------------------------------------
clock Clk (rise edge)                      0.00       0.00
clock network delay (propagated)           1.10 *     1.10
FF1/CLK (fdef1a15)                         0.00       1.10 r
FF1/Q (fdef1a15)                           0.50 *     1.60 r
U2/Y   (buf1a27)                           0.11 *     1.71 r
U3/Y   (buf1a27)                           0.11 *     1.82 r
FF2/D (fdef1a15)                           0.05 *     1.87 r
data arrival time                                     1.87

clock Clk (rise edge)                      4.00       4.00
clock network delay (propagated)           1.00 *     5.00
FF2/CLK (fdef1a15)                                    5.00 r
library setup time                        -0.21 *     4.79
data required time                                    4.79
------------------------------------------------------------
data required time                                    4.79
data arrival time                                    -1.87
------------------------------------------------------------
slack (MET)                                           2.92
```

Slack

PrimeTime – timing report

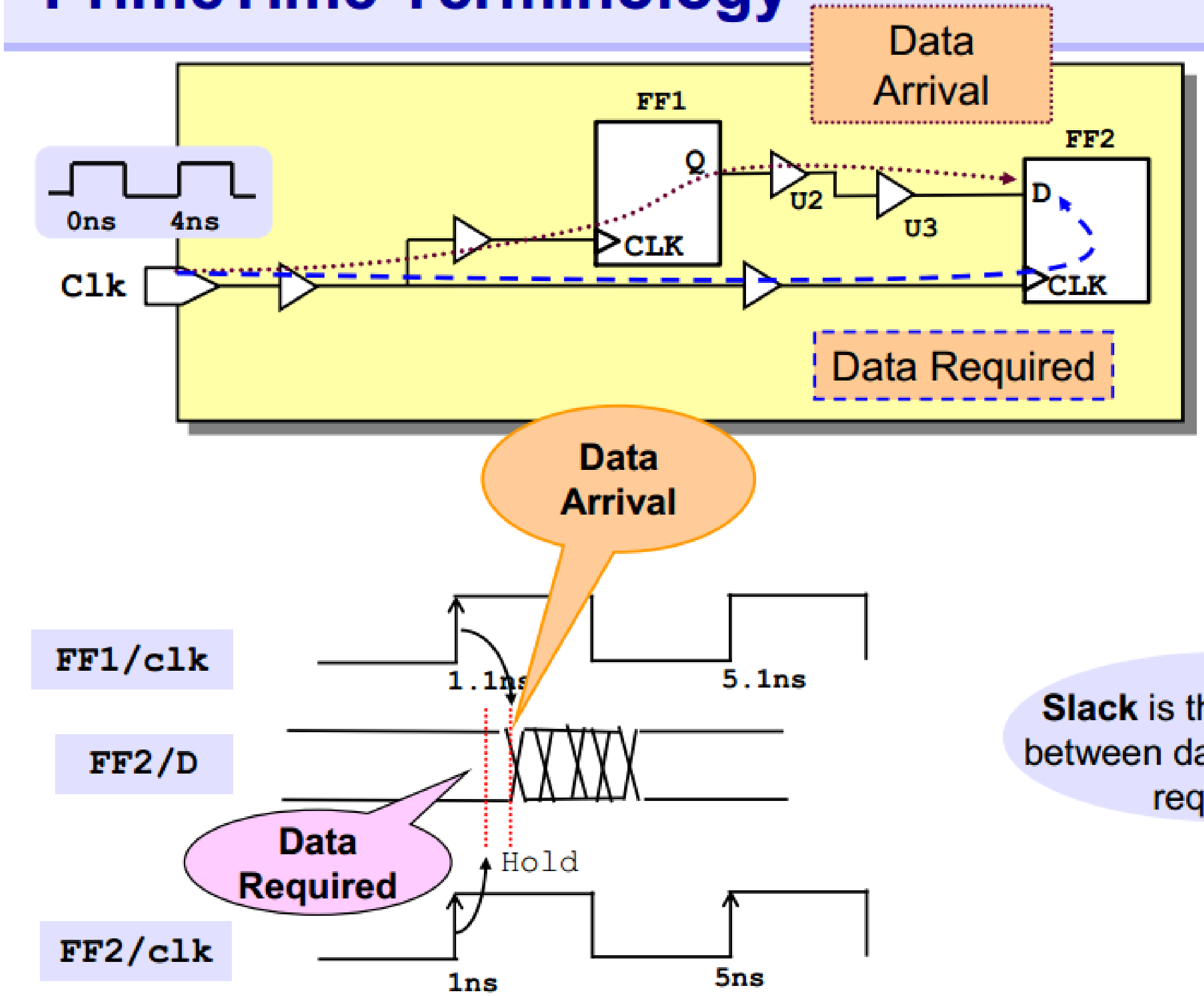
- **Which Edges are Used in a Timing Report?**





PrimeTime – timing report

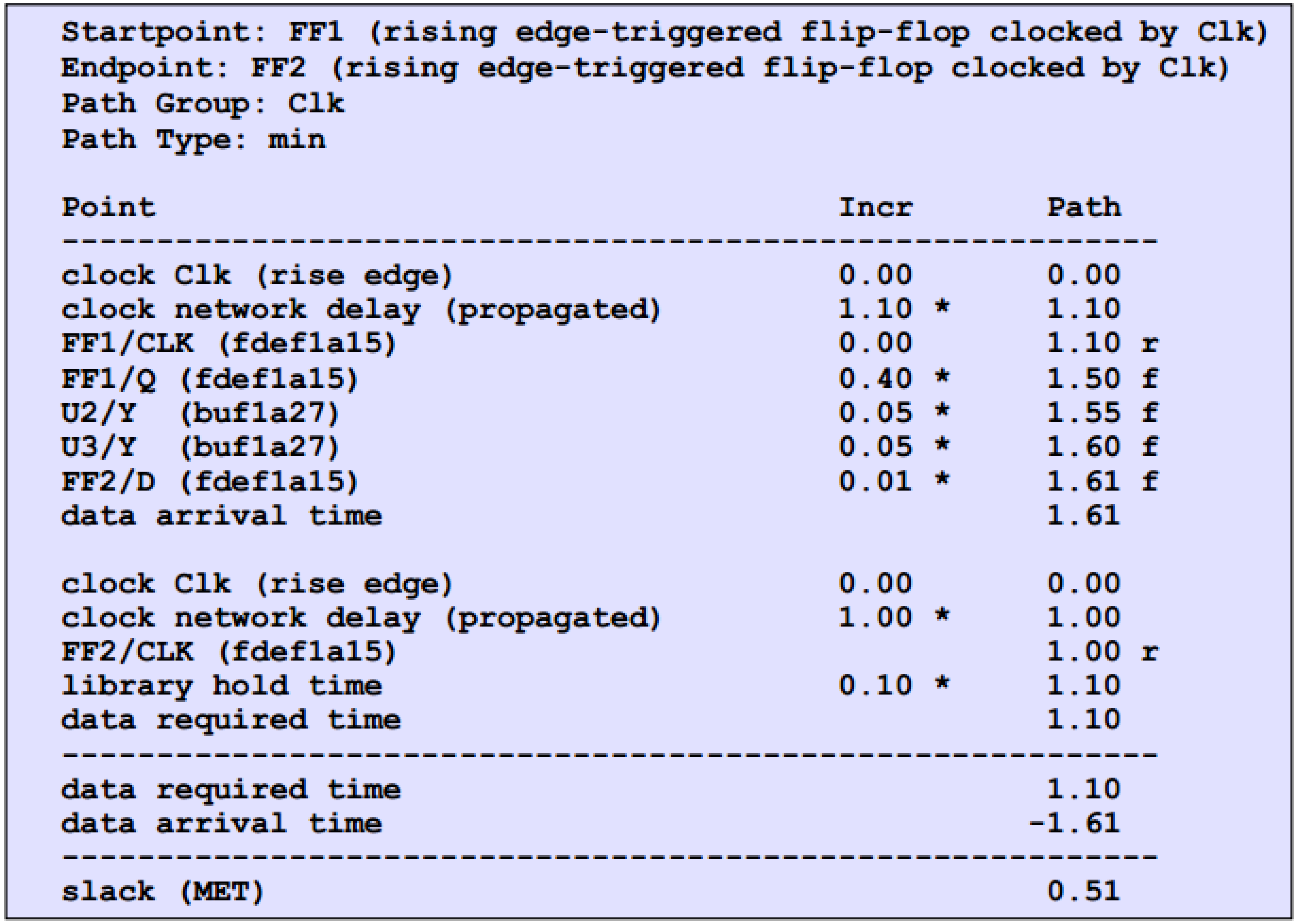
PrimeTime Terminology



Slack is the difference between data arrival and required.

PrimeTime – timing report

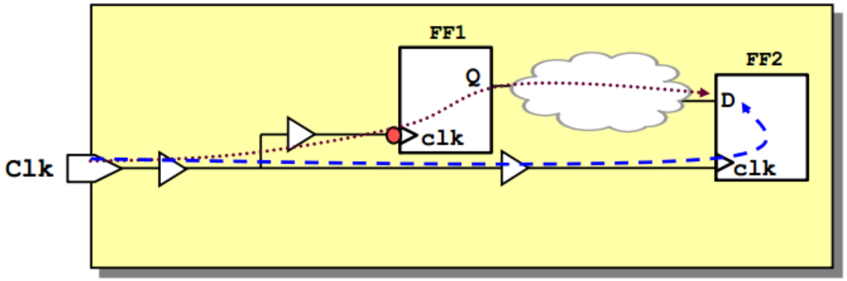
- **Example of Hold Timing report**

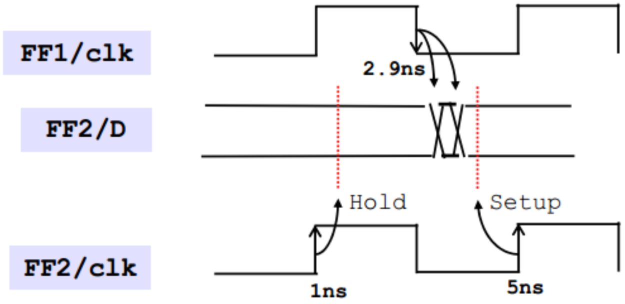


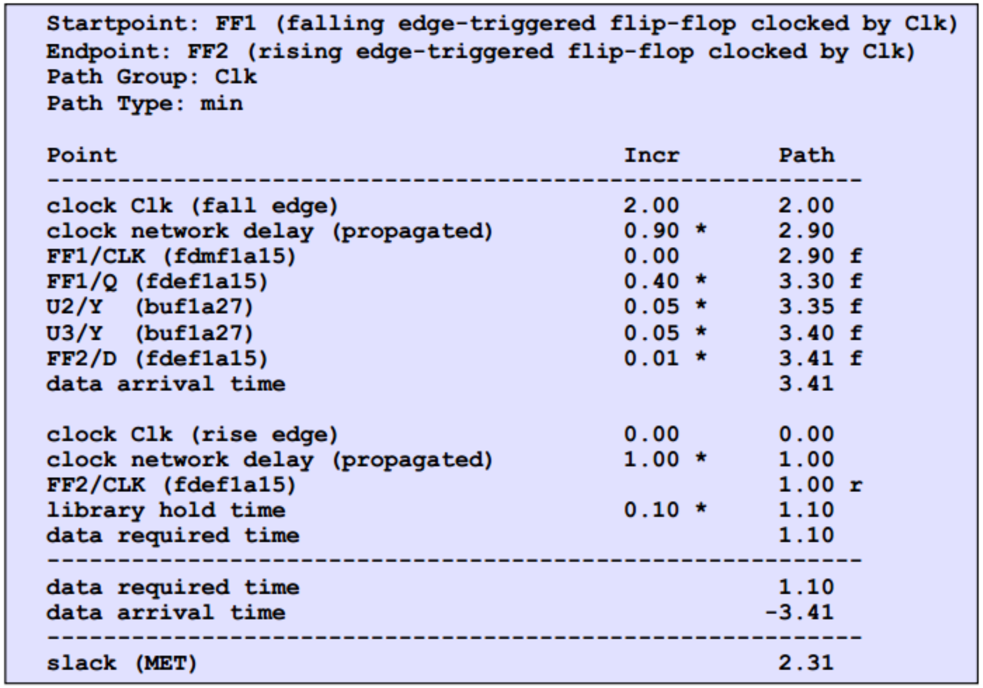
```
Startpoint: FF1 (rising edge-triggered flip-flop clocked by Clk)
Endpoint: FF2 (rising edge-triggered flip-flop clocked by Clk)
Path Group: Clk
Path Type: min

Point                                    Incr       Path
----------------------------------------------------------
clock Clk (rise edge)                    0.00       0.00
clock network delay (propagated)         1.10 *     1.10
FF1/CLK (fdef1a15)                       0.00       1.10 r
FF1/Q (fdef1a15)                         0.40 *     1.50 f
U2/Y  (buf1a27)                          0.05 *     1.55 f
U3/Y  (buf1a27)                          0.05 *     1.60 f
FF2/D (fdef1a15)                         0.01 *     1.61 f
data arrival time                                   1.61

clock Clk (rise edge)                    0.00       0.00
clock network delay (propagated)         1.00 *     1.00
FF2/CLK (fdef1a15)                                  1.00 r
library hold time                        0.10 *     1.10
data required time                                  1.10
----------------------------------------------------------
data required time                                  1.10
data arrival time                                  -1.61
----------------------------------------------------------
slack (MET)                                         0.51
```

PrimeTime – timing report

- **Negative edge triggered FF**







```
Startpoint: FF1 (falling edge-triggered flip-flop clocked by Clk)
Endpoint: FF2 (rising edge-triggered flip-flop clocked by Clk)
Path Group: Clk
Path Type: min

Point                                     Incr        Path
----------------------------------------------------------
clock Clk (fall edge)                     2.00        2.00
clock network delay (propagated)          0.90 *      2.90
FF1/CLK (fdmf1a15)                        0.00        2.90 f
FF1/Q (fdef1a15)                          0.40 *      3.30 f
U2/Y  (buf1a27)                           0.05 *      3.35 f
U3/Y  (buf1a27)                           0.05 *      3.40 f
FF2/D (fdef1a15)                          0.01 *      3.41 f
data arrival time                                     3.41

clock Clk (rise edge)                     0.00        0.00
clock network delay (propagated)          1.00 *      1.00
FF2/CLK (fdef1a15)                                    1.00 r
library hold time                         0.10 *      1.10
data required time                                    1.10
----------------------------------------------------------
data required time                                    1.10
data arrival time                                    -3.41
----------------------------------------------------------
slack (MET)                                           2.31
```

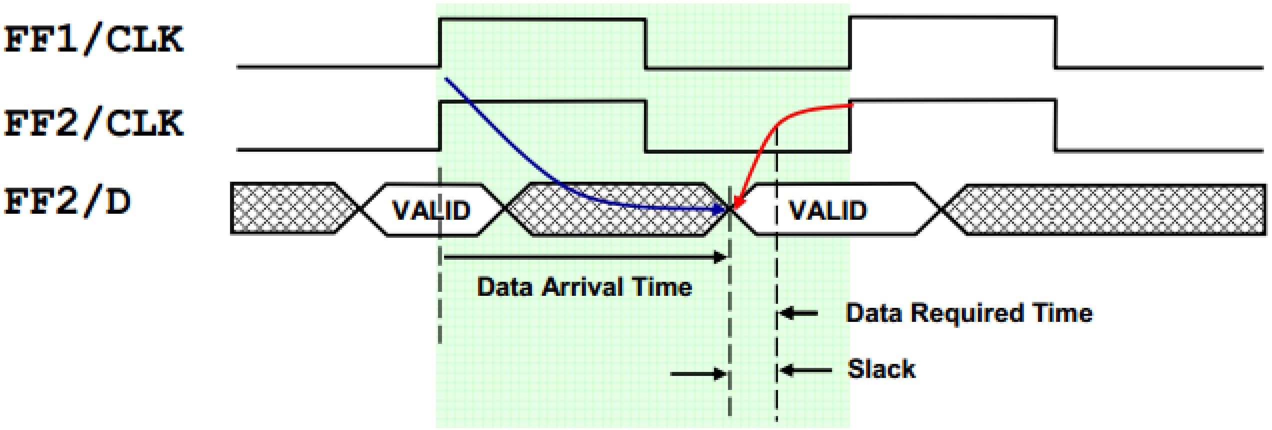
Setup check summary

Data must become valid and stable at least one setup time before being captured by flip-flop.

EQN 1 $\text{Slack}_{\text{setup}} = \text{Data Required Time} - \text{Data Arrival Time} \geq 0$

EQN 2 $\text{Slack}_{\text{setup}} = (T_{\text{capture}} - t_{\text{setup}}) - (T_{\text{launch}} + t_{\text{prop}}) \geq 0$

Clk Spec Library Clk Spec Cell + Net



Hold check summary

Data remains stable for a minimum time as required by capture flip-flop. (Hold Check)

EQN 1 $\text{Slack}_{\text{hold}} = \text{Data Arrival Time} - \text{Data Required Time} \geq 0$

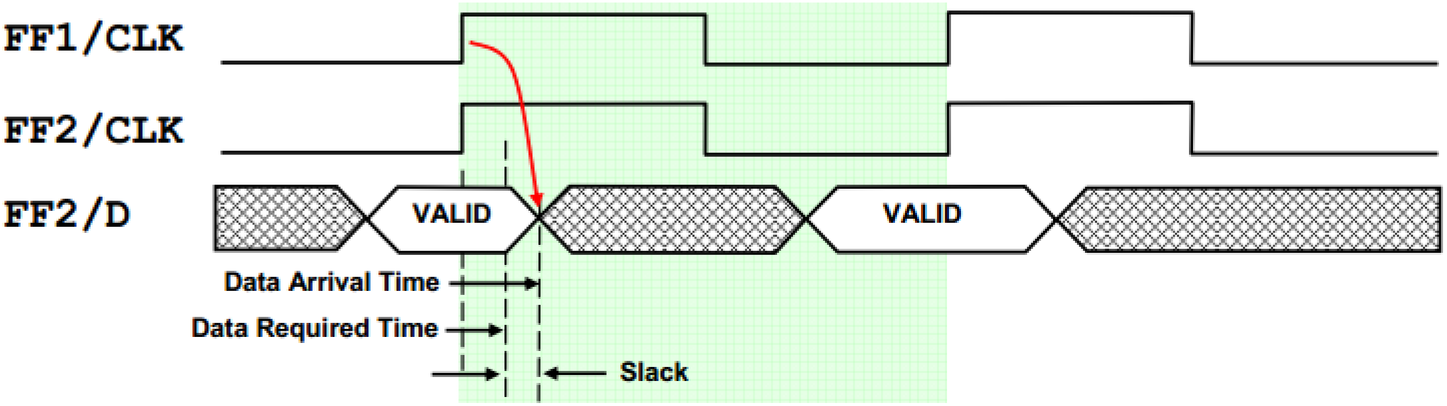
EQN 2 $\text{Slack}_{\text{hold}} = (T_{\text{launch}} + t_{\text{prop}}) - (T_{\text{capture}} + t_{\text{hold}}) \geq 0$

Clk Spec

Cell + Net

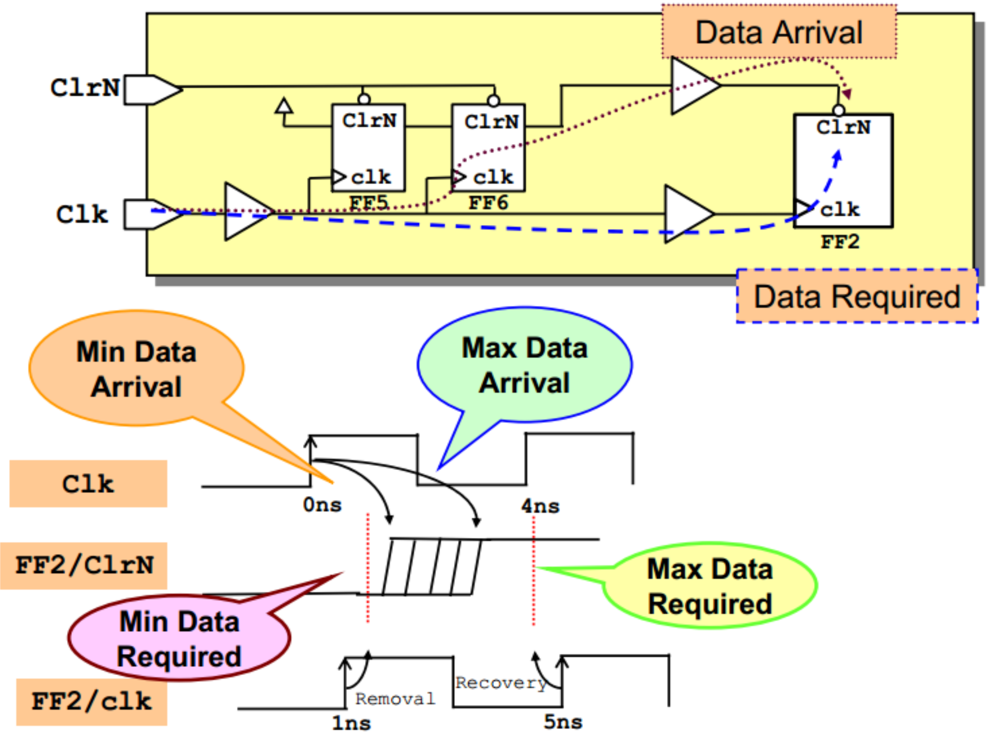
Clk Spec

Library



Recovery/Removal check

- **For asynchronous input pin of FF**
- Although a flip-flop is asynchronously set or clear , the negation from its reset state is synchronous .
- A **recovery** timing check specifies a minimum amount of time allowed between the release of a asynchronous signal from the active state to the next active clock edge .
- A **removal** timing check specifies the minimum amount of time between an active edge and the release of an asynchronous control signal.



Delays

- RTL Simulation
  - No gate delay , No wire-delays
- Post Synthesis Simulation
  - Gate Delays, No wire-delay considered
- Post Synthesis Simulation with Annotation Information
  - Wire-delays are modeled based on wire-models (estimated)
- Post Layout Annotation Information
  - Wire delays are accurately estimated.

Suggestions

- Pre-/Post layout design

Getting experienced by comparing pre- and post- layout design

Set reasonable timing margin to avoid **LARGE** loop in design flow, e.g.,

- clock_uncertainty : justify the value with post-layout report
- clock_period: post-layout period= pre-layout period + margin, depending on process technology

Meet timing requirement as early as possible

- keep in mind the delay information when design the circuits, e.g., pipeline schedule, parallel, et. al.
- set reasonable constraint for synthesis
- optimize the design at early stage of P&R

Commands in Primetime

On pt_shell prompt:

- To see list of available commands, use “help”
- To see detailed description of any command “man <command_name>”
- Ex: man read_verilog
- Get yourself familiarize with the commands used in your script
- When entering individual command on dc_shell prompt, if command is successful, then “1” is displayed at the end of output of command.