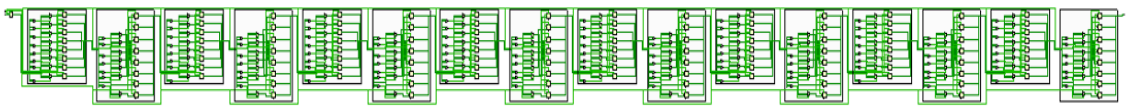
# Report for Homework 1

Github repo: https://github.com/KevinWang96/EE599_YihaoWang_7410178057

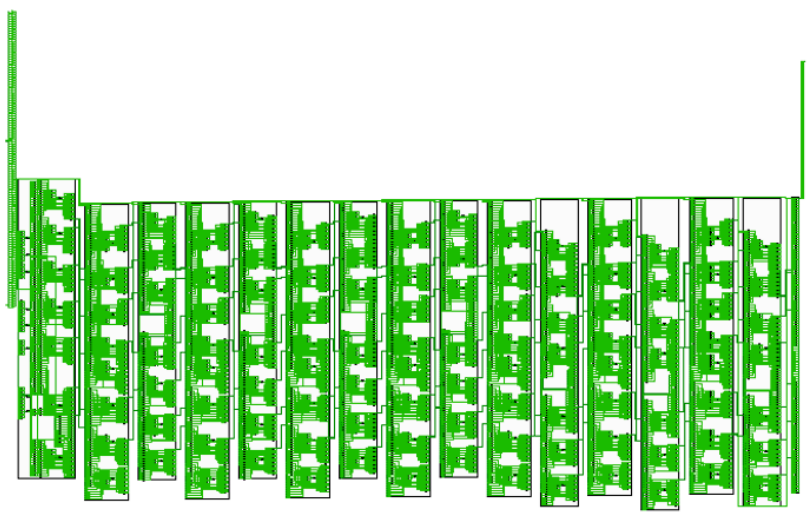
1. **Odd-even Transposition Sort**

   **(a) 16 elements design**

   Schematic of elaboration:



   Schematic of synthesized design:



   Resource report:

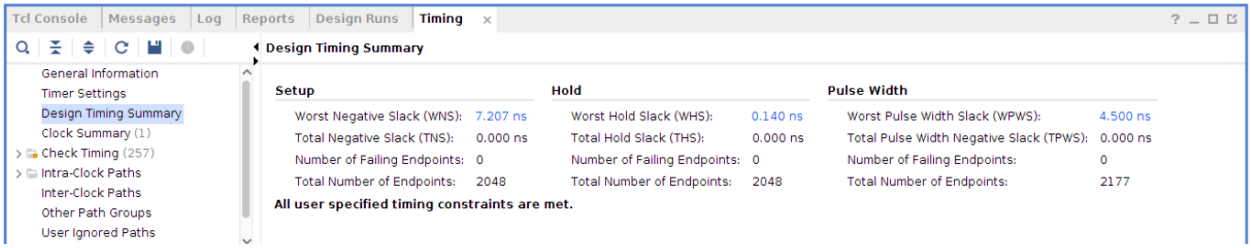
Tcl Console | Messages | Log | Reports | Design Runs | Power | Utilization

Hierarchy

- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (10%)
    - LUT as Logic (10%)
  - Slice Registers (8%)
    - Register as Flip Flop (8
- Memory
- DSP
- IO and GT Specific
  - Bonded IOB (>100%)
- Clocking
  - BUFGCTRL (3%)
- Specific Feature
- Primitives
- Black Boxes
- Instantiated Netlists

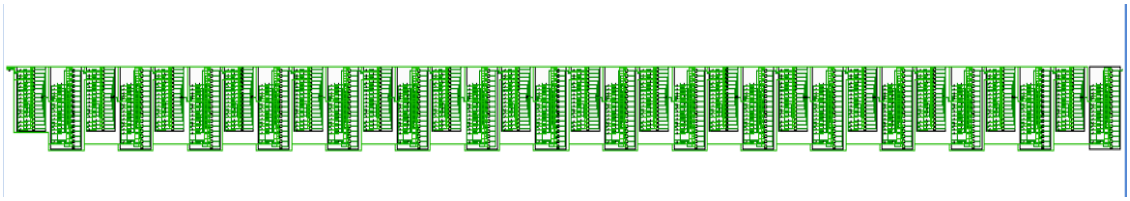
| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| odd_even_sort | 1440 | 2176 | 258 | 1 |
| genblk1.stage_loop[0].stage (odd_even_sort_stage) | 180 | 128 | 0 | 0 |
| genblk1.stage_loop[1].stage (odd_even_sort_stage__parameterized0_5) | 96 | 128 | 0 | 0 |
| genblk1.stage_loop[2].stage (odd_even_sort_stage_6) | 84 | 128 | 0 | 0 |
| genblk1.stage_loop[3].stage (odd_even_sort_stage__parameterized0_7) | 96 | 128 | 0 | 0 |
| genblk1.stage_loop[4].stage (odd_even_sort_stage_8) | 84 | 128 | 0 | 0 |
| genblk1.stage_loop[5].stage (odd_even_sort_stage__parameterized0_9) | 96 | 128 | 0 | 0 |
| genblk1.stage_loop[6].stage (odd_even_sort_stage_10) | 84 | 128 | 0 | 0 |
| genblk1.stage_loop[7].stage (odd_even_sort_stage__parameterized0_11) | 96 | 128 | 0 | 0 |
| genblk1.stage_loop[8].stage (odd_even_sort_stage_12) | 84 | 128 | 0 | 0 |
| genblk1.stage_loop[9].stage (odd_even_sort_stage__parameterized0_13) | 96 | 128 | 0 | 0 |
| genblk1.stage_loop[10].stage (odd_even_sort_stage_0) | 84 | 128 | 0 | 0 |
| genblk1.stage_loop[11].stage (odd_even_sort_stage__parameterized0) | 96 | 128 | 0 | 0 |
| genblk1.stage_loop[12].stage (odd_even_sort_stage_1) | 84 | 128 | 0 | 0 |
| genblk1.stage_loop[13].stage (odd_even_sort_stage__parameterized0_2) | 96 | 128 | 0 | 0 |
| genblk1.stage_loop[14].stage (odd_even_sort_stage_3) | 84 | 128 | 0 | 0 |
| genblk1.stage_loop[15].stage (odd_even_sort_stage__parameterized0_4) | 0 | 128 | 0 | 0 |

Timing report:

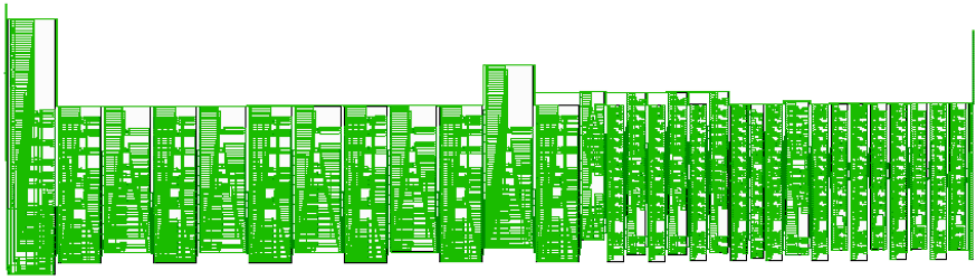



## (b) 32 elements design

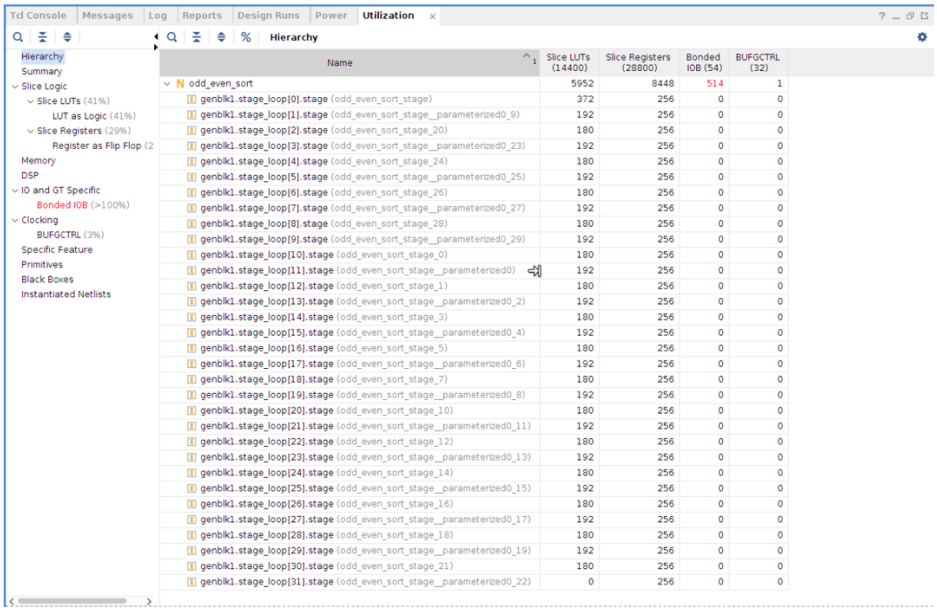
Schematic of elaboration:



Schematic of synthesized design:

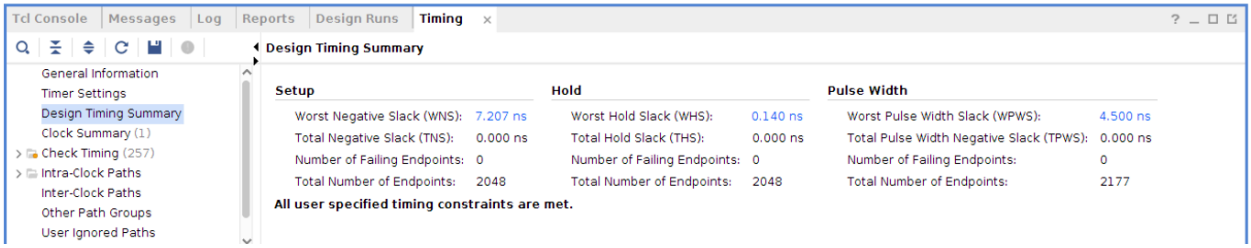


Resource report:




| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| odd_even_sort | 5952 | 8448 | 514 | 1 |
| genblk1.stage_loop[0].stage (odd_even_sort_stage) | 372 | 256 | 0 | 0 |
| genblk1.stage_loop[1].stage (odd_even_sort_stage__parameterized0_9) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[2].stage (odd_even_sort_stage_20) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[3].stage (odd_even_sort_stage__parameterized0_23) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[4].stage (odd_even_sort_stage_24) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[5].stage (odd_even_sort_stage__parameterized0_25) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[6].stage (odd_even_sort_stage_26) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[7].stage (odd_even_sort_stage__parameterized0_27) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[8].stage (odd_even_sort_stage_28) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[9].stage (odd_even_sort_stage__parameterized0_29) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[10].stage (odd_even_sort_stage_0) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[11].stage (odd_even_sort_stage__parameterized0) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[12].stage (odd_even_sort_stage_1) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[13].stage (odd_even_sort_stage__parameterized0_2) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[14].stage (odd_even_sort_stage_3) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[15].stage (odd_even_sort_stage__parameterized0_4) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[16].stage (odd_even_sort_stage_5) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[17].stage (odd_even_sort_stage__parameterized0_6) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[18].stage (odd_even_sort_stage_7) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[19].stage (odd_even_sort_stage__parameterized0_8) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[20].stage (odd_even_sort_stage_10) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[21].stage (odd_even_sort_stage__parameterized0_11) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[22].stage (odd_even_sort_stage_12) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[23].stage (odd_even_sort_stage__parameterized0_13) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[24].stage (odd_even_sort_stage_14) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[25].stage (odd_even_sort_stage__parameterized0_15) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[26].stage (odd_even_sort_stage_16) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[27].stage (odd_even_sort_stage__parameterized0_17) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[28].stage (odd_even_sort_stage_18) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[29].stage (odd_even_sort_stage__parameterized0_19) | 192 | 256 | 0 | 0 |
| genblk1.stage_loop[30].stage (odd_even_sort_stage_21) | 180 | 256 | 0 | 0 |
| genblk1.stage_loop[31].stage (odd_even_sort_stage__parameterized0_22) | 0 | 256 | 0 | 0 |

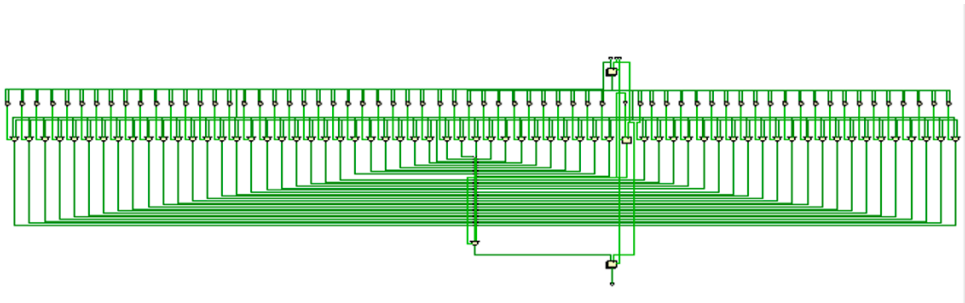
Timing report:



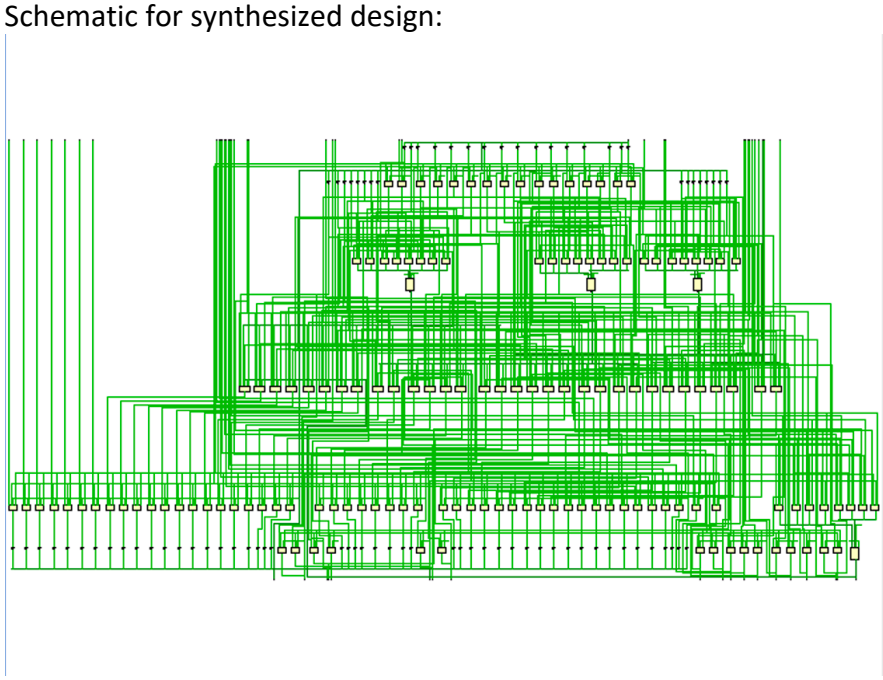

**(c) 64 elements design**

Note that the previous design is based on pipeline design which consume too much resource. FPGA can't support it for 64 elements or 128 elements sorting, so I change my design into one stage design which save resource but decrease the throughput.

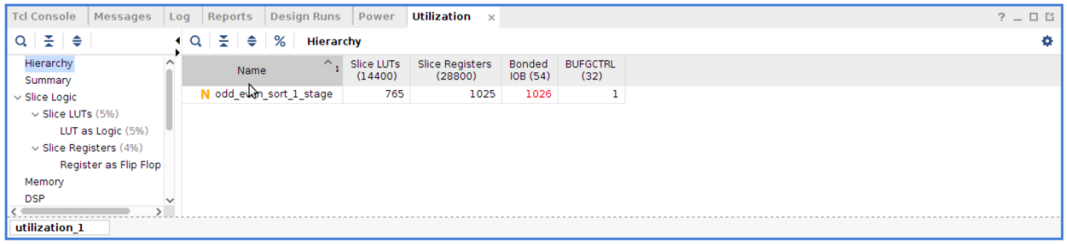
Schematic for elaboration:



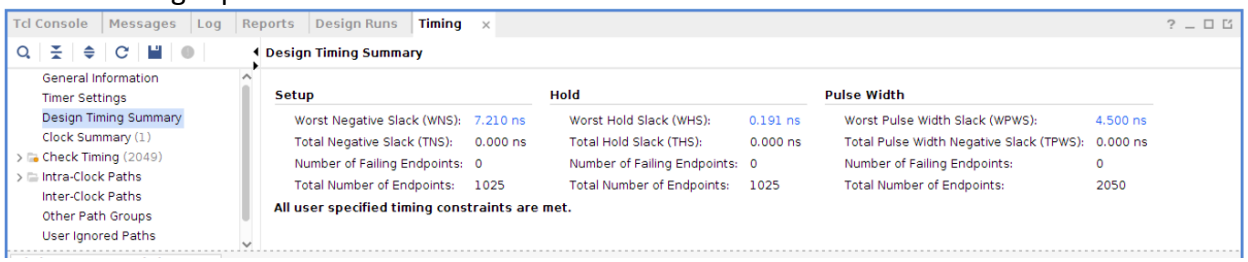
Schematic for synthesized design:



Resource report:

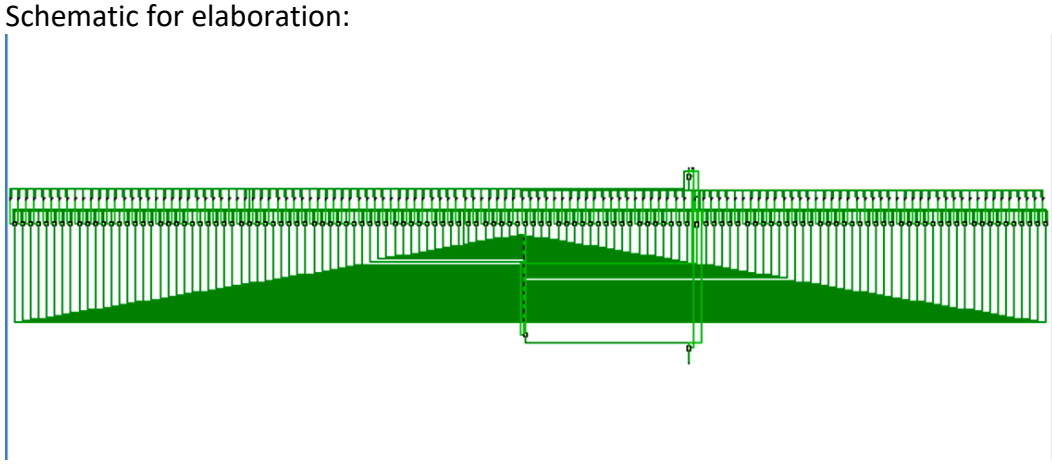



Timing report:

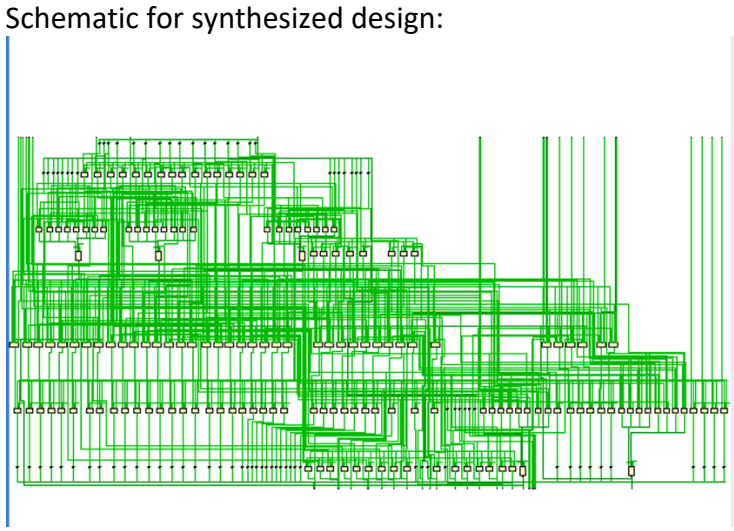



## (d) 128 elements design

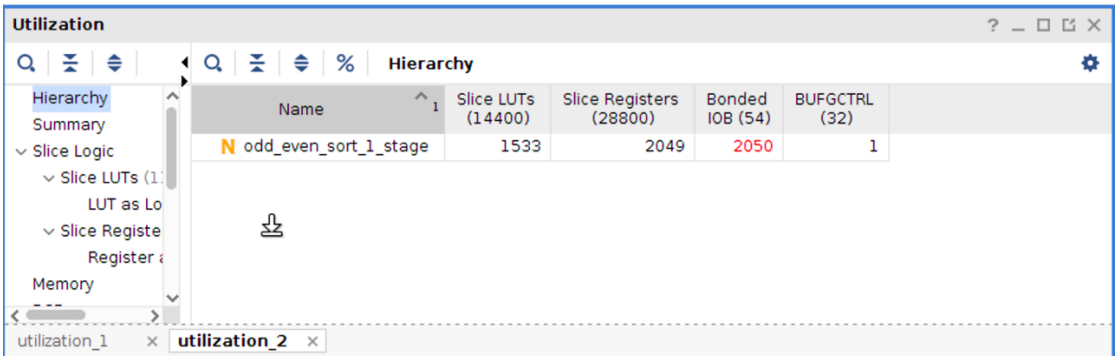
Schematic for elaboration:



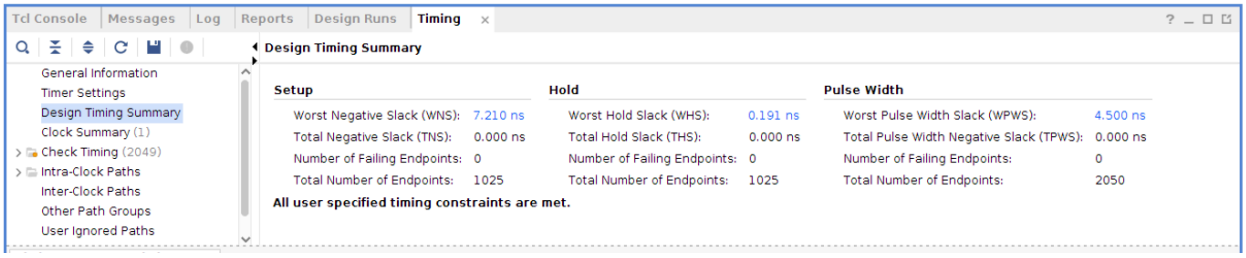
Schematic for synthesized design:



Resource report:




Timing report:



## 2. Dense Matrix-Matrix Multiplication

### 2.1.1 Design problems

**(1) How many Multiply units needed for the entire design?**

We need n multiply units to implement our design

**(2) Consider an adder stage r, how many adder modules needed for that stage (Assume multiplication stage as stage 0)?**

(n / 2 ^ r) adder modules (r starts from 1)

**(3) If all the inputs to the design represented using k bits, how many bits are needed to represent the final result of the Multiply and Adder Tree?**

(k / (2 * 8 * n)) * 2 * 8 bits

**(4) How may Adder modules need for the entire multiply and adder tree design?**

n/2 + n/4 + n/8 + …. + 1

**(5) How many clock cycles need to produce the first output element in the adder tree?**

Log(n) + 1

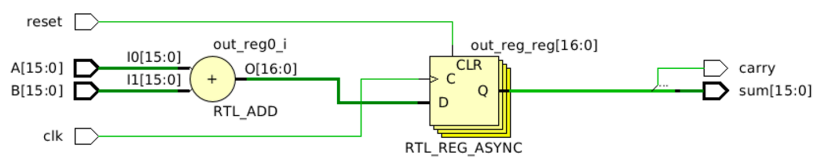
**(6) How many clock cycles need to multiply two n × n matrices?**

Log(n) + 1, if we generate all n x n elements in parallel

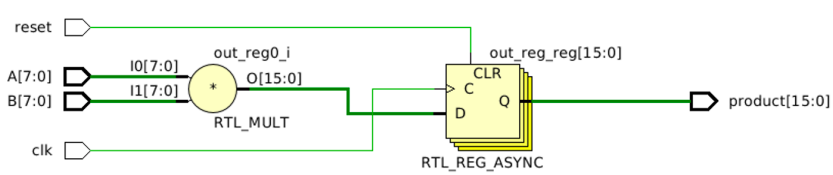
### 2.1.3 Post Implementation

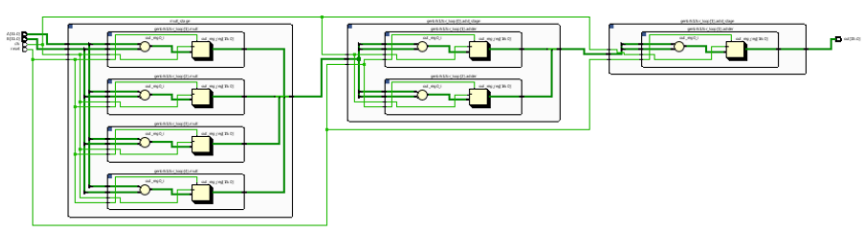
**(a) Design for 4x4:**

Schematic for elaboration (Adder):

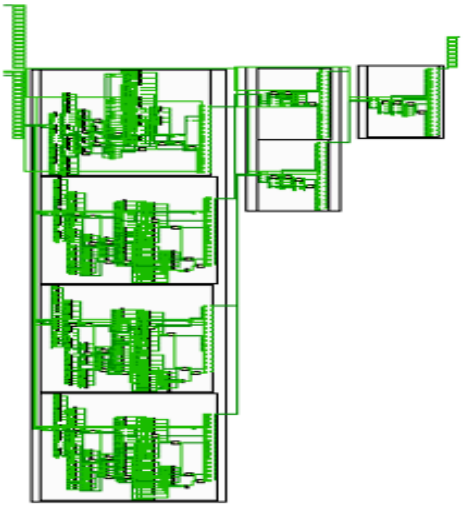



Schematic for elaboration (Multiply):



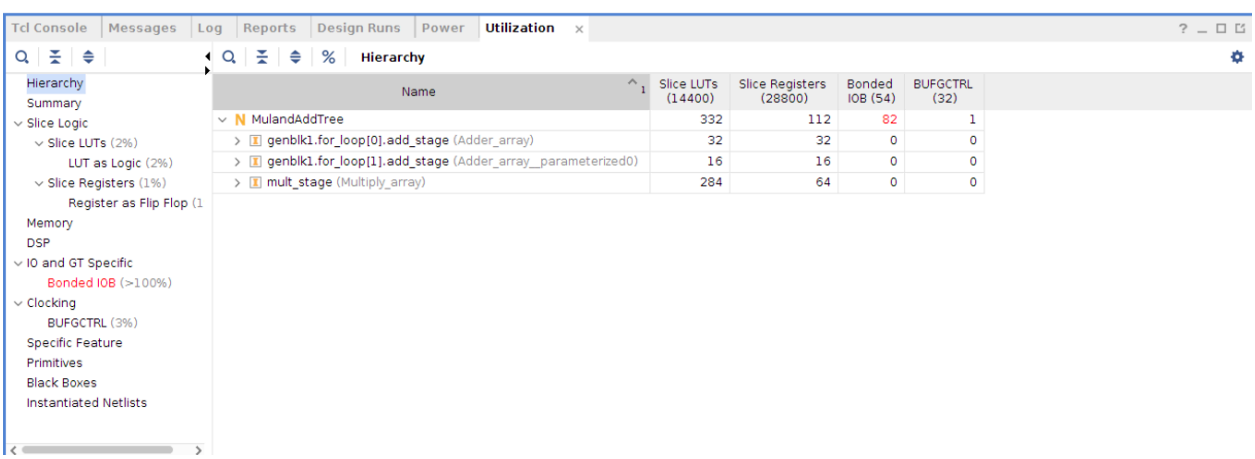



Schematic for synthesized design:



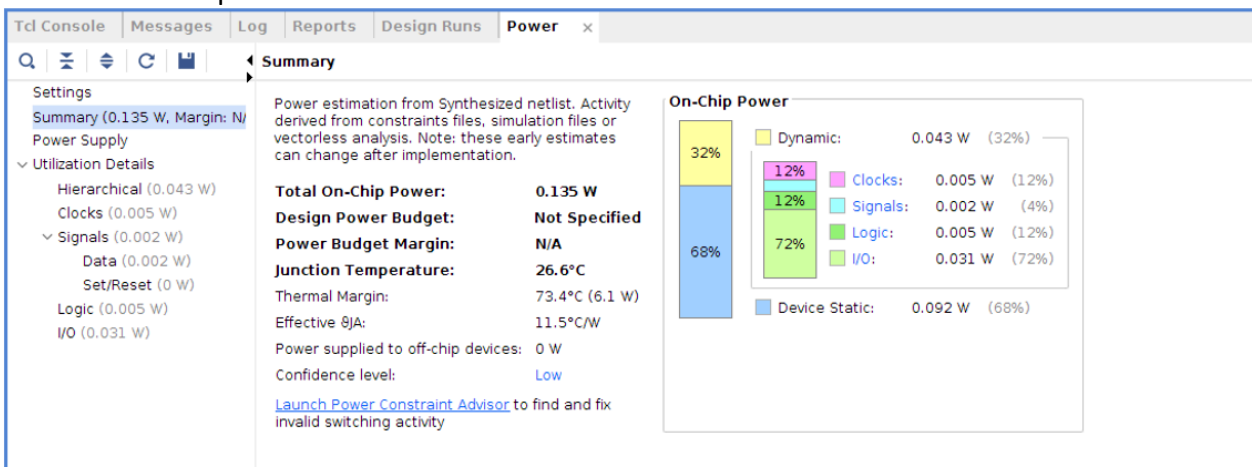
Timing report:

Resource report:



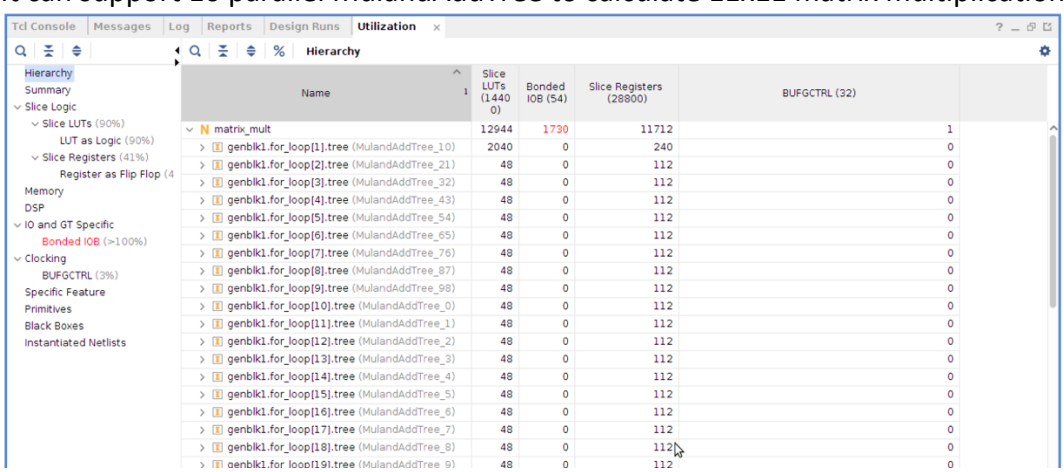

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| MulandAddTree | 332 | 112 | 82 | 1 |
| genblk1.for_loop[0].add_stage (Adder_array) | 32 | 32 | 0 | 0 |
| genblk1.for_loop[1].add_stage (Adder_array__parameterized0) | 16 | 16 | 0 | 0 |
| mult_stage (Multiply_array) | 284 | 64 | 0 | 0 |

Power report:



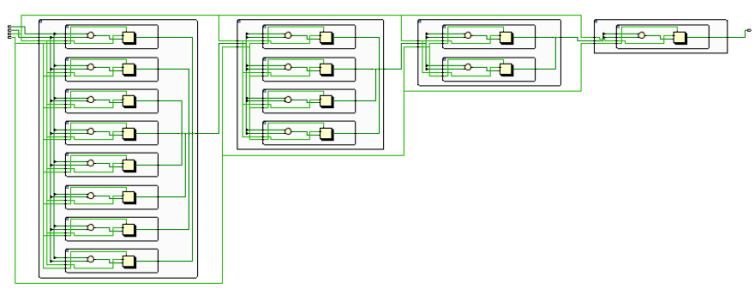

**(b) How many of parallel MulandAddTrees can be implemented in this FPGA (Provide resource utilization reports with parallel MulandAddTres)?**

It can support 10 parallel MulandAddTree to calculate 11x11 matrix multiplication



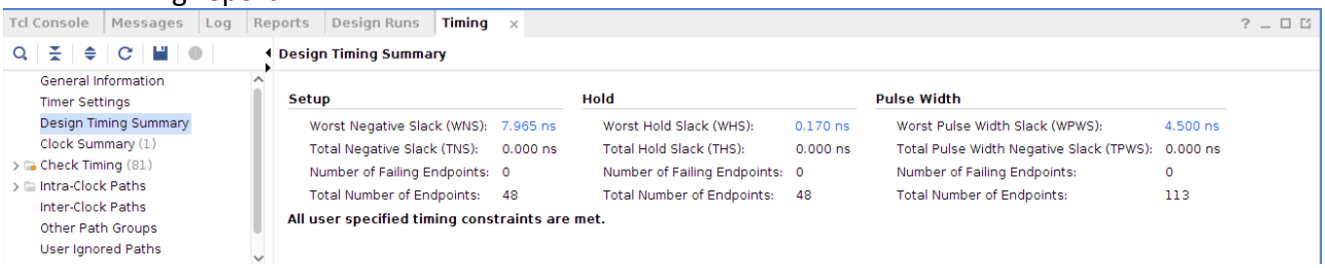

**(c) Design for 8x8:**

Schematic for elaboration:

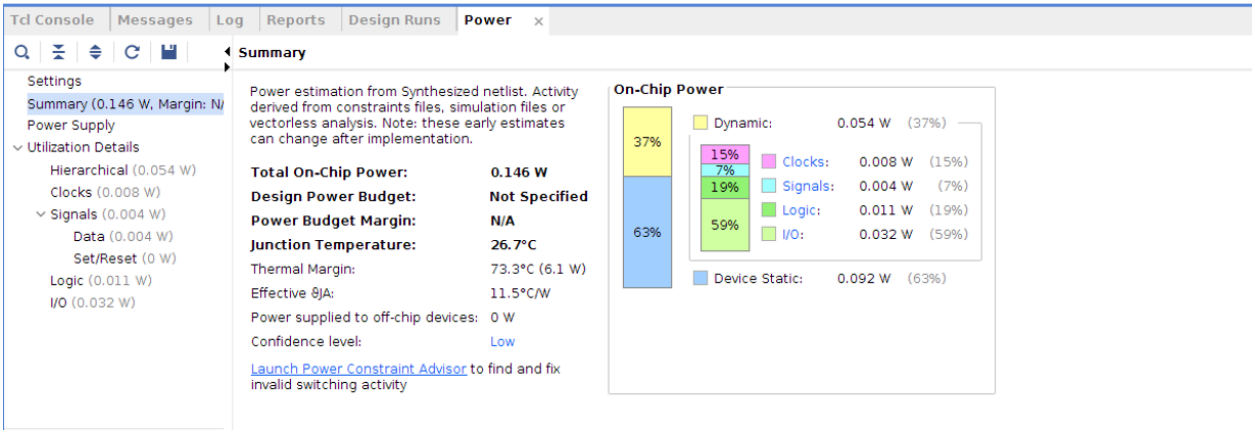


Schematic for synthesized design:

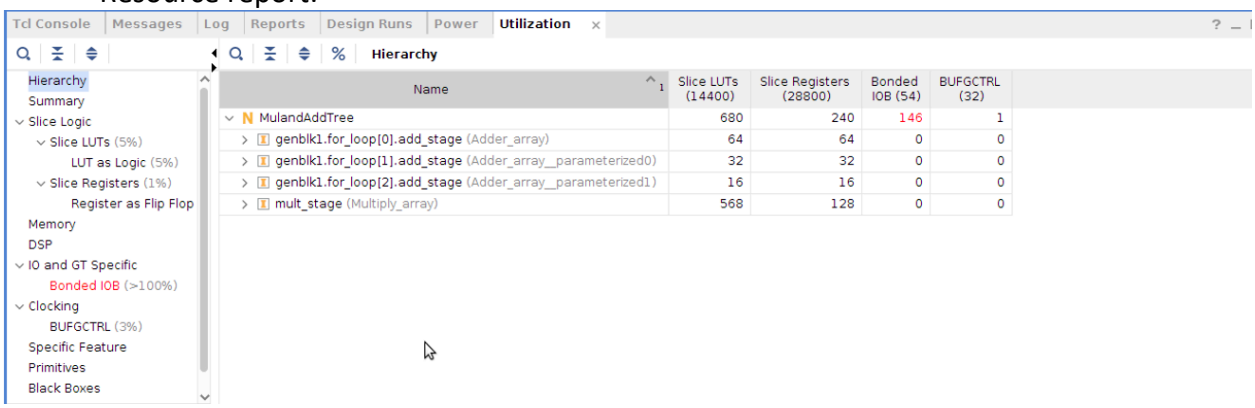
Timing report:




Power report:



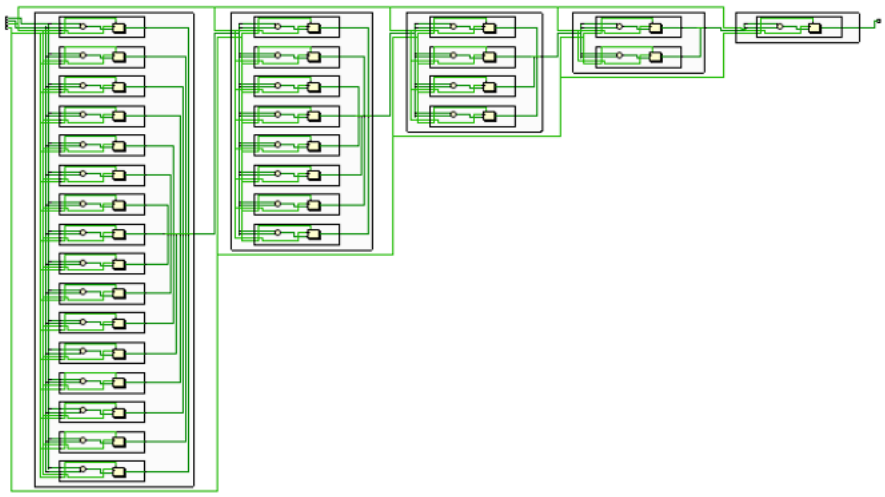
Resource report:



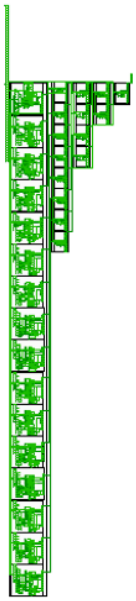

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| MulandAddTree | 680 | 240 | 146 | 1 |
| genblk1.for_loop[0].add_stage (Adder_array) | 64 | 64 | 0 | 0 |
| genblk1.for_loop[1].add_stage (Adder_array__parameterized0) | 32 | 32 | 0 | 0 |
| genblk1.for_loop[2].add_stage (Adder_array__parameterized1) | 16 | 16 | 0 | 0 |
| mult_stage (Multiply_array) | 568 | 128 | 0 | 0 |

**(d) Design for 16x16**

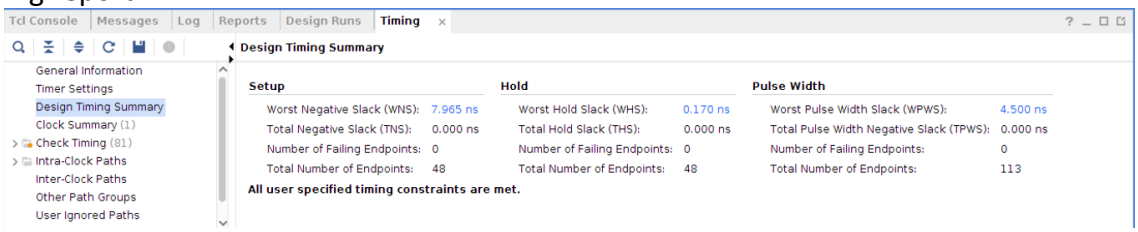
Schematic for elaboration:



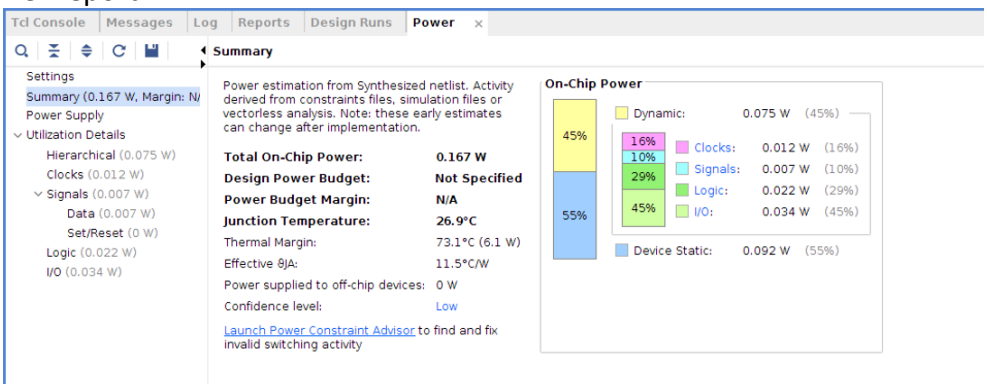
Schematic for synthesized design:



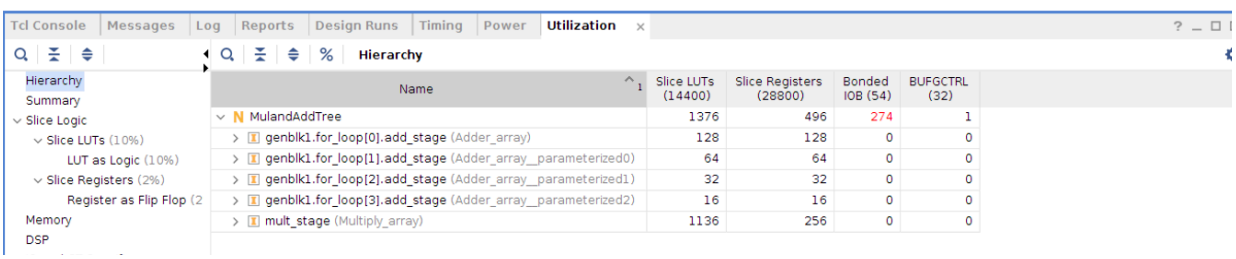
Timing report:




Power report:



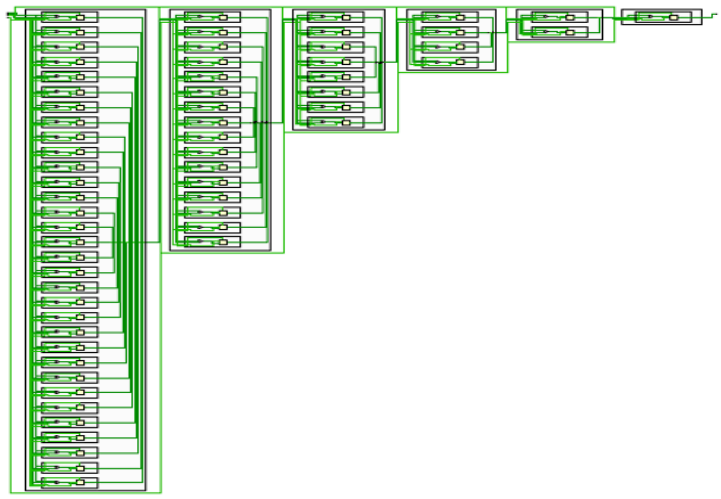

Resource report:




| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| MulandAddTree | 1376 | 496 | 274 | 1 |
| genblk1.for_loop[0].add_stage (Adder_array) | 128 | 128 | 0 | 0 |
| genblk1.for_loop[1].add_stage (Adder_array__parameterized0) | 64 | 64 | 0 | 0 |
| genblk1.for_loop[2].add_stage (Adder_array__parameterized1) | 32 | 32 | 0 | 0 |
| genblk1.for_loop[3].add_stage (Adder_array__parameterized2) | 16 | 16 | 0 | 0 |
| mult_stage (Multiply_array) | 1136 | 256 | 0 | 0 |

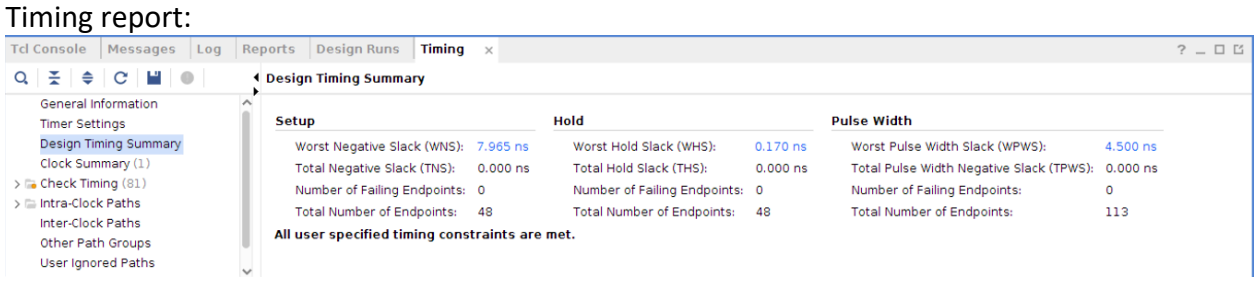
## (e) Design for 32x32

Schematic for elaboration:

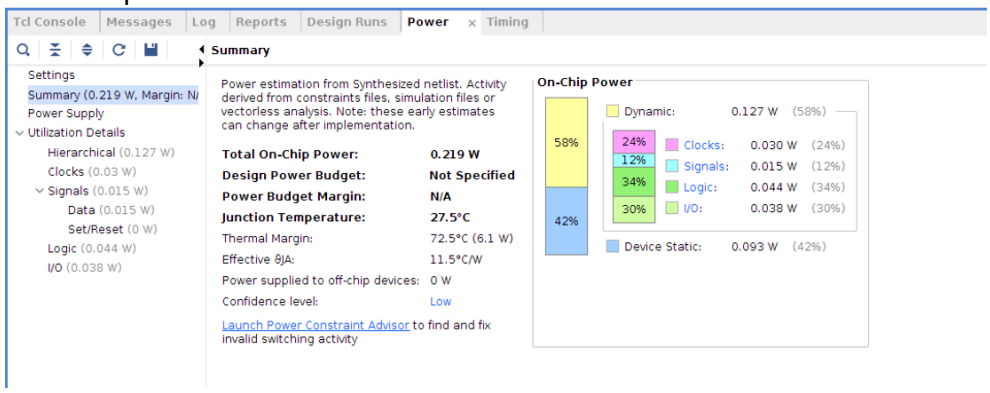


Schematic for synthesized design:

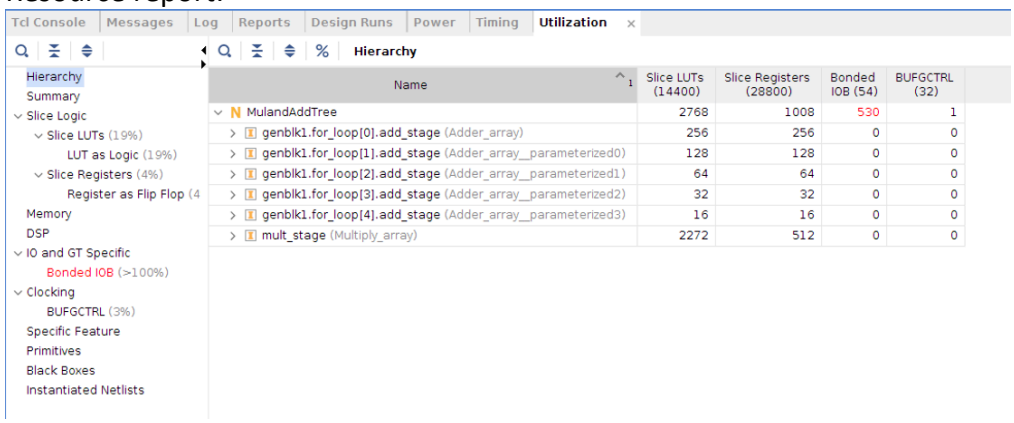
Timing report:



## Power report:




## Resource report:




| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| MulandAddTree | 2768 | 1008 | 530 | 1 |
| genblk1.for_loop[0].add_stage (Adder_array) | 256 | 256 | 0 | 0 |
| genblk1.for_loop[1].add_stage (Adder_array__parameterized0) | 128 | 128 | 0 | 0 |
| genblk1.for_loop[2].add_stage (Adder_array__parameterized1) | 64 | 64 | 0 | 0 |
| genblk1.for_loop[3].add_stage (Adder_array__parameterized2) | 32 | 32 | 0 | 0 |
| genblk1.for_loop[4].add_stage (Adder_array__parameterized3) | 16 | 16 | 0 | 0 |
| mult_stage (Multiply_array) | 2272 | 512 | 0 | 0 |