

# EE599 Assignment 2

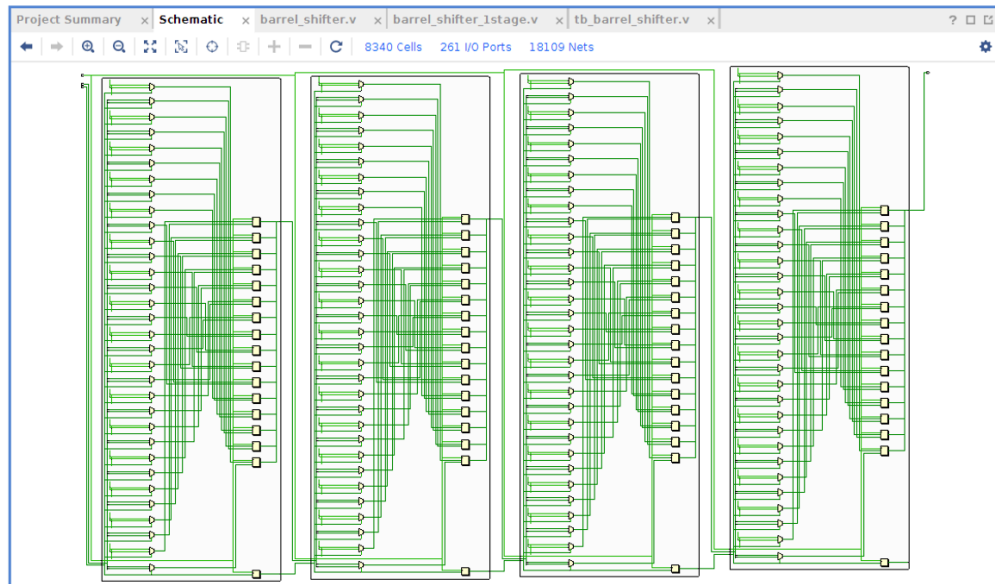
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Github Repo Link: [https://github.com/KevinWang96/EE599\\_YihaoWang\\_7410178057.git](https://github.com/KevinWang96/EE599_YihaoWang_7410178057.git)

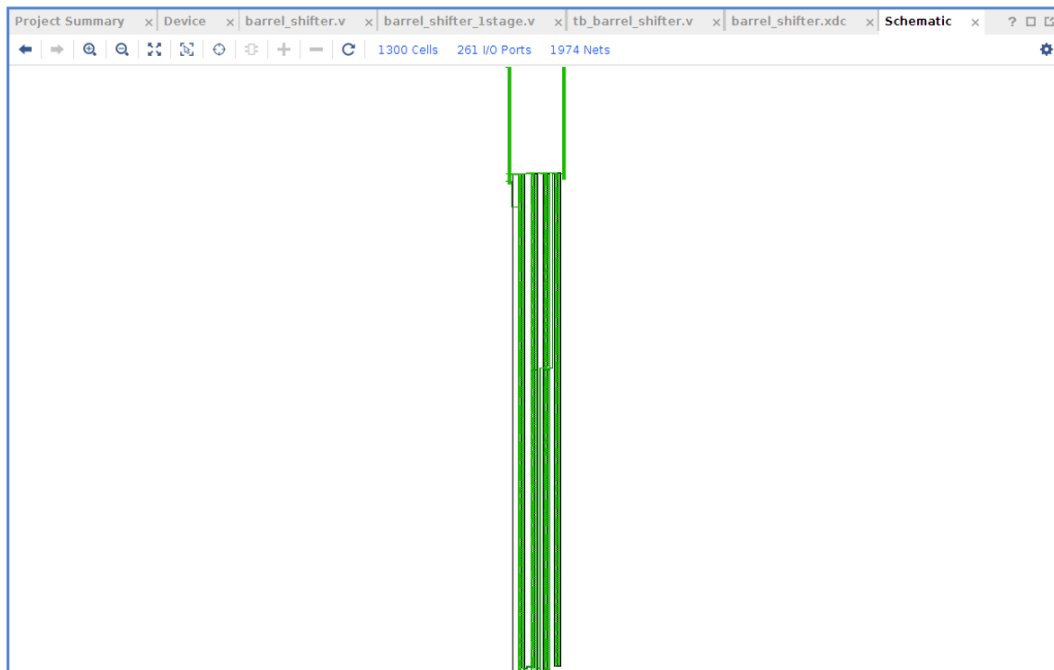
## 1. Barrel Shifter

### 1.1 16 elements design

#### a. Schematic of elaborated design



#### b. Schematic of synthesized design



### c. Timing report (clock cycle is 10 ns)

Tcl Console	Messages	Log	Reports	Design Runs	Timing	Power	Utilization	
Design Timing Summary								
General Information								
Timer Settings								
Design Timing Summary								
Clock Summary (1)								
Check Timing (260)								
Intra-Clock Paths								
Inter-Clock Paths								
Other Path Groups								
User Ignored Paths								
Unconstrained Paths								
Setup								
Worst Negative Slack (WNS): 8.226 ns								
Total Negative Slack (TNS): 0.000 ns								
Number of Failing Endpoints: 0								
Total Number of Endpoints: 1539								
Hold								
Worst Hold Slack (WHS): 0.140 ns								
Total Hold Slack (THS): 0.000 ns								
Number of Failing Endpoints: 0								
Total Number of Endpoints: 1539								
Pulse Width								
Worst Pulse Width Slack (WPWS): 4.500 ns								
Total Pulse Width Negative Slack (TPWS): 0.000 ns								
Number of Failing Endpoints: 0								
Total Number of Endpoints: 1031								
All user specified timing constraints are met.								

### d. Utilization report

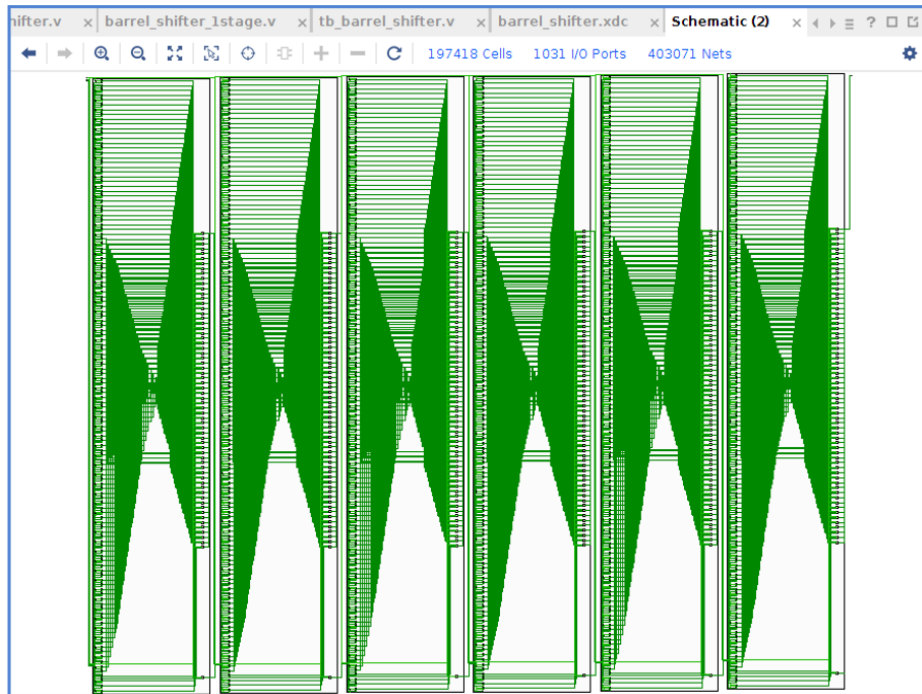
Tcl Console	Messages	Log	Reports	Design Runs	Power	Utilization	
Hierarchy							
Summary							
Slice Logic							
Slice LUTs (<1%)							
LUT as Logic (<1%)							
Slice Registers (4%)							
Register as Flip Flop (4)							
Memory							
DSP							
IO and GT Specific							
Bonded IOB (>100%)							
Clocking							
BUFGCTRL (3%)							
Specific Feature							
Primitives							
Black Boxes							
Instantiated Netlists							
utilization_1							

### e. Power report

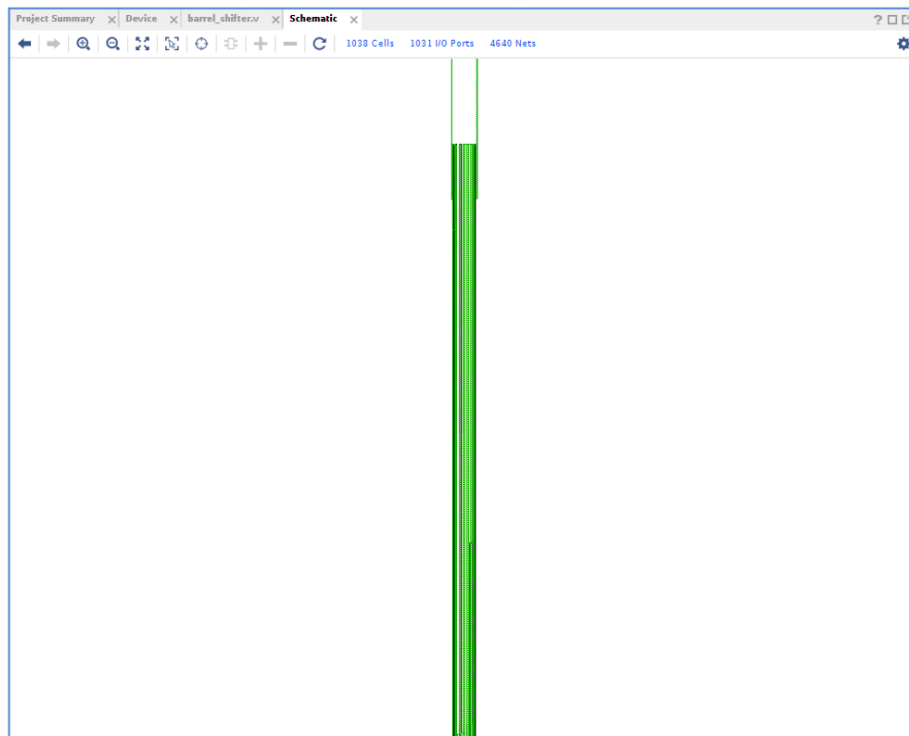
Tcl Console	Messages	Log	Reports	Design Runs	Power	
Summary						
Settings						
Summary (0.115 W, Margin: N/A)						
Power Supply						
Utilization Details						
Hierarchical (0.023 W)						
Clocks (0.014 W)						
Signals (0.001 W)						
Data (0.001 W)						
Clock Enable (<0.001 W)						
Logic (<0.001 W)						
I/O (0.009 W)						
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.						
Total On-Chip Power: 0.115 W						
Design Power Budget: Not Specified						
Power Budget Margin: N/A						
Junction Temperature: 26.3°C						
Thermal Margin: 73.7°C (6.2 W)						
Effective $\theta_{JA}$ : 11.5°C/W						
Power supplied to off-chip devices: 0 W						
Confidence level: Low						
<a href="#">Launch Power Constraint Advisor</a> to find and fix invalid switching activity						
On-Chip Power						
Dynamic: 0.023 W (20%)						
Clocks: 0.014 W (59%)						
Signals: 0.001 W (4%)						
Logic: <0.001 W (1%)						
I/O: 0.009 W (36%)						
Device Static: 0.092 W (80%)						

## 1.2 64 elements design

### a. Schematic of elaborated design



### b. Schematic of synthesized design



## c. Timing report (clock cycle is 10 ns)

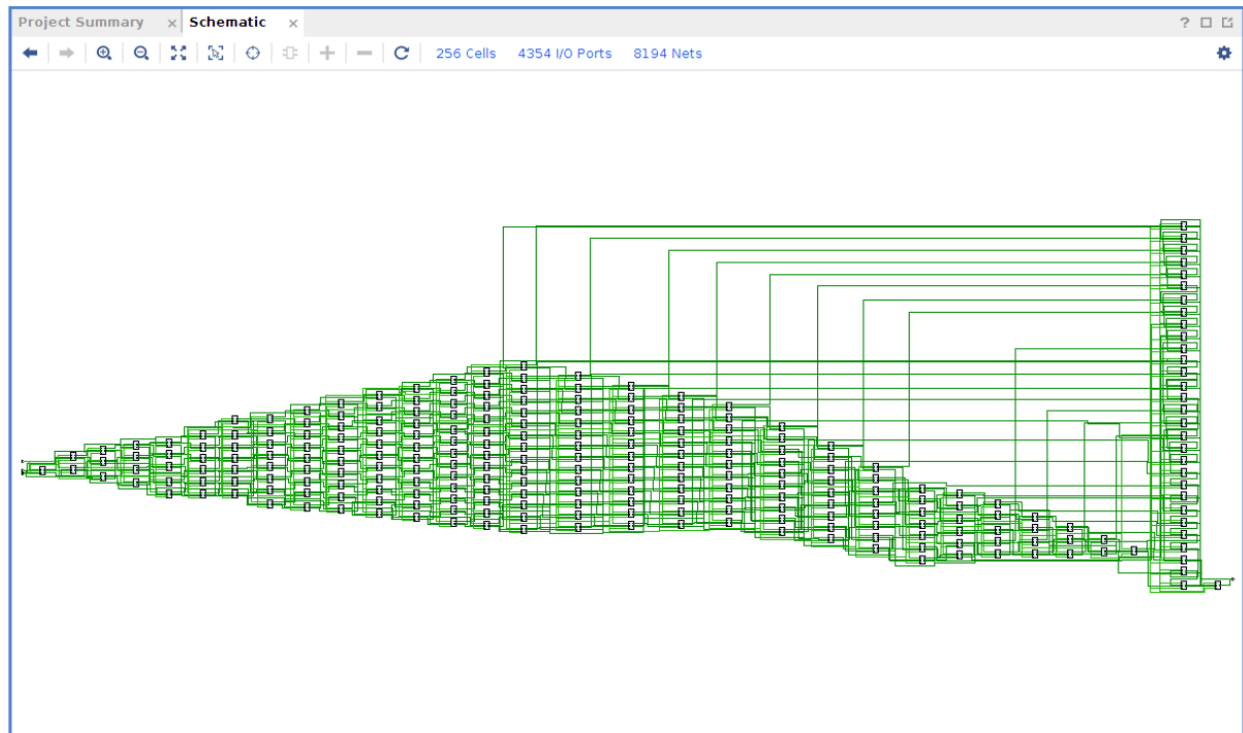
Tcl Console	Messages	Log	Reports	Design Runs	Timing	Power	Utilization
Design Timing Summary							
General Information							
Timer Settings							
Design Timing Summary							
Clock Summary (1)							
Check Timing (1030)							
Intra-Clock Paths							
Inter-Clock Paths							
Other Path Groups							
User Ignored Paths							
Unconstrained Paths							
Setup							
Worst Negative Slack (WNS): 8.158 ns							
Total Negative Slack (TNS): 0.000 ns							
Number of Failing Endpoints: 0							
Total Number of Endpoints: 10247							
Hold							
Worst Hold Slack (WHS): 0.059 ns							
Total Hold Slack (THS): 0.000 ns							
Number of Failing Endpoints: 0							
Total Number of Endpoints: 10247							
Pulse Width							
Worst Pulse Width Slack (WPWS): 4.146 ns							
Total Pulse Width Negative Slack (TPWS): 0.000 ns							
Number of Failing Endpoints: 0							
Total Number of Endpoints: 6157							
All user specified timing constraints are met.							

## d. Utilization report

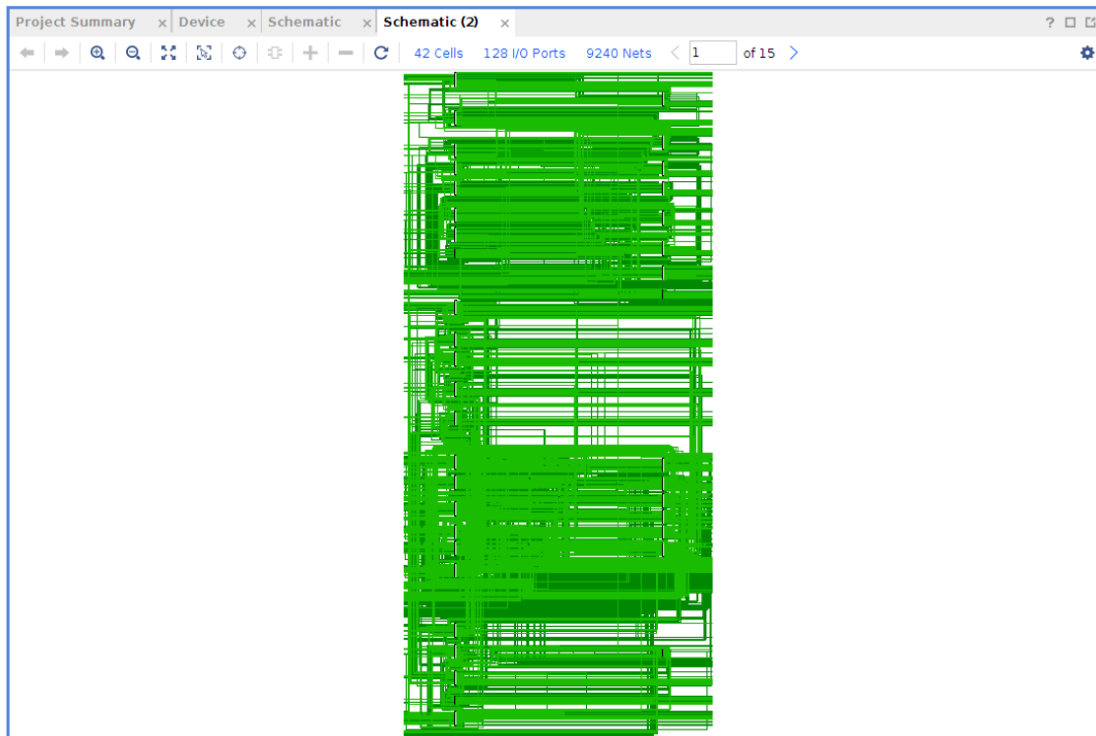
Tcl Console	Messages	Log	Reports	Design Runs	Power	Utilization
Hierarchy						
Hierarchy						
Summary						
Slice Logic						
Slice LUTs (<1%)						
LUT as Memory (<1%)						
LUT as Shift Register						
LUT as Logic (<1%)						
Slice Registers (21%)						
Register as Flip Flop (21%)						
Memory						
DSP						
IO and GT Specific						
Bonded IOB (>100%)						
Clocking						
BUFGCTRL (3%)						
Specific Feature						
Primitives						
Black Boxes						
Instantiated Netlists						
Name						
Slice LUTs (14400)						
Slice Registers (28800)						
Bonded IOB (54)						
BUFGCTRL (32)						
barrel_shifter						
genblk1_for_loop[0].shifter (barrel_shifter_1stage)						
genblk1_for_loop[1].shifter (barrel_shifter_1stage__parameterized0)						
genblk1_for_loop[2].shifter (barrel_shifter_1stage__parameterized1)						
genblk1_for_loop[3].shifter (barrel_shifter_1stage__parameterized2)						
genblk1_for_loop[4].shifter (barrel_shifter_1stage__parameterized3)						
genblk1_for_loop[5].shifter (barrel_shifter_1stage__parameterized4)						

## e. Power report

Tcl Console	Messages	Log	Reports	Design Runs	Power
Summary					
Settings					
Summary (0.173 W, Margin: N/A)					
Power Supply					
Utilization Details					
Hierarchical (0.08 W)					
Clocks (0.041 W)					
Signals (0.005 W)					
Data (0.004 W)					
Clock Enable (0.001 W)					
Logic (<0.001 W)					
I/O (0.034 W)					
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.					
Total On-Chip Power: 0.173 W					
Design Power Budget: Not Specified					
Power Budget Margin: N/A					
Junction Temperature: 27.0°C					
Thermal Margin: 73.0°C (6.1 W)					
Effective $\theta_{JA}$ : 11.5°C/W					
Power supplied to off-chip devices: 0 W					
Confidence level: Low					
Launch Power Constraint Advisor to find and fix invalid switching activity					
On-Chip Power					
Dynamic: 0.080 W (47%)					
50% Clocks: 0.041 W (50%)					
7% Signals: 0.005 W (7%)					
42% Logic: <0.001 W (1%)					
I/O: 0.034 W (42%)					
Device Static: 0.092 W (53%)					



### c. Schematic of synthesized design



### d. Timing report (clock cycle is 10 ns)

The image shows a screenshot of a timing report window titled 'Timing'. The report provides a summary of timing constraints and their results. The clock cycle is 10 ns. The report is organized into three main sections: Setup, Hold, and Pulse Width. Each section lists various timing metrics and their values.

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.728 ns	Worst Hold Slack (WHS): 0.115 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 7680	Total Number of Endpoints: 7680	Total Number of Endpoints: 7937

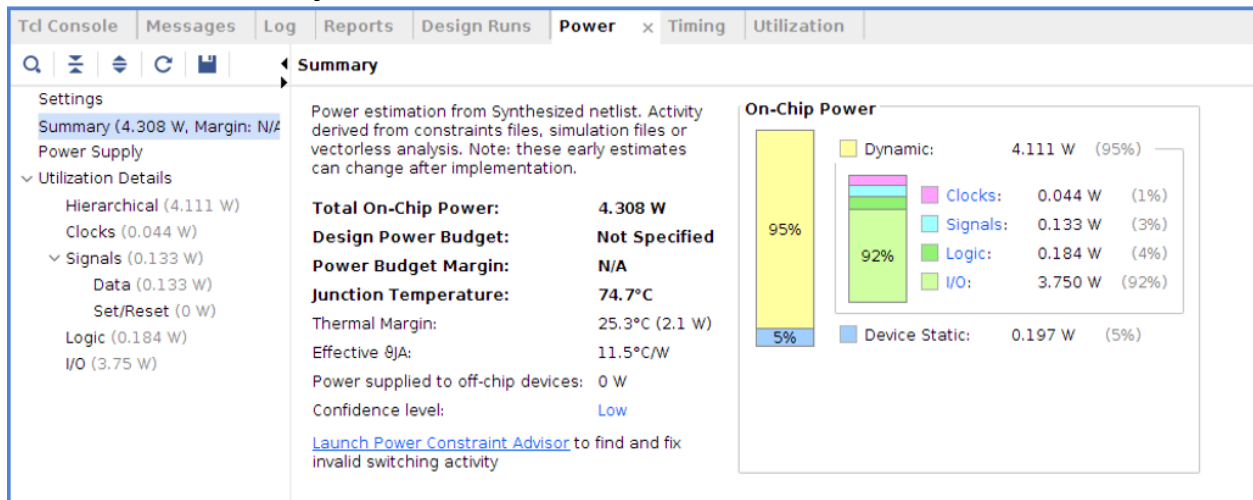
All user specified timing constraints are met.

### e. Utilization report

The image shows a screenshot of a utilization report window titled 'Utilization'. The report provides a detailed breakdown of resource usage across the design hierarchy. The report is organized into a table with columns for Name, Slice LUTs, Slice Registers, Bonded IOB (54), and BUFGCTRL (32). The hierarchy is shown on the left, with the main table displaying the utilization for each component.

Name	Slice LUTs	Slice Registers	Bonded IOB (54)	BUFGCTRL (32)
systolic_array	21999	7936	4354	1
genblk1_for_row[0].for_col[0].pe (systolic_array_pe)	179	32	0	0
genblk1_for_row[0].for_col[1].pe (systolic_array_pe_6)	107	32	0	0
genblk1_for_row[0].for_col[2].pe (systolic_array_pe_7)	105	32	0	0
genblk1_for_row[0].for_col[3].pe (systolic_array_pe_8)	103	32	0	0
genblk1_for_row[0].for_col[4].pe (systolic_array_pe_9)	105	32	0	0
genblk1_for_row[0].for_col[5].pe (systolic_array_pe_10)	106	32	0	0
genblk1_for_row[0].for_col[6].pe (systolic_array_pe_11)	103	32	0	0
genblk1_for_row[0].for_col[7].pe (systolic_array_pe_12)	104	32	0	0
genblk1_for_row[0].for_col[8].pe (systolic_array_pe_13)	104	32	0	0
genblk1_for_row[0].for_col[9].pe (systolic_array_pe_14)	105	32	0	0
genblk1_for_row[0].for_col[10].pe (systolic_array_pe_0)	104	32	0	0
genblk1_for_row[0].for_col[11].pe (systolic_array_pe_1)	104	32	0	0
genblk1_for_row[0].for_col[12].pe (systolic_array_pe_2)	106	32	0	0
genblk1_for_row[0].for_col[13].pe (systolic_array_pe_3)	105	32	0	0
genblk1_for_row[0].for_col[14].pe (systolic_array_pe_4)	106	32	0	0

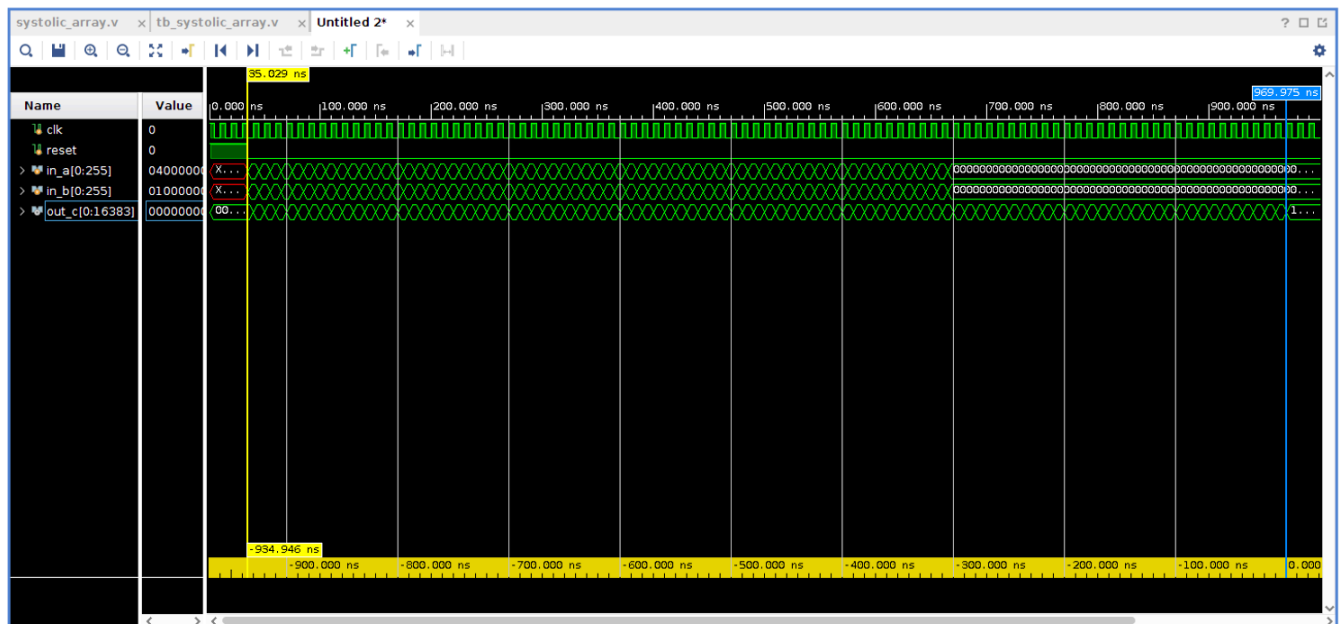
## f. Power report



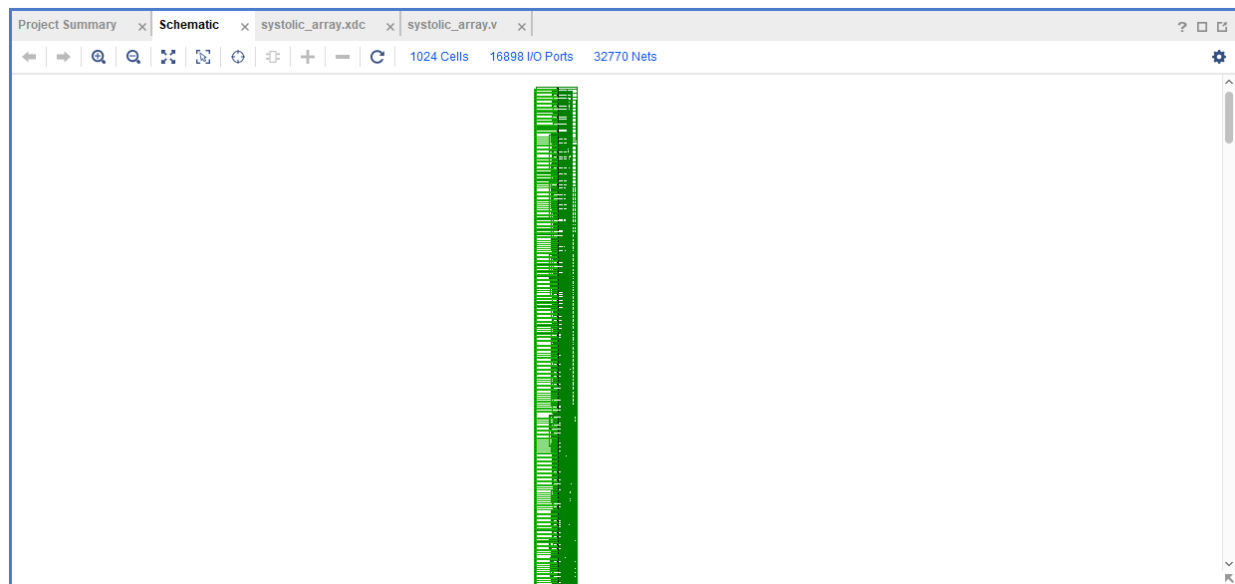
## 2.2 32x32 Design

### a. Waveform

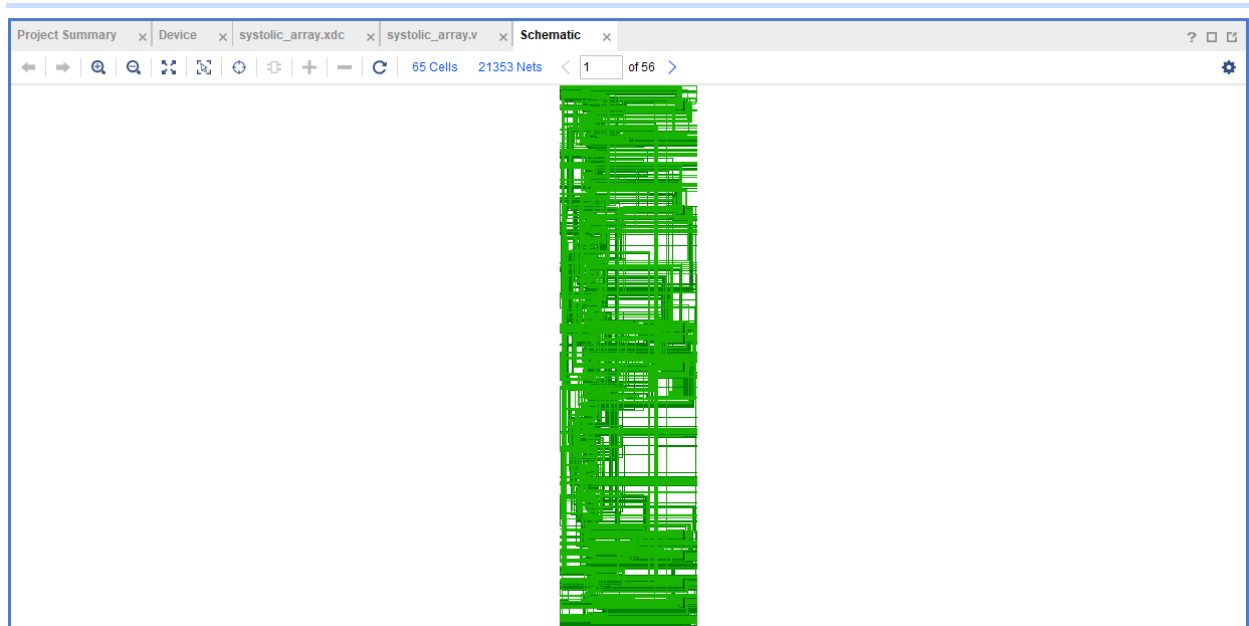
The input stream starts at yellow marker and results come out at blue marker.



## b. Schematic of elaborated design



## c. Schematic of synthesized design





## d. Timing report (clock cycle is 10 ns)

Tcl Console	Messages	Log	Reports	Design Runs	Timing x	Power	Utilization
Q [Icons] Design Timing Summary							
<b>General Information</b>							
<b>Timer Settings</b>							
<b>Design Timing Summary</b>							
<b>Clock Summary (1)</b>							
> Check Timing (16897)							
> Intra-Clock Paths							
Inter-Clock Paths							
Other Path Groups							
User Ignored Paths							
> Unconstrained Paths							
			<b>Setup</b>		<b>Hold</b>		<b>Pulse Width</b>
			Worst Negative Slack (WNS): 2.641 ns		Worst Hold Slack (WHS): 0.118 ns		Worst Pulse Width Slack (WPWS): 4.500 ns
			Total Negative Slack (TNS): 0.000 ns		Total Hold Slack (THS): 0.000 ns		Total Pulse Width Negative Slack (TPWS): 0.000 ns
			Number of Failing Endpoints: 0		Number of Failing Endpoints: 0		Number of Failing Endpoints: 0
			Total Number of Endpoints: 31744		Total Number of Endpoints: 31744		Total Number of Endpoints: 32257
All user specified timing constraints are met.							

## e. Utilization report

Tcl Console		Messages		Log	Reports	Design Runs	Power	Utilization		
Q		Z		A		%		Hierarchy		
Hierarchy										
Summary										
v Slice Logic										
v Slice LUTs (>100%)										
LUT as Logic (>100%)										
v Slice Registers (25%)										
Register as Flip Flop (25%)										
Memory										
DSP										
v IO and GT Specific										
Bonded IOB (>100%)										
v Clocking										
BUFGCTRL (3%)										
Specific Feature										
Primitives										
Black Boxes										
Instantiated Netlists										
utilization_1										

## f. Power report

Tcl Console	Messages	Log	Reports	Design Runs	Power x
Q [Icons] Summary					
<b>Settings</b>					
<b>Summary (16.817 W, Margin: N/A)</b>					
<b>Power Supply</b>					
v Utilization Details					
Hierarchical (16.396 W)					
Clocks (0.177 W)					
v Signals (0.5 W)					
Data (0.5 W)					
Set/Reset (0 W)					
Logic (0.724 W)					
I/O (14.994 W)					
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.					
<b>Total On-Chip Power: 16.817 W (Junction temp exceeded!)</b>					
<b>Design Power Budget: Not Specified</b>					
<b>Power Budget Margin: N/A</b>					
<b>Junction Temperature: 101.7°C</b>					
Thermal Margin: -16.7°C (-3.5 W)					
Effective RJA: 4.6°C/W					
Power supplied to off-chip devices: 0 W					
Confidence level: Low					
<a href="#">Launch Power Constraint Advisor</a> to find and fix invalid switching activity					
<b>On-Chip Power</b>					
Dynamic: 16.396 W (98%)					
Clocks: 0.177 W (1%)					
Signals: 0.500 W (3%)					
Logic: 0.724 W (4%)					
I/O: 14.994 W (92%)					
Device Static: 0.419 W (2%)					