ECE6100 Project1 Report

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1 Methodology

Using all the possible values compare the return result of ATT. Also, record the metadata of different parameters.

2 Rationale

The following code is the code for generating CSV file for the test data. After generating the CSV file. We can analysis those CSV to conclude.

```
#include "cachesim.hpp"
#include <iostream>
#include <fstream>
#include <string>
#include <vector>
#include <cstdint>
#include <cmath>
#include "cachesim.cpp"
using namespace std;
struct test_config_t {
    int c_l1, b_l1, s_l1, c_l2, s_l2;
    bool prefetcher_disabled, strided_prefetch_disabled;
};

int main() {
    string traceFilePath = "traces/gcc.trace";
    ofstream csvFile ("gkwsim/gcc_simulation_results.csv");
    csvFile << "C_L1,B_L1,S_L1,C_L2,S_L2,Prefetcher,Stride,Tag-Storage-L1-(bits),Tag-Storage
        -L2-(bits),ATT-L1\n";
    if (!csvFile.is_open()) {
        cerr << "Failed to open CSV file for writing." << endl;
        return 1;
    }
    vector<bool> boolVec;
    boolVec.push_back(true);
    boolVec.push_back(false);
    int c1 = 15; // Example cache size for L1
    int c2 = 17; // Example cache size for L2
    // Define a set of configurations to test
    for (int b = 5; b < 7; b++) {
        for (int s1 = 0; s1 < c1; s1++) {
            for (int s2 = 0; s2 < c2; s2++) {
                for (bool prefetcher : boolVec) { // Simplified loop for boolean
                    for (bool stride : boolVec) { // Simplified loop for boolean

                        if (s2 <= s1) continue;
                        if ((c2 - s2) <= (c1 - s1)) continue;
                        if(c2 - s2 < b || c1 - s1 < b) continue;

                        // Dynamic configuration based on loop variables
                        test_config_t config = {c1, b, s1, c2, s2, !prefetcher, !stride};
```

```
                        cache_config_t l1Config = {
                                .disabled = false,
                                .prefetcher_disabled = config.prefetcher_disabled,
                                .strided_prefetch_disabled = config.
                                    strided_prefetch_disabled,
                                .c = config.c_l1,
                                .b = config.b_l1,
                                .s = config.s_l1,
                                .replace_policy = REPLACE_POLICY_LRU,
                                .prefetch_insert_policy = INSERT_POLICY_MIP,
                                .write_strat = WRITE_STRAT_WBWA
                        };

                        cache_config_t l2Config = {
                                .disabled = false,
                                .prefetcher_disabled = config.prefetcher_disabled,
                                .strided_prefetch_disabled = config.
                                    strided_prefetch_disabled,
                                .c = config.c_l2,
                                .b = config.b_l1, // Assuming L2 uses the same block size as
                                     L1
                                .s = config.s_l2,
                                .replace_policy = REPLACE_POLICY_LRU,
                                .prefetch_insert_policy = INSERT_POLICY_MIP,
                                .write_strat = WRITE_STRAT_WTWNA
                        };

                        sim_config_t simConfig = {
                                .l1_config = l1Config,
                                .l2_config = l2Config
                        };

                        sim_setup(&simConfig);

                        ifstream traceFile(traceFilePath);
                        string line;
                        sim_stats_t stats = {};

                        if (!traceFile.is_open()) {
                            cerr << "Failed to open trace file: " << traceFilePath << endl;
                            return 1;
                        }

                        // Process each line in the trace file
                        while (getline(traceFile, line)) {
                            if (line[0] == 'R' || line[0] == 'W') {
                                char op = line[0];
                                uint64_t address;
                                sscanf(line.c_str() + 2, "%lx", &address);
                                sim_access(op, address, &stats);
                            }
                        }

                        traceFile.close();

                        sim_finish(&stats);

                        // Output relevant statistics for this configuration
//                        csvFile << config.c_l1 << ", " << config.b_l1 << ", " << config.
    s_l1 << ", "
//                                << config.c_l2 << ", " << config.s_l2 << ", " << stats.
    avg_access_time_l1 << "\n";
                        cout
                                << "L1, C=" << config.c_l1 << ", B=" << config.b_l1 << ", S=
                                    " << config.s_l1
                                << ", L2, C=" << config.c_l2 << ", S=" << config.s_l2 <<", 
                                    ATT=" << stats.avg_access_time_l1<< endl;
```

```
                        unsigned long long tagStorageL1 = pow(2, config.c_l1 - config.b_l1)
                            * (64 - (config.c_l1 - config.s_l1) + 2);
                        unsigned long long tagStorageL2 = pow(2, config.c_l2 - config.b_l1)
                            * (64 - (config.c_l2 - config.s_l2) + 1);
                        csvFile << config.c_l1 << "," << config.b_l1 << "," << config.s_l1
                            << ","
                                << config.c_l2 << "," << config.s_l2 << "," << (prefetcher ?
                                    "True" : "False") << ","
                                << (stride ? "True" : "False") << "," << tagStorageL1 << ","
                                    << tagStorageL2 << ","
                                << stats.avg_access_time_l1 << "\n";
                    }
                }
            }
        }
    }
    csvFile.close();
    return 0;
}
```

3 Results

Table 1: Optimal Cache Configurations for Each Trace

Trace	C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage (bits)	ATT L1
MCF	15	6	3	17	4	False	True	27648, 106496	2.19268
Leea	15	6	2	17	3	True	False	27136, 104448	2.29932
Matmul Naive	15	6	8	17	9	True	True	30208, 116736	2.78544
Matmul Tiled	15	6	1	17	2	False	False	26624, 102400	2.58035
Linpack	15	6	7	17	8	True	False	29696, 114688	6.64999
GCC	15	6	2	17	3	True	False	27136, 104448	2.46506

The selection process involved analyzing the data to identify configurations that not only minimize the Average Access Time (AAT) but also reduce the metadata requirements. This approach ensures an efficient use of cache resources, optimizing for both speed and storage efficiency.

4 Appendix

Table 2: MCF Simulation Results

C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	5	0	17	1	True	True	52224	200704	2.93815
15	5	0	17	1	True	False	52224	200704	2.85955
15	5	0	17	1	False	True	52224	200704	2.99515
15	5	0	17	1	False	False	52224	200704	2.99515
15	5	1	17	2	True	True	53248	204800	2.74849
15	5	1	17	2	True	False	53248	204800	2.68189
15	5	1	17	2	False	True	53248	204800	2.81769
15	5	1	17	2	False	False	53248	204800	2.81769
15	5	2	17	3	True	True	54272	208896	2.58622
15	5	2	17	3	True	False	54272	208896	2.52202
15	5	2	17	3	False	True	54272	208896	2.65802
15	5	2	17	3	False	False	54272	208896	2.65802
15	5	3	17	4	True	True	55296	212992	2.43563
15	5	3	17	4	True	False	55296	212992	2.37123
15	5	3	17	4	False	True	55296	212992	2.50743

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C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	5	3	17	4	False	False	55296	212992	2.50743
15	5	4	17	5	True	True	56320	217088	2.43544
15	5	4	17	5	True	False	56320	217088	2.37104
15	5	4	17	5	False	True	56320	217088	2.50744
15	5	4	17	5	False	False	56320	217088	2.50744
15	5	5	17	6	True	True	57344	221184	2.43572
15	5	5	17	6	True	False	57344	221184	2.37132
15	5	5	17	6	False	True	57344	221184	2.50772
15	5	5	17	6	False	False	57344	221184	2.50772
15	5	6	17	7	True	True	58368	225280	2.43598
15	5	6	17	7	True	False	58368	225280	2.37158
15	5	6	17	7	False	True	58368	225280	2.50798
15	5	6	17	7	False	False	58368	225280	2.50798
15	5	7	17	8	True	True	59392	229376	2.43606
15	5	7	17	8	True	False	59392	229376	2.37166
15	5	7	17	8	False	True	59392	229376	2.50806
15	5	7	17	8	False	False	59392	229376	2.50806
15	5	8	17	9	True	True	60416	233472	2.4362
15	5	8	17	9	True	False	60416	233472	2.3718
15	5	8	17	9	False	True	60416	233472	2.5082
15	5	8	17	9	False	False	60416	233472	2.5082
15	5	9	17	10	True	True	61440	237568	2.43626
15	5	9	17	10	True	False	61440	237568	2.37186
15	5	9	17	10	False	True	61440	237568	2.50826
15	5	9	17	10	False	False	61440	237568	2.50826
15	5	10	17	11	True	True	62464	241664	2.43623
15	5	10	17	11	True	False	62464	241664	2.37183
15	5	10	17	11	False	True	62464	241664	2.50823
15	5	10	17	11	False	False	62464	241664	2.50823
15	6	0	17	1	True	True	26112	100352	2.67797
15	6	0	17	1	True	False	26112	100352	2.60217
15	6	0	17	1	False	True	26112	100352	2.68297
15	6	0	17	1	False	False	26112	100352	2.68297
15	6	1	17	2	True	True	26624	102400	2.47729
15	6	1	17	2	True	False	26624	102400	2.42489
15	6	1	17	2	False	True	26624	102400	2.50469
15	6	1	17	2	False	False	26624	102400	2.50469
15	6	2	17	3	True	True	27136	104448	2.31415
15	6	2	17	3	True	False	27136	104448	2.26415
15	6	2	17	3	False	True	27136	104448	2.34375
15	6	2	17	3	False	False	27136	104448	2.34375
15	6	3	17	4	True	True	27648	106496	2.16128
15	6	3	17	4	True	False	27648	106496	2.11248
15	6	3	17	4	False	True	27648	106496	2.19268
15	6	3	17	4	False	False	27648	106496	2.19268
15	6	4	17	5	True	True	28160	108544	2.16156
15	6	4	17	5	True	False	28160	108544	2.11256
15	6	4	17	5	False	True	28160	108544	2.19276
15	6	4	17	5	False	False	28160	108544	2.19276
15	6	5	17	6	True	True	28672	110592	2.16141
15	6	5	17	6	True	False	28672	110592	2.11241
15	6	5	17	6	False	True	28672	110592	2.19281
15	6	5	17	6	False	False	28672	110592	2.19281
15	6	6	17	7	True	True	29184	112640	2.16141
15	6	6	17	7	True	False	29184	112640	2.11241
15	6	6	17	7	False	True	29184	112640	2.19281
15	6	6	17	7	False	False	29184	112640	2.19281
15	6	7	17	8	True	True	29696	114688	2.16141
15	6	7	17	8	True	False	29696	114688	2.11241
15	6	7	17	8	False	True	29696	114688	2.19281
15	6	7	17	8	False	False	29696	114688	2.19281
15	6	8	17	9	True	True	30208	116736	2.16141

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Table 2 Continued from previous page

C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	6	8	17	9	True	False	30208	116736	2.11241
15	6	8	17	9	False	True	30208	116736	2.19281
15	6	8	17	9	False	False	30208	116736	2.19281
15	6	9	17	10	True	True	30720	118784	2.16141
15	6	9	17	10	True	False	30720	118784	2.11241
15	6	9	17	10	False	True	30720	118784	2.19281
15	6	9	17	10	False	False	30720	118784	2.19281

Table 3: LEEA Simulation Results

C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	5	0	17	1	True	True	52224	200704	3.05992
15	5	0	17	1	True	False	52224	200704	2.97552
15	5	0	17	1	False	True	52224	200704	3.24132
15	5	0	17	1	False	False	52224	200704	3.24132
15	5	1	17	2	True	True	53248	204800	2.84978
15	5	1	17	2	True	False	53248	204800	2.76418
15	5	1	17	2	False	True	53248	204800	3.03238
15	5	1	17	2	False	False	53248	204800	3.03238
15	5	2	17	3	True	True	54272	208896	2.69655
15	5	2	17	3	True	False	54272	208896	2.61175
15	5	2	17	3	False	True	54272	208896	2.87975
15	5	2	17	3	False	False	54272	208896	2.87975
15	5	3	17	4	True	True	55296	212992	2.54681
15	5	3	17	4	True	False	55296	212992	2.46201
15	5	3	17	4	False	True	55296	212992	2.73021
15	5	3	17	4	False	False	55296	212992	2.73021
15	5	4	17	5	True	True	56320	217088	2.54708
15	5	4	17	5	True	False	56320	217088	2.46228
15	5	4	17	5	False	True	56320	217088	2.73048
15	5	4	17	5	False	False	56320	217088	2.73048
15	5	5	17	6	True	True	57344	221184	2.54722
15	5	5	17	6	True	False	57344	221184	2.46242
15	5	5	17	6	False	True	57344	221184	2.73062
15	5	5	17	6	False	False	57344	221184	2.73062
15	5	6	17	7	True	True	58368	225280	2.54484
15	5	6	17	7	True	False	58368	225280	2.46004
15	5	6	17	7	False	True	58368	225280	2.72824
15	5	6	17	7	False	False	58368	225280	2.72824
15	5	7	17	8	True	True	59392	229376	2.54503
15	5	7	17	8	True	False	59392	229376	2.46023
15	5	7	17	8	False	True	59392	229376	2.72843
15	5	7	17	8	False	False	59392	229376	2.72843
15	5	8	17	9	True	True	60416	233472	2.5408
15	5	8	17	9	True	False	60416	233472	2.456
15	5	8	17	9	False	True	60416	233472	2.7242
15	5	8	17	9	False	False	60416	233472	2.7242
15	5	9	17	10	True	True	61440	237568	2.5408
15	5	9	17	10	True	False	61440	237568	2.456
15	5	9	17	10	False	True	61440	237568	2.7242
15	5	9	17	10	False	False	61440	237568	2.7242
15	5	10	17	11	True	True	62464	241664	2.5408
15	5	10	17	11	True	False	62464	241664	2.456
15	5	10	17	11	False	True	62464	241664	2.7242
15	5	10	17	11	False	False	62464	241664	2.7242
15	6	0	17	1	True	True	26112	100352	2.70955
15	6	0	17	1	True	False	26112	100352	2.67235
15	6	0	17	1	False	True	26112	100352	2.79835
15	6	0	17	1	False	False	26112	100352	2.79835
15	6	1	17	2	True	True	26624	102400	2.48775

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Table 3 Continued from previous page

C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	6	1	17	2	True	False	26624	102400	2.45215
15	6	1	17	2	False	True	26624	102400	2.58035
15	6	1	17	2	False	False	26624	102400	2.58035
15	6	2	17	3	True	True	27136	104448	2.33512
15	6	2	17	3	True	False	27136	104448	2.29932
15	6	2	17	3	False	True	27136	104448	2.42792
15	6	2	17	3	False	False	27136	104448	2.42792
15	6	3	17	4	True	True	27648	106496	2.18511
15	6	3	17	4	True	False	27648	106496	2.14951
15	6	3	17	4	False	True	27648	106496	2.27811
15	6	3	17	4	False	False	27648	106496	2.27811
15	6	4	17	5	True	True	28160	108544	2.18505
15	6	4	17	5	True	False	28160	108544	2.14965
15	6	4	17	5	False	True	28160	108544	2.27805
15	6	4	17	5	False	False	28160	108544	2.27805
15	6	5	17	6	True	True	28672	110592	2.18512
15	6	5	17	6	True	False	28672	110592	2.14972
15	6	5	17	6	False	True	28672	110592	2.27812
15	6	5	17	6	False	False	28672	110592	2.27812
15	6	6	17	7	True	True	29184	112640	2.18359
15	6	6	17	7	True	False	29184	112640	2.14819
15	6	6	17	7	False	True	29184	112640	2.27659
15	6	6	17	7	False	False	29184	112640	2.27659
15	6	7	17	8	True	True	29696	114688	2.18341
15	6	7	17	8	True	False	29696	114688	2.14801
15	6	7	17	8	False	True	29696	114688	2.27641
15	6	7	17	8	False	False	29696	114688	2.27641
15	6	8	17	9	True	True	30208	116736	2.18138
15	6	8	17	9	True	False	30208	116736	2.14598
15	6	8	17	9	False	True	30208	116736	2.27438
15	6	8	17	9	False	False	30208	116736	2.27438
15	6	9	17	10	True	True	30720	118784	2.18138
15	6	9	17	10	True	False	30720	118784	2.14598
15	6	9	17	10	False	True	30720	118784	2.27438
15	6	9	17	10	False	False	30720	118784	2.27438

Table 4: matmul naive Simulation Results

C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	5	0	17	1	True	True	52224	200704	5.56425
15	5	0	17	1	True	False	52224	200704	5.43265
15	5	0	17	1	False	True	52224	200704	5.84305
15	5	0	17	1	False	False	52224	200704	5.84305
15	5	1	17	2	True	True	53248	204800	5.30856
15	5	1	17	2	True	False	53248	204800	5.17616
15	5	1	17	2	False	True	53248	204800	5.58696
15	5	1	17	2	False	False	53248	204800	5.58696
15	5	2	17	3	True	True	54272	208896	5.05729
15	5	2	17	3	True	False	54272	208896	4.92489
15	5	2	17	3	False	True	54272	208896	5.33609
15	5	2	17	3	False	False	54272	208896	5.33609
15	5	3	17	4	True	True	55296	212992	4.90674
15	5	3	17	4	True	False	55296	212992	4.77434
15	5	3	17	4	False	True	55296	212992	5.18554
15	5	3	17	4	False	False	55296	212992	5.18554
15	5	4	17	5	True	True	56320	217088	4.90635
15	5	4	17	5	True	False	56320	217088	4.77395
15	5	4	17	5	False	True	56320	217088	5.18515
15	5	4	17	5	False	False	56320	217088	5.18515
15	5	5	17	6	True	True	57344	221184	4.90608

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Table 4 Continued from previous page

C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	5	5	17	6	True	False	57344	221184	4.77368
15	5	5	17	6	False	True	57344	221184	5.18488
15	5	5	17	6	False	False	57344	221184	5.18488
15	5	6	17	7	True	True	58368	225280	4.90608
15	5	6	17	7	True	False	58368	225280	4.77368
15	5	6	17	7	False	True	58368	225280	5.18488
15	5	6	17	7	False	False	58368	225280	5.18488
15	5	7	17	8	True	True	59392	229376	4.89126
15	5	7	17	8	True	False	59392	229376	4.75886
15	5	7	17	8	False	True	59392	229376	5.17006
15	5	7	17	8	False	False	59392	229376	5.17006
15	5	8	17	9	True	True	60416	233472	3.8013
15	5	8	17	9	True	False	60416	233472	3.6689
15	5	8	17	9	False	True	60416	233472	4.0801
15	5	8	17	9	False	False	60416	233472	4.0801
15	5	9	17	10	True	True	61440	237568	3.8013
15	5	9	17	10	True	False	61440	237568	3.6689
15	5	9	17	10	False	True	61440	237568	4.0801
15	5	9	17	10	False	False	61440	237568	4.0801
15	5	10	17	11	True	True	62464	241664	3.8013
15	5	10	17	11	True	False	62464	241664	3.6689
15	5	10	17	11	False	True	62464	241664	4.0801
15	5	10	17	11	False	False	62464	241664	4.0801
15	6	0	17	1	True	True	26112	100352	5.01896
15	6	0	17	1	True	False	26112	100352	4.95116
15	6	0	17	1	False	True	26112	100352	5.16056
15	6	0	17	1	False	False	26112	100352	5.16056
15	6	1	17	2	True	True	26624	102400	4.76171
15	6	1	17	2	True	False	26624	102400	4.69491
15	6	1	17	2	False	True	26624	102400	4.90411
15	6	1	17	2	False	False	26624	102400	4.90411
15	6	2	17	3	True	True	27136	104448	4.51162
15	6	2	17	3	True	False	27136	104448	4.44382
15	6	2	17	3	False	True	27136	104448	4.65402
15	6	2	17	3	False	False	27136	104448	4.65402
15	6	3	17	4	True	True	27648	106496	4.36125
15	6	3	17	4	True	False	27648	106496	4.29345
15	6	3	17	4	False	True	27648	106496	4.50365
15	6	3	17	4	False	False	27648	106496	4.50365
15	6	4	17	5	True	True	28160	108544	4.36105
15	6	4	17	5	True	False	28160	108544	4.29325
15	6	4	17	5	False	True	28160	108544	4.50345
15	6	4	17	5	False	False	28160	108544	4.50345
15	6	5	17	6	True	True	28672	110592	4.36091
15	6	5	17	6	True	False	28672	110592	4.29311
15	6	5	17	6	False	True	28672	110592	4.50331
15	6	5	17	6	False	False	28672	110592	4.50331
15	6	6	17	7	True	True	29184	112640	4.36091
15	6	6	17	7	True	False	29184	112640	4.29311
15	6	6	17	7	False	True	29184	112640	4.50331
15	6	6	17	7	False	False	29184	112640	4.50331
15	6	7	17	8	True	True	29696	114688	4.34878
15	6	7	17	8	True	False	29696	114688	4.28098
15	6	7	17	8	False	True	29696	114688	4.49118
15	6	7	17	8	False	False	29696	114688	4.49118
15	6	8	17	9	True	True	30208	116736	2.78544
15	6	8	17	9	True	False	30208	116736	2.71764
15	6	8	17	9	False	True	30208	116736	2.92784
15	6	8	17	9	False	False	30208	116736	2.92784
15	6	9	17	10	True	True	30720	118784	2.78544
15	6	9	17	10	True	False	30720	118784	2.71764
15	6	9	17	10	False	True	30720	118784	2.92784
15	6	9	17	10	False	False	30720	118784	2.92784

Table 5: Linpack Simulation Results

C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	5	0	17	1	True	True	52224	200704	14.3536
15	5	0	17	1	True	False	52224	200704	12.4092
15	5	0	17	1	False	True	52224	200704	20.7492
15	5	0	17	1	False	False	52224	200704	20.7492
15	5	1	17	2	True	True	53248	204800	13.5352
15	5	1	17	2	True	False	53248	204800	11.8944
15	5	1	17	2	False	True	53248	204800	20.2184
15	5	1	17	2	False	False	53248	204800	20.2184
15	5	2	17	3	True	True	54272	208896	13.3351
15	5	2	17	3	True	False	54272	208896	11.6943
15	5	2	17	3	False	True	54272	208896	20.0183
15	5	2	17	3	False	False	54272	208896	20.0183
15	5	3	17	4	True	True	55296	212992	13.1851
15	5	3	17	4	True	False	55296	212992	11.5443
15	5	3	17	4	False	True	55296	212992	19.8683
15	5	3	17	4	False	False	55296	212992	19.8683
15	5	4	17	5	True	True	56320	217088	13.1851
15	5	4	17	5	True	False	56320	217088	11.5443
15	5	4	17	5	False	True	56320	217088	19.8683
15	5	4	17	5	False	False	56320	217088	19.8683
15	5	5	17	6	True	True	57344	221184	13.1851
15	5	5	17	6	True	False	57344	221184	11.5443
15	5	5	17	6	False	True	57344	221184	19.8683
15	5	5	17	6	False	False	57344	221184	19.8683
15	5	6	17	7	True	True	58368	225280	13.1851
15	5	6	17	7	True	False	58368	225280	11.5443
15	5	6	17	7	False	True	58368	225280	19.8683
15	5	6	17	7	False	False	58368	225280	19.8683
15	5	7	17	8	True	True	59392	229376	13.1851
15	5	7	17	8	True	False	59392	229376	11.5443
15	5	7	17	8	False	True	59392	229376	19.8683
15	5	7	17	8	False	False	59392	229376	19.8683
15	5	8	17	9	True	True	60416	233472	13.1851
15	5	8	17	9	True	False	60416	233472	11.5443
15	5	8	17	9	False	True	60416	233472	19.8683
15	5	8	17	9	False	False	60416	233472	19.8683
15	5	9	17	10	True	True	61440	237568	13.1851
15	5	9	17	10	True	False	61440	237568	11.5443
15	5	9	17	10	False	True	61440	237568	19.8683
15	5	9	17	10	False	False	61440	237568	19.8683
15	5	10	17	11	True	True	62464	241664	13.1851
15	5	10	17	11	True	False	62464	241664	11.5443
15	5	10	17	11	False	True	62464	241664	19.8683
15	5	10	17	11	False	False	62464	241664	19.8683
15	6	0	17	1	True	True	26112	100352	8.38989
15	6	0	17	1	True	False	26112	100352	7.30569
15	6	0	17	1	False	True	26112	100352	11.4823
15	6	0	17	1	False	False	26112	100352	11.4823
15	6	1	17	2	True	True	26624	102400	7.87914
15	6	1	17	2	True	False	26624	102400	6.97514
15	6	1	17	2	False	True	26624	102400	11.1459
15	6	1	17	2	False	False	26624	102400	11.1459
15	6	2	17	3	True	True	27136	104448	7.70399
15	6	2	17	3	True	False	27136	104448	6.79999
15	6	2	17	3	False	True	27136	104448	10.9708
15	6	2	17	3	False	False	27136	104448	10.9708
15	6	3	17	4	True	True	27648	106496	7.55399
15	6	3	17	4	True	False	27648	106496	6.64999
15	6	3	17	4	False	True	27648	106496	10.8208
15	6	3	17	4	False	False	27648	106496	10.8208
15	6	4	17	5	True	True	28160	108544	7.55399

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Table 5 Continued from previous page

C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	6	4	17	5	True	False	28160	108544	6.64999
15	6	4	17	5	False	True	28160	108544	10.8208
15	6	4	17	5	False	False	28160	108544	10.8208
15	6	5	17	6	True	True	28672	110592	7.55399
15	6	5	17	6	True	False	28672	110592	6.64999
15	6	5	17	6	False	True	28672	110592	10.8208
15	6	5	17	6	False	False	28672	110592	10.8208
15	6	6	17	7	True	True	29184	112640	7.55399
15	6	6	17	7	True	False	29184	112640	6.64999
15	6	6	17	7	False	True	29184	112640	10.8208
15	6	6	17	7	False	False	29184	112640	10.8208
15	6	7	17	8	True	True	29696	114688	7.55399
15	6	7	17	8	True	False	29696	114688	6.64999
15	6	7	17	8	False	True	29696	114688	10.8208
15	6	7	17	8	False	False	29696	114688	10.8208
15	6	8	17	9	True	True	30208	116736	7.55399
15	6	8	17	9	True	False	30208	116736	6.64999
15	6	8	17	9	False	True	30208	116736	10.8208
15	6	8	17	9	False	False	30208	116736	10.8208
15	6	9	17	10	True	True	30720	118784	7.55399
15	6	9	17	10	True	False	30720	118784	6.64999
15	6	9	17	10	False	True	30720	118784	10.8208
15	6	9	17	10	False	False	30720	118784	10.8208

Table 6: Matmul Tiled Simulation Results

C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	5	0	17	1	True	True	52224	200704	3.05992
15	5	0	17	1	True	False	52224	200704	2.97552
15	5	0	17	1	False	True	52224	200704	3.24132
15	5	0	17	1	False	False	52224	200704	3.24132
15	5	1	17	2	True	True	53248	204800	2.84978
15	5	1	17	2	True	False	53248	204800	2.76418
15	5	1	17	2	False	True	53248	204800	3.03238
15	5	1	17	2	False	False	53248	204800	3.03238
15	5	2	17	3	True	True	54272	208896	2.69655
15	5	2	17	3	True	False	54272	208896	2.61175
15	5	2	17	3	False	True	54272	208896	2.87975
15	5	2	17	3	False	False	54272	208896	2.87975
15	5	3	17	4	True	True	55296	212992	2.54681
15	5	3	17	4	True	False	55296	212992	2.46201
15	5	3	17	4	False	True	55296	212992	2.73021
15	5	3	17	4	False	False	55296	212992	2.73021
15	5	4	17	5	True	True	56320	217088	2.54708
15	5	4	17	5	True	False	56320	217088	2.46228
15	5	4	17	5	False	True	56320	217088	2.73048
15	5	4	17	5	False	False	56320	217088	2.73048
15	5	5	17	6	True	True	57344	221184	2.54722
15	5	5	17	6	True	False	57344	221184	2.46242
15	5	5	17	6	False	True	57344	221184	2.73062
15	5	5	17	6	False	False	57344	221184	2.73062
15	5	6	17	7	True	True	58368	225280	2.54484
15	5	6	17	7	True	False	58368	225280	2.46004
15	5	6	17	7	False	True	58368	225280	2.72824
15	5	6	17	7	False	False	58368	225280	2.72824
15	5	7	17	8	True	True	59392	229376	2.54503
15	5	7	17	8	True	False	59392	229376	2.46023
15	5	7	17	8	False	True	59392	229376	2.72843
15	5	7	17	8	False	False	59392	229376	2.72843
15	5	8	17	9	True	True	60416	233472	2.5408

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Table 6 Continued from previous page

C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	5	8	17	9	True	False	60416	233472	2.456
15	5	8	17	9	False	True	60416	233472	2.7242
15	5	8	17	9	False	False	60416	233472	2.7242
15	5	9	17	10	True	True	61440	237568	2.5408
15	5	9	17	10	True	False	61440	237568	2.456
15	5	9	17	10	False	True	61440	237568	2.7242
15	5	9	17	10	False	False	61440	237568	2.7242
15	5	10	17	11	True	True	62464	241664	2.5408
15	5	10	17	11	True	False	62464	241664	2.456
15	5	10	17	11	False	True	62464	241664	2.7242
15	5	10	17	11	False	False	62464	241664	2.7242
15	6	0	17	1	True	True	26112	100352	2.70955
15	6	0	17	1	True	False	26112	100352	2.67235
15	6	0	17	1	False	True	26112	100352	2.79835
15	6	0	17	1	False	False	26112	100352	2.79835
15	6	1	17	2	True	True	26624	102400	2.48775
15	6	1	17	2	True	False	26624	102400	2.45215
15	6	1	17	2	False	True	26624	102400	2.58035
15	6	1	17	2	False	False	26624	102400	2.58035
15	6	2	17	3	True	True	27136	104448	2.33512
15	6	2	17	3	True	False	27136	104448	2.29932
15	6	2	17	3	False	True	27136	104448	2.42792
15	6	2	17	3	False	False	27136	104448	2.42792
15	6	3	17	4	True	True	27648	106496	2.18511
15	6	3	17	4	True	False	27648	106496	2.14951
15	6	3	17	4	False	True	27648	106496	2.27811
15	6	3	17	4	False	False	27648	106496	2.27811
15	6	4	17	5	True	True	28160	108544	2.18505
15	6	4	17	5	True	False	28160	108544	2.14965
15	6	4	17	5	False	True	28160	108544	2.27805
15	6	4	17	5	False	False	28160	108544	2.27805
15	6	5	17	6	True	True	28672	110592	2.18512
15	6	5	17	6	True	False	28672	110592	2.14972
15	6	5	17	6	False	True	28672	110592	2.27812
15	6	5	17	6	False	False	28672	110592	2.27812
15	6	6	17	7	True	True	29184	112640	2.18359
15	6	6	17	7	True	False	29184	112640	2.14819
15	6	6	17	7	False	True	29184	112640	2.27659
15	6	6	17	7	False	False	29184	112640	2.27659
15	6	7	17	8	True	True	29696	114688	2.18341
15	6	7	17	8	True	False	29696	114688	2.14801
15	6	7	17	8	False	True	29696	114688	2.27641
15	6	7	17	8	False	False	29696	114688	2.27641
15	6	8	17	9	True	True	30208	116736	2.18138
15	6	8	17	9	True	False	30208	116736	2.14598
15	6	8	17	9	False	True	30208	116736	2.27438
15	6	8	17	9	False	False	30208	116736	2.27438
15	6	9	17	10	True	True	30720	118784	2.18138
15	6	9	17	10	True	False	30720	118784	2.14598
15	6	9	17	10	False	True	30720	118784	2.27438
15	6	9	17	10	False	False	30720	118784	2.27438

Table 7: GCC Simulation Results

C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	5	0	17	1	True	True	52224	200704	3.51899
15	5	0	17	1	True	False	52224	200704	3.34459
15	5	0	17	1	False	True	52224	200704	3.57059
15	5	0	17	1	False	False	52224	200704	3.57059
15	5	1	17	2	True	True	53248	204800	3.13518

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Table 7 Continued from previous page

C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	5	1	17	2	True	False	53248	204800	3.00578
15	5	1	17	2	False	True	53248	204800	3.22678
15	5	1	17	2	False	False	53248	204800	3.22678
15	5	2	17	3	True	True	54272	208896	2.93854
15	5	2	17	3	True	False	54272	208896	2.81614
15	5	2	17	3	False	True	54272	208896	3.03674
15	5	2	17	3	False	False	54272	208896	3.03674
15	5	3	17	4	True	True	55296	212992	2.76708
15	5	3	17	4	True	False	55296	212992	2.64248
15	5	3	17	4	False	True	55296	212992	2.86528
15	5	3	17	4	False	False	55296	212992	2.86528
15	5	4	17	5	True	True	56320	217088	2.76491
15	5	4	17	5	True	False	56320	217088	2.63551
15	5	4	17	5	False	True	56320	217088	2.86051
15	5	4	17	5	False	False	56320	217088	2.86051
15	5	5	17	6	True	True	57344	221184	2.7593
15	5	5	17	6	True	False	57344	221184	2.6297
15	5	5	17	6	False	True	57344	221184	2.8573
15	5	5	17	6	False	False	57344	221184	2.8573
15	5	6	17	7	True	True	58368	225280	2.75728
15	5	6	17	7	True	False	58368	225280	2.62668
15	5	6	17	7	False	True	58368	225280	2.85688
15	5	6	17	7	False	False	58368	225280	2.85688
15	5	7	17	8	True	True	59392	229376	2.75707
15	5	7	17	8	True	False	59392	229376	2.62627
15	5	7	17	8	False	True	59392	229376	2.85627
15	5	7	17	8	False	False	59392	229376	2.85627
15	5	8	17	9	True	True	60416	233472	2.75668
15	5	8	17	9	True	False	60416	233472	2.62648
15	5	8	17	9	False	True	60416	233472	2.85668
15	5	8	17	9	False	False	60416	233472	2.85668
15	5	9	17	10	True	True	61440	237568	2.76244
15	5	9	17	10	True	False	61440	237568	2.62664
15	5	9	17	10	False	True	61440	237568	2.85684
15	5	9	17	10	False	False	61440	237568	2.85684
15	5	10	17	11	True	True	62464	241664	2.75909
15	5	10	17	11	True	False	62464	241664	2.62669
15	5	10	17	11	False	True	62464	241664	2.85689
15	5	10	17	11	False	False	62464	241664	2.85689
15	6	0	17	1	True	True	26112	100352	3.14305
15	6	0	17	1	True	False	26112	100352	2.98205
15	6	0	17	1	False	True	26112	100352	3.09945
15	6	0	17	1	False	False	26112	100352	3.09945
15	6	1	17	2	True	True	26624	102400	2.77622
15	6	1	17	2	True	False	26624	102400	2.65882
15	6	1	17	2	False	True	26624	102400	2.77142
15	6	1	17	2	False	False	26624	102400	2.77142
15	6	2	17	3	True	True	27136	104448	2.57506
15	6	2	17	3	True	False	27136	104448	2.46506
15	6	2	17	3	False	True	27136	104448	2.58106
15	6	2	17	3	False	False	27136	104448	2.58106
15	6	3	17	4	True	True	27648	106496	2.39948
15	6	3	17	4	True	False	27648	106496	2.29408
15	6	3	17	4	False	True	27648	106496	2.40808
15	6	3	17	4	False	False	27648	106496	2.40808
15	6	4	17	5	True	True	28160	108544	2.39691
15	6	4	17	5	True	False	28160	108544	2.28671
15	6	4	17	5	False	True	28160	108544	2.39871
15	6	4	17	5	False	False	28160	108544	2.39871
15	6	5	17	6	True	True	28672	110592	2.39712
15	6	5	17	6	True	False	28672	110592	2.28252
15	6	5	17	6	False	True	28672	110592	2.39372

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Table 7 Continued from previous page

C_L1	B_L1	S_L1	C_L2	S_L2	Prefetcher	Stride	Tag Storage L1 (bits)	Tag Storage L2 (bits)	ATT L1
15	6	5	17	6	False	False	28672	110592	2.39372
15	6	6	17	7	True	True	29184	112640	2.39312
15	6	6	17	7	True	False	29184	112640	2.28212
15	6	6	17	7	False	True	29184	112640	2.39052
15	6	6	17	7	False	False	29184	112640	2.39052
15	6	7	17	8	True	True	29696	114688	2.39442
15	6	7	17	8	True	False	29696	114688	2.28082
15	6	7	17	8	False	True	29696	114688	2.38982
15	6	7	17	8	False	False	29696	114688	2.38982
15	6	8	17	9	True	True	30208	116736	2.3958
15	6	8	17	9	True	False	30208	116736	2.2776
15	6	8	17	9	False	True	30208	116736	2.3894
15	6	8	17	9	False	False	30208	116736	2.3894
15	6	9	17	10	True	True	30720	118784	2.39786
15	6	9	17	10	True	False	30720	118784	2.28706
15	6	9	17	10	False	True	30720	118784	2.38906
15	6	9	17	10	False	False	30720	118784	2.38906