Kevin Wang

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PROJECT EXPERIENCE

Senior Research Engineer @SpeedproRobot 2016.7-now

LCD Module Tester

- Built a Zynq based Multi-channel LCD module tester with LVDS/MIPI/TTL output, to test different types of LCD modules.
- Designed a video pattern generator to read data from VDMA(AXI-stream) and convert pixel data to video patterns to fulfill the timing requirements of different LCD modules.
- Designed an IO controller to improve the flexibility of the Power On/Off sequence and to ensure the FFC is well connected, so the LCD module and the tester won't be damaged due to hot-swap or oblique insertion.
- Designed an AXI-M SPI controller to send mass data to bridge chip in a specific order. Significantly reduced the number of communications and the time required for programming the LCD module’s Tcom IC.
- Built a standalone app for ARM(zynq) to initialize peripherals(FPGA) and communicate with PC.

Smart Camera

- Designed a Zynq based system for image processing, machine vision, and control mechanical equipment like Delta Robot.
- Built vision sensor interfaces for parallel pixel(ar0134) and LVDS pixel (Python 1300/2000) data input.
- Developed an image signal processors (ISP) that supports BLC/LSC/HQ_Demosaic/RGB2YUV to improve image quality.
- Adapted the image processing algorithms to FPGA, which improved processing speed by more than 75%.
- Designed a processor that fetches the customized instructions from FIFO and send commands to the Delta Robot based on its status,so the Robot will grasps correctly.
- Implemented a noise cancelling system that recognizes and filters out ms-level electromagnetic interferences to improve the stability of the system.

Research Engineer @SHARP 2012.6-2016.7

Pattern Generator for LCD Panel/Cell

- Created a pattern generator system that can generate check patterns for LCD cells with 48 programmable voltage output channels using an ARM and multiple FPGAs.
- Built a processor that can control the DAC and do branches based on custom instructions, which was used to generate arbitrary waveforms for each channel.
- Designed multi-channel parameters query module so the user can change the parameters of the output of all channels in real-time while keep the synchronization among them.
- Developed an algorithm to generate ramp voltage waveform without using DSPs, which prevented the residual charge and ESD from damaging the panel.
- Built the GUI tool in VB for the users to config the output waveforms with ease.

MIPI Signal board

- Design a system with FPGA, to keep LCD Module(MIPI interface) display through the Reliability test(ESD/high temperature and humidity/low temperature) and to develop specific functions for specific LCD models.
- Built a pattern generator that can generate complex patterns with OSD, and is able to switch between Video Mode and CMD Mode,two diffferent work modes for LCD module.
- Developed a simple processor to communicate with PC through UART and LCD module's Tcon IC for the model designer to adjust the color temperature of the LCD module.
- Designed an algorithm to stabilize the ADC input value, stop the output digital value from floating.
- Improved the stability of the system to make sure the board is fully functional under high temperature and humidity (80°C-95%) or low temperature(-20°C), and last for more than 3600 hours.

EDUCATION

Bachelor’s Degree in Electronical and Information Engineering @Southeast University 2008~2012

SKILLS

- Code/Tool: Verilog(VIVADO ISE), C#(GUI app /VS), C++(standalone app/Xilinx SDK), HLS(VIVADO),Schematic(orCAD).
- IPs: MIG, VDMA,BRAM,AXI_BRAM,FIFO,clock_wiz,AXI_clock,SelectIO.
- Interface: LVDS, MIPI, miniLVDS, SPI, I2C, UART, RS232.
- Architecture, Schematic design, RTL, Simulation, Implementation, bring-up and debug.
- https://github.com/KevinwangNs/