Experiment Report

Start of automated test report 2023-05-03 23:07:31
Author=UNKNOWN@workstation obo Luke Vassallo

Machine Information

sysname=Linux
nodename=workstation
release=5.19.0-40-generic
version=#41~22.04.1-Ubuntu SMP PREEMPT_DYNAMIC Fri Mar 31 16:00:14 UTC 2
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz
CPU cores : 8
CPU base clock : 3.8000 GHz
CPU boost clock : 3.7920 GHz
System Memory : 31.35GB
Nvidia driver version : 525.105.17
Device 0 : NVIDIA GeForce GTX 1080
Device 0 : 8.0GB

Library Information

python : 3.8.16
torch : 1.13.1+cu117
optuna : 3.1.0
numpy : 1.23.3
pandas : 1.5.3
matplotlib : 3.7.1
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

parameter_experiment_262:1682846453_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_0	78.67 ± 5.84 (3)	76.75 ± 7.11 (3)	78.2 ± 6.65 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846453_0	22.35 ± 1.87 (3)	22.21 ± 1.99 (3)	23.64 ± 3.02 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846453_0	97.78 ± 2.94 (4)	93.91 ± 8.67 (4)	93.91 ± 8.67 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_0	99.89 ± 3.02 (3)	92.45 ± 12.86 (3)	90.53 ± 11.63 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846453_0	23.07 ± 6.33 (3)	23.05 ± 6.35 (3)	23.23 ± 5.51 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846453_0	117.02 ± 9.34 (4)	114.48 ± 12.97 (4)	114.48 ± 12.97 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682846453_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_1	26.4 ± 0.0 (1)	26.4 ± 0.0 (1)	28.54 ± 3.97 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846453_1	18.3 ± 2.08 (4)	13.45 ± 1.45 (4)	12.79 ± 1.34 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846453_1	51.95 ± 0.0 (1)	51.95 ± 0.0 (1)	48.58 ± 3.37 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_1	29.04 ± 0.0 (1)	29.04 ± 0.0 (1)	32.8 ± 4.77 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846453_1	17.71 ± 1.53 (4)	13.39 ± 2.82 (4)	11.86 ± 1.47 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846453_1	69.97 ± 0.0 (1)	69.97 ± 0.0 (1)	58.6 ± 11.37 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682846453_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_2	28.6 ± 0.0 (1)	28.96 ± 2.43 (4)	27.64 ± 1.81 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846453_2	15.84 ± 2.38 (4)	14.11 ± 1.17 (4)	13.48 ± 1.36 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846453_2	nan ± nan (0)	52.58 ± 0.0 (1)	52.34 ± 0.29 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_2	34.02 ± 0.0 (1)	32.49 ± 3.18 (4)	30.37 ± 3.92 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846453_2	16.33 ± 3.05 (4)	16.31 ± 3.33 (4)	13.61 ± 3.21 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846453_2	nan ± nan (0)	64.34 ± 0.0 (1)	67.56 ± 3.89 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682846453_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_3	31.41 ± 3.73 (2)	29.85 ± 3.76 (3)	28.96 ± 2.47 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846453_3	18.73 ± 2.55 (3)	14.76 ± 1.12 (3)	13.09 ± 1.06 (3)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846453_3	49.41 ± 1.29 (2)	49.41 ± 1.29 (2)	49.14 ± 1.12 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_3	36.05 ± 8.37 (2)	34.58 ± 7.14 (3)	33.55 ± 5.5 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846453_3	20.83 ± 1.96 (3)	15.06 ± 4.11 (3)	12.71 ± 2.16 (3)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846453_3	61.2 ± 2.8 (2)	61.2 ± 2.8 (2)	61.34 ± 2.29 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682980649_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_0	34.13 ± 0.0 (1)	33.53 ± 0.6 (2)	30.12 ± 1.96 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980649_0	15.68 ± 0.45 (4)	14.74 ± 0.28 (4)	13.97 ± 0.18 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980649_0	nan ± nan (0)	51.85 ± 0.0 (1)	49.62 ± 1.98 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_0	32.46 ± 0.0 (1)	36.34 ± 3.88 (2)	33.98 ± 4.54 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980649_0	14.14 ± 0.85 (4)	13.45 ± 0.87 (4)	12.87 ± 0.98 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980649_0	nan ± nan (0)	59.83 ± 0.0 (1)	60.35 ± 4.2 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682980649_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_1	nan ± nan (0)	32.27 ± 0.0 (1)	28.32 ± 2.8 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980649_1	15.48 ± 0.84 (4)	13.61 ± 1.32 (4)	13.05 ± 1.38 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980649_1	nan ± nan (0)	51.53 ± 5.57 (3)	48.24 ± 3.97 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_1	nan ± nan (0)	38.02 ± 0.0 (1)	29.39 ± 3.56 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980649_1	15.73 ± 2.66 (4)	14.18 ± 2.78 (4)	13.88 ± 2.9 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980649_1	nan ± nan (0)	66.58 ± 13.73 (3)	61.89 ± 10.59 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682980649_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_2	nan ± nan (0)	30.83 ± 3.94 (3)	29.65 ± 4.8 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980649_2	16.53 ± 2.86 (4)	13.58 ± 1.26 (4)	12.85 ± 1.19 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980649_2	nan ± nan (0)	nan ± nan (0)	45.17 ± 2.01 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_2	nan ± nan (0)	34.12 ± 5.32 (3)	34.95 ± 7.01 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980649_2	16.34 ± 3.89 (4)	12.07 ± 1.18 (4)	11.65 ± 1.1 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980649_2	nan ± nan (0)	nan ± nan (0)	51.84 ± 4.43 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682980649_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_3	nan ± nan (0)	28.94 ± 0.98 (2)	29.11 ± 0.74 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980649_3	13.4 ± 1.36 (4)	11.65 ± 0.06 (4)	11.52 ± 0.19 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980649_3	nan ± nan (0)	54.58 ± 0.0 (1)	41.42 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_3	nan ± nan (0)	34.58 ± 3.7 (2)	31.2 ± 3.22 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980649_3	13.45 ± 2.64 (4)	11.79 ± 1.57 (4)	11.57 ± 1.57 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980649_3	nan ± nan (0)	56.77 ± 0.0 (1)	47.17 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682846451_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_0	41.99 ± 0.0 (1)	33.76 ± 8.23 (2)	32.08 ± 7.16 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846451_0	17.28 ± 2.08 (4)	14.16 ± 1.63 (4)	12.64 ± 1.78 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846451_0	nan ± nan (0)	47.02 ± 0.0 (1)	44.08 ± 2.94 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_0	52.6 ± 0.0 (1)	41.75 ± 10.85 (2)	38.28 ± 10.26 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846451_0	17.5 ± 3.6 (4)	14.72 ± 5.55 (4)	13.53 ± 4.82 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846451_0	nan ± nan (0)	49.7 ± 0.0 (1)	48.71 ± 0.99 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682846451_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_1	26.09 ± 0.0 (1)	28.81 ± 1.94 (3)	27.34 ± 1.84 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846451_1	15.52 ± 1.08 (4)	13.64 ± 0.94 (4)	13.12 ± 1.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846451_1	nan ± nan (0)	48.65 ± 1.18 (2)	47.91 ± 3.28 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_1	28.25 ± 0.0 (1)	30.21 ± 2.01 (3)	32.73 ± 5.58 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846451_1	18.19 ± 4.28 (4)	12.74 ± 1.52 (4)	12.23 ± 1.75 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846451_1	nan ± nan (0)	59.15 ± 4.2 (2)	59.14 ± 7.95 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682846451_2

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_2	nan ± nan (0)	29.91 ± 0.0 (1)	33.16 ± 7.04 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846451_2	15.43 ± 1.98 (4)	13.5 ± 1.25 (4)	13.08 ± 1.34 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846451_2	nan ± nan (0)	nan ± nan (0)	45.73 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_2	nan ± nan (0)	28.55 ± 0.0 (1)	37.69 ± 9.04 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846451_2	16.68 ± 3.4 (4)	13.35 ± 3.03 (4)	12.91 ± 2.73 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846451_2	nan ± nan (0)	nan ± nan (0)	58.11 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682846451_3

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_3	28.45 ± 0.0 (1)	28.45 ± 0.0 (1)	27.87 ± 0.0 (1)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846451_3	15.13 ± 1.81 (4)	13.86 ± 1.35 (4)	12.98 ± 1.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846451_3	45.67 ± 0.0 (1)	45.67 ± 0.0 (1)	45.13 ± 3.5 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_3	31.21 ± 0.0 (1)	31.21 ± 0.0 (1)	37.46 ± 0.0 (1)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846451_3	16.1 ± 2.96 (4)	16.38 ± 4.41 (4)	15.55 ± 4.19 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846451_3	50.58 ± 0.0 (1)	50.58 ± 0.0 (1)	52.55 ± 6.47 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682978327_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_0	nan ± nan (0)	26.29 ± 0.0 (1)	27.26 ± 1.02 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682978327_0	20.05 ± 5.66 (4)	18.27 ± 5.21 (4)	13.3 ± 1.47 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682978327_0	nan ± nan (0)	46.04 ± 0.0 (1)	46.04 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_0	nan ± nan (0)	37.25 ± 0.0 (1)	30.05 ± 5.26 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682978327_0	20.29 ± 2.96 (4)	17.69 ± 3.02 (4)	13.11 ± 2.6 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682978327_0	nan ± nan (0)	43.9 ± 0.0 (1)	43.9 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682978327_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_1	nan ± nan (0)	nan ± nan (0)	39.4 ± 21.83 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682978327_1	15.12 ± 0.9 (4)	13.83 ± 0.74 (4)	12.52 ± 1.44 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682978327_1	nan ± nan (0)	nan ± nan (0)	43.3 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_1	nan ± nan (0)	nan ± nan (0)	50.1 ± 25.62 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682978327_1	14.61 ± 1.8 (4)	12.24 ± 1.14 (4)	11.24 ± 1.55 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682978327_1	nan ± nan (0)	nan ± nan (0)	49.67 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682978327_2

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_2	26.93 ± 0.0 (1)	26.84 ± 0.08 (2)	38.16 ± 20.45 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682978327_2	17.69 ± 2.14 (3)	13.36 ± 1.13 (4)	12.83 ± 1.07 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682978327_2	46.7 ± 0.0 (1)	45.04 ± 1.66 (2)	45.16 ± 1.89 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_2	31.81 ± 0.0 (1)	31.42 ± 0.38 (2)	46.22 ± 27.76 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682978327_2	16.35 ± 1.99 (3)	11.65 ± 1.38 (4)	11.58 ± 1.03 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682978327_2	65.85 ± 0.0 (1)	58.22 ± 7.62 (2)	54.7 ± 5.47 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682978327_3

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_3	nan ± nan (0)	32.74 ± 0.0 (1)	27.8 ± 2.23 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682978327_3	16.04 ± 2.31 (4)	13.5 ± 1.87 (4)	12.59 ± 1.44 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682978327_3	48.31 ± 0.0 (1)	48.31 ± 0.0 (1)	46.72 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_3	nan ± nan (0)	30.93 ± 0.0 (1)	31.25 ± 4.5 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682978327_3	16.52 ± 3.64 (4)	12.27 ± 1.99 (4)	12.72 ± 3.0 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682978327_3	67.14 ± 0.0 (1)	67.14 ± 0.0 (1)	56.85 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682846455_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_0	38.7 ± 2.3 (4)	38.41 ± 2.18 (4)	37.07 ± 3.59 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846455_0	14.28 ± 0.35 (4)	14.24 ± 0.37 (4)	14.24 ± 0.37 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846455_0	56.13 ± 6.11 (3)	55.16 ± 5.74 (4)	53.87 ± 4.25 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_0	43.43 ± 8.84 (4)	44.05 ± 9.76 (4)	44.7 ± 9.2 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846455_0	14.42 ± 1.73 (4)	13.52 ± 0.54 (4)	13.52 ± 0.54 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846455_0	63.08 ± 10.86 (3)	63.41 ± 9.35 (4)	64.91 ± 9.15 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682846455_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_1	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846455_1	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846455_1	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_1	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846455_1	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846455_1	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682846455_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_2	41.04 ± 3.61 (4)	38.06 ± 4.64 (4)	37.16 ± 4.62 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846455_2	14.71 ± 1.06 (4)	14.36 ± 0.88 (4)	14.11 ± 1.06 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846455_2	54.72 ± 3.17 (3)	54.71 ± 3.89 (4)	52.87 ± 3.05 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_2	46.91 ± 7.78 (4)	42.78 ± 7.35 (4)	43.94 ± 9.97 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846455_2	15.31 ± 4.08 (4)	14.27 ± 2.56 (4)	14.28 ± 2.71 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846455_2	63.55 ± 1.45 (3)	66.97 ± 5.73 (4)	68.24 ± 3.76 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682846455_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_3	36.69 ± 2.96 (4)	34.86 ± 3.28 (4)	34.58 ± 3.24 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846455_3	16.51 ± 1.75 (4)	16.44 ± 1.7 (4)	16.42 ± 1.68 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846455_3	59.39 ± 5.01 (4)	53.18 ± 4.34 (4)	51.96 ± 3.92 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_3	41.38 ± 5.19 (4)	38.35 ± 4.84 (4)	35.49 ± 3.24 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846455_3	18.09 ± 3.38 (4)	16.63 ± 2.54 (4)	17.92 ± 3.23 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846455_3	64.46 ± 3.92 (4)	64.01 ± 6.35 (4)	67.79 ± 7.9 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682980882_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_0	45.32 ± 11.85 (3)	41.08 ± 9.07 (4)	40.93 ± 9.19 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980882_0	14.69 ± 1.96 (4)	14.01 ± 2.07 (4)	13.85 ± 2.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980882_0	57.27 ± 3.92 (3)	54.95 ± 3.87 (4)	54.36 ± 3.81 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_0	58.71 ± 17.41 (3)	54.99 ± 18.44 (4)	53.81 ± 19.45 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980882_0	12.84 ± 1.24 (4)	12.07 ± 1.64 (4)	11.96 ± 1.7 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980882_0	68.18 ± 8.51 (3)	68.17 ± 6.13 (4)	65.05 ± 8.13 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682980882_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_1	34.64 ± 3.27 (3)	32.08 ± 2.99 (4)	31.84 ± 2.77 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980882_1	14.8 ± 0.46 (4)	14.62 ± 0.3 (4)	14.47 ± 0.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980882_1	63.71 ± 12.03 (3)	53.52 ± 2.28 (4)	52.49 ± 3.07 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_1	41.31 ± 3.44 (3)	41.28 ± 7.47 (4)	37.26 ± 2.21 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980882_1	16.7 ± 0.9 (4)	16.31 ± 1.52 (4)	15.03 ± 0.82 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980882_1	77.41 ± 14.28 (3)	64.15 ± 9.84 (4)	61.29 ± 7.01 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682980882_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_2	37.9 ± 2.78 (4)	36.1 ± 2.58 (4)	35.28 ± 2.65 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980882_2	14.28 ± 0.59 (4)	14.18 ± 0.55 (4)	14.14 ± 0.58 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980882_2	54.47 ± 0.11 (3)	53.27 ± 0.71 (4)	51.84 ± 0.94 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_2	48.68 ± 9.8 (4)	40.67 ± 4.54 (4)	40.74 ± 4.59 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980882_2	17.08 ± 0.99 (4)	16.1 ± 2.16 (4)	15.94 ± 2.4 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980882_2	61.06 ± 3.38 (3)	59.84 ± 4.72 (4)	61.0 ± 5.24 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682980882_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_3	37.22 ± 3.59 (3)	33.2 ± 5.2 (4)	32.96 ± 5.22 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980882_3	14.38 ± 0.83 (4)	13.84 ± 0.74 (4)	13.71 ± 0.67 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980882_3	57.84 ± 3.16 (4)	55.99 ± 3.42 (4)	55.06 ± 3.42 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_3	41.12 ± 3.45 (3)	45.22 ± 11.11 (4)	44.91 ± 11.38 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980882_3	15.7 ± 4.15 (4)	14.52 ± 3.29 (4)	14.38 ± 3.24 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980882_3	69.18 ± 6.78 (4)	69.3 ± 11.5 (4)	65.44 ± 7.07 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682846457_0

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_0	nan ± nan (0)	nan ± nan (0)	27.54 ± 4.44 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846457_0	15.59 ± 0.21 (4)	13.86 ± 1.16 (4)	13.44 ± 1.21 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846457_0	44.81 ± 0.0 (1)	44.81 ± 0.0 (1)	44.81 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_0	nan ± nan (0)	nan ± nan (0)	31.53 ± 8.76 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846457_0	15.61 ± 1.83 (4)	14.75 ± 2.57 (4)	13.66 ± 2.6 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846457_0	48.1 ± 0.0 (1)	48.1 ± 0.0 (1)	48.1 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682846457_1

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_1	nan ± nan (0)	nan ± nan (0)	28.84 ± 0.0 (1)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846457_1	14.74 ± 0.86 (4)	13.36 ± 0.69 (4)	12.98 ± 0.59 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846457_1	nan ± nan (0)	42.77 ± 0.0 (1)	42.72 ± 2.07 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_1	nan ± nan (0)	nan ± nan (0)	27.98 ± 0.0 (1)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846457_1	14.03 ± 2.2 (4)	11.37 ± 1.26 (4)	11.17 ± 1.16 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846457_1	nan ± nan (0)	45.1 ± 0.0 (1)	47.24 ± 2.22 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682846457_2

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_2	28.02 ± 0.59 (2)	28.02 ± 0.59 (2)	27.21 ± 1.24 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846457_2	13.6 ± 1.8 (4)	13.48 ± 1.69 (4)	13.13 ± 1.47 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846457_2	nan ± nan (0)	44.88 ± 0.0 (1)	47.39 ± 2.5 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_2	38.75 ± 0.77 (2)	38.75 ± 0.77 (2)	36.43 ± 3.35 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846457_2	14.14 ± 4.4 (4)	12.45 ± 2.21 (4)	12.33 ± 2.52 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846457_2	nan ± nan (0)	50.0 ± 0.0 (1)	54.18 ± 4.18 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682846457_3

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_3	nan ± nan (0)	nan ± nan (0)	27.29 ± 1.05 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846457_3	14.6 ± 2.48 (3)	13.04 ± 1.73 (4)	12.8 ± 1.69 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846457_3	42.61 ± 0.0 (1)	42.61 ± 0.0 (1)	42.61 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_3	nan ± nan (0)	nan ± nan (0)	44.46 ± 6.06 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846457_3	14.42 ± 3.48 (3)	12.29 ± 2.06 (4)	12.75 ± 2.92 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846457_3	49.69 ± 0.0 (1)	49.69 ± 0.0 (1)	49.69 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682981272_0

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_0	nan ± nan (0)	27.44 ± 1.25 (2)	26.19 ± 1.53 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682981272_0	13.73 ± 1.32 (4)	13.43 ± 1.41 (4)	12.86 ± 1.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682981272_0	nan ± nan (0)	nan ± nan (0)	44.33 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_0	nan ± nan (0)	31.66 ± 3.38 (2)	30.01 ± 3.46 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682981272_0	12.49 ± 1.45 (4)	14.13 ± 3.77 (4)	14.67 ± 2.68 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682981272_0	nan ± nan (0)	nan ± nan (0)	40.69 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682981272_1

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_1	nan ± nan (0)	nan ± nan (0)	29.49 ± 2.54 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682981272_1	15.32 ± 1.58 (4)	13.37 ± 1.15 (4)	12.61 ± 1.42 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682981272_1	nan ± nan (0)	47.0 ± 2.97 (4)	45.96 ± 2.05 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_1	nan ± nan (0)	nan ± nan (0)	31.72 ± 3.36 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682981272_1	16.39 ± 3.67 (4)	16.22 ± 5.15 (4)	13.04 ± 3.62 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682981272_1	nan ± nan (0)	51.91 ± 6.49 (4)	52.12 ± 7.12 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682981272_2

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_2	30.32 ± 0.0 (1)	27.57 ± 2.75 (2)	27.5 ± 2.45 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682981272_2	15.84 ± 1.15 (4)	13.9 ± 0.6 (4)	12.8 ± 1.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682981272_2	nan ± nan (0)	45.88 ± 2.45 (3)	45.88 ± 2.45 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_2	28.12 ± 0.0 (1)	26.42 ± 1.7 (2)	28.5 ± 1.47 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682981272_2	14.92 ± 2.63 (4)	12.21 ± 1.29 (4)	11.7 ± 1.32 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682981272_2	nan ± nan (0)	53.31 ± 7.31 (3)	53.31 ± 7.31 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682981272_3

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_3	nan ± nan (0)	72.47 ± 0.0 (1)	46.38 ± 14.23 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682981272_3	16.49 ± 0.72 (4)	14.49 ± 0.84 (4)	13.01 ± 1.3 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682981272_3	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_3	nan ± nan (0)	84.58 ± 0.0 (1)	47.04 ± 13.98 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682981272_3	18.81 ± 2.91 (4)	14.23 ± 2.19 (4)	11.63 ± 1.68 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682981272_3	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed