Experiment Report

Start of automated test report 2023-03-07 07:51:37
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Machine Information

sysname=Linux
nodename=workstation
release=5.4.0-144-generic
version=#161~18.04.1-Ubuntu SMP Fri Feb 10 15:55:22 UTC 2023
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz
CPU cores : 16
CPU base clock : 3.8000 GHz
CPU boost clock : 4.7894 GHz
System Memory : 62.64GB
Nvidia driver version : 470.161.03
Device 0 : NVIDIA GeForce GTX 1080
Device 0 : 7.93GB

Library Information

python : 3.8.13
torch : 1.11.0+cu102
optuna : 3.1.0
numpy : 1.23.3
pandas : 1.5.3
matplotlib : 3.7.0
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

training_td3_cpu_622:1678118952_0

Steps per trial = 200

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/tests/01_training_td3_cpu/work/eval_testing_set/1678118952_0

pcb name	trial	0% overlap	10% overlap	20% overlap
voltage_datalogger_adc0	trial_0	32.6	32.6	32.6
voltage_datalogger_adc0	trial_1	28.69	28.69	28.69
voltage_datalogger_adc2	trial_0	14.87	11.67	11.67
voltage_datalogger_adc2	trial_1	16.22	15.5	14.64

Mean over all trials in run //home/luke/work/rl_pcb/tests/01_training_td3_cpu/work/eval_testing_set/1678118952_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]
voltage_datalogger_adc0	1678118952_0	30.65 ± 1.96 (2)	30.65 ± 1.96 (2)	30.65 ± 1.96 (2)
voltage_datalogger_adc2	1678118952_0	15.54 ± 0.67 (2)	13.58 ± 1.92 (2)	13.16 ± 1.49 (2)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/tests/01_training_td3_cpu/work/eval_testing_set/1678118952_0

pcb name	trial	0% overlap	10% overlap	20% overlap
voltage_datalogger_adc0	trial_0	34.45	34.45	34.45
voltage_datalogger_adc0	trial_1	40.74	40.74	40.74
voltage_datalogger_adc2	trial_0	12.07	10.31	10.31
voltage_datalogger_adc2	trial_1	16.89	17.65	16.59

Mean over all trials in run //home/luke/work/rl_pcb/tests/01_training_td3_cpu/work/eval_testing_set/1678118952_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]
voltage_datalogger_adc0	1678118952_0	37.6 ± 3.14 (2)	37.6 ± 3.14 (2)	37.6 ± 3.14 (2)
voltage_datalogger_adc2	1678118952_0	14.48 ± 2.41 (2)	13.98 ± 3.67 (2)	13.45 ± 3.14 (2)

[1] # indicates the number of layouts over which the mean ± std was computed

training_td3_cpu_622:1678118952_1

Steps per trial = 200

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/tests/01_training_td3_cpu/work/eval_testing_set/1678118952_1

pcb name	trial	0% overlap	10% overlap	20% overlap
voltage_datalogger_adc0	trial_0	-	-	27.0
voltage_datalogger_adc2	trial_0	29.81	14.32	12.58
voltage_datalogger_adc2	trial_1	-	14.07	14.07

Mean over all trials in run //home/luke/work/rl_pcb/tests/01_training_td3_cpu/work/eval_testing_set/1678118952_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]
voltage_datalogger_adc0	1678118952_1	nan ± nan (0)	nan ± nan (0)	27.0 ± 0.0 (1)
voltage_datalogger_adc2	1678118952_1	29.81 ± 0.0 (1)	14.2 ± 0.12 (2)	13.32 ± 0.75 (2)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/tests/01_training_td3_cpu/work/eval_testing_set/1678118952_1

pcb name	trial	0% overlap	10% overlap	20% overlap
voltage_datalogger_adc0	trial_0	-	-	26.35
voltage_datalogger_adc2	trial_0	22.59	11.36	10.19
voltage_datalogger_adc2	trial_1	-	18.03	18.03

Mean over all trials in run //home/luke/work/rl_pcb/tests/01_training_td3_cpu/work/eval_testing_set/1678118952_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]
voltage_datalogger_adc0	1678118952_1	nan ± nan (0)	nan ± nan (0)	26.35 ± 0.0 (1)

voltage_datalogger_adc2	1678118952_1	22.59 ± 0.0 (1)	14.7 ± 3.34 (2)	14.11 ± 3.92 (2)

[1] # indicates the number of layouts over which the mean ± std was computed