Experiment Report

Start of automated test report 2023-05-30 06:09:34
Author=UNKNOWN@workstation obo Luke Vassallo

Machine Information

sysname=Linux
nodename=workstation
release=5.19.0-41-generic
version=#42~22.04.1-Ubuntu SMP PREEMPT_DYNAMIC Tue Apr 18 17:40:00 UTC 2
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz
CPU cores : 8
CPU base clock : 3.8000 GHz
CPU boost clock : 3.7920 GHz
System Memory : 31.35GB
Nvidia driver version : 525.105.17
Device 0 : NVIDIA GeForce GTX 1080
Device 0 : 8.0GB

Library Information

python : 3.8.16
torch : 1.13.1+cu117
optuna : 3.1.1
numpy : 1.23.3
pandas : 2.0.2
matplotlib : 3.7.1
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

training_sac_cuda_262:1685397120_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/gitlab-runner/builds/TfLwHVT9/1/luke/rl_pcb/tests/07_training_sac_cuda_fast/work/eval_testing_set/1685397120_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1685397120_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1685397120_0	12.54 ± 1.04 (4)	11.88 ± 0.95 (4)	11.24 ± 0.62 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1685397120_0	nan ± nan (0)	nan ± nan (0)	53.16 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/gitlab-runner/builds/TfLwHVT9/1/luke/rl_pcb/tests/07_training_sac_cuda_fast/work/eval_testing_set/1685397120_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1685397120_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1685397120_0	11.76 ± 0.57 (4)	10.83 ± 0.15 (4)	10.36 ± 0.15 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1685397120_0	nan ± nan (0)	nan ± nan (0)	62.5 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

training_sac_cuda_262:1685397120_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/gitlab-runner/builds/TfLwHVT9/1/luke/rl_pcb/tests/07_training_sac_cuda_fast/work/eval_testing_set/1685397120_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1685397120_1	31.99 ± 0.0 (1)	32.93 ± 0.94 (2)	29.28 ± 2.71 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1685397120_1	15.22 ± 1.23 (4)	13.68 ± 1.32 (4)	13.0 ± 1.32 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1685397120_1	37.89 ± 0.0 (1)	49.09 ± 7.97 (3)	50.61 ± 7.38 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/gitlab-runner/builds/TfLwHVT9/1/luke/rl_pcb/tests/07_training_sac_cuda_fast/work/eval_testing_set/1685397120_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1685397120_1	32.78 ± 0.0 (1)	40.8 ± 8.02 (2)	34.64 ± 1.86 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1685397120_1	14.42 ± 2.19 (4)	13.67 ± 2.68 (4)	13.03 ± 2.44 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1685397120_1	40.23 ± 0.0 (1)	59.54 ± 14.07 (3)	55.33 ± 9.23 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed