Experiment Report

Start of automated test report 2023-04-14 13:14:04
Author=UNKNOWN@workstation obo Luke Vassallo

Machine Information

sysname=Linux
nodename=workstation
release=5.19.0-38-generic
version=#39~22.04.1-Ubuntu SMP PREEMPT_DYNAMIC Fri Mar 17 21:16:15 UTC 2
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz
CPU cores : 8
CPU base clock : 3.8000 GHz
CPU boost clock : 3.7920 GHz
System Memory : 31.35GB
Nvidia driver version : 525.105.17
Device 0 : NVIDIA GeForce GTX 1080
Device 0 : 8.0GB

Library Information

python : 3.8.16
torch : 1.13.1+cu117
optuna : 3.1.0
numpy : 1.23.3
pandas : 1.5.3
matplotlib : 3.7.1
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

training_sac_cuda_622:1681372314_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1681372314_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372314_0	30.55 ± 0.0 (1)	28.7 ± 1.85 (2)	28.47 ± 1.16 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681372314_0	15.36 ± 1.41 (4)	13.47 ± 1.59 (4)	12.79 ± 1.69 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681372314_0	47.18 ± 0.0 (1)	47.81 ± 0.46 (3)	47.81 ± 0.46 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1681372314_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372314_0	29.94 ± 0.0 (1)	32.58 ± 2.64 (2)	31.11 ± 2.92 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681372314_0	14.15 ± 2.34 (4)	13.15 ± 2.7 (4)	11.6 ± 1.71 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681372314_0	57.31 ± 0.0 (1)	58.13 ± 1.75 (3)	58.13 ± 1.75 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

training_sac_cuda_622:1681372314_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1681372314_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372314_1	nan ± nan (0)	31.9 ± 2.5 (2)	30.07 ± 2.91 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681372314_1	15.0 ± 1.61 (4)	13.77 ± 1.25 (4)	12.36 ± 1.4 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681372314_1	46.63 ± 2.42 (2)	46.63 ± 2.42 (2)	45.44 ± 2.6 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1681372314_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372314_1	nan ± nan (0)	31.58 ± 2.79 (2)	33.1 ± 6.03 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681372314_1	13.04 ± 1.49 (4)	12.7 ± 1.33 (4)	11.64 ± 1.58 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681372314_1	61.0 ± 5.86 (2)	61.0 ± 5.86 (2)	57.66 ± 6.72 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

training_sac_cuda_622:1681372314_2

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1681372314_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372314_2	nan ± nan (0)	nan ± nan (0)	32.72 ± 0.0 (1)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681372314_2	16.69 ± 2.33 (3)	15.06 ± 0.89 (4)	13.5 ± 1.71 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681372314_2	nan ± nan (0)	nan ± nan (0)	51.31 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1681372314_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372314_2	nan ± nan (0)	nan ± nan (0)	35.07 ± 0.0 (1)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681372314_2	19.89 ± 4.63 (3)	15.74 ± 2.89 (4)	13.63 ± 3.26 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681372314_2	nan ± nan (0)	nan ± nan (0)	46.62 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

training_sac_cuda_622:1681372314_3

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1681372314_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372314_3	31.47 ± 0.0 (1)	28.88 ± 2.59 (2)	28.88 ± 2.59 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681372314_3	14.82 ± 0.77 (4)	13.32 ± 1.24 (4)	12.04 ± 1.14 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681372314_3	nan ± nan (0)	nan ± nan (0)	48.71 ± 3.17 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1681372314_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372314_3	36.77 ± 0.0 (1)	31.29 ± 5.49 (2)	31.29 ± 5.49 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681372314_3	14.56 ± 1.82 (4)	12.98 ± 2.31 (4)	13.01 ± 3.19 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681372314_3	nan ± nan (0)	nan ± nan (0)	54.93 ± 2.92 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed