

# Experiment Report

Start of automated test report 2023-04-14 13:14:03

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## Machine Information

sysname=Linux

nodename=workstation

release=5.19.0-38-generic

version=#39~22.04.1-Ubuntu SMP PREEMPT\_DYNAMIC Fri Mar 17 21:16:15 UTC 2

machine=x86\_64

CPU arch : X86\_64

CPU bits : 64

CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz

CPU cores : 8

CPU base clock : 3.8000 GHz

CPU boost clock : 3.7920 GHz

System Memory : 31.35GB

Nvidia driver version : 525.105.17

Device 0 : NVIDIA GeForce GTX 1080

Device 0 : 8.0GB

## Library Information

python : 3.8.16

torch : 1.13.1+cu117

optuna : 3.1.0

numpy : 1.23.3

pandas : 1.5.3

matplotlib : 3.7.1

seaborn : 0.12.2

pcb library: generation of .pcb files.

Library version : 0.0.12

Library built with : C++14

Library built on : Mar 3 2023 23:10:31

netlist\_graph: Graph pre-processing library for PCB component placement.

Library version : 0.1.16

Library built with : C++14

Library built on : Mar 3 2023 23:10:32

## training\_td3\_cuda\_622:1681372339\_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

### Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl\_pcb/tests/02\_training\_td3\_cuda/work/eval\_testing\_set/1681372339\_0

pcb name	run	0% overlap (#) <sup>1</sup>	10% overlap (#) <sup>1</sup>	20% overlap (#) <sup>1</sup>	simulated annealing
voltage_datalogger_adc0	1681372339_0	nan ± nan (0)	30.49 ± 0.0 (1)	28.42 ± 1.96 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681372339_0	18.15 ± 3.61 (4)	16.52 ± 3.77 (4)	16.0 ± 4.07 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681372339_0	nan ± nan (0)	43.57 ± 0.0 (1)	45.45 ± 1.88 (2)	48.58 ± 2.08 (4)

<sup>1</sup> # indicates the number of layouts over which the mean ± std was computed

### Routed Wirelength

Mean over all trials in run //home/luke/work/rl\_pcb/tests/02\_training\_td3\_cuda/work/eval\_testing\_set/1681372339\_0

pcb name	run	0% overlap (#) <sup>1</sup>	10% overlap (#) <sup>1</sup>	20% overlap (#) <sup>1</sup>	simulated annealing
voltage_datalogger_adc0	1681372339_0	nan ± nan (0)	38.44 ± 0.0 (1)	34.32 ± 2.67 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681372339_0	18.42 ± 1.78 (4)	17.54 ± 1.57 (4)	15.82 ± 2.14 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681372339_0	nan ± nan (0)	46.82 ± 0.0 (1)	55.3 ± 8.48 (2)	75.3 ± 3.94 (4)

<sup>1</sup> # indicates the number of layouts over which the mean ± std was computed

## training\_td3\_cuda\_622:1681372339\_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

### Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl\_pcb/tests/02\_training\_td3\_cuda/work/eval\_testing\_set/1681372339\_1

pcb name	run	0% overlap (#) <sup>1</sup>	10% overlap (#) <sup>1</sup>	20% overlap (#) <sup>1</sup>	simulated annealing
voltage_datalogger_adc0	1681372339_1	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681372339_1	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681372339_1	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

<sup>1</sup> # indicates the number of layouts over which the mean ± std was computed

### Routed Wirelength

Mean over all trials in run //home/luke/work/rl\_pcb/tests/02\_training\_td3\_cuda/work/eval\_testing\_set/1681372339\_1

pcb name	run	0% overlap (#) <sup>1</sup>	10% overlap (#) <sup>1</sup>	20% overlap (#) <sup>1</sup>	simulated annealing
voltage_datalogger_adc0	1681372339_1	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681372339_1	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681372339_1	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

<sup>1</sup> # indicates the number of layouts over which the mean ± std was computed

## training\_td3\_cuda\_622:1681372339\_2

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

### Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl\_pcb/tests/02\_training\_td3\_cuda/work/eval\_testing\_set/1681372339\_2

pcb name	run	0% overlap (#) <sup>1</sup>	10% overlap (#) <sup>1</sup>	20% overlap (#) <sup>1</sup>	simulated annealing
voltage_datalogger_adc0	1681372339_2	41.96 ± 0.0 (1)	34.2 ± 7.76 (2)	28.13 ± 2.9 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681372339_2	14.05 ± 1.11 (3)	12.84 ± 1.57 (3)	16.19 ± 6.64 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681372339_2	nan ± nan (0)	nan ± nan (0)	48.28 ± 2.62 (3)	48.58 ± 2.08 (4)

<sup>1</sup> # indicates the number of layouts over which the mean ± std was computed

### Routed Wirelength

Mean over all trials in run //home/luke/work/rl\_pcb/tests/02\_training\_td3\_cuda/work/eval\_testing\_set/1681372339\_2

pcb name	run	0% overlap (#) <sup>1</sup>	10% overlap (#) <sup>1</sup>	20% overlap (#) <sup>1</sup>	simulated annealing
voltage_datalogger_adc0	1681372339_2	55.87 ± 0.0 (1)	43.89 ± 11.98 (2)	37.18 ± 6.44 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681372339_2	13.71 ± 3.6 (3)	13.12 ± 3.5 (3)	17.84 ± 9.86 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681372339_2	nan ± nan (0)	nan ± nan (0)	64.5 ± 8.7 (3)	75.3 ± 3.94 (4)

<sup>1</sup> # indicates the number of layouts over which the mean ± std was computed

## training\_td3\_cuda\_622:1681372339\_3

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

### Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl\_pcb/tests/02\_training\_td3\_cuda/work/eval\_testing\_set/1681372339\_3

pcb name	run	0% overlap (#) <sup>1</sup>	10% overlap (#) <sup>1</sup>	20% overlap (#) <sup>1</sup>	simulated annealing
voltage_datalogger_adc0	1681372339_3	nan ± nan (0)	nan ± nan (0)	32.27 ± 4.03 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681372339_3	15.82 ± 1.23 (4)	14.33 ± 1.29 (4)	13.15 ± 1.36 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681372339_3	nan ± nan (0)	nan ± nan (0)	44.83 ± 0.0 (1)	48.58 ± 2.08 (4)

<sup>1</sup> # indicates the number of layouts over which the mean ± std was computed

### Routed Wirelength

Mean over all trials in run //home/luke/work/rl\_pcb/tests/02\_training\_td3\_cuda/work/eval\_testing\_set/1681372339\_3

pcb name	run	0% overlap (#) <sup>1</sup>	10% overlap (#) <sup>1</sup>	20% overlap (#) <sup>1</sup>	simulated annealing
voltage_datalogger_adc0	1681372339_3	nan ± nan (0)	nan ± nan (0)	40.4 ± 1.93 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681372339_3	16.86 ± 4.79 (4)	17.03 ± 3.54 (4)	14.85 ± 4.18 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681372339_3	nan ± nan (0)	nan ± nan (0)	51.27 ± 0.0 (1)	75.3 ± 3.94 (4)

<sup>1</sup> # indicates the number of layouts over which the mean ± std was computed