Experiment Report

Start of automated test report 2023-04-20 21:39:51
Author=UNKNOWN@workstation obo Luke Vassallo

Machine Information

sysname=Linux
nodename=workstation
release=5.19.0-38-generic
version=#39~22.04.1-Ubuntu SMP PREEMPT_DYNAMIC Fri Mar 17 21:16:15 UTC 2
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz
CPU cores : 8
CPU base clock : 3.8000 GHz
CPU boost clock : 3.7920 GHz
System Memory : 31.35GB
Nvidia driver version : 525.105.17
Device 0 : NVIDIA GeForce GTX 1080
Device 0 : 8.0GB

Library Information

python : 3.8.16
torch : 1.13.1+cu117
optuna : 3.1.0
numpy : 1.23.3
pandas : 1.5.3
matplotlib : 3.7.1
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

parameter_experiment_262:1681717898_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681717898_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	30.21	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	25.49	25.49	36.03
voltage_datalogger_adc0	trial_3	-	-	75.82	28.57
voltage_datalogger_adc2	trial_0	12.57	11.62	11.07	12.81
voltage_datalogger_adc2	trial_1	15.21	14.59	14.0	12.18
voltage_datalogger_adc2	trial_2	13.01	11.61	11.01	13.9
voltage_datalogger_adc2	trial_3	18.16	16.28	15.0	12.85
voltage_datalogger_afe	trial_0	-	42.76	42.76	49.34
voltage_datalogger_afe	trial_1	-	42.69	42.69	49.26
voltage_datalogger_afe	trial_2	-	43.96	43.96	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_0	nan ± nan (0)	25.49 ± 0.0 (1)	43.84 ± 22.7 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717898_0	14.74 ± 2.21 (4)	13.52 ± 2.0 (4)	12.77 ± 1.77 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717898_0	nan ± nan (0)	43.14 ± 0.58 (3)	43.14 ± 0.58 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	39.37	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	29.29	29.29	41.48
voltage_datalogger_adc0	trial_3	-	-	102.78	29.14
voltage_datalogger_adc2	trial_0	11.79	10.72	10.43	12.02
voltage_datalogger_adc2	trial_1	13.65	13.11	12.53	12.07
voltage_datalogger_adc2	trial_2	11.92	10.65	10.19	13.34
voltage_datalogger_adc2	trial_3	25.23	21.76	20.02	15.88
voltage_datalogger_afe	trial_0	-	45.68	45.68	77.93
voltage_datalogger_afe	trial_1	-	54.41	54.41	78.01
voltage_datalogger_afe	trial_2	-	51.03	51.03	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_0	nan ± nan (0)	29.29 ± 0.0 (1)	57.15 ± 32.53 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717898_0	15.65 ± 5.58 (4)	14.06 ± 4.55 (4)	13.29 ± 3.99 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717898_0	nan ± nan (0)	50.37 ± 3.59 (3)	50.37 ± 3.59 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681717898_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681717898_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	81.59	81.59	81.59	36.03
voltage_datalogger_adc0	trial_3	81.83	81.83	81.83	28.57
voltage_datalogger_adc2	trial_0	35.08	35.08	35.08	12.81
voltage_datalogger_adc2	trial_1	-	-	28.62	12.18
voltage_datalogger_adc2	trial_2	26.02	26.02	26.02	13.9
voltage_datalogger_adc2	trial_3	24.05	24.05	24.05	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	97.19	97.19	97.19	45.1
voltage_datalogger_afe	trial_3	97.25	97.25	97.25	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_1	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717898_1	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717898_1	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	92.68	92.68	92.68	41.48
voltage_datalogger_adc0	trial_3	96.93	96.93	96.93	29.14
voltage_datalogger_adc2	trial_0	28.52	28.52	28.52	12.02
voltage_datalogger_adc2	trial_1	-	-	34.5	12.07
voltage_datalogger_adc2	trial_2	21.81	21.81	21.81	13.34
voltage_datalogger_adc2	trial_3	30.96	30.96	30.96	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	120.97	120.97	120.97	76.72
voltage_datalogger_afe	trial_3	122.94	122.94	122.94	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_1	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717898_1	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717898_1	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681717898_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681717898_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	29.98	29.98	30.87
voltage_datalogger_adc0	trial_1	-	26.09	25.33	25.52
voltage_datalogger_adc0	trial_2	-	-	28.31	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	12.09	12.09	11.1	12.81
voltage_datalogger_adc2	trial_1	15.86	14.79	13.74	12.18
voltage_datalogger_adc2	trial_2	15.49	14.79	11.21	13.9
voltage_datalogger_adc2	trial_3	18.27	14.78	13.81	12.85
voltage_datalogger_afe	trial_0	-	54.84	54.84	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_2	nan ± nan (0)	28.04 ± 1.95 (2)	27.87 ± 1.92 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717898_2	15.43 ± 2.2 (4)	14.11 ± 1.17 (4)	12.46 ± 1.31 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717898_2	nan ± nan (0)	54.84 ± 0.0 (1)	54.84 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	35.95	35.95	58.96
voltage_datalogger_adc0	trial_1	-	30.53	29.04	25.98
voltage_datalogger_adc0	trial_2	-	-	32.11	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	9.87	9.87	9.91	12.02
voltage_datalogger_adc2	trial_1	20.58	15.29	12.51	12.07
voltage_datalogger_adc2	trial_2	19.59	16.91	10.23	13.34
voltage_datalogger_adc2	trial_3	18.07	21.56	17.38	15.88
voltage_datalogger_afe	trial_0	-	60.35	60.35	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_2	nan ± nan (0)	33.24 ± 2.71 (2)	32.37 ± 2.83 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717898_2	17.03 ± 4.23 (4)	15.91 ± 4.18 (4)	12.51 ± 2.99 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717898_2	nan ± nan (0)	60.35 ± 0.0 (1)	60.35 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681717898_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681717898_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	29.06	29.06	30.87
voltage_datalogger_adc0	trial_1	-	-	27.25	25.52
voltage_datalogger_adc0	trial_2	-	-	30.07	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	16.34	16.34	12.68	12.81
voltage_datalogger_adc2	trial_1	15.51	14.78	14.37	12.18
voltage_datalogger_adc2	trial_2	16.51	13.23	11.73	13.9
voltage_datalogger_adc2	trial_3	15.37	14.5	13.93	12.85
voltage_datalogger_afe	trial_0	-	46.93	46.71	49.34
voltage_datalogger_afe	trial_1	-	-	53.52	49.26
voltage_datalogger_afe	trial_2	-	-	46.82	45.1
voltage_datalogger_afe	trial_3	-	-	47.51	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_3	nan ± nan (0)	29.06 ± 0.0 (1)	28.79 ± 1.17 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717898_3	15.93 ± 0.5 (4)	14.71 ± 1.11 (4)	13.18 ± 1.04 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717898_3	nan ± nan (0)	46.93 ± 0.0 (1)	48.64 ± 2.83 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	27.71	27.71	58.96
voltage_datalogger_adc0	trial_1	-	-	36.37	25.98
voltage_datalogger_adc0	trial_2	-	-	32.34	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	13.61	13.61	11.12	12.02
voltage_datalogger_adc2	trial_1	18.43	15.01	14.06	12.07
voltage_datalogger_adc2	trial_2	21.7	10.33	9.92	13.34
voltage_datalogger_adc2	trial_3	13.64	12.99	12.66	15.88
voltage_datalogger_afe	trial_0	-	62.12	52.91	77.93
voltage_datalogger_afe	trial_1	-	-	59.88	78.01
voltage_datalogger_afe	trial_2	-	-	56.55	76.72
voltage_datalogger_afe	trial_3	-	-	52.67	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_3	nan ± nan (0)	27.71 ± 0.0 (1)	32.14 ± 3.54 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717898_3	16.84 ± 3.42 (4)	12.98 ± 1.7 (4)	11.94 ± 1.56 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717898_3	nan ± nan (0)	62.12 ± 0.0 (1)	55.5 ± 2.96 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681852441_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	21.84	30.87
voltage_datalogger_adc0	trial_1	-	23.41	23.41	25.52
voltage_datalogger_adc0	trial_2	27.41	27.41	27.41	36.03
voltage_datalogger_adc0	trial_3	-	31.68	31.68	28.57
voltage_datalogger_adc2	trial_0	20.11	11.5	10.71	12.81
voltage_datalogger_adc2	trial_1	12.15	11.72	10.96	12.18
voltage_datalogger_adc2	trial_2	11.94	11.34	10.57	13.9
voltage_datalogger_adc2	trial_3	13.48	11.9	11.29	12.85
voltage_datalogger_afe	trial_0	-	-	41.96	49.34
voltage_datalogger_afe	trial_1	-	-	43.45	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	45.13	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_0	27.41 ± 0.0 (1)	27.5 ± 3.38 (3)	26.08 ± 3.82 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852441_0	14.42 ± 3.34 (4)	11.62 ± 0.21 (4)	10.88 ± 0.27 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852441_0	nan ± nan (0)	nan ± nan (0)	43.51 ± 1.29 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	29.43	58.96
voltage_datalogger_adc0	trial_1	-	35.18	35.18	25.98
voltage_datalogger_adc0	trial_2	30.84	30.84	30.84	41.48
voltage_datalogger_adc0	trial_3	-	29.58	29.58	29.14
voltage_datalogger_adc2	trial_0	18.06	13.43	13.06	12.02
voltage_datalogger_adc2	trial_1	10.94	10.56	10.09	12.07
voltage_datalogger_adc2	trial_2	13.97	13.29	12.57	13.34
voltage_datalogger_adc2	trial_3	11.57	10.54	10.17	15.88
voltage_datalogger_afe	trial_0	-	-	48.07	77.93
voltage_datalogger_afe	trial_1	-	-	63.01	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	63.13	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_0	30.84 ± 0.0 (1)	31.87 ± 2.4 (3)	31.26 ± 2.33 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852441_0	13.64 ± 2.79 (4)	11.96 ± 1.41 (4)	11.47 ± 1.35 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852441_0	nan ± nan (0)	nan ± nan (0)	58.07 ± 7.07 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681852441_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681852441_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	18.6	30.87
voltage_datalogger_adc0	trial_1	-	-	27.15	25.52
voltage_datalogger_adc0	trial_2	-	-	26.52	36.03
voltage_datalogger_adc0	trial_3	30.18	30.18	30.18	28.57
voltage_datalogger_adc2	trial_0	11.48	10.93	10.5	12.81
voltage_datalogger_adc2	trial_1	28.22	12.27	11.06	12.18
voltage_datalogger_adc2	trial_2	12.02	11.4	10.47	13.9
voltage_datalogger_adc2	trial_3	22.07	12.02	11.01	12.85
voltage_datalogger_afe	trial_0	-	44.1	43.42	49.34
voltage_datalogger_afe	trial_1	-	-	49.29	49.26
voltage_datalogger_afe	trial_2	47.87	47.87	47.87	45.1
voltage_datalogger_afe	trial_3	-	-	47.28	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_1	30.18 ± 0.0 (1)	30.18 ± 0.0 (1)	25.61 ± 4.28 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852441_1	18.45 ± 7.04 (4)	11.66 ± 0.52 (4)	10.76 ± 0.28 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852441_1	47.87 ± 0.0 (1)	45.98 ± 1.88 (2)	46.96 ± 2.17 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	27.33	58.96
voltage_datalogger_adc0	trial_1	-	-	27.45	25.98
voltage_datalogger_adc0	trial_2	-	-	27.11	41.48
voltage_datalogger_adc0	trial_3	34.53	34.53	34.53	29.14
voltage_datalogger_adc2	trial_0	11.1	10.5	10.38	12.02
voltage_datalogger_adc2	trial_1	32.51	10.68	9.87	12.07
voltage_datalogger_adc2	trial_2	10.64	10.54	10.08	13.34
voltage_datalogger_adc2	trial_3	26.41	10.6	9.73	15.88
voltage_datalogger_afe	trial_0	-	48.17	52.22	77.93
voltage_datalogger_afe	trial_1	-	-	74.0	78.01
voltage_datalogger_afe	trial_2	55.2	55.2	55.2	76.72
voltage_datalogger_afe	trial_3	-	-	63.4	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_1	34.53 ± 0.0 (1)	34.53 ± 0.0 (1)	29.1 ± 3.13 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852441_1	20.16 ± 9.54 (4)	10.58 ± 0.07 (4)	10.02 ± 0.24 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852441_1	55.2 ± 0.0 (1)	51.68 ± 3.52 (2)	61.21 ± 8.45 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681852441_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681852441_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	29.0	28.56	30.87
voltage_datalogger_adc0	trial_1	-	-	30.91	25.52
voltage_datalogger_adc0	trial_2	-	22.52	21.97	36.03
voltage_datalogger_adc0	trial_3	-	77.36	71.46	28.57
voltage_datalogger_adc2	trial_0	14.15	12.17	10.93	12.81
voltage_datalogger_adc2	trial_1	15.45	15.33	14.39	12.18
voltage_datalogger_adc2	trial_2	11.11	11.11	10.75	13.9
voltage_datalogger_adc2	trial_3	15.23	14.82	13.83	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	46.55	49.26
voltage_datalogger_afe	trial_2	-	-	47.55	45.1
voltage_datalogger_afe	trial_3	-	-	47.02	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_2	nan ± nan (0)	42.96 ± 24.47 (3)	38.22 ± 19.47 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852441_2	13.98 ± 1.73 (4)	13.36 ± 1.77 (4)	12.48 ± 1.65 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852441_2	nan ± nan (0)	nan ± nan (0)	47.04 ± 0.41 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	34.69	27.65	58.96
voltage_datalogger_adc0	trial_1	-	-	31.29	25.98
voltage_datalogger_adc0	trial_2	-	26.18	44.39	41.48
voltage_datalogger_adc0	trial_3	-	93.4	87.32	29.14
voltage_datalogger_adc2	trial_0	11.24	10.49	9.73	12.02
voltage_datalogger_adc2	trial_1	14.65	14.1	13.55	12.07
voltage_datalogger_adc2	trial_2	10.23	10.23	9.63	13.34
voltage_datalogger_adc2	trial_3	16.57	13.11	20.46	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	55.0	78.01
voltage_datalogger_afe	trial_2	-	-	55.56	76.72
voltage_datalogger_afe	trial_3	-	-	63.67	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_2	nan ± nan (0)	51.42 ± 29.88 (3)	47.66 ± 23.73 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852441_2	13.17 ± 2.56 (4)	11.98 ± 1.66 (4)	13.34 ± 4.4 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852441_2	nan ± nan (0)	nan ± nan (0)	58.08 ± 3.96 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681852441_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681852441_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	33.14	33.14	29.45	30.87
voltage_datalogger_adc0	trial_1	-	-	26.19	25.52
voltage_datalogger_adc0	trial_2	-	26.36	26.0	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	13.2	12.07	11.19	12.81
voltage_datalogger_adc2	trial_1	15.7	14.58	14.17	12.18
voltage_datalogger_adc2	trial_2	12.01	11.56	11.5	13.9
voltage_datalogger_adc2	trial_3	15.55	14.97	14.28	12.85
voltage_datalogger_afe	trial_0	52.57	49.99	46.83	49.34
voltage_datalogger_afe	trial_1	-	48.57	48.57	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_3	33.14 ± 0.0 (1)	29.75 ± 3.39 (2)	27.21 ± 1.58 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852441_3	14.11 ± 1.57 (4)	13.3 ± 1.5 (4)	12.78 ± 1.44 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852441_3	52.57 ± 0.0 (1)	49.28 ± 0.71 (2)	47.7 ± 0.87 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	39.81	39.81	35.47	58.96
voltage_datalogger_adc0	trial_1	-	-	24.73	25.98
voltage_datalogger_adc0	trial_2	-	30.63	29.04	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	11.19	10.46	10.05	12.02
voltage_datalogger_adc2	trial_1	22.2	13.01	12.86	12.07
voltage_datalogger_adc2	trial_2	11.19	10.75	10.49	13.34
voltage_datalogger_adc2	trial_3	21.96	20.34	18.35	15.88
voltage_datalogger_afe	trial_0	58.1	54.2	51.88	77.93
voltage_datalogger_afe	trial_1	-	53.01	53.01	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_3	39.81 ± 0.0 (1)	35.22 ± 4.59 (2)	29.75 ± 4.41 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852441_3	16.63 ± 5.45 (4)	13.64 ± 3.99 (4)	12.94 ± 3.3 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852441_3	58.1 ± 0.0 (1)	53.6 ± 0.6 (2)	52.44 ± 0.56 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681717896_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681717896_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	29.86	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	29.85	29.85	28.57
voltage_datalogger_adc2	trial_0	30.18	11.64	11.17	12.81
voltage_datalogger_adc2	trial_1	15.24	14.61	13.8	12.18
voltage_datalogger_adc2	trial_2	12.35	12.35	12.35	13.9
voltage_datalogger_adc2	trial_3	16.45	14.58	14.27	12.85
voltage_datalogger_afe	trial_0	-	48.27	48.27	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	45.23	45.23	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_0	nan ± nan (0)	29.85 ± 0.0 (1)	29.86 ± 0.0 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717896_0	18.56 ± 6.88 (4)	13.3 ± 1.32 (4)	12.9 ± 1.22 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717896_0	nan ± nan (0)	46.75 ± 1.52 (2)	46.75 ± 1.52 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	37.19	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	30.81	30.81	29.14
voltage_datalogger_adc2	trial_0	22.78	10.13	9.97	12.02
voltage_datalogger_adc2	trial_1	14.35	14.16	12.98	12.07
voltage_datalogger_adc2	trial_2	11.03	11.03	11.03	13.34
voltage_datalogger_adc2	trial_3	23.08	18.22	13.33	15.88
voltage_datalogger_afe	trial_0	-	58.6	58.6	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	50.94	50.94	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_0	nan ± nan (0)	30.81 ± 0.0 (1)	34.0 ± 3.19 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717896_0	17.81 ± 5.25 (4)	13.38 ± 3.17 (4)	11.83 ± 1.38 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717896_0	nan ± nan (0)	54.77 ± 3.83 (2)	54.77 ± 3.83 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681717896_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681717896_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	81.59	81.59	81.59	36.03
voltage_datalogger_adc0	trial_3	81.83	81.83	81.83	28.57
voltage_datalogger_adc2	trial_0	35.08	35.08	35.08	12.81
voltage_datalogger_adc2	trial_1	-	-	28.62	12.18
voltage_datalogger_adc2	trial_2	26.02	26.02	26.02	13.9
voltage_datalogger_adc2	trial_3	24.05	24.05	24.05	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	97.19	97.19	97.19	45.1
voltage_datalogger_afe	trial_3	97.25	97.25	97.25	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_1	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717896_1	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717896_1	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	92.68	92.68	92.68	41.48
voltage_datalogger_adc0	trial_3	96.93	96.93	96.93	29.14
voltage_datalogger_adc2	trial_0	28.52	28.52	28.52	12.02
voltage_datalogger_adc2	trial_1	-	-	34.5	12.07
voltage_datalogger_adc2	trial_2	21.81	21.81	21.81	13.34
voltage_datalogger_adc2	trial_3	30.96	30.96	30.96	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	120.97	120.97	120.97	76.72
voltage_datalogger_afe	trial_3	122.94	122.94	122.94	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_1	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717896_1	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717896_1	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681717896_2

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681717896_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	34.69	30.87
voltage_datalogger_adc0	trial_1	-	-	26.47	25.52
voltage_datalogger_adc0	trial_2	-	-	27.21	36.03
voltage_datalogger_adc0	trial_3	-	27.72	27.59	28.57
voltage_datalogger_adc2	trial_0	28.14	14.79	13.1	12.81
voltage_datalogger_adc2	trial_1	18.06	14.4	14.04	12.18
voltage_datalogger_adc2	trial_2	16.06	13.77	12.23	13.9
voltage_datalogger_adc2	trial_3	15.45	14.66	14.47	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	44.71	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	49.68	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_2	nan ± nan (0)	27.72 ± 0.0 (1)	28.99 ± 3.32 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717896_2	19.43 ± 5.12 (4)	14.4 ± 0.39 (4)	13.46 ± 0.87 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717896_2	nan ± nan (0)	nan ± nan (0)	47.2 ± 2.48 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	32.16	58.96
voltage_datalogger_adc0	trial_1	-	-	26.92	25.98
voltage_datalogger_adc0	trial_2	-	-	29.02	41.48
voltage_datalogger_adc0	trial_3	-	27.54	27.0	29.14
voltage_datalogger_adc2	trial_0	22.17	12.14	12.2	12.02
voltage_datalogger_adc2	trial_1	15.48	13.09	12.63	12.07
voltage_datalogger_adc2	trial_2	16.79	11.28	9.96	13.34
voltage_datalogger_adc2	trial_3	17.75	12.9	12.75	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	46.72	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	54.31	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_2	nan ± nan (0)	27.54 ± 0.0 (1)	28.78 ± 2.13 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717896_2	18.05 ± 2.51 (4)	12.35 ± 0.71 (4)	11.88 ± 1.13 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717896_2	nan ± nan (0)	nan ± nan (0)	50.52 ± 3.8 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681717896_3

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	27.77	30.87
voltage_datalogger_adc0	trial_1	-	-	31.11	25.52
voltage_datalogger_adc0	trial_2	-	-	23.27	36.03
voltage_datalogger_adc0	trial_3	-	68.77	68.77	28.57
voltage_datalogger_adc2	trial_0	12.86	12.35	11.22	12.81
voltage_datalogger_adc2	trial_1	15.37	14.52	14.41	12.18
voltage_datalogger_adc2	trial_2	15.43	14.48	11.4	13.9
voltage_datalogger_adc2	trial_3	14.65	14.65	14.06	12.85
voltage_datalogger_afe	trial_0	-	53.82	46.94	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	47.58	45.1
voltage_datalogger_afe	trial_3	-	-	37.88	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_3	nan ± nan (0)	68.77 ± 0.0 (1)	37.73 ± 18.14 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717896_3	14.58 ± 1.04 (4)	14.0 ± 0.95 (4)	12.77 ± 1.47 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717896_3	nan ± nan (0)	53.82 ± 0.0 (1)	44.13 ± 4.43 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	27.89	58.96
voltage_datalogger_adc0	trial_1	-	-	31.84	25.98
voltage_datalogger_adc0	trial_2	-	-	35.87	41.48
voltage_datalogger_adc0	trial_3	-	86.5	86.5	29.14
voltage_datalogger_adc2	trial_0	11.59	11.43	10.55	12.02
voltage_datalogger_adc2	trial_1	14.84	13.42	13.47	12.07
voltage_datalogger_adc2	trial_2	16.15	12.14	10.32	13.34
voltage_datalogger_adc2	trial_3	15.6	15.6	21.19	15.88
voltage_datalogger_afe	trial_0	-	58.29	54.0	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	59.96	76.72
voltage_datalogger_afe	trial_3	-	-	43.84	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_3	nan ± nan (0)	86.5 ± 0.0 (1)	45.52 ± 23.82 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717896_3	14.54 ± 1.77 (4)	13.15 ± 1.59 (4)	13.88 ± 4.4 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717896_3	nan ± nan (0)	58.29 ± 0.0 (1)	52.6 ± 6.66 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681851168_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681851168_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	31.33	31.33	30.87
voltage_datalogger_adc0	trial_1	-	-	30.58	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	25.17	14.07	12.58	12.81
voltage_datalogger_adc2	trial_1	17.35	14.75	14.64	12.18
voltage_datalogger_adc2	trial_2	14.6	13.66	12.54	13.9
voltage_datalogger_adc2	trial_3	17.02	14.79	14.07	12.85
voltage_datalogger_afe	trial_0	44.29	44.29	44.29	49.34
voltage_datalogger_afe	trial_1	-	-	46.28	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	42.64	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_0	nan ± nan (0)	31.33 ± 0.0 (1)	30.96 ± 0.38 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681851168_0	18.54 ± 3.98 (4)	14.32 ± 0.48 (4)	13.46 ± 0.92 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681851168_0	44.29 ± 0.0 (1)	44.29 ± 0.0 (1)	44.4 ± 1.49 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	30.85	30.85	58.96
voltage_datalogger_adc0	trial_1	-	-	30.99	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	21.49	12.86	11.51	12.02
voltage_datalogger_adc2	trial_1	15.05	13.33	13.31	12.07
voltage_datalogger_adc2	trial_2	15.57	10.65	13.75	13.34
voltage_datalogger_adc2	trial_3	21.44	18.78	17.49	15.88
voltage_datalogger_afe	trial_0	55.33	55.33	55.33	77.93
voltage_datalogger_afe	trial_1	-	-	54.19	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	43.61	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_0	nan ± nan (0)	30.85 ± 0.0 (1)	30.92 ± 0.07 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681851168_0	18.39 ± 3.08 (4)	13.9 ± 2.99 (4)	14.02 ± 2.17 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681851168_0	55.33 ± 0.0 (1)	55.33 ± 0.0 (1)	51.04 ± 5.28 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681851168_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681851168_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	31.25	30.87
voltage_datalogger_adc0	trial_1	-	-	32.45	25.52
voltage_datalogger_adc0	trial_2	-	-	25.05	36.03
voltage_datalogger_adc0	trial_3	-	-	26.29	28.57
voltage_datalogger_adc2	trial_0	14.23	11.47	11.11	12.81
voltage_datalogger_adc2	trial_1	15.95	14.82	14.14	12.18
voltage_datalogger_adc2	trial_2	13.29	11.54	10.85	13.9
voltage_datalogger_adc2	trial_3	14.77	14.77	13.96	12.85
voltage_datalogger_afe	trial_0	49.46	47.11	45.62	49.34
voltage_datalogger_afe	trial_1	-	-	47.78	49.26
voltage_datalogger_afe	trial_2	-	-	43.05	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_1	nan ± nan (0)	nan ± nan (0)	28.76 ± 3.15 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681851168_1	14.56 ± 0.96 (4)	13.15 ± 1.65 (4)	12.52 ± 1.54 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681851168_1	49.46 ± 0.0 (1)	47.11 ± 0.0 (1)	45.48 ± 1.93 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	32.7	58.96
voltage_datalogger_adc0	trial_1	-	-	33.46	25.98
voltage_datalogger_adc0	trial_2	-	-	27.19	41.48
voltage_datalogger_adc0	trial_3	-	-	29.06	29.14
voltage_datalogger_adc2	trial_0	11.72	10.15	9.98	12.02
voltage_datalogger_adc2	trial_1	22.56	20.88	12.73	12.07
voltage_datalogger_adc2	trial_2	10.83	10.52	9.73	13.34
voltage_datalogger_adc2	trial_3	18.82	18.82	12.85	15.88
voltage_datalogger_afe	trial_0	54.31	60.65	49.88	77.93
voltage_datalogger_afe	trial_1	-	-	55.31	78.01
voltage_datalogger_afe	trial_2	-	-	49.79	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_1	nan ± nan (0)	nan ± nan (0)	30.6 ± 2.58 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681851168_1	15.98 ± 4.9 (4)	15.09 ± 4.81 (4)	11.32 ± 1.47 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681851168_1	54.31 ± 0.0 (1)	60.65 ± 0.0 (1)	51.66 ± 2.58 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681851168_2

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681851168_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	29.74	25.52
voltage_datalogger_adc0	trial_2	-	27.42	25.55	36.03
voltage_datalogger_adc0	trial_3	-	-	29.41	28.57
voltage_datalogger_adc2	trial_0	14.4	13.23	12.63	12.81
voltage_datalogger_adc2	trial_1	15.46	14.79	14.25	12.18
voltage_datalogger_adc2	trial_2	18.41	16.88	12.38	13.9
voltage_datalogger_adc2	trial_3	15.44	15.25	14.18	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	44.27	45.1
voltage_datalogger_afe	trial_3	-	-	43.67	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_2	nan ± nan (0)	27.42 ± 0.0 (1)	28.23 ± 1.9 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681851168_2	15.93 ± 1.5 (4)	15.04 ± 1.3 (4)	13.36 ± 0.86 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681851168_2	nan ± nan (0)	nan ± nan (0)	43.97 ± 0.3 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	37.19	25.98
voltage_datalogger_adc0	trial_2	-	38.4	26.55	41.48
voltage_datalogger_adc0	trial_3	-	-	32.58	29.14
voltage_datalogger_adc2	trial_0	11.38	10.39	10.01	12.02
voltage_datalogger_adc2	trial_1	14.9	14.52	13.95	12.07
voltage_datalogger_adc2	trial_2	19.72	18.11	9.86	13.34
voltage_datalogger_adc2	trial_3	14.73	15.06	14.3	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	49.34	76.72
voltage_datalogger_afe	trial_3	-	-	52.32	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_2	nan ± nan (0)	38.4 ± 0.0 (1)	32.11 ± 4.36 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681851168_2	15.18 ± 2.97 (4)	14.52 ± 2.75 (4)	12.03 ± 2.1 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681851168_2	nan ± nan (0)	nan ± nan (0)	50.83 ± 1.49 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681851168_3

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681851168_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	20.65	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	28.22	36.03
voltage_datalogger_adc0	trial_3	-	-	28.65	28.57
voltage_datalogger_adc2	trial_0	16.95	10.85	10.32	12.81
voltage_datalogger_adc2	trial_1	13.73	12.41	11.35	12.18
voltage_datalogger_adc2	trial_2	15.67	11.64	11.28	13.9
voltage_datalogger_adc2	trial_3	12.84	12.84	10.85	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	47.65	47.65	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_3	nan ± nan (0)	nan ± nan (0)	25.84 ± 3.67 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681851168_3	14.8 ± 1.61 (4)	11.93 ± 0.76 (4)	10.95 ± 0.41 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681851168_3	nan ± nan (0)	47.65 ± 0.0 (1)	47.65 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.9	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	32.9	41.48
voltage_datalogger_adc0	trial_3	-	-	28.43	29.14
voltage_datalogger_adc2	trial_0	19.26	10.86	10.14	12.02
voltage_datalogger_adc2	trial_1	12.62	11.57	9.95	12.07
voltage_datalogger_adc2	trial_2	16.66	13.58	13.23	13.34
voltage_datalogger_adc2	trial_3	11.36	11.36	9.71	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	56.83	56.83	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_3	nan ± nan (0)	nan ± nan (0)	30.08 ± 2.01 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681851168_3	14.98 ± 3.15 (4)	11.84 ± 1.04 (4)	10.76 ± 1.44 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681851168_3	nan ± nan (0)	56.83 ± 0.0 (1)	56.83 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681717900_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681717900_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	33.62	29.85	29.71	30.87
voltage_datalogger_adc0	trial_1	35.81	35.81	35.33	25.52
voltage_datalogger_adc0	trial_2	34.39	33.16	32.81	36.03
voltage_datalogger_adc0	trial_3	37.23	37.14	37.1	28.57
voltage_datalogger_adc2	trial_0	15.93	15.93	15.93	12.81
voltage_datalogger_adc2	trial_1	15.71	15.05	15.05	12.18
voltage_datalogger_adc2	trial_2	15.29	15.14	15.14	13.9
voltage_datalogger_adc2	trial_3	15.23	15.02	15.02	12.85
voltage_datalogger_afe	trial_0	-	57.21	56.2	49.34
voltage_datalogger_afe	trial_1	-	49.54	49.54	49.26
voltage_datalogger_afe	trial_2	-	44.99	44.76	45.1
voltage_datalogger_afe	trial_3	-	53.83	53.64	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_0	35.26 ± 1.38 (4)	33.99 ± 2.79 (4)	33.74 ± 2.78 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717900_0	15.54 ± 0.29 (4)	15.28 ± 0.37 (4)	15.28 ± 0.37 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717900_0	nan ± nan (0)	51.39 ± 4.59 (4)	51.04 ± 4.33 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	38.86	38.33	45.13	58.96
voltage_datalogger_adc0	trial_1	35.58	35.58	41.74	25.98
voltage_datalogger_adc0	trial_2	43.32	32.58	32.61	41.48
voltage_datalogger_adc0	trial_3	39.28	40.13	40.15	29.14
voltage_datalogger_adc2	trial_0	12.51	12.51	12.51	12.02
voltage_datalogger_adc2	trial_1	18.78	20.22	20.22	12.07
voltage_datalogger_adc2	trial_2	16.11	17.78	17.78	13.34
voltage_datalogger_adc2	trial_3	14.39	14.19	14.19	15.88
voltage_datalogger_afe	trial_0	-	67.41	68.96	77.93
voltage_datalogger_afe	trial_1	-	58.23	58.23	78.01
voltage_datalogger_afe	trial_2	-	51.95	60.45	76.72
voltage_datalogger_afe	trial_3	-	77.51	76.97	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_0	39.26 ± 2.75 (4)	36.66 ± 2.86 (4)	39.91 ± 4.58 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717900_0	15.45 ± 2.31 (4)	16.18 ± 3.01 (4)	16.18 ± 3.01 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717900_0	nan ± nan (0)	63.77 ± 9.65 (4)	66.15 ± 7.42 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681717900_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681717900_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	38.69	37.92	37.92	30.87
voltage_datalogger_adc0	trial_1	48.15	35.38	32.97	25.52
voltage_datalogger_adc0	trial_2	-	43.64	42.86	36.03
voltage_datalogger_adc0	trial_3	29.32	27.44	27.44	28.57
voltage_datalogger_adc2	trial_0	13.18	13.17	13.17	12.81
voltage_datalogger_adc2	trial_1	15.08	14.82	14.69	12.18
voltage_datalogger_adc2	trial_2	12.75	12.75	12.65	13.9
voltage_datalogger_adc2	trial_3	15.16	14.76	14.76	12.85
voltage_datalogger_afe	trial_0	58.05	52.71	51.2	49.34
voltage_datalogger_afe	trial_1	51.63	50.46	49.36	49.26
voltage_datalogger_afe	trial_2	77.62	73.49	70.66	45.1
voltage_datalogger_afe	trial_3	57.15	56.85	56.85	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_1	38.72 ± 7.69 (3)	36.1 ± 5.82 (4)	35.3 ± 5.73 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717900_1	14.04 ± 1.09 (4)	13.88 ± 0.93 (4)	13.82 ± 0.93 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717900_1	61.11 ± 9.84 (4)	58.38 ± 9.02 (4)	57.02 ± 8.35 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	34.2	33.65	33.65	58.96
voltage_datalogger_adc0	trial_1	51.46	32.83	42.5	25.98
voltage_datalogger_adc0	trial_2	-	52.38	53.48	41.48
voltage_datalogger_adc0	trial_3	32.22	33.26	33.26	29.14
voltage_datalogger_adc2	trial_0	10.82	10.82	10.82	12.02
voltage_datalogger_adc2	trial_1	19.13	17.64	18.55	12.07
voltage_datalogger_adc2	trial_2	10.65	10.65	15.72	13.34
voltage_datalogger_adc2	trial_3	18.78	17.56	17.56	15.88
voltage_datalogger_afe	trial_0	65.34	56.69	56.1	77.93
voltage_datalogger_afe	trial_1	56.32	82.18	60.98	78.01
voltage_datalogger_afe	trial_2	89.59	87.65	87.56	76.72
voltage_datalogger_afe	trial_3	73.37	77.71	77.71	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_1	39.29 ± 8.64 (3)	38.03 ± 8.29 (4)	40.72 ± 8.24 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717900_1	14.84 ± 4.11 (4)	14.17 ± 3.43 (4)	15.66 ± 2.97 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717900_1	71.16 ± 12.23 (4)	76.06 ± 11.72 (4)	70.59 ± 12.66 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681717900_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681717900_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	30.87	30.87	30.87	30.87
voltage_datalogger_adc0	trial_1	-	27.31	26.44	25.52
voltage_datalogger_adc0	trial_2	34.69	34.69	34.69	36.03
voltage_datalogger_adc0	trial_3	34.16	32.83	32.61	28.57
voltage_datalogger_adc2	trial_0	13.5	12.92	12.92	12.81
voltage_datalogger_adc2	trial_1	15.4	14.85	14.49	12.18
voltage_datalogger_adc2	trial_2	14.73	14.18	13.98	13.9
voltage_datalogger_adc2	trial_3	16.79	14.01	14.01	12.85
voltage_datalogger_afe	trial_0	58.51	54.34	53.91	49.34
voltage_datalogger_afe	trial_1	58.48	57.5	55.8	49.26
voltage_datalogger_afe	trial_2	44.51	44.51	42.09	45.1
voltage_datalogger_afe	trial_3	-	51.99	51.93	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_2	33.24 ± 1.69 (3)	31.42 ± 2.73 (4)	31.15 ± 3.04 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717900_2	15.1 ± 1.19 (4)	13.99 ± 0.69 (4)	13.85 ± 0.57 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717900_2	53.83 ± 6.59 (3)	52.08 ± 4.79 (4)	50.93 ± 5.29 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	37.04	37.04	37.04	58.96
voltage_datalogger_adc0	trial_1	-	28.96	27.9	25.98
voltage_datalogger_adc0	trial_2	32.38	32.38	32.48	41.48
voltage_datalogger_adc0	trial_3	48.8	51.72	37.95	29.14
voltage_datalogger_adc2	trial_0	10.96	10.6	10.6	12.02
voltage_datalogger_adc2	trial_1	14.87	17.17	15.85	12.07
voltage_datalogger_adc2	trial_2	15.34	14.75	14.7	13.34
voltage_datalogger_adc2	trial_3	17.96	13.37	13.37	15.88
voltage_datalogger_afe	trial_0	70.98	64.14	64.88	77.93
voltage_datalogger_afe	trial_1	81.8	78.84	64.61	78.01
voltage_datalogger_afe	trial_2	48.88	48.88	46.1	76.72
voltage_datalogger_afe	trial_3	-	71.06	71.19	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_2	39.41 ± 6.91 (3)	37.52 ± 8.68 (4)	33.84 ± 4.01 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717900_2	14.78 ± 2.5 (4)	13.97 ± 2.38 (4)	13.63 ± 1.96 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717900_2	67.22 ± 13.7 (3)	65.73 ± 11.03 (4)	61.7 ± 9.38 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681717900_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681717900_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	31.14	30.25	30.19	30.87
voltage_datalogger_adc0	trial_1	-	47.07	47.03	25.52
voltage_datalogger_adc0	trial_2	38.45	38.45	38.45	36.03
voltage_datalogger_adc0	trial_3	35.56	35.27	35.08	28.57
voltage_datalogger_adc2	trial_0	14.25	13.32	13.07	12.81
voltage_datalogger_adc2	trial_1	15.16	15.15	15.15	12.18
voltage_datalogger_adc2	trial_2	12.77	12.75	12.75	13.9
voltage_datalogger_adc2	trial_3	14.89	13.85	13.85	12.85
voltage_datalogger_afe	trial_0	47.71	47.71	46.64	49.34
voltage_datalogger_afe	trial_1	-	61.35	61.06	49.26
voltage_datalogger_afe	trial_2	-	54.76	52.98	45.1
voltage_datalogger_afe	trial_3	62.73	61.84	61.84	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_3	35.05 ± 3.01 (3)	37.76 ± 6.12 (4)	37.69 ± 6.14 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717900_3	14.27 ± 0.93 (4)	13.77 ± 0.89 (4)	13.7 ± 0.93 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717900_3	55.22 ± 7.51 (2)	56.42 ± 5.75 (4)	55.63 ± 6.24 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	29.72	27.95	28.44	58.96
voltage_datalogger_adc0	trial_1	-	60.59	59.38	25.98
voltage_datalogger_adc0	trial_2	47.65	47.65	47.65	41.48
voltage_datalogger_adc0	trial_3	39.72	39.52	39.24	29.14
voltage_datalogger_adc2	trial_0	16.21	13.42	12.32	12.02
voltage_datalogger_adc2	trial_1	18.33	18.33	18.33	12.07
voltage_datalogger_adc2	trial_2	11.05	11.05	11.05	13.34
voltage_datalogger_adc2	trial_3	18.16	18.29	18.29	15.88
voltage_datalogger_afe	trial_0	48.01	48.01	57.27	77.93
voltage_datalogger_afe	trial_1	-	68.49	79.14	78.01
voltage_datalogger_afe	trial_2	-	63.02	88.4	76.72
voltage_datalogger_afe	trial_3	91.04	88.58	88.58	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_3	39.03 ± 7.34 (3)	43.93 ± 11.9 (4)	43.68 ± 11.34 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717900_3	15.94 ± 2.94 (4)	15.27 ± 3.15 (4)	15.0 ± 3.34 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717900_3	69.53 ± 21.52 (2)	67.03 ± 14.53 (4)	78.35 ± 12.75 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681852463_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681852463_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	39.14	37.21	37.21	30.87
voltage_datalogger_adc0	trial_1	34.99	31.68	31.45	25.52
voltage_datalogger_adc0	trial_2	28.55	28.55	27.74	36.03
voltage_datalogger_adc0	trial_3	42.64	29.53	29.22	28.57
voltage_datalogger_adc2	trial_0	14.06	13.19	12.52	12.81
voltage_datalogger_adc2	trial_1	15.6	14.88	14.88	12.18
voltage_datalogger_adc2	trial_2	13.98	13.41	13.41	13.9
voltage_datalogger_adc2	trial_3	15.05	14.75	14.52	12.85
voltage_datalogger_afe	trial_0	59.39	57.24	57.0	49.34
voltage_datalogger_afe	trial_1	49.6	48.0	45.71	49.26
voltage_datalogger_afe	trial_2	-	50.3	49.58	45.1
voltage_datalogger_afe	trial_3	-	57.38	57.19	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_0	36.33 ± 5.24 (4)	31.74 ± 3.35 (4)	31.4 ± 3.6 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852463_0	14.67 ± 0.68 (4)	14.06 ± 0.76 (4)	13.83 ± 0.93 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852463_0	54.5 ± 4.89 (2)	53.23 ± 4.16 (4)	52.37 ± 4.92 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	36.65	35.39	35.39	58.96
voltage_datalogger_adc0	trial_1	41.57	44.31	43.86	25.98
voltage_datalogger_adc0	trial_2	31.46	31.46	31.3	41.48
voltage_datalogger_adc0	trial_3	53.95	34.01	34.93	29.14
voltage_datalogger_adc2	trial_0	16.09	16.32	15.43	12.02
voltage_datalogger_adc2	trial_1	14.34	13.57	13.78	12.07
voltage_datalogger_adc2	trial_2	13.17	15.68	15.68	13.34
voltage_datalogger_adc2	trial_3	18.92	18.42	16.57	15.88
voltage_datalogger_afe	trial_0	78.04	75.44	76.52	77.93
voltage_datalogger_afe	trial_1	47.83	44.31	42.94	78.01
voltage_datalogger_afe	trial_2	-	52.94	52.98	76.72
voltage_datalogger_afe	trial_3	-	67.46	76.16	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_0	40.91 ± 8.34 (4)	36.29 ± 4.84 (4)	36.37 ± 4.61 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852463_0	15.63 ± 2.17 (4)	16.0 ± 1.73 (4)	15.36 ± 1.01 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852463_0	62.94 ± 15.11 (2)	60.04 ± 12.15 (4)	62.15 ± 14.63 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681852463_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681852463_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	40.03	38.63	30.87
voltage_datalogger_adc0	trial_1	44.83	41.82	41.68	25.52
voltage_datalogger_adc0	trial_2	50.7	41.68	41.68	36.03
voltage_datalogger_adc0	trial_3	48.91	46.44	46.03	28.57
voltage_datalogger_adc2	trial_0	11.97	11.69	11.48	12.81
voltage_datalogger_adc2	trial_1	15.41	14.7	13.93	12.18
voltage_datalogger_adc2	trial_2	15.25	14.83	14.77	13.9
voltage_datalogger_adc2	trial_3	15.31	14.3	14.05	12.85
voltage_datalogger_afe	trial_0	62.39	58.24	56.69	49.34
voltage_datalogger_afe	trial_1	-	60.5	57.79	49.26
voltage_datalogger_afe	trial_2	-	57.07	54.09	45.1
voltage_datalogger_afe	trial_3	66.89	65.32	63.53	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_1	48.15 ± 2.46 (3)	42.49 ± 2.39 (4)	42.0 ± 2.64 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852463_1	14.49 ± 1.45 (4)	13.88 ± 1.28 (4)	13.56 ± 1.24 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852463_1	64.64 ± 2.25 (2)	60.28 ± 3.16 (4)	58.02 ± 3.45 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	44.45	45.63	58.96
voltage_datalogger_adc0	trial_1	56.9	54.23	45.76	25.98
voltage_datalogger_adc0	trial_2	79.33	58.48	58.48	41.48
voltage_datalogger_adc0	trial_3	57.52	61.33	66.33	29.14
voltage_datalogger_adc2	trial_0	11.12	11.15	11.05	12.02
voltage_datalogger_adc2	trial_1	16.34	13.1	12.95	12.07
voltage_datalogger_adc2	trial_2	15.83	17.85	17.57	13.34
voltage_datalogger_adc2	trial_3	13.64	22.33	22.13	15.88
voltage_datalogger_afe	trial_0	93.68	63.08	67.75	77.93
voltage_datalogger_afe	trial_1	-	74.48	80.34	78.01
voltage_datalogger_afe	trial_2	-	75.99	69.48	76.72
voltage_datalogger_afe	trial_3	81.48	75.29	107.94	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_1	64.58 ± 10.43 (3)	54.62 ± 6.39 (4)	54.05 ± 8.8 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852463_1	14.23 ± 2.06 (4)	16.11 ± 4.34 (4)	15.92 ± 4.3 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852463_1	87.58 ± 6.1 (2)	72.21 ± 5.3 (4)	81.38 ± 16.08 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681852463_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681852463_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	51.18	47.34	47.18	30.87
voltage_datalogger_adc0	trial_1	35.51	34.74	34.74	25.52
voltage_datalogger_adc0	trial_2	-	37.17	36.37	36.03
voltage_datalogger_adc0	trial_3	36.68	35.64	33.72	28.57
voltage_datalogger_adc2	trial_0	13.18	12.71	12.32	12.81
voltage_datalogger_adc2	trial_1	15.24	15.02	14.29	12.18
voltage_datalogger_adc2	trial_2	13.56	11.45	11.42	13.9
voltage_datalogger_adc2	trial_3	14.84	14.8	14.8	12.85
voltage_datalogger_afe	trial_0	53.15	52.84	51.13	49.34
voltage_datalogger_afe	trial_1	51.07	47.37	46.12	49.26
voltage_datalogger_afe	trial_2	56.41	54.71	53.07	45.1
voltage_datalogger_afe	trial_3	66.51	63.03	63.03	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_2	41.12 ± 7.13 (3)	38.72 ± 5.05 (4)	38.0 ± 5.38 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852463_2	14.21 ± 0.86 (4)	13.5 ± 1.49 (4)	13.21 ± 1.39 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852463_2	56.78 ± 5.93 (4)	54.49 ± 5.62 (4)	53.34 ± 6.14 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	53.85	48.68	50.69	58.96
voltage_datalogger_adc0	trial_1	37.85	37.54	37.54	25.98
voltage_datalogger_adc0	trial_2	-	35.5	34.75	41.48
voltage_datalogger_adc0	trial_3	36.77	42.62	36.12	29.14
voltage_datalogger_adc2	trial_0	10.51	10.06	9.92	12.02
voltage_datalogger_adc2	trial_1	17.88	17.62	14.4	12.07
voltage_datalogger_adc2	trial_2	15.96	10.59	10.59	13.34
voltage_datalogger_adc2	trial_3	17.94	17.94	17.94	15.88
voltage_datalogger_afe	trial_0	58.38	57.64	49.42	77.93
voltage_datalogger_afe	trial_1	50.72	49.81	52.32	78.01
voltage_datalogger_afe	trial_2	74.69	60.44	67.91	76.72
voltage_datalogger_afe	trial_3	76.35	72.04	72.04	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_2	42.82 ± 7.81 (3)	41.08 ± 5.09 (4)	39.78 ± 6.38 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852463_2	15.57 ± 3.03 (4)	14.05 ± 3.73 (4)	13.21 ± 3.22 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852463_2	65.04 ± 10.85 (4)	59.98 ± 7.98 (4)	60.42 ± 9.72 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681852463_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681852463_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	55.69	55.05	55.05	30.87
voltage_datalogger_adc0	trial_1	43.08	42.04	42.04	25.52
voltage_datalogger_adc0	trial_2	47.91	42.89	41.09	36.03
voltage_datalogger_adc0	trial_3	53.62	49.44	49.24	28.57
voltage_datalogger_adc2	trial_0	14.29	13.84	13.84	12.81
voltage_datalogger_adc2	trial_1	15.17	14.97	14.76	12.18
voltage_datalogger_adc2	trial_2	15.25	13.79	13.3	13.9
voltage_datalogger_adc2	trial_3	15.29	14.92	14.79	12.85
voltage_datalogger_afe	trial_0	60.55	60.55	60.55	49.34
voltage_datalogger_afe	trial_1	51.9	49.47	49.47	49.26
voltage_datalogger_afe	trial_2	62.99	58.45	56.3	45.1
voltage_datalogger_afe	trial_3	63.36	61.37	60.62	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_3	50.08 ± 4.94 (4)	47.36 ± 5.29 (4)	46.86 ± 5.68 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852463_3	15.0 ± 0.41 (4)	14.38 ± 0.57 (4)	14.17 ± 0.63 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852463_3	59.7 ± 4.63 (4)	57.46 ± 4.73 (4)	56.74 ± 4.54 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	76.95	69.98	69.98	58.96
voltage_datalogger_adc0	trial_1	61.44	59.08	59.08	25.98
voltage_datalogger_adc0	trial_2	60.24	47.16	45.87	41.48
voltage_datalogger_adc0	trial_3	68.55	66.37	56.63	29.14
voltage_datalogger_adc2	trial_0	13.65	13.84	13.84	12.02
voltage_datalogger_adc2	trial_1	18.33	18.06	14.75	12.07
voltage_datalogger_adc2	trial_2	14.03	12.91	11.97	13.34
voltage_datalogger_adc2	trial_3	18.37	14.42	15.08	15.88
voltage_datalogger_afe	trial_0	81.12	81.12	81.12	77.93
voltage_datalogger_afe	trial_1	77.09	75.65	75.65	78.01
voltage_datalogger_afe	trial_2	76.67	67.32	64.61	76.72
voltage_datalogger_afe	trial_3	73.12	83.71	80.38	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_3	66.8 ± 6.67 (4)	60.65 ± 8.72 (4)	57.89 ± 8.57 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852463_3	16.1 ± 2.26 (4)	14.81 ± 1.95 (4)	13.91 ± 1.21 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852463_3	77.0 ± 2.83 (4)	76.95 ± 6.28 (4)	75.44 ± 6.6 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681717902_0

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681717902_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	27.83	30.87
voltage_datalogger_adc0	trial_1	-	28.03	26.68	25.52
voltage_datalogger_adc0	trial_2	-	-	28.01	36.03
voltage_datalogger_adc0	trial_3	-	30.08	29.13	28.57
voltage_datalogger_adc2	trial_0	23.13	21.49	11.25	12.81
voltage_datalogger_adc2	trial_1	-	14.74	14.29	12.18
voltage_datalogger_adc2	trial_2	21.18	14.12	12.26	13.9
voltage_datalogger_adc2	trial_3	15.34	14.81	14.2	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_0	nan ± nan (0)	29.06 ± 1.02 (2)	27.91 ± 0.87 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717902_0	19.88 ± 3.31 (3)	16.29 ± 3.01 (4)	13.0 ± 1.3 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717902_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.47	58.96
voltage_datalogger_adc0	trial_1	-	41.69	32.56	25.98
voltage_datalogger_adc0	trial_2	-	-	28.97	41.48
voltage_datalogger_adc0	trial_3	-	30.95	30.77	29.14
voltage_datalogger_adc2	trial_0	17.83	16.52	10.49	12.02
voltage_datalogger_adc2	trial_1	-	18.99	14.01	12.07
voltage_datalogger_adc2	trial_2	17.82	14.91	14.02	13.34
voltage_datalogger_adc2	trial_3	20.73	18.78	12.57	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_0	nan ± nan (0)	36.32 ± 5.37 (2)	30.19 ± 1.61 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717902_0	18.79 ± 1.37 (3)	17.3 ± 1.69 (4)	12.77 ± 1.44 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717902_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681717902_1

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	28.27	27.65	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	24.5	36.03
voltage_datalogger_adc0	trial_3	-	-	28.28	28.57
voltage_datalogger_adc2	trial_0	13.05	12.56	10.81	12.81
voltage_datalogger_adc2	trial_1	-	14.58	13.82	12.18
voltage_datalogger_adc2	trial_2	18.0	14.44	11.23	13.9
voltage_datalogger_adc2	trial_3	15.67	14.04	13.67	12.85
voltage_datalogger_afe	trial_0	43.63	43.63	43.63	49.34
voltage_datalogger_afe	trial_1	-	-	47.68	49.26
voltage_datalogger_afe	trial_2	-	-	46.0	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_1	nan ± nan (0)	28.27 ± 0.0 (1)	26.81 ± 1.65 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717902_1	15.57 ± 2.02 (3)	13.9 ± 0.8 (4)	12.38 ± 1.37 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717902_1	43.63 ± 0.0 (1)	43.63 ± 0.0 (1)	45.77 ± 1.66 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	27.95	27.14	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	38.94	41.48
voltage_datalogger_adc0	trial_3	-	-	42.25	29.14
voltage_datalogger_adc2	trial_0	11.32	10.99	9.77	12.02
voltage_datalogger_adc2	trial_1	-	13.24	12.67	12.07
voltage_datalogger_adc2	trial_2	18.36	14.84	10.46	13.34
voltage_datalogger_adc2	trial_3	14.08	17.79	12.25	15.88
voltage_datalogger_afe	trial_0	56.09	56.09	56.09	77.93
voltage_datalogger_afe	trial_1	-	-	54.16	78.01
voltage_datalogger_afe	trial_2	-	-	54.68	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_1	nan ± nan (0)	27.95 ± 0.0 (1)	36.11 ± 6.49 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717902_1	14.59 ± 2.9 (3)	14.22 ± 2.48 (4)	11.29 ± 1.21 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717902_1	56.09 ± 0.0 (1)	56.09 ± 0.0 (1)	54.98 ± 0.82 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681717902_2

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.25	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	31.21	36.03
voltage_datalogger_adc0	trial_3	-	-	29.63	28.57
voltage_datalogger_adc2	trial_0	25.89	19.84	11.96	12.81
voltage_datalogger_adc2	trial_1	15.18	14.42	13.8	12.18
voltage_datalogger_adc2	trial_2	14.67	13.81	13.06	13.9
voltage_datalogger_adc2	trial_3	15.29	14.79	13.9	12.85
voltage_datalogger_afe	trial_0	-	40.6	40.6	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_2	nan ± nan (0)	nan ± nan (0)	29.7 ± 1.21 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717902_2	17.76 ± 4.7 (4)	15.72 ± 2.41 (4)	13.18 ± 0.78 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717902_2	nan ± nan (0)	40.6 ± 0.0 (1)	40.6 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	35.55	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	40.6	41.48
voltage_datalogger_adc0	trial_3	-	-	39.78	29.14
voltage_datalogger_adc2	trial_0	20.33	15.91	9.38	12.02
voltage_datalogger_adc2	trial_1	13.55	12.91	12.6	12.07
voltage_datalogger_adc2	trial_2	15.27	14.52	13.71	13.34
voltage_datalogger_adc2	trial_3	17.98	17.86	12.66	15.88
voltage_datalogger_afe	trial_0	-	43.88	43.88	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_2	nan ± nan (0)	nan ± nan (0)	38.64 ± 2.21 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717902_2	16.78 ± 2.59 (4)	15.3 ± 1.82 (4)	12.09 ± 1.62 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717902_2	nan ± nan (0)	43.88 ± 0.0 (1)	43.88 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681717902_3

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	25.7	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	28.74	28.57
voltage_datalogger_adc2	trial_0	25.43	12.51	12.51	12.81
voltage_datalogger_adc2	trial_1	15.37	14.98	13.93	12.18
voltage_datalogger_adc2	trial_2	13.76	11.63	11.35	13.9
voltage_datalogger_adc2	trial_3	16.23	15.11	14.49	12.85
voltage_datalogger_afe	trial_0	-	46.1	46.1	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_3	nan ± nan (0)	nan ± nan (0)	27.22 ± 1.52 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717902_3	17.7 ± 4.55 (4)	13.56 ± 1.52 (4)	13.07 ± 1.23 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717902_3	nan ± nan (0)	46.1 ± 0.0 (1)	46.1 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	36.73	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	29.74	29.14
voltage_datalogger_adc2	trial_0	19.47	10.65	10.65	12.02
voltage_datalogger_adc2	trial_1	20.72	14.29	12.64	12.07
voltage_datalogger_adc2	trial_2	11.85	10.73	10.02	13.34
voltage_datalogger_adc2	trial_3	20.32	13.44	12.96	15.88
voltage_datalogger_afe	trial_0	-	64.08	64.08	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_3	nan ± nan (0)	nan ± nan (0)	33.24 ± 3.49 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717902_3	18.09 ± 3.63 (4)	12.28 ± 1.62 (4)	11.57 ± 1.26 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717902_3	nan ± nan (0)	64.08 ± 0.0 (1)	64.08 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681853385_0

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681853385_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	27.84	30.87
voltage_datalogger_adc0	trial_1	-	-	32.41	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	23.76	28.57
voltage_datalogger_adc2	trial_0	17.4	11.27	10.88	12.81
voltage_datalogger_adc2	trial_1	-	14.39	13.65	12.18
voltage_datalogger_adc2	trial_2	17.63	14.45	12.45	13.9
voltage_datalogger_adc2	trial_3	-	14.51	13.79	12.85
voltage_datalogger_afe	trial_0	48.27	48.27	48.27	49.34
voltage_datalogger_afe	trial_1	-	48.1	48.1	49.26
voltage_datalogger_afe	trial_2	-	-	43.72	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_0	nan ± nan (0)	nan ± nan (0)	28.0 ± 3.53 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681853385_0	17.52 ± 0.12 (2)	13.66 ± 1.38 (4)	12.69 ± 1.17 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681853385_0	48.27 ± 0.0 (1)	48.18 ± 0.09 (2)	46.7 ± 2.11 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	30.78	58.96
voltage_datalogger_adc0	trial_1	-	-	35.72	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	23.61	29.14
voltage_datalogger_adc2	trial_0	19.01	9.91	9.67	12.02
voltage_datalogger_adc2	trial_1	-	12.97	12.4	12.07
voltage_datalogger_adc2	trial_2	18.4	14.51	14.3	13.34
voltage_datalogger_adc2	trial_3	-	12.93	12.44	15.88
voltage_datalogger_afe	trial_0	46.91	46.91	46.91	77.93
voltage_datalogger_afe	trial_1	-	51.89	51.89	78.01
voltage_datalogger_afe	trial_2	-	-	49.35	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_0	nan ± nan (0)	nan ± nan (0)	30.04 ± 4.97 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681853385_0	18.7 ± 0.31 (2)	12.58 ± 1.67 (4)	12.2 ± 1.65 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681853385_0	46.91 ± 0.0 (1)	49.4 ± 2.49 (2)	49.38 ± 2.03 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681853385_1

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681853385_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	29.73	30.87
voltage_datalogger_adc0	trial_1	-	-	24.75	25.52
voltage_datalogger_adc0	trial_2	-	-	25.25	36.03
voltage_datalogger_adc0	trial_3	35.16	35.16	31.93	28.57
voltage_datalogger_adc2	trial_0	33.79	12.35	11.51	12.81
voltage_datalogger_adc2	trial_1	15.37	15.17	14.67	12.18
voltage_datalogger_adc2	trial_2	15.66	11.08	11.08	13.9
voltage_datalogger_adc2	trial_3	15.22	14.65	14.21	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	56.63	56.63	53.41	49.26
voltage_datalogger_afe	trial_2	-	-	45.18	45.1
voltage_datalogger_afe	trial_3	-	-	50.08	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_1	35.16 ± 0.0 (1)	35.16 ± 0.0 (1)	27.92 ± 3.02 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681853385_1	20.01 ± 7.96 (4)	13.31 ± 1.67 (4)	12.87 ± 1.59 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681853385_1	56.63 ± 0.0 (1)	56.63 ± 0.0 (1)	49.56 ± 3.38 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	35.49	58.96
voltage_datalogger_adc0	trial_1	-	-	32.79	25.98
voltage_datalogger_adc0	trial_2	-	-	34.96	41.48
voltage_datalogger_adc0	trial_3	36.21	36.21	34.53	29.14
voltage_datalogger_adc2	trial_0	29.05	10.69	9.85	12.02
voltage_datalogger_adc2	trial_1	13.75	13.55	13.17	12.07
voltage_datalogger_adc2	trial_2	16.47	10.69	10.69	13.34
voltage_datalogger_adc2	trial_3	19.03	13.13	12.81	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	63.03	63.03	60.88	78.01
voltage_datalogger_afe	trial_2	-	-	53.95	76.72
voltage_datalogger_afe	trial_3	-	-	66.24	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_1	36.21 ± 0.0 (1)	36.21 ± 0.0 (1)	34.44 ± 1.01 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681853385_1	19.58 ± 5.78 (4)	12.02 ± 1.33 (4)	11.63 ± 1.4 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681853385_1	63.03 ± 0.0 (1)	63.03 ± 0.0 (1)	60.36 ± 5.03 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681853385_2

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681853385_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	27.96	30.87
voltage_datalogger_adc0	trial_1	-	29.25	26.66	25.52
voltage_datalogger_adc0	trial_2	-	-	29.28	36.03
voltage_datalogger_adc0	trial_3	-	-	29.7	28.57
voltage_datalogger_adc2	trial_0	17.51	12.67	11.43	12.81
voltage_datalogger_adc2	trial_1	15.67	14.4	13.79	12.18
voltage_datalogger_adc2	trial_2	19.76	11.69	10.69	13.9
voltage_datalogger_adc2	trial_3	14.69	14.58	13.96	12.85
voltage_datalogger_afe	trial_0	-	-	44.57	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	47.16	46.12	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_2	nan ± nan (0)	29.25 ± 0.0 (1)	28.4 ± 1.19 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681853385_2	16.91 ± 1.93 (4)	13.34 ± 1.21 (4)	12.47 ± 1.43 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681853385_2	nan ± nan (0)	47.16 ± 0.0 (1)	45.34 ± 0.77 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	41.54	58.96
voltage_datalogger_adc0	trial_1	-	43.56	23.99	25.98
voltage_datalogger_adc0	trial_2	-	-	30.41	41.48
voltage_datalogger_adc0	trial_3	-	-	33.54	29.14
voltage_datalogger_adc2	trial_0	19.03	10.18	9.45	12.02
voltage_datalogger_adc2	trial_1	18.4	13.45	13.38	12.07
voltage_datalogger_adc2	trial_2	21.75	10.45	9.58	13.34
voltage_datalogger_adc2	trial_3	15.7	12.9	13.11	15.88
voltage_datalogger_afe	trial_0	-	-	66.05	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	66.51	52.51	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_2	nan ± nan (0)	43.56 ± 0.0 (1)	32.37 ± 6.32 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681853385_2	18.72 ± 2.15 (4)	11.74 ± 1.45 (4)	11.38 ± 1.87 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681853385_2	nan ± nan (0)	66.51 ± 0.0 (1)	59.28 ± 6.77 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681853385_3

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_experiments/work/eval_testing_set/1681853385_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	29.57	26.31	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	13.99	13.45	13.0	12.81
voltage_datalogger_adc2	trial_1	15.78	14.67	14.06	12.18
voltage_datalogger_adc2	trial_2	15.22	12.36	11.41	13.9
voltage_datalogger_adc2	trial_3	15.5	14.66	14.34	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	43.43	43.43	49.26
voltage_datalogger_afe	trial_2	-	-	45.84	45.1
voltage_datalogger_afe	trial_3	-	-	48.7	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_3	nan ± nan (0)	29.57 ± 0.0 (1)	26.31 ± 0.0 (1)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681853385_3	15.12 ± 0.68 (4)	13.78 ± 0.96 (4)	13.2 ± 1.15 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681853385_3	nan ± nan (0)	43.43 ± 0.0 (1)	45.99 ± 2.15 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	36.35	38.47	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	14.82	14.46	13.85	12.02
voltage_datalogger_adc2	trial_1	14.77	13.05	13.09	12.07
voltage_datalogger_adc2	trial_2	15.63	10.97	10.13	13.34
voltage_datalogger_adc2	trial_3	13.91	13.07	19.08	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	51.39	51.39	78.01
voltage_datalogger_afe	trial_2	-	-	54.67	76.72
voltage_datalogger_afe	trial_3	-	-	81.57	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_3	nan ± nan (0)	36.35 ± 0.0 (1)	38.47 ± 0.0 (1)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681853385_3	14.78 ± 0.61 (4)	12.89 ± 1.25 (4)	14.04 ± 3.23 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681853385_3	nan ± nan (0)	51.39 ± 0.0 (1)	62.54 ± 13.52 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed