Experiment Report

Start of automated test report 2023-04-30 00:11:02
Author=UNKNOWN@workstation obo Luke Vassallo

Machine Information

sysname=Linux
nodename=workstation
release=5.19.0-40-generic
version=#41~22.04.1-Ubuntu SMP PREEMPT_DYNAMIC Fri Mar 31 16:00:14 UTC 2
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz
CPU cores : 8
CPU base clock : 3.8000 GHz
CPU boost clock : 3.7920 GHz
System Memory : 31.35GB
Nvidia driver version : 525.105.17
Device 0 : NVIDIA GeForce GTX 1080
Device 0 : 8.0GB

Library Information

python : 3.8.16
torch : 1.13.1+cu117
optuna : 3.1.0
numpy : 1.23.3
pandas : 1.5.3
matplotlib : 3.7.1
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

ablation_experiment_055:1682487597_0

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_0	36.68 ± 0.96 (3)	34.65 ± 1.98 (4)	33.95 ± 2.23 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487597_0	14.68 ± 1.56 (4)	14.07 ± 1.83 (4)	13.87 ± 1.9 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487597_0	56.9 ± 0.52 (2)	59.36 ± 7.05 (4)	57.26 ± 5.92 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_0	45.0 ± 4.58 (3)	41.99 ± 5.93 (4)	40.99 ± 7.39 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487597_0	15.86 ± 4.55 (4)	16.13 ± 4.53 (4)	15.82 ± 4.31 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487597_0	61.78 ± 2.76 (2)	66.78 ± 10.63 (4)	65.54 ± 10.47 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682487597_1

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_1	51.29 ± 21.74 (3)	34.23 ± 3.72 (4)	33.98 ± 3.84 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487597_1	14.75 ± 1.54 (4)	14.65 ± 1.54 (4)	14.37 ± 1.42 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487597_1	58.67 ± 2.66 (3)	57.3 ± 1.67 (4)	57.3 ± 1.67 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_1	61.35 ± 26.62 (3)	37.97 ± 4.9 (4)	40.52 ± 4.34 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487597_1	16.12 ± 3.46 (4)	15.98 ± 3.32 (4)	15.77 ± 3.25 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487597_1	66.86 ± 0.88 (3)	66.17 ± 2.07 (4)	66.17 ± 2.07 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682487597_2

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_2	45.08 ± 3.45 (4)	43.28 ± 2.89 (4)	41.97 ± 2.96 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487597_2	14.66 ± 1.69 (4)	13.73 ± 1.0 (4)	13.58 ± 0.97 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487597_2	54.51 ± 3.8 (3)	51.46 ± 2.1 (4)	49.78 ± 2.35 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_2	54.2 ± 4.38 (4)	50.99 ± 7.06 (4)	57.09 ± 13.63 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487597_2	16.88 ± 6.18 (4)	13.05 ± 2.4 (4)	12.25 ± 1.19 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487597_2	63.02 ± 8.86 (3)	61.36 ± 9.22 (4)	61.54 ± 11.61 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682487597_3

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_3	46.73 ± 6.5 (3)	38.83 ± 4.08 (4)	38.66 ± 4.16 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487597_3	14.99 ± 1.29 (4)	14.9 ± 1.27 (4)	14.85 ± 1.19 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487597_3	60.66 ± 4.35 (4)	55.96 ± 3.3 (4)	54.76 ± 2.78 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_3	62.97 ± 11.08 (3)	51.3 ± 6.21 (4)	48.66 ± 5.35 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487597_3	16.37 ± 3.93 (4)	16.85 ± 3.87 (4)	16.74 ± 3.71 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487597_3	66.94 ± 3.56 (4)	68.7 ± 6.61 (4)	63.11 ± 6.15 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682619637_0

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_0	35.39 ± 2.61 (2)	33.66 ± 1.8 (4)	32.08 ± 2.29 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682619637_0	12.82 ± 0.96 (4)	11.64 ± 0.19 (4)	11.27 ± 0.3 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682619637_0	56.74 ± 2.38 (2)	55.52 ± 1.1 (3)	56.95 ± 8.98 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_0	38.34 ± 2.62 (2)	44.02 ± 7.92 (4)	41.88 ± 6.38 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682619637_0	13.97 ± 2.26 (4)	12.53 ± 1.59 (4)	11.27 ± 1.27 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682619637_0	69.38 ± 4.44 (2)	64.47 ± 8.0 (3)	70.67 ± 20.85 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682619637_1

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_1	41.96 ± 8.4 (3)	34.03 ± 4.93 (4)	33.39 ± 5.25 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682619637_1	14.18 ± 2.08 (4)	13.6 ± 2.35 (4)	13.31 ± 2.2 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682619637_1	49.6 ± 2.37 (2)	46.7 ± 0.53 (2)	47.58 ± 1.62 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_1	49.12 ± 7.64 (3)	42.62 ± 7.34 (4)	42.93 ± 10.28 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682619637_1	14.58 ± 4.44 (4)	13.95 ± 4.85 (4)	13.56 ± 4.6 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682619637_1	62.52 ± 0.95 (2)	58.78 ± 2.8 (2)	56.94 ± 9.59 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682619637_2

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_2	36.17 ± 0.0 (1)	36.74 ± 4.54 (4)	32.33 ± 2.71 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682619637_2	13.99 ± 1.11 (4)	13.81 ± 1.1 (4)	13.74 ± 1.04 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682619637_2	56.16 ± 6.18 (2)	53.98 ± 3.98 (4)	52.21 ± 3.02 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_2	38.12 ± 0.0 (1)	45.8 ± 10.98 (4)	39.5 ± 5.84 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682619637_2	15.57 ± 2.81 (4)	15.02 ± 3.27 (4)	14.73 ± 2.99 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682619637_2	59.56 ± 11.7 (2)	61.78 ± 10.49 (4)	60.32 ± 9.73 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682619637_3

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_3	42.01 ± 2.3 (3)	42.0 ± 4.85 (4)	41.37 ± 4.84 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682619637_3	14.81 ± 1.84 (4)	14.58 ± 1.89 (4)	14.29 ± 1.92 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682619637_3	58.63 ± 5.6 (4)	52.13 ± 2.23 (4)	51.73 ± 2.34 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_3	47.33 ± 5.58 (3)	50.23 ± 10.15 (4)	51.3 ± 11.12 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682619637_3	13.92 ± 1.59 (4)	16.17 ± 3.68 (4)	14.81 ± 3.81 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682619637_3	61.17 ± 6.43 (4)	63.46 ± 8.03 (4)	59.27 ± 7.61 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682487601_0

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_0	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487601_0	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487601_0	97.64 ± 0.38 (2)	97.64 ± 0.38 (2)	97.64 ± 0.38 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_0	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487601_0	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487601_0	126.32 ± 3.39 (2)	126.32 ± 3.39 (2)	126.32 ± 3.39 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682487601_1

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_1	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487601_1	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487601_1	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_1	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487601_1	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487601_1	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682487601_2

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_2	43.2 ± 5.88 (4)	42.23 ± 5.91 (4)	41.76 ± 5.23 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487601_2	15.48 ± 1.1 (4)	15.26 ± 1.01 (4)	15.13 ± 1.03 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487601_2	65.47 ± 3.36 (4)	62.16 ± 2.73 (4)	61.26 ± 2.56 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_2	44.89 ± 5.72 (4)	47.53 ± 10.68 (4)	44.39 ± 5.15 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487601_2	15.55 ± 3.71 (4)	15.38 ± 3.69 (4)	15.91 ± 4.7 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487601_2	86.0 ± 14.9 (4)	75.75 ± 6.67 (4)	74.39 ± 5.62 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682487601_3

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_3	41.74 ± 3.8 (4)	40.3 ± 4.32 (4)	40.03 ± 4.11 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487601_3	15.8 ± 0.91 (4)	15.52 ± 1.11 (4)	15.52 ± 1.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487601_3	68.1 ± 4.55 (4)	66.48 ± 4.31 (4)	65.56 ± 5.06 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_3	49.58 ± 10.19 (4)	51.29 ± 11.06 (4)	51.86 ± 11.33 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487601_3	17.03 ± 3.55 (4)	17.2 ± 3.64 (4)	17.2 ± 3.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487601_3	85.43 ± 7.76 (4)	77.4 ± 8.17 (4)	74.56 ± 10.63 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682622818_0

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_0	47.53 ± 8.83 (4)	46.46 ± 8.47 (4)	46.34 ± 8.41 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622818_0	19.12 ± 1.33 (4)	19.12 ± 1.33 (4)	19.12 ± 1.33 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622818_0	60.72 ± 3.72 (4)	60.5 ± 3.96 (4)	59.98 ± 3.85 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_0	56.42 ± 13.34 (4)	52.13 ± 11.41 (4)	52.74 ± 11.36 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622818_0	21.34 ± 2.41 (4)	21.34 ± 2.41 (4)	21.34 ± 2.41 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622818_0	67.26 ± 8.52 (4)	67.17 ± 8.26 (4)	69.92 ± 9.63 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682622818_1

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_1	47.25 ± 8.51 (4)	39.04 ± 3.66 (4)	38.94 ± 3.64 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622818_1	15.12 ± 1.46 (4)	14.87 ± 1.39 (4)	14.87 ± 1.39 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622818_1	68.04 ± 13.76 (4)	65.03 ± 11.12 (4)	62.7 ± 8.63 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_1	59.14 ± 10.83 (4)	49.87 ± 11.09 (4)	50.16 ± 11.11 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622818_1	17.34 ± 5.3 (4)	17.07 ± 5.28 (4)	17.07 ± 5.28 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622818_1	90.41 ± 15.99 (4)	79.8 ± 5.28 (4)	74.27 ± 12.08 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682622818_2

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_2	52.66 ± 0.35 (3)	48.42 ± 2.5 (4)	48.05 ± 2.7 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622818_2	15.94 ± 2.47 (4)	15.74 ± 2.39 (4)	15.64 ± 2.3 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622818_2	61.8 ± 8.06 (3)	58.28 ± 9.63 (4)	57.51 ± 9.77 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_2	64.39 ± 7.13 (3)	62.86 ± 8.89 (4)	61.79 ± 7.82 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622818_2	17.44 ± 4.05 (4)	17.6 ± 4.31 (4)	17.39 ± 4.02 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622818_2	72.12 ± 3.6 (3)	66.43 ± 16.52 (4)	64.55 ± 15.4 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682622818_3

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_3	49.04 ± 8.22 (4)	47.54 ± 7.41 (4)	47.43 ± 7.22 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622818_3	15.48 ± 1.55 (4)	15.47 ± 1.55 (4)	15.47 ± 1.55 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622818_3	61.15 ± 4.13 (4)	57.5 ± 3.66 (4)	57.26 ± 3.42 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_3	59.59 ± 9.44 (4)	60.5 ± 10.04 (4)	60.32 ± 9.86 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622818_3	16.29 ± 3.5 (4)	16.29 ± 3.5 (4)	16.29 ± 3.5 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622818_3	73.79 ± 3.53 (4)	73.59 ± 4.79 (4)	73.41 ± 4.63 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682487599_0

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_0	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487599_0	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487599_0	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_0	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487599_0	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487599_0	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682487599_1

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_1	29.79 ± 0.0 (1)	32.3 ± 2.79 (3)	30.9 ± 2.42 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487599_1	14.9 ± 2.03 (4)	13.93 ± 1.72 (4)	13.59 ± 1.68 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487599_1	nan ± nan (0)	44.28 ± 0.16 (2)	44.28 ± 0.16 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_1	28.98 ± 0.0 (1)	41.82 ± 8.55 (3)	38.45 ± 8.52 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487599_1	15.52 ± 4.05 (4)	15.8 ± 4.59 (4)	15.07 ± 4.13 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487599_1	nan ± nan (0)	45.96 ± 1.07 (2)	45.96 ± 1.07 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682487599_2

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_2	31.78 ± 0.0 (1)	32.18 ± 0.53 (3)	29.75 ± 1.83 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487599_2	13.84 ± 1.6 (4)	13.27 ± 1.4 (4)	12.57 ± 1.26 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487599_2	47.0 ± 0.92 (2)	47.0 ± 0.92 (2)	45.0 ± 2.19 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_2	36.56 ± 0.0 (1)	34.53 ± 1.44 (3)	31.97 ± 3.6 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487599_2	14.02 ± 2.88 (4)	13.15 ± 2.79 (4)	11.15 ± 1.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487599_2	50.82 ± 2.19 (2)	50.82 ± 2.19 (2)	50.82 ± 2.74 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682487599_3

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_3	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487599_3	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487599_3	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_3	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487599_3	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487599_3	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682622426_0

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_0	24.22 ± 0.0 (1)	28.62 ± 4.46 (2)	27.05 ± 3.35 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622426_0	15.85 ± 0.87 (4)	13.29 ± 1.52 (4)	12.6 ± 1.56 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622426_0	nan ± nan (0)	50.1 ± 0.68 (2)	49.78 ± 0.61 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_0	26.56 ± 0.0 (1)	28.71 ± 2.25 (2)	29.94 ± 2.51 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622426_0	19.11 ± 1.87 (4)	15.15 ± 4.73 (4)	13.85 ± 3.85 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622426_0	nan ± nan (0)	50.77 ± 1.61 (2)	57.19 ± 8.9 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682622426_1

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_1	nan ± nan (0)	38.03 ± 5.39 (3)	35.03 ± 6.37 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622426_1	15.01 ± 2.09 (4)	14.63 ± 1.9 (4)	14.39 ± 1.68 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622426_1	64.96 ± 4.44 (2)	58.54 ± 2.58 (4)	53.78 ± 1.13 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_1	nan ± nan (0)	39.5 ± 5.65 (3)	37.19 ± 6.33 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622426_1	16.24 ± 4.35 (4)	16.94 ± 4.13 (4)	15.74 ± 4.13 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622426_1	76.59 ± 3.23 (2)	67.69 ± 8.91 (4)	65.74 ± 8.61 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682622426_2

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_2	33.28 ± 0.0 (1)	32.39 ± 2.48 (3)	29.74 ± 3.34 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622426_2	17.13 ± 1.0 (4)	14.04 ± 0.91 (4)	13.18 ± 1.13 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622426_2	47.13 ± 1.2 (2)	47.13 ± 1.2 (2)	48.07 ± 1.65 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_2	43.35 ± 0.0 (1)	37.58 ± 5.02 (3)	35.12 ± 5.15 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622426_2	16.07 ± 1.58 (4)	13.48 ± 2.45 (4)	12.95 ± 2.07 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622426_2	60.28 ± 2.25 (2)	60.28 ± 2.25 (2)	63.45 ± 4.85 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682622426_3

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_3	nan ± nan (0)	33.35 ± 5.04 (4)	30.54 ± 4.79 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622426_3	15.72 ± 0.57 (4)	14.43 ± 1.05 (4)	13.68 ± 1.05 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622426_3	49.57 ± 0.0 (1)	48.35 ± 2.16 (4)	46.81 ± 1.8 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_3	nan ± nan (0)	39.96 ± 5.29 (4)	39.2 ± 5.88 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622426_3	21.51 ± 1.09 (4)	15.68 ± 1.01 (4)	13.64 ± 2.25 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622426_3	80.86 ± 0.0 (1)	59.03 ± 7.45 (4)	53.28 ± 3.72 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682487603_0

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_0	33.79 ± 0.33 (3)	31.83 ± 2.16 (4)	31.35 ± 2.74 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487603_0	15.31 ± 1.76 (4)	13.76 ± 0.47 (4)	13.41 ± 0.65 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487603_0	53.24 ± 2.68 (3)	52.78 ± 2.93 (4)	51.91 ± 2.5 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_0	35.5 ± 1.74 (3)	33.4 ± 1.16 (4)	35.36 ± 1.99 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487603_0	16.94 ± 1.52 (4)	15.5 ± 2.68 (4)	15.11 ± 2.58 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487603_0	64.4 ± 12.43 (3)	63.42 ± 11.15 (4)	65.66 ± 11.61 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682487603_1

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_1	39.16 ± 2.95 (4)	35.8 ± 6.18 (4)	34.6 ± 5.02 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487603_1	17.5 ± 4.84 (4)	14.28 ± 0.86 (4)	13.45 ± 0.5 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487603_1	61.0 ± 0.0 (1)	55.7 ± 4.33 (3)	54.67 ± 4.1 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_1	45.08 ± 8.11 (4)	43.47 ± 9.23 (4)	44.13 ± 9.51 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487603_1	18.9 ± 2.52 (4)	16.86 ± 2.79 (4)	13.4 ± 2.55 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487603_1	70.89 ± 0.0 (1)	57.15 ± 9.83 (3)	63.2 ± 13.3 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682487603_2

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_2	35.77 ± 1.72 (3)	34.61 ± 1.53 (4)	34.24 ± 1.2 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487603_2	14.74 ± 0.64 (3)	14.32 ± 0.57 (3)	14.32 ± 0.57 (3)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487603_2	57.14 ± 1.71 (4)	56.12 ± 1.77 (4)	54.57 ± 1.59 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_2	36.45 ± 4.65 (3)	33.96 ± 1.6 (4)	37.39 ± 7.05 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487603_2	15.35 ± 1.18 (3)	14.93 ± 1.37 (3)	14.93 ± 1.37 (3)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487603_2	67.42 ± 9.64 (4)	67.15 ± 9.66 (4)	56.34 ± 4.41 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682487603_3

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_3	35.34 ± 1.04 (3)	30.2 ± 1.49 (4)	29.77 ± 1.61 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487603_3	14.04 ± 0.84 (4)	13.35 ± 1.13 (4)	13.2 ± 0.98 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487603_3	53.28 ± 0.0 (1)	49.18 ± 0.48 (3)	48.21 ± 1.64 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_3	37.31 ± 3.78 (3)	34.94 ± 2.29 (4)	32.19 ± 3.63 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487603_3	14.58 ± 2.44 (4)	12.78 ± 1.53 (4)	12.79 ± 1.52 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487603_3	78.35 ± 0.0 (1)	52.76 ± 1.17 (3)	54.53 ± 5.72 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682623793_0

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_0	34.06 ± 0.41 (2)	30.33 ± 1.53 (4)	29.54 ± 0.91 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682623793_0	15.12 ± 1.54 (4)	13.25 ± 1.63 (4)	12.79 ± 1.68 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682623793_0	53.9 ± 1.41 (4)	52.75 ± 2.54 (4)	51.68 ± 2.55 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_0	35.02 ± 3.63 (2)	32.6 ± 2.45 (4)	30.56 ± 3.35 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682623793_0	15.46 ± 2.41 (4)	12.46 ± 1.9 (4)	12.14 ± 1.94 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682623793_0	64.95 ± 10.78 (4)	60.92 ± 6.54 (4)	65.12 ± 10.14 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682623793_1

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_1	35.66 ± 0.88 (2)	34.8 ± 1.85 (4)	33.28 ± 1.82 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682623793_1	14.57 ± 1.41 (4)	13.51 ± 1.44 (4)	13.05 ± 1.24 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682623793_1	56.77 ± 4.36 (3)	50.48 ± 2.83 (4)	49.64 ± 2.82 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_1	36.1 ± 3.49 (2)	36.67 ± 5.13 (4)	37.14 ± 8.62 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682623793_1	15.46 ± 2.98 (4)	13.58 ± 3.07 (4)	12.9 ± 2.77 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682623793_1	61.27 ± 3.59 (3)	61.34 ± 1.93 (4)	58.76 ± 1.64 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682623793_2

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_2	34.36 ± 2.36 (3)	30.19 ± 3.72 (4)	28.12 ± 2.51 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682623793_2	14.61 ± 1.0 (4)	14.28 ± 1.22 (4)	14.03 ± 1.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682623793_2	nan ± nan (0)	50.23 ± 3.09 (3)	48.21 ± 2.58 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_2	37.96 ± 5.32 (3)	34.42 ± 1.62 (4)	34.62 ± 5.53 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682623793_2	16.16 ± 2.93 (4)	15.83 ± 3.2 (4)	14.77 ± 3.5 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682623793_2	nan ± nan (0)	53.9 ± 3.12 (3)	56.41 ± 7.39 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682623793_3

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_3	36.19 ± 1.43 (3)	33.25 ± 2.79 (4)	31.38 ± 2.37 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682623793_3	14.38 ± 1.26 (4)	14.16 ± 1.18 (4)	13.7 ± 1.31 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682623793_3	57.16 ± 0.0 (1)	48.35 ± 2.71 (4)	47.18 ± 2.65 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_3	35.01 ± 2.09 (3)	33.63 ± 5.51 (4)	30.81 ± 1.53 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682623793_3	16.35 ± 3.24 (4)	15.04 ± 2.86 (4)	13.53 ± 1.6 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682623793_3	72.9 ± 0.0 (1)	56.24 ± 4.15 (4)	56.73 ± 5.09 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682487605_0

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_0	31.48 ± 0.0 (1)	47.95 ± 24.1 (3)	27.23 ± 1.76 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487605_0	15.61 ± 0.42 (4)	14.08 ± 1.08 (4)	13.34 ± 0.91 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487605_0	52.49 ± 0.0 (1)	52.49 ± 0.0 (1)	48.48 ± 4.01 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_0	37.79 ± 0.0 (1)	55.94 ± 29.85 (3)	29.74 ± 2.69 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487605_0	15.64 ± 1.61 (4)	12.94 ± 1.35 (4)	11.88 ± 1.28 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487605_0	69.28 ± 0.0 (1)	69.28 ± 0.0 (1)	64.31 ± 4.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682487605_1

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_1	35.2 ± 0.0 (1)	45.83 ± 18.95 (3)	30.92 ± 3.69 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487605_1	14.31 ± 1.16 (4)	13.47 ± 1.21 (4)	13.18 ± 1.33 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487605_1	nan ± nan (0)	47.47 ± 1.48 (2)	45.11 ± 2.02 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_1	62.78 ± 0.0 (1)	61.18 ± 22.34 (3)	39.65 ± 13.6 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487605_1	14.51 ± 2.4 (4)	13.02 ± 2.93 (4)	12.75 ± 2.65 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487605_1	nan ± nan (0)	57.77 ± 0.76 (2)	57.9 ± 7.44 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682487605_2

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_2	nan ± nan (0)	26.12 ± 0.0 (1)	30.05 ± 2.81 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487605_2	14.1 ± 0.98 (4)	13.73 ± 0.85 (4)	13.19 ± 0.77 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487605_2	38.16 ± 0.0 (1)	38.16 ± 0.0 (1)	47.17 ± 6.95 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_2	nan ± nan (0)	32.7 ± 0.0 (1)	34.55 ± 1.74 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487605_2	15.1 ± 4.0 (4)	15.53 ± 4.32 (4)	15.02 ± 4.18 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487605_2	42.65 ± 0.0 (1)	42.65 ± 0.0 (1)	50.55 ± 5.72 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682487605_3

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_3	32.65 ± 0.0 (1)	30.26 ± 2.38 (2)	28.85 ± 1.88 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487605_3	15.36 ± 1.83 (4)	13.32 ± 1.32 (4)	12.62 ± 1.31 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487605_3	nan ± nan (0)	nan ± nan (0)	48.6 ± 1.44 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_3	33.79 ± 0.0 (1)	30.64 ± 3.15 (2)	29.26 ± 2.15 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487605_3	15.84 ± 3.29 (4)	13.35 ± 3.72 (4)	11.83 ± 1.47 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487605_3	nan ± nan (0)	nan ± nan (0)	58.95 ± 7.21 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682624196_0

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_0	nan ± nan (0)	nan ± nan (0)	28.63 ± 2.33 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624196_0	15.16 ± 1.1 (4)	14.07 ± 0.65 (4)	13.61 ± 0.25 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624196_0	51.39 ± 0.0 (1)	49.12 ± 2.27 (2)	50.22 ± 3.89 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_0	nan ± nan (0)	nan ± nan (0)	31.05 ± 5.9 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624196_0	17.37 ± 4.51 (4)	16.26 ± 2.59 (4)	13.29 ± 2.07 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624196_0	88.37 ± 0.0 (1)	73.1 ± 15.26 (2)	62.94 ± 14.88 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682624196_1

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_1	nan ± nan (0)	30.74 ± 0.0 (1)	27.54 ± 1.7 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624196_1	16.5 ± 1.4 (4)	14.77 ± 0.82 (4)	13.24 ± 0.85 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624196_1	nan ± nan (0)	51.23 ± 0.0 (1)	46.71 ± 2.36 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_1	nan ± nan (0)	29.26 ± 0.0 (1)	28.62 ± 1.07 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624196_1	16.74 ± 2.55 (4)	15.09 ± 2.23 (4)	12.43 ± 2.99 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624196_1	nan ± nan (0)	58.4 ± 0.0 (1)	57.19 ± 6.58 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682624196_2

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_2	nan ± nan (0)	30.5 ± 0.54 (2)	26.94 ± 3.02 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624196_2	15.19 ± 3.05 (4)	12.56 ± 1.02 (4)	12.2 ± 1.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624196_2	nan ± nan (0)	57.09 ± 0.0 (1)	46.85 ± 6.77 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_2	nan ± nan (0)	29.66 ± 1.54 (2)	29.36 ± 4.32 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624196_2	15.5 ± 1.72 (4)	13.16 ± 1.22 (4)	13.02 ± 1.34 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624196_2	nan ± nan (0)	67.51 ± 0.0 (1)	61.03 ± 13.69 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682624196_3

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_3	nan ± nan (0)	31.61 ± 0.63 (2)	28.28 ± 0.54 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624196_3	16.66 ± 3.04 (3)	13.3 ± 1.1 (4)	12.24 ± 0.37 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624196_3	53.99 ± 0.0 (1)	53.99 ± 0.0 (1)	50.63 ± 2.84 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_3	nan ± nan (0)	34.6 ± 3.22 (2)	32.18 ± 3.54 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624196_3	16.04 ± 0.84 (3)	11.46 ± 0.52 (4)	11.1 ± 0.91 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624196_3	69.98 ± 0.0 (1)	69.98 ± 0.0 (1)	65.72 ± 2.05 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682487607_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_0	80.51 ± 1.32 (2)	80.51 ± 1.32 (2)	80.51 ± 1.32 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487607_0	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487607_0	96.55 ± 0.7 (2)	96.55 ± 0.7 (2)	96.55 ± 0.7 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_0	96.52 ± 0.41 (2)	96.52 ± 0.41 (2)	96.52 ± 0.41 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487607_0	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487607_0	121.58 ± 1.35 (2)	121.58 ± 1.35 (2)	121.58 ± 1.35 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682487607_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_1	42.8 ± 4.59 (4)	40.94 ± 5.96 (4)	40.93 ± 5.96 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487607_1	20.4 ± 5.1 (3)	20.01 ± 4.58 (4)	20.01 ± 4.58 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487607_1	56.78 ± 6.53 (4)	56.08 ± 6.48 (4)	55.32 ± 6.17 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_1	45.99 ± 6.45 (4)	43.57 ± 6.78 (4)	43.29 ± 6.76 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487607_1	21.34 ± 3.43 (3)	21.58 ± 4.51 (4)	21.58 ± 4.51 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487607_1	72.52 ± 8.28 (4)	66.44 ± 4.71 (4)	64.78 ± 7.06 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682487607_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_2	41.72 ± 4.68 (4)	41.04 ± 4.52 (4)	41.04 ± 4.52 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487607_2	15.02 ± 0.45 (4)	14.77 ± 0.58 (4)	14.6 ± 0.39 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487607_2	60.57 ± 6.2 (4)	59.76 ± 6.43 (4)	59.21 ± 6.56 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_2	46.5 ± 6.43 (4)	47.66 ± 6.53 (4)	47.66 ± 6.53 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487607_2	15.02 ± 1.51 (4)	15.55 ± 2.27 (4)	16.22 ± 2.9 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487607_2	78.69 ± 16.43 (4)	74.02 ± 16.75 (4)	71.61 ± 17.18 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682487607_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_3	40.06 ± 6.32 (4)	39.8 ± 6.35 (4)	39.79 ± 6.33 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487607_3	14.05 ± 1.43 (4)	13.57 ± 1.28 (4)	13.47 ± 1.22 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487607_3	61.01 ± 3.12 (4)	59.31 ± 3.72 (4)	58.99 ± 3.91 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_3	43.2 ± 8.87 (4)	46.59 ± 14.03 (4)	46.28 ± 13.51 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487607_3	15.36 ± 3.02 (4)	15.99 ± 4.52 (4)	16.0 ± 4.5 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487607_3	71.51 ± 7.88 (4)	72.97 ± 9.94 (4)	69.3 ± 11.58 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682624534_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_0	40.6 ± 5.34 (4)	39.35 ± 5.46 (4)	39.31 ± 5.51 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624534_0	14.49 ± 1.11 (4)	14.44 ± 1.08 (4)	14.44 ± 1.08 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624534_0	62.1 ± 5.11 (3)	58.64 ± 4.86 (4)	58.54 ± 4.95 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_0	49.94 ± 13.12 (4)	48.5 ± 11.13 (4)	47.76 ± 12.07 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624534_0	13.94 ± 2.2 (4)	13.95 ± 2.39 (4)	13.95 ± 2.39 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624534_0	76.4 ± 3.96 (3)	75.04 ± 10.07 (4)	69.76 ± 6.51 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682624534_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_1	47.1 ± 9.76 (4)	45.68 ± 10.69 (4)	45.55 ± 10.76 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624534_1	15.53 ± 0.55 (4)	14.99 ± 1.07 (4)	14.9 ± 1.14 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624534_1	67.58 ± 6.79 (4)	66.24 ± 6.5 (4)	65.65 ± 6.64 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_1	60.84 ± 17.98 (4)	55.26 ± 16.79 (4)	52.75 ± 17.5 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624534_1	16.52 ± 2.92 (4)	15.86 ± 3.63 (4)	15.87 ± 3.7 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624534_1	84.65 ± 4.17 (4)	79.87 ± 12.07 (4)	78.79 ± 11.55 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682624534_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_2	47.55 ± 11.08 (3)	42.59 ± 11.89 (4)	42.28 ± 12.01 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624534_2	14.77 ± 1.74 (4)	14.41 ± 1.74 (4)	14.18 ± 1.94 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624534_2	61.4 ± 5.84 (4)	54.67 ± 4.56 (4)	54.14 ± 5.14 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_2	55.82 ± 13.77 (3)	50.04 ± 18.25 (4)	49.44 ± 18.43 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624534_2	17.02 ± 4.56 (4)	16.69 ± 5.48 (4)	16.86 ± 5.44 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624534_2	74.16 ± 8.76 (4)	67.89 ± 15.68 (4)	67.17 ± 16.1 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682624534_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_3	45.26 ± 4.33 (4)	44.38 ± 4.75 (4)	44.28 ± 4.78 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624534_3	14.22 ± 1.02 (4)	13.65 ± 0.78 (4)	13.65 ± 0.78 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624534_3	60.0 ± 5.72 (4)	58.53 ± 5.29 (4)	58.2 ± 5.2 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_3	48.3 ± 9.33 (4)	50.98 ± 10.46 (4)	54.27 ± 9.57 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624534_3	16.35 ± 2.9 (4)	15.21 ± 3.2 (4)	15.21 ± 3.2 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624534_3	71.73 ± 11.43 (4)	66.28 ± 7.99 (4)	66.16 ± 8.36 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed