# Experiment Report

Start of automated test report 2023-05-23 17:38:22
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# Machine Information

sysname=Linux
nodename=workstation
release=5.19.0-41-generic
version=#42~22.04.1-Ubuntu SMP PREEMPT_DYNAMIC Tue Apr 18 17:40:00 UTC 2
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz
CPU cores : 8
CPU base clock : 3.8000 GHz
CPU boost clock : 3.7920 GHz
System Memory : 31.35GB
Nvidia driver version : 525.105.17
Device 0 : NVIDIA GeForce GTX 1080
Device 0 : 8.0GB

# Library Information

python : 3.8.16
torch : 1.13.1+cpu
optuna : 3.1.1
numpy : 1.23.3
pandas : 2.0.1
matplotlib : 3.7.1
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

# training_td3_cpu_262:1684830998_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

## Estimated Wirelength (HPWL)

Mean over all trials in run //home/gitlab-runner/builds/TfLwHVT9/2/luke/rl_pcb/tests/06_training_td3_cpu_fast/work/eval_testing_set/1684830998_0

| pcb name | run | 0% overlap (#)[1] | 10% overlap (#)[1] | 20% overlap (#)[1] | simulated annealing |
|---|---|---|---|---|---|
| voltage_datalogger_adc0 | 1684830998_0 | 81.71 ± 0.12 (2) | 81.71 ± 0.12 (2) | 81.71 ± 0.12 (2) | 30.25 ± 3.84 (4) |
| voltage_datalogger_adc2 | 1684830998_0 | 28.38 ± 4.8 (3) | 28.38 ± 4.8 (3) | 28.44 ± 4.16 (4) | 12.94 ± 0.62 (4) |
| voltage_datalogger_afe | 1684830998_0 | 97.22 ± 0.03 (2) | 97.22 ± 0.03 (2) | 97.22 ± 0.03 (2) | 48.58 ± 2.08 (4) |

[1] # indicates the number of layouts over which the mean ± std was computed

## Routed Wirelength

Mean over all trials in run //home/gitlab-runner/builds/TfLwHVT9/2/luke/rl_pcb/tests/06_training_td3_cpu_fast/work/eval_testing_set/1684830998_0

| pcb name | run | 0% overlap (#)[1] | 10% overlap (#)[1] | 20% overlap (#)[1] | simulated annealing |
|---|---|---|---|---|---|
| voltage_datalogger_adc0 | 1684830998_0 | 94.8 ± 2.12 (2) | 94.8 ± 2.12 (2) | 94.8 ± 2.12 (2) | 38.89 ± 12.95 (4) |
| voltage_datalogger_adc2 | 1684830998_0 | 27.1 ± 3.87 (3) | 27.1 ± 3.87 (3) | 28.95 ± 4.64 (4) | 13.33 ± 1.57 (4) |
| voltage_datalogger_afe | 1684830998_0 | 121.96 ± 0.98 (2) | 121.96 ± 0.98 (2) | 121.96 ± 0.98 (2) | 75.3 ± 3.94 (4) |

[1] # indicates the number of layouts over which the mean ± std was computed

# training_td3_cpu_262:1684830998_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

## Estimated Wirelength (HPWL)

Mean over all trials in run //home/gitlab-runner/builds/TfLwHVT9/2/luke/rl_pcb/tests/06_training_td3_cpu_fast/work/eval_testing_set/1684830998_1

| pcb name | run | 0% overlap (#)[1] | 10% overlap (#)[1] | 20% overlap (#)[1] | simulated annealing |
|---|---|---|---|---|---|
| voltage_datalogger_adc0 | 1684830998_1 | 81.71 ± 0.12 (2) | 81.71 ± 0.12 (2) | 81.71 ± 0.12 (2) | 30.25 ± 3.84 (4) |
| voltage_datalogger_adc2 | 1684830998_1 | 28.38 ± 4.8 (3) | 28.38 ± 4.8 (3) | 28.44 ± 4.16 (4) | 12.94 ± 0.62 (4) |
| voltage_datalogger_afe | 1684830998_1 | 97.22 ± 0.03 (2) | 97.22 ± 0.03 (2) | 97.22 ± 0.03 (2) | 48.58 ± 2.08 (4) |

[1] # indicates the number of layouts over which the mean ± std was computed

## Routed Wirelength

Mean over all trials in run //home/gitlab-runner/builds/TfLwHVT9/2/luke/rl_pcb/tests/06_training_td3_cpu_fast/work/eval_testing_set/1684830998_1

| pcb name | run | 0% overlap (#)[1] | 10% overlap (#)[1] | 20% overlap (#)[1] | simulated annealing |
|---|---|---|---|---|---|
| voltage_datalogger_adc0 | 1684830998_1 | 95.0 ± 1.93 (2) | 95.0 ± 1.93 (2) | 95.0 ± 1.93 (2) | 38.89 ± 12.95 (4) |
| voltage_datalogger_adc2 | 1684830998_1 | 27.1 ± 3.87 (3) | 27.1 ± 3.87 (3) | 28.95 ± 4.64 (4) | 13.33 ± 1.57 (4) |
| voltage_datalogger_afe | 1684830998_1 | 121.96 ± 0.98 (2) | 121.96 ± 0.98 (2) | 121.96 ± 0.98 (2) | 75.3 ± 3.94 (4) |

[1] # indicates the number of layouts over which the mean ± std was computed