Experiment Report

Start of automated test report 2023-03-07 07:58:35
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Machine Information

sysname=Linux
nodename=workstation
release=5.4.0-144-generic
version=#161~18.04.1-Ubuntu SMP Fri Feb 10 15:55:22 UTC 2023
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz
CPU cores : 16
CPU base clock : 3.8000 GHz
CPU boost clock : 4.2000 GHz
System Memory : 62.64GB
Nvidia driver version : 470.161.03
Device 0 : NVIDIA GeForce GTX 1080
Device 0 : 7.93GB

Library Information

python : 3.8.13
torch : 1.11.0+cu102
optuna : 3.1.0
numpy : 1.23.3
pandas : 1.5.3
matplotlib : 3.7.0
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

training_sac_cpu_622:1678118995_0

Steps per trial = 200

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/tests/03_training_sac_cpu/work/eval_testing_set/1678118995_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]
voltage_datalogger_adc0	1678118995_0	nan ± nan (0)	nan ± nan (0)	33.18 ± 3.28 (2)
voltage_datalogger_adc2	1678118995_0	16.17 ± 0.0 (1)	14.34 ± 0.63 (2)	12.63 ± 1.11 (2)
voltage_datalogger_afe	1678118995_0	nan ± nan (0)	50.64 ± 0.0 (1)	47.76 ± 2.88 (2)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/tests/03_training_sac_cpu/work/eval_testing_set/1678118995_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]
voltage_datalogger_adc0	1678118995_0	nan ± nan (0)	nan ± nan (0)	34.5 ± 1.75 (2)
voltage_datalogger_adc2	1678118995_0	17.0 ± 0.0 (1)	14.64 ± 1.19 (2)	12.08 ± 1.28 (2)
voltage_datalogger_afe	1678118995_0	nan ± nan (0)	53.27 ± 0.0 (1)	53.18 ± 0.09 (2)

[1] # indicates the number of layouts over which the mean ± std was computed

training_sac_cpu_622:1678118995_1

Steps per trial = 200

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/tests/03_training_sac_cpu/work/eval_testing_set/1678118995_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]
voltage_datalogger_adc0	1678118995_1	nan ± nan (0)	31.38 ± 0.6 (2)	28.44 ± 0.73 (2)
voltage_datalogger_adc2	1678118995_1	19.36 ± 2.11 (2)	14.02 ± 0.55 (2)	12.8 ± 1.43 (2)
voltage_datalogger_afe	1678118995_1	nan ± nan (0)	nan ± nan (0)	45.1 ± 0.0 (1)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/tests/03_training_sac_cpu/work/eval_testing_set/1678118995_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]
voltage_datalogger_adc0	1678118995_1	nan ± nan (0)	31.96 ± 2.54 (2)	28.77 ± 1.81 (2)
voltage_datalogger_adc2	1678118995_1	17.77 ± 0.7 (2)	14.51 ± 1.4 (2)	11.7 ± 1.16 (2)
voltage_datalogger_afe	1678118995_1	nan ± nan (0)	nan ± nan (0)	56.25 ± 0.0 (1)

[1] # indicates the number of layouts over which the mean ± std was computed