

Experiment Report

Start of automated test report 2023-03-08 07:52:15

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Machine Information

sysname=Linux

nodename=workstation

release=5.4.0-144-generic

version=#161~18.04.1-Ubuntu SMP Fri Feb 10 15:55:22 UTC 2023

machine=x86_64

CPU arch : X86_64

CPU bits : 64

CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz

CPU cores : 16

CPU base clock : 3.8000 GHz

CPU boost clock : 4.4644 GHz

System Memory : 62.64GB

Nvidia driver version : 470.161.03

Device 0 : NVIDIA GeForce GTX 1080

Device 0 : 7.93GB

Library Information

python : 3.8.13

torch : 1.11.0+cu102

optuna : 3.1.0

numpy : 1.23.3

pandas : 1.5.3

matplotlib : 3.7.0

seaborn : 0.12.2

pcb library: generation of .pcb files.

Library version : 0.0.12

Library built with : C++14

Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.

Library version : 0.1.16

Library built with : C++14

Library built on : Mar 3 2023 23:10:32

training_td3_cuda_622:1678211692_0

Steps per trial = 200

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1678211692_0

| pcb name | trial | 0% overlap | 10% overlap | 20% overlap |
|-------------------------|---------|------------|-------------|-------------|
| voltage_datalogger_adc0 | trial_0 | - | 27.28 | 27.28 |
| voltage_datalogger_adc0 | trial_1 | - | 26.42 | 26.42 |
| voltage_datalogger_adc2 | trial_0 | 32.96 | 11.76 | 10.75 |
| voltage_datalogger_adc2 | trial_1 | 16.15 | 15.41 | 14.29 |
| voltage_datalogger_afe | trial_0 | - | 49.84 | 46.95 |

Mean over all trials in run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1678211692_0

| pcb name | run | 0% overlap (#) ¹ | 10% overlap (#) ¹ | 20% overlap (#) ¹ |
|-------------------------|--------------|-----------------------------|------------------------------|------------------------------|
| voltage_datalogger_adc0 | 1678211692_0 | nan ± nan (0) | 26.85 ± 0.43 (2) | 26.85 ± 0.43 (2) |
| voltage_datalogger_adc2 | 1678211692_0 | 24.56 ± 8.41 (2) | 13.58 ± 1.83 (2) | 12.52 ± 1.77 (2) |
| voltage_datalogger_afe | 1678211692_0 | nan ± nan (0) | 49.84 ± 0.0 (1) | 46.95 ± 0.0 (1) |

¹ # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1678211692_0

| pcb name | trial | 0% overlap | 10% overlap | 20% overlap |
|-------------------------|---------|------------|-------------|-------------|
| voltage_datalogger_adc0 | trial_0 | - | 25.37 | 25.37 |
| voltage_datalogger_adc0 | trial_1 | - | 33.38 | 33.38 |
| voltage_datalogger_adc2 | trial_0 | 24.84 | 11.05 | 10.15 |
| voltage_datalogger_adc2 | trial_1 | 14.49 | 15.43 | 16.83 |

| | | | | |
|------------------------|---------|---|-------|-------|
| voltage_datalogger_afe | trial_0 | - | 59.56 | 70.33 |
|------------------------|---------|---|-------|-------|

Mean over all trials in run //home/luke/work/rl_pcb/tests/02_training_td3_cu
da/work/eval_testing_set/1678211692_0

| pcb name | run | 0% overlap (#) ¹ | 10% overlap (#) ¹ | 20% overlap (#) ¹ |
|-------------------------|--------------|-----------------------------|------------------------------|------------------------------|
| voltage_datalogger_adc0 | 1678211692_0 | nan ± nan (0) | 29.38 ± 4.01 (2) | 29.38 ± 4.01 (2) |
| voltage_datalogger_adc2 | 1678211692_0 | 19.66 ± 5.18 (2) | 13.24 ± 2.19 (2) | 13.49 ± 3.34 (2) |
| voltage_datalogger_afe | 1678211692_0 | nan ± nan (0) | 59.56 ± 0.0 (1) | 70.33 ± 0.0 (1) |

¹ # indicates the number of layouts over which the mean ± std was computed

training_td3_cuda_622:1678211692_1

Steps per trial = 200

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1678211692_1

| pcb name | trial | 0% overlap | 10% overlap | 20% overlap |
|-------------------------|---------|------------|-------------|-------------|
| voltage_datalogger_adc0 | trial_0 | - | 28.65 | 28.65 |
| voltage_datalogger_adc2 | trial_0 | 13.59 | 12.95 | 12.87 |
| voltage_datalogger_adc2 | trial_1 | 16.81 | 15.57 | 15.48 |
| voltage_datalogger_afe | trial_0 | - | 47.24 | 47.24 |

Mean over all trials in run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1678211692_1

| pcb name | run | 0% overlap (#) ¹ | 10% overlap (#) ¹ | 20% overlap (#) ¹ |
|-------------------------|--------------|-----------------------------|------------------------------|------------------------------|
| voltage_datalogger_adc0 | 1678211692_1 | nan ± nan (0) | 28.65 ± 0.0 (1) | 28.65 ± 0.0 (1) |
| voltage_datalogger_adc2 | 1678211692_1 | 15.2 ± 1.61 (2) | 14.26 ± 1.31 (2) | 14.18 ± 1.31 (2) |
| voltage_datalogger_afe | 1678211692_1 | nan ± nan (0) | 47.24 ± 0.0 (1) | 47.24 ± 0.0 (1) |

¹ # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1678211692_1

| pcb name | trial | 0% overlap | 10% overlap | 20% overlap |
|-------------------------|---------|------------|-------------|-------------|
| voltage_datalogger_adc0 | trial_0 | - | 29.39 | 29.39 |
| voltage_datalogger_adc2 | trial_0 | 11.01 | 10.5 | 10.8 |
| voltage_datalogger_adc2 | trial_1 | 20.14 | 14.19 | 14.09 |
| voltage_datalogger_afe | trial_0 | - | 57.48 | 57.48 |

Mean over all trials in run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1678211692_1

da/work/eval_testing_set/1678211692_1

| pcb name | run | 0% overlap (#) ¹ | 10% overlap (#) ¹ | 20% overlap (#) ¹ |
|-------------------------|--------------|-----------------------------|------------------------------|------------------------------|
| voltage_datalogger_adc0 | 1678211692_1 | nan ± nan (0) | 29.39 ± 0.0 (1) | 29.39 ± 0.0 (1) |
| voltage_datalogger_adc2 | 1678211692_1 | 15.58 ± 4.57 (2) | 12.34 ± 1.84 (2) | 12.44 ± 1.64 (2) |
| voltage_datalogger_afe | 1678211692_1 | nan ± nan (0) | 57.48 ± 0.0 (1) | 57.48 ± 0.0 (1) |

¹ # indicates the number of layouts over which the mean ± std was computed