

Experiment Report

Start of automated test report 2023-03-08 07:52:16

Author=luke@workstation obo Luke Vassallo

Machine Information

sysname=Linux

nodename=workstation

release=5.4.0-144-generic

version=#161~18.04.1-Ubuntu SMP Fri Feb 10 15:55:22 UTC 2023

machine=x86_64

CPU arch : X86_64

CPU bits : 64

CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz

CPU cores : 16

CPU base clock : 3.8000 GHz

CPU boost clock : 4.4561 GHz

System Memory : 62.64GB

Nvidia driver version : 470.161.03

Device 0 : NVIDIA GeForce GTX 1080

Device 0 : 7.93GB

Library Information

python : 3.8.13

torch : 1.11.0+cu102

optuna : 3.1.0

numpy : 1.23.3

pandas : 1.5.3

matplotlib : 3.7.0

seaborn : 0.12.2

pcb library: generation of .pcb files.

Library version : 0.0.12

Library built with : C++14

Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.

Library version : 0.1.16

Library built with : C++14

Library built on : Mar 3 2023 23:10:32

training_sac_cuda_622:1678211720_0

Steps per trial = 200

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1678211720_0

pcb name	trial	0% overlap	10% overlap	20% overlap
voltage_datalogger_adc0	trial_0	-	-	29.43
voltage_datalogger_adc2	trial_0	15.44	11.75	10.91
voltage_datalogger_adc2	trial_1	13.9	13.9	13.9
voltage_datalogger_afe	trial_0	-	-	44.14
voltage_datalogger_afe	trial_1	-	53.15	53.15

Mean over all trials in run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1678211720_0

pcb name	run	0% overlap (#) ¹	10% overlap (#) ¹	20% overlap (#) ¹
voltage_datalogger_adc0	1678211720_0	nan ± nan (0)	nan ± nan (0)	29.43 ± 0.0 (1)
voltage_datalogger_adc2	1678211720_0	14.67 ± 0.77 (2)	12.82 ± 1.08 (2)	12.4 ± 1.5 (2)
voltage_datalogger_afe	1678211720_0	nan ± nan (0)	53.15 ± 0.0 (1)	48.64 ± 4.5 (2)

¹ # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1678211720_0

pcb name	trial	0% overlap	10% overlap	20% overlap
voltage_datalogger_adc0	trial_0	-	-	28.56
voltage_datalogger_adc2	trial_0	12.24	10.41	9.68
voltage_datalogger_adc2	trial_1	14.58	14.58	14.58
voltage_datalogger_afe	trial_0	-	-	48.69

voltage_datalogger_afe	trial_1	-	59.33	59.33
------------------------	---------	---	-------	-------

Mean over all trials in run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1678211720_0

pcb name	run	0% overlap (#) ¹	10% overlap (#) ¹	20% overlap (#) ¹
voltage_datalogger_adc0	1678211720_0	nan ± nan (0)	nan ± nan (0)	28.56 ± 0.0 (1)
voltage_datalogger_adc2	1678211720_0	13.41 ± 1.17 (2)	12.5 ± 2.08 (2)	12.13 ± 2.45 (2)
voltage_datalogger_afe	1678211720_0	nan ± nan (0)	59.33 ± 0.0 (1)	54.01 ± 5.32 (2)

¹ # indicates the number of layouts over which the mean ± std was computed

training_sac_cuda_622:1678211720_1

Steps per trial = 200

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1678211720_1

pcb name	trial	0% overlap	10% overlap	20% overlap
voltage_datalogger_adc0	trial_0	-	-	29.12
voltage_datalogger_adc0	trial_1	-	-	25.79
voltage_datalogger_adc2	trial_0	15.27	12.9	11.35
voltage_datalogger_adc2	trial_1	15.3	14.74	14.27
voltage_datalogger_afe	trial_0	-	-	43.01
voltage_datalogger_afe	trial_1	-	49.21	49.21

Mean over all trials in run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1678211720_1

pcb name	run	0% overlap (#) ¹	10% overlap (#) ¹	20% overlap (#) ¹
voltage_datalogger_adc0	1678211720_1	nan ± nan (0)	nan ± nan (0)	27.46 ± 1.67 (2)
voltage_datalogger_adc2	1678211720_1	15.28 ± 0.02 (2)	13.82 ± 0.92 (2)	12.81 ± 1.46 (2)
voltage_datalogger_afe	1678211720_1	nan ± nan (0)	49.21 ± 0.0 (1)	46.11 ± 3.1 (2)

¹ # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1678211720_1

pcb name	trial	0% overlap	10% overlap	20% overlap
voltage_datalogger_adc0	trial_0	-	-	27.41
voltage_datalogger_adc0	trial_1	-	-	31.19
voltage_datalogger_adc2	trial_0	17.27	11.71	10.57

voltage_datalogger_adc2	trial_1	13.88	13.11	12.75
voltage_datalogger_afe	trial_0	-	-	50.34
voltage_datalogger_afe	trial_1	-	46.46	46.46

Mean over all trials in run //home/luke/work/rl_pcb/tests/04_training_sac_cuda/work/eval_testing_set/1678211720_1

pcb name	run	0% overlap (#) ¹	10% overlap (#) ¹	20% overlap (#) ¹
voltage_datalogger_adc0	1678211720_1	nan ± nan (0)	nan ± nan (0)	29.3 ± 1.89 (2)
voltage_datalogger_adc2	1678211720_1	15.58 ± 1.69 (2)	12.41 ± 0.7 (2)	11.66 ± 1.09 (2)
voltage_datalogger_afe	1678211720_1	nan ± nan (0)	46.46 ± 0.0 (1)	48.4 ± 1.94 (2)

¹ # indicates the number of layouts over which the mean ± std was computed