Experiment Report

Start of automated test report 2023-04-14 13:14:00
Author=UNKNOWN@workstation obo Luke Vassallo

Machine Information

sysname=Linux
nodename=workstation
release=5.19.0-38-generic
version=#39~22.04.1-Ubuntu SMP PREEMPT_DYNAMIC Fri Mar 17 21:16:15 UTC 2
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz
CPU cores : 8
CPU base clock : 3.8000 GHz
CPU boost clock : 3.7920 GHz
System Memory : 31.35GB
Nvidia driver version : 525.105.17
Device 0 : NVIDIA GeForce GTX 1080
Device 0 : 8.0GB

Library Information

python : 3.8.16
torch : 1.13.1+cu117
optuna : 3.1.0
numpy : 1.23.3
pandas : 1.5.3
matplotlib : 3.7.1
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

training_td3_cuda_622:1681372339_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	30.49	26.24	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	30.99	36.03
voltage_datalogger_adc0	trial_3	-	-	28.04	28.57
voltage_datalogger_adc2	trial_0	22.89	22.89	22.89	12.81
voltage_datalogger_adc2	trial_1	16.04	14.9	14.32	12.18
voltage_datalogger_adc2	trial_2	13.54	13.04	12.3	13.9
voltage_datalogger_adc2	trial_3	20.13	15.26	14.49	12.85
voltage_datalogger_afe	trial_0	-	43.57	43.57	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	47.33	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372339_0	nan ± nan (0)	30.49 ± 0.0 (1)	28.42 ± 1.96 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681372339_0	18.15 ± 3.61 (4)	16.52 ± 3.77 (4)	16.0 ± 4.07 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681372339_0	nan ± nan (0)	43.57 ± 0.0 (1)	45.45 ± 1.88 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	38.44	33.67	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	31.42	41.48
voltage_datalogger_adc0	trial_3	-	-	37.87	29.14
voltage_datalogger_adc2	trial_0	18.71	18.71	18.71	12.02
voltage_datalogger_adc2	trial_1	19.34	17.7	16.94	12.07
voltage_datalogger_adc2	trial_2	15.48	14.93	14.44	13.34
voltage_datalogger_adc2	trial_3	20.17	18.84	13.21	15.88
voltage_datalogger_afe	trial_0	-	46.82	46.82	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	63.77	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372339_0	nan ± nan (0)	38.44 ± 0.0 (1)	34.32 ± 2.67 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681372339_0	18.42 ± 1.78 (4)	17.54 ± 1.57 (4)	15.82 ± 2.14 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681372339_0	nan ± nan (0)	46.82 ± 0.0 (1)	55.3 ± 8.48 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

training_td3_cuda_622:1681372339_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	81.59	81.59	81.59	36.03
voltage_datalogger_adc0	trial_3	81.83	81.83	81.83	28.57
voltage_datalogger_adc2	trial_0	35.08	35.08	35.08	12.81
voltage_datalogger_adc2	trial_1	-	-	28.62	12.18
voltage_datalogger_adc2	trial_2	26.02	26.02	26.02	13.9
voltage_datalogger_adc2	trial_3	24.05	24.05	24.05	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	97.19	97.19	97.19	45.1
voltage_datalogger_afe	trial_3	97.25	97.25	97.25	50.63

Mean over all trials in run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372339_1	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681372339_1	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681372339_1	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	92.68	92.68	92.68	41.48
voltage_datalogger_adc0	trial_3	96.93	96.93	96.93	29.14
voltage_datalogger_adc2	trial_0	28.52	28.52	28.52	12.02
voltage_datalogger_adc2	trial_1	-	-	34.5	12.07
voltage_datalogger_adc2	trial_2	21.81	21.81	21.81	13.34
voltage_datalogger_adc2	trial_3	30.96	30.96	30.96	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	120.97	120.97	120.97	76.72
voltage_datalogger_afe	trial_3	122.94	122.94	122.94	68.54

Mean over all trials in run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372339_1	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681372339_1	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681372339_1	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

training_td3_cuda_622:1681372339_2

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	41.96	41.96	32.21	30.87
voltage_datalogger_adc0	trial_1	-	26.45	26.45	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	25.73	28.57
voltage_datalogger_adc2	trial_0	13.09	11.7	11.7	12.81
voltage_datalogger_adc2	trial_1	-	-	27.57	12.18
voltage_datalogger_adc2	trial_2	13.46	11.76	11.53	13.9
voltage_datalogger_adc2	trial_3	15.61	15.07	13.97	12.85
voltage_datalogger_afe	trial_0	-	-	48.03	49.34
voltage_datalogger_afe	trial_1	-	-	45.2	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	51.6	50.63

Mean over all trials in run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372339_2	41.96 ± 0.0 (1)	34.2 ± 7.76 (2)	28.13 ± 2.9 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681372339_2	14.05 ± 1.11 (3)	12.84 ± 1.57 (3)	16.19 ± 6.64 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681372339_2	nan ± nan (0)	nan ± nan (0)	48.28 ± 2.62 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	55.87	55.87	46.25	58.96
voltage_datalogger_adc0	trial_1	-	31.91	31.91	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	33.37	29.14
voltage_datalogger_adc2	trial_0	10.63	10.45	10.45	12.02
voltage_datalogger_adc2	trial_1	-	-	34.48	12.07
voltage_datalogger_adc2	trial_2	11.73	10.85	10.54	13.34
voltage_datalogger_adc2	trial_3	18.76	18.06	15.88	15.88
voltage_datalogger_afe	trial_0	-	-	57.44	77.93
voltage_datalogger_afe	trial_1	-	-	59.29	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	76.76	68.54

Mean over all trials in run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372339_2	55.87 ± 0.0 (1)	43.89 ± 11.98 (2)	37.18 ± 6.44 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681372339_2	13.71 ± 3.6 (3)	13.12 ± 3.5 (3)	17.84 ± 9.86 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681372339_2	nan ± nan (0)	nan ± nan (0)	64.5 ± 8.7 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

training_td3_cuda_622:1681372339_3

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.24	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	36.3	28.57
voltage_datalogger_adc2	trial_0	15.7	14.62	11.96	12.81
voltage_datalogger_adc2	trial_1	17.69	14.9	14.48	12.18
voltage_datalogger_adc2	trial_2	14.25	12.18	11.63	13.9
voltage_datalogger_adc2	trial_3	15.62	15.62	14.52	12.85
voltage_datalogger_afe	trial_0	-	-	44.83	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372339_3	nan ± nan (0)	nan ± nan (0)	32.27 ± 4.03 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681372339_3	15.82 ± 1.23 (4)	14.33 ± 1.29 (4)	13.15 ± 1.36 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681372339_3	nan ± nan (0)	nan ± nan (0)	44.83 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	38.47	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	42.33	29.14
voltage_datalogger_adc2	trial_0	12.89	16.48	11.51	12.02
voltage_datalogger_adc2	trial_1	23.77	21.19	19.23	12.07
voltage_datalogger_adc2	trial_2	11.94	11.63	9.92	13.34
voltage_datalogger_adc2	trial_3	18.83	18.83	18.75	15.88
voltage_datalogger_afe	trial_0	-	-	51.27	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/tests/02_training_td3_cuda/work/eval_testing_set/1681372339_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681372339_3	nan ± nan (0)	nan ± nan (0)	40.4 ± 1.93 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681372339_3	16.86 ± 4.79 (4)	17.03 ± 3.54 (4)	14.85 ± 4.18 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681372339_3	nan ± nan (0)	nan ± nan (0)	51.27 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed