Experiment Report

Start of automated test report 2023-05-03 23:07:29
Author=UNKNOWN@workstation obo Luke Vassallo

Machine Information

sysname=Linux
nodename=workstation
release=5.19.0-40-generic
version=#41~22.04.1-Ubuntu SMP PREEMPT_DYNAMIC Fri Mar 31 16:00:14 UTC 2
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz
CPU cores : 8
CPU base clock : 3.8000 GHz
CPU boost clock : 3.7920 GHz
System Memory : 31.35GB
Nvidia driver version : 525.105.17
Device 0 : NVIDIA GeForce GTX 1080
Device 0 : 8.0GB

Library Information

python : 3.8.16
torch : 1.13.1+cu117
optuna : 3.1.0
numpy : 1.23.3
pandas : 1.5.3
matplotlib : 3.7.1
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

parameter_experiment_262:1682846453_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	76.31	70.56	70.56	30.87
voltage_datalogger_adc0	trial_1	86.7	86.7	86.7	25.52
voltage_datalogger_adc0	trial_2	-	-	82.55	36.03
voltage_datalogger_adc0	trial_3	72.99	72.99	72.99	28.57
voltage_datalogger_adc2	trial_0	21.22	21.22	21.22	12.81
voltage_datalogger_adc2	trial_1	-	-	27.95	12.18
voltage_datalogger_adc2	trial_2	20.85	20.42	20.42	13.9
voltage_datalogger_adc2	trial_3	24.98	24.98	24.98	12.85
voltage_datalogger_afe	trial_0	95.02	79.52	79.52	49.34
voltage_datalogger_afe	trial_1	102.48	102.48	102.48	49.26
voltage_datalogger_afe	trial_2	95.61	95.61	95.61	45.1
voltage_datalogger_afe	trial_3	98.03	98.03	98.03	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_0	78.67 ± 5.84 (3)	76.75 ± 7.11 (3)	78.2 ± 6.65 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846453_0	22.35 ± 1.87 (3)	22.21 ± 1.99 (3)	23.64 ± 3.02 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846453_0	97.78 ± 2.94 (4)	93.91 ± 8.67 (4)	93.91 ± 8.67 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	96.83	74.5	74.5	58.96
voltage_datalogger_adc0	trial_1	104.0	104.0	104.0	25.98
voltage_datalogger_adc0	trial_2	-	-	84.77	41.48
voltage_datalogger_adc0	trial_3	98.84	98.84	98.84	29.14
voltage_datalogger_adc2	trial_0	19.38	19.38	19.38	12.02
voltage_datalogger_adc2	trial_1	-	-	23.78	12.07
voltage_datalogger_adc2	trial_2	17.84	17.78	17.78	13.34
voltage_datalogger_adc2	trial_3	31.98	31.98	31.98	15.88
voltage_datalogger_afe	trial_0	104.85	94.7	94.7	77.93
voltage_datalogger_afe	trial_1	117.85	117.85	117.85	78.01
voltage_datalogger_afe	trial_2	130.93	130.93	130.93	76.72
voltage_datalogger_afe	trial_3	114.46	114.46	114.46	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_0	99.89 ± 3.02 (3)	92.45 ± 12.86 (3)	90.53 ± 11.63 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846453_0	23.07 ± 6.33 (3)	23.05 ± 6.35 (3)	23.23 ± 5.51 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846453_0	117.02 ± 9.34 (4)	114.48 ± 12.97 (4)	114.48 ± 12.97 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682846453_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	31.6	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	26.4	26.4	22.94	36.03
voltage_datalogger_adc0	trial_3	-	-	31.09	28.57
voltage_datalogger_adc2	trial_0	21.18	11.87	11.1	12.81
voltage_datalogger_adc2	trial_1	15.33	15.13	14.22	12.18
voltage_datalogger_adc2	trial_2	18.68	12.15	11.87	13.9
voltage_datalogger_adc2	trial_3	18.0	14.64	13.98	12.85
voltage_datalogger_afe	trial_0	-	-	45.22	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	51.95	51.95	51.95	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_1	26.4 ± 0.0 (1)	26.4 ± 0.0 (1)	28.54 ± 3.97 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846453_1	18.3 ± 2.08 (4)	13.45 ± 1.45 (4)	12.79 ± 1.34 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846453_1	51.95 ± 0.0 (1)	51.95 ± 0.0 (1)	48.58 ± 3.37 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	39.45	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	29.04	29.04	28.52	41.48
voltage_datalogger_adc0	trial_3	-	-	30.42	29.14
voltage_datalogger_adc2	trial_0	16.34	10.98	9.87	12.02
voltage_datalogger_adc2	trial_1	16.23	17.99	13.32	12.07
voltage_datalogger_adc2	trial_2	19.91	11.18	11.04	13.34
voltage_datalogger_adc2	trial_3	18.34	13.42	13.21	15.88
voltage_datalogger_afe	trial_0	-	-	47.23	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	69.97	69.97	69.97	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_1	29.04 ± 0.0 (1)	29.04 ± 0.0 (1)	32.8 ± 4.77 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846453_1	17.71 ± 1.53 (4)	13.39 ± 2.82 (4)	11.86 ± 1.47 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846453_1	69.97 ± 0.0 (1)	69.97 ± 0.0 (1)	58.6 ± 11.37 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682846453_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	28.6	28.6	26.98	30.87
voltage_datalogger_adc0	trial_1	-	25.16	24.99	25.52
voltage_datalogger_adc0	trial_2	-	31.44	29.0	36.03
voltage_datalogger_adc0	trial_3	-	30.65	29.58	28.57
voltage_datalogger_adc2	trial_0	12.18	12.09	11.14	12.81
voltage_datalogger_adc2	trial_1	18.45	14.97	14.34	12.18
voltage_datalogger_adc2	trial_2	17.35	14.7	13.96	13.9
voltage_datalogger_adc2	trial_3	15.4	14.67	14.46	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	52.58	52.58	49.26
voltage_datalogger_afe	trial_2	-	-	52.51	45.1
voltage_datalogger_afe	trial_3	-	-	51.94	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_2	28.6 ± 0.0 (1)	28.96 ± 2.43 (4)	27.64 ± 1.81 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846453_2	15.84 ± 2.38 (4)	14.11 ± 1.17 (4)	13.48 ± 1.36 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846453_2	nan ± nan (0)	52.58 ± 0.0 (1)	52.34 ± 0.29 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	34.02	34.02	27.43	58.96
voltage_datalogger_adc0	trial_1	-	27.06	26.08	25.98
voltage_datalogger_adc0	trial_2	-	33.73	36.02	41.48
voltage_datalogger_adc0	trial_3	-	35.14	31.96	29.14
voltage_datalogger_adc2	trial_0	11.24	11.32	10.19	12.02
voltage_datalogger_adc2	trial_1	16.97	20.46	14.15	12.07
voltage_datalogger_adc2	trial_2	17.79	15.77	11.5	13.34
voltage_datalogger_adc2	trial_3	19.31	17.68	18.59	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	64.34	64.34	78.01
voltage_datalogger_afe	trial_2	-	-	65.32	76.72
voltage_datalogger_afe	trial_3	-	-	73.03	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_2	34.02 ± 0.0 (1)	32.49 ± 3.18 (4)	30.37 ± 3.92 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846453_2	16.33 ± 3.05 (4)	16.31 ± 3.33 (4)	13.61 ± 3.21 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846453_2	nan ± nan (0)	64.34 ± 0.0 (1)	67.56 ± 3.89 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682846453_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	27.68	27.68	27.2	30.87
voltage_datalogger_adc0	trial_1	-	26.73	26.34	25.52
voltage_datalogger_adc0	trial_2	-	-	29.57	36.03
voltage_datalogger_adc0	trial_3	35.14	35.14	32.72	28.57
voltage_datalogger_adc2	trial_0	22.23	16.02	12.41	12.81
voltage_datalogger_adc2	trial_1	-	-	-	12.18
voltage_datalogger_adc2	trial_2	17.74	13.3	12.26	13.9
voltage_datalogger_adc2	trial_3	16.22	14.95	14.59	12.85
voltage_datalogger_afe	trial_0	50.7	50.7	50.7	49.34
voltage_datalogger_afe	trial_1	-	-	48.61	49.26
voltage_datalogger_afe	trial_2	48.12	48.12	48.12	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_3	31.41 ± 3.73 (2)	29.85 ± 3.76 (3)	28.96 ± 2.47 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846453_3	18.73 ± 2.55 (3)	14.76 ± 1.12 (3)	13.09 ± 1.06 (3)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846453_3	49.41 ± 1.29 (2)	49.41 ± 1.29 (2)	49.14 ± 1.12 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	27.68	27.68	29.18	58.96
voltage_datalogger_adc0	trial_1	-	31.63	31.45	25.98
voltage_datalogger_adc0	trial_2	-	-	30.61	41.48
voltage_datalogger_adc0	trial_3	44.42	44.42	42.97	29.14
voltage_datalogger_adc2	trial_0	20.72	12.53	9.76	12.02
voltage_datalogger_adc2	trial_1	-	-	-	12.07
voltage_datalogger_adc2	trial_2	18.49	11.78	14.87	13.34
voltage_datalogger_adc2	trial_3	23.29	20.86	13.51	15.88
voltage_datalogger_afe	trial_0	58.4	58.4	58.4	77.93
voltage_datalogger_afe	trial_1	-	-	61.63	78.01
voltage_datalogger_afe	trial_2	63.99	63.99	63.99	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846453_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846453_3	36.05 ± 8.37 (2)	34.58 ± 7.14 (3)	33.55 ± 5.5 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846453_3	20.83 ± 1.96 (3)	15.06 ± 4.11 (3)	12.71 ± 2.16 (3)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846453_3	61.2 ± 2.8 (2)	61.2 ± 2.8 (2)	61.34 ± 2.29 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682980649_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	32.93	31.59	30.87
voltage_datalogger_adc0	trial_1	-	-	27.77	25.52
voltage_datalogger_adc0	trial_2	34.13	34.13	28.67	36.03
voltage_datalogger_adc0	trial_3	-	-	32.47	28.57
voltage_datalogger_adc2	trial_0	15.42	15.21	14.27	12.81
voltage_datalogger_adc2	trial_1	16.41	14.7	13.8	12.18
voltage_datalogger_adc2	trial_2	15.22	14.46	13.91	13.9
voltage_datalogger_adc2	trial_3	15.67	14.6	13.91	12.85
voltage_datalogger_afe	trial_0	-	51.85	51.25	49.34
voltage_datalogger_afe	trial_1	-	-	50.78	49.26
voltage_datalogger_afe	trial_2	-	-	46.83	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_0	34.13 ± 0.0 (1)	33.53 ± 0.6 (2)	30.12 ± 1.96 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980649_0	15.68 ± 0.45 (4)	14.74 ± 0.28 (4)	13.97 ± 0.18 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980649_0	nan ± nan (0)	51.85 ± 0.0 (1)	49.62 ± 1.98 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	40.23	41.37	58.96
voltage_datalogger_adc0	trial_1	-	-	31.3	25.98
voltage_datalogger_adc0	trial_2	32.46	32.46	29.42	41.48
voltage_datalogger_adc0	trial_3	-	-	33.81	29.14
voltage_datalogger_adc2	trial_0	12.84	12.74	11.98	12.02
voltage_datalogger_adc2	trial_1	14.64	13.17	12.55	12.07
voltage_datalogger_adc2	trial_2	15.09	14.93	14.53	13.34
voltage_datalogger_adc2	trial_3	13.99	12.97	12.43	15.88
voltage_datalogger_afe	trial_0	-	59.83	55.9	77.93
voltage_datalogger_afe	trial_1	-	-	65.99	78.01
voltage_datalogger_afe	trial_2	-	-	59.17	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_0	32.46 ± 0.0 (1)	36.34 ± 3.88 (2)	33.98 ± 4.54 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980649_0	14.14 ± 0.85 (4)	13.45 ± 0.87 (4)	12.87 ± 0.98 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980649_0	nan ± nan (0)	59.83 ± 0.0 (1)	60.35 ± 4.2 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682980649_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	32.27	30.49	30.87
voltage_datalogger_adc0	trial_1	-	-	26.22	25.52
voltage_datalogger_adc0	trial_2	-	-	31.62	36.03
voltage_datalogger_adc0	trial_3	-	-	24.94	28.57
voltage_datalogger_adc2	trial_0	15.7	11.51	11.25	12.81
voltage_datalogger_adc2	trial_1	15.88	14.71	13.96	12.18
voltage_datalogger_adc2	trial_2	14.07	13.46	12.24	13.9
voltage_datalogger_adc2	trial_3	16.27	14.76	14.76	12.85
voltage_datalogger_afe	trial_0	-	47.1	44.39	49.34
voltage_datalogger_afe	trial_1	-	48.1	46.16	49.26
voltage_datalogger_afe	trial_2	-	-	47.56	45.1
voltage_datalogger_afe	trial_3	-	59.38	54.83	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_1	nan ± nan (0)	32.27 ± 0.0 (1)	28.32 ± 2.8 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980649_1	15.48 ± 0.84 (4)	13.61 ± 1.32 (4)	13.05 ± 1.38 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980649_1	nan ± nan (0)	51.53 ± 5.57 (3)	48.24 ± 3.97 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	38.02	29.0	58.96
voltage_datalogger_adc0	trial_1	-	-	27.07	25.98
voltage_datalogger_adc0	trial_2	-	-	35.31	41.48
voltage_datalogger_adc0	trial_3	-	-	26.19	29.14
voltage_datalogger_adc2	trial_0	13.57	10.25	10.07	12.02
voltage_datalogger_adc2	trial_1	14.04	13.91	12.85	12.07
voltage_datalogger_adc2	trial_2	15.07	14.47	14.49	13.34
voltage_datalogger_adc2	trial_3	20.23	18.09	18.09	15.88
voltage_datalogger_afe	trial_0	-	66.41	63.82	77.93
voltage_datalogger_afe	trial_1	-	49.85	48.67	78.01
voltage_datalogger_afe	trial_2	-	-	57.37	76.72
voltage_datalogger_afe	trial_3	-	83.49	77.69	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_1	nan ± nan (0)	38.02 ± 0.0 (1)	29.39 ± 3.56 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980649_1	15.73 ± 2.66 (4)	14.18 ± 2.78 (4)	13.88 ± 2.9 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980649_1	nan ± nan (0)	66.58 ± 13.73 (3)	61.89 ± 10.59 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682980649_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	30.54	30.54	30.87
voltage_datalogger_adc0	trial_1	-	35.79	35.04	25.52
voltage_datalogger_adc0	trial_2	-	26.15	23.38	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	13.43	12.18	11.14	12.81
voltage_datalogger_adc2	trial_1	16.09	14.99	13.93	12.18
voltage_datalogger_adc2	trial_2	21.19	12.48	12.34	13.9
voltage_datalogger_adc2	trial_3	15.4	14.69	14.01	12.85
voltage_datalogger_afe	trial_0	-	-	46.37	49.34
voltage_datalogger_afe	trial_1	-	-	46.79	49.26
voltage_datalogger_afe	trial_2	-	-	42.34	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_2	nan ± nan (0)	30.83 ± 3.94 (3)	29.65 ± 4.8 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980649_2	16.53 ± 2.86 (4)	13.58 ± 1.26 (4)	12.85 ± 1.19 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980649_2	nan ± nan (0)	nan ± nan (0)	45.17 ± 2.01 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	36.04	36.04	58.96
voltage_datalogger_adc0	trial_1	-	39.46	42.94	25.98
voltage_datalogger_adc0	trial_2	-	26.85	25.87	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	11.63	10.62	9.96	12.02
voltage_datalogger_adc2	trial_1	18.65	13.45	12.71	12.07
voltage_datalogger_adc2	trial_2	21.42	11.22	11.41	13.34
voltage_datalogger_adc2	trial_3	13.65	13.0	12.53	15.88
voltage_datalogger_afe	trial_0	-	-	57.86	77.93
voltage_datalogger_afe	trial_1	-	-	50.33	78.01
voltage_datalogger_afe	trial_2	-	-	47.33	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_2	nan ± nan (0)	34.12 ± 5.32 (3)	34.95 ± 7.01 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980649_2	16.34 ± 3.89 (4)	12.07 ± 1.18 (4)	11.65 ± 1.1 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980649_2	nan ± nan (0)	nan ± nan (0)	51.84 ± 4.43 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1682980649_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	29.92	29.88	30.87
voltage_datalogger_adc0	trial_1	-	-	29.61	25.52
voltage_datalogger_adc0	trial_2	-	27.97	27.97	36.03
voltage_datalogger_adc0	trial_3	-	-	28.97	28.57
voltage_datalogger_adc2	trial_0	13.47	11.67	11.22	12.81
voltage_datalogger_adc2	trial_1	12.18	11.74	11.74	12.18
voltage_datalogger_adc2	trial_2	15.59	11.56	11.53	13.9
voltage_datalogger_adc2	trial_3	12.36	11.64	11.61	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	54.58	41.42	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_3	nan ± nan (0)	28.94 ± 0.98 (2)	29.11 ± 0.74 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980649_3	13.4 ± 1.36 (4)	11.65 ± 0.06 (4)	11.52 ± 0.19 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980649_3	nan ± nan (0)	54.58 ± 0.0 (1)	41.42 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	38.28	36.42	58.96
voltage_datalogger_adc0	trial_1	-	-	29.82	25.98
voltage_datalogger_adc0	trial_2	-	30.87	30.87	41.48
voltage_datalogger_adc0	trial_3	-	-	27.69	29.14
voltage_datalogger_adc2	trial_0	15.08	13.48	13.13	12.02
voltage_datalogger_adc2	trial_1	10.67	10.35	9.87	12.07
voltage_datalogger_adc2	trial_2	16.92	13.24	13.14	13.34
voltage_datalogger_adc2	trial_3	11.12	10.09	10.13	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	56.77	47.17	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980649_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980649_3	nan ± nan (0)	34.58 ± 3.7 (2)	31.2 ± 3.22 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980649_3	13.45 ± 2.64 (4)	11.79 ± 1.57 (4)	11.57 ± 1.57 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980649_3	nan ± nan (0)	56.77 ± 0.0 (1)	47.17 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682846451_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.94	30.87
voltage_datalogger_adc0	trial_1	-	25.53	25.32	25.52
voltage_datalogger_adc0	trial_2	41.99	41.99	41.99	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	14.02	11.47	10.65	12.81
voltage_datalogger_adc2	trial_1	17.99	14.8	14.4	12.18
voltage_datalogger_adc2	trial_2	19.75	14.52	11.09	13.9
voltage_datalogger_adc2	trial_3	17.37	15.85	14.44	12.85
voltage_datalogger_afe	trial_0	-	47.02	47.02	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	41.14	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_0	41.99 ± 0.0 (1)	33.76 ± 8.23 (2)	32.08 ± 7.16 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846451_0	17.28 ± 2.08 (4)	14.16 ± 1.63 (4)	12.64 ± 1.78 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846451_0	nan ± nan (0)	47.02 ± 0.0 (1)	44.08 ± 2.94 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	33.19	58.96
voltage_datalogger_adc0	trial_1	-	30.9	29.06	25.98
voltage_datalogger_adc0	trial_2	52.6	52.6	52.6	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	11.58	10.52	9.99	12.02
voltage_datalogger_adc2	trial_1	20.65	12.53	12.51	12.07
voltage_datalogger_adc2	trial_2	20.13	11.6	9.95	13.34
voltage_datalogger_adc2	trial_3	17.62	24.25	21.68	15.88
voltage_datalogger_afe	trial_0	-	49.7	49.7	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	47.72	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_0	52.6 ± 0.0 (1)	41.75 ± 10.85 (2)	38.28 ± 10.26 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846451_0	17.5 ± 3.6 (4)	14.72 ± 5.55 (4)	13.53 ± 4.82 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846451_0	nan ± nan (0)	49.7 ± 0.0 (1)	48.71 ± 0.99 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682846451_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	30.43	29.6	30.87
voltage_datalogger_adc0	trial_1	26.09	26.09	24.47	25.52
voltage_datalogger_adc0	trial_2	-	-	27.57	36.03
voltage_datalogger_adc0	trial_3	-	29.92	27.73	28.57
voltage_datalogger_adc2	trial_0	13.7	12.23	11.27	12.81
voltage_datalogger_adc2	trial_1	15.77	14.43	13.7	12.18
voltage_datalogger_adc2	trial_2	16.17	13.35	13.35	13.9
voltage_datalogger_adc2	trial_3	16.45	14.55	14.16	12.85
voltage_datalogger_afe	trial_0	-	-	42.8	49.34
voltage_datalogger_afe	trial_1	-	47.47	47.47	49.26
voltage_datalogger_afe	trial_2	-	49.83	49.83	45.1
voltage_datalogger_afe	trial_3	-	-	51.53	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_1	26.09 ± 0.0 (1)	28.81 ± 1.94 (3)	27.34 ± 1.84 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846451_1	15.52 ± 1.08 (4)	13.64 ± 0.94 (4)	13.12 ± 1.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846451_1	nan ± nan (0)	48.65 ± 1.18 (2)	47.91 ± 3.28 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	29.41	28.27	58.96
voltage_datalogger_adc0	trial_1	28.25	28.25	26.16	25.98
voltage_datalogger_adc0	trial_2	-	-	38.82	41.48
voltage_datalogger_adc0	trial_3	-	32.97	37.66	29.14
voltage_datalogger_adc2	trial_0	11.36	10.39	9.55	12.02
voltage_datalogger_adc2	trial_1	22.24	13.01	12.39	12.07
voltage_datalogger_adc2	trial_2	17.79	14.65	14.47	13.34
voltage_datalogger_adc2	trial_3	21.37	12.9	12.51	15.88
voltage_datalogger_afe	trial_0	-	-	48.7	77.93
voltage_datalogger_afe	trial_1	-	54.95	54.95	78.01
voltage_datalogger_afe	trial_2	-	63.35	63.35	76.72
voltage_datalogger_afe	trial_3	-	-	69.57	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_1	28.25 ± 0.0 (1)	30.21 ± 2.01 (3)	32.73 ± 5.58 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846451_1	18.19 ± 4.28 (4)	12.74 ± 1.52 (4)	12.23 ± 1.75 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846451_1	nan ± nan (0)	59.15 ± 4.2 (2)	59.14 ± 7.95 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682846451_2

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	29.91	29.06	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	43.06	36.03
voltage_datalogger_adc0	trial_3	-	-	27.35	28.57
voltage_datalogger_adc2	trial_0	16.91	12.23	11.36	12.81
voltage_datalogger_adc2	trial_1	17.31	14.67	14.24	12.18
voltage_datalogger_adc2	trial_2	12.28	12.28	12.19	13.9
voltage_datalogger_adc2	trial_3	15.21	14.84	14.53	12.85
voltage_datalogger_afe	trial_0	-	-	45.73	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_2	nan ± nan (0)	29.91 ± 0.0 (1)	33.16 ± 7.04 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846451_2	15.43 ± 1.98 (4)	13.5 ± 1.25 (4)	13.08 ± 1.34 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846451_2	nan ± nan (0)	nan ± nan (0)	45.73 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	28.55	27.83	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	49.67	41.48
voltage_datalogger_adc0	trial_3	-	-	35.56	29.14
voltage_datalogger_adc2	trial_0	17.61	10.95	10.45	12.02
voltage_datalogger_adc2	trial_1	18.85	13.2	12.8	12.07
voltage_datalogger_adc2	trial_2	10.89	10.89	10.99	13.34
voltage_datalogger_adc2	trial_3	19.36	18.35	17.39	15.88
voltage_datalogger_afe	trial_0	-	-	58.11	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_2	nan ± nan (0)	28.55 ± 0.0 (1)	37.69 ± 9.04 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846451_2	16.68 ± 3.4 (4)	13.35 ± 3.03 (4)	12.91 ± 2.73 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846451_2	nan ± nan (0)	nan ± nan (0)	58.11 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682846451_3

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	28.45	28.45	27.87	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	12.36	11.87	11.01	12.81
voltage_datalogger_adc2	trial_1	17.23	15.05	13.97	12.18
voltage_datalogger_adc2	trial_2	14.81	13.36	13.36	13.9
voltage_datalogger_adc2	trial_3	16.12	15.17	13.59	12.85
voltage_datalogger_afe	trial_0	-	-	44.79	49.34
voltage_datalogger_afe	trial_1	45.67	45.67	45.67	49.26
voltage_datalogger_afe	trial_2	-	-	40.1	45.1
voltage_datalogger_afe	trial_3	-	-	49.95	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_3	28.45 ± 0.0 (1)	28.45 ± 0.0 (1)	27.87 ± 0.0 (1)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846451_3	15.13 ± 1.81 (4)	13.86 ± 1.35 (4)	12.98 ± 1.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846451_3	45.67 ± 0.0 (1)	45.67 ± 0.0 (1)	45.13 ± 3.5 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	31.21	31.21	37.46	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	11.51	10.09	9.69	12.02
voltage_datalogger_adc2	trial_1	19.63	20.32	16.79	12.07
voltage_datalogger_adc2	trial_2	15.98	14.41	14.41	13.34
voltage_datalogger_adc2	trial_3	17.28	20.72	21.31	15.88
voltage_datalogger_afe	trial_0	-	-	44.66	77.93
voltage_datalogger_afe	trial_1	50.58	50.58	50.58	78.01
voltage_datalogger_afe	trial_2	-	-	52.33	76.72
voltage_datalogger_afe	trial_3	-	-	62.62	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846451_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846451_3	31.21 ± 0.0 (1)	31.21 ± 0.0 (1)	37.46 ± 0.0 (1)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846451_3	16.1 ± 2.96 (4)	16.38 ± 4.41 (4)	15.55 ± 4.19 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846451_3	50.58 ± 0.0 (1)	50.58 ± 0.0 (1)	52.55 ± 6.47 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682978327_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.67	30.87
voltage_datalogger_adc0	trial_1	-	-	26.81	25.52
voltage_datalogger_adc0	trial_2	-	26.29	26.29	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	29.77	27.28	10.95	12.81
voltage_datalogger_adc2	trial_1	15.6	15.28	14.64	12.18
voltage_datalogger_adc2	trial_2	17.15	15.61	13.14	13.9
voltage_datalogger_adc2	trial_3	17.69	14.9	14.45	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	46.04	46.04	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_0	nan ± nan (0)	26.29 ± 0.0 (1)	27.26 ± 1.02 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682978327_0	20.05 ± 5.66 (4)	18.27 ± 5.21 (4)	13.3 ± 1.47 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682978327_0	nan ± nan (0)	46.04 ± 0.0 (1)	46.04 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.07	58.96
voltage_datalogger_adc0	trial_1	-	-	24.82	25.98
voltage_datalogger_adc0	trial_2	-	37.25	37.25	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	24.3	22.67	11.09	12.02
voltage_datalogger_adc2	trial_1	17.13	17.02	13.05	12.07
voltage_datalogger_adc2	trial_2	17.79	16.52	10.92	13.34
voltage_datalogger_adc2	trial_3	21.93	14.54	17.37	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	43.9	43.9	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_0	nan ± nan (0)	37.25 ± 0.0 (1)	30.05 ± 5.26 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682978327_0	20.29 ± 2.96 (4)	17.69 ± 3.02 (4)	13.11 ± 2.6 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682978327_0	nan ± nan (0)	43.9 ± 0.0 (1)	43.9 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682978327_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.07	30.87
voltage_datalogger_adc0	trial_1	-	-	26.13	25.52
voltage_datalogger_adc0	trial_2	-	-	26.22	36.03
voltage_datalogger_adc0	trial_3	-	-	77.19	28.57
voltage_datalogger_adc2	trial_0	13.65	13.41	10.89	12.81
voltage_datalogger_adc2	trial_1	15.32	14.47	14.0	12.18
voltage_datalogger_adc2	trial_2	16.08	12.83	11.29	13.9
voltage_datalogger_adc2	trial_3	15.43	14.6	13.89	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	43.3	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_1	nan ± nan (0)	nan ± nan (0)	39.4 ± 21.83 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682978327_1	15.12 ± 0.9 (4)	13.83 ± 0.74 (4)	12.52 ± 1.44 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682978327_1	nan ± nan (0)	nan ± nan (0)	43.3 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	37.42	58.96
voltage_datalogger_adc0	trial_1	-	-	30.45	25.98
voltage_datalogger_adc0	trial_2	-	-	38.37	41.48
voltage_datalogger_adc0	trial_3	-	-	94.16	29.14
voltage_datalogger_adc2	trial_0	12.15	10.63	9.55	12.02
voltage_datalogger_adc2	trial_1	15.86	13.6	13.0	12.07
voltage_datalogger_adc2	trial_2	16.73	11.76	9.85	13.34
voltage_datalogger_adc2	trial_3	13.7	12.98	12.55	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	49.67	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_1	nan ± nan (0)	nan ± nan (0)	50.1 ± 25.62 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682978327_1	14.61 ± 1.8 (4)	12.24 ± 1.14 (4)	11.24 ± 1.55 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682978327_1	nan ± nan (0)	nan ± nan (0)	49.67 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682978327_2

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	27.85	30.87
voltage_datalogger_adc0	trial_1	26.93	26.93	26.42	25.52
voltage_datalogger_adc0	trial_2	-	26.76	24.83	36.03
voltage_datalogger_adc0	trial_3	-	-	73.54	28.57
voltage_datalogger_adc2	trial_0	20.5	12.15	12.09	12.81
voltage_datalogger_adc2	trial_1	-	14.49	13.91	12.18
voltage_datalogger_adc2	trial_2	17.27	12.31	11.47	13.9
voltage_datalogger_adc2	trial_3	15.3	14.49	13.84	12.85
voltage_datalogger_afe	trial_0	46.7	46.7	46.3	49.34
voltage_datalogger_afe	trial_1	-	-	46.69	49.26
voltage_datalogger_afe	trial_2	-	43.39	42.49	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_2	26.93 ± 0.0 (1)	26.84 ± 0.08 (2)	38.16 ± 20.45 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682978327_2	17.69 ± 2.14 (3)	13.36 ± 1.13 (4)	12.83 ± 1.07 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682978327_2	46.7 ± 0.0 (1)	45.04 ± 1.66 (2)	45.16 ± 1.89 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	32.43	58.96
voltage_datalogger_adc0	trial_1	31.81	31.81	32.17	25.98
voltage_datalogger_adc0	trial_2	-	31.04	26.18	41.48
voltage_datalogger_adc0	trial_3	-	-	94.1	29.14
voltage_datalogger_adc2	trial_0	17.62	10.1	10.45	12.02
voltage_datalogger_adc2	trial_1	-	13.13	12.66	12.07
voltage_datalogger_adc2	trial_2	17.89	10.45	10.65	13.34
voltage_datalogger_adc2	trial_3	13.55	12.93	12.55	15.88
voltage_datalogger_afe	trial_0	65.85	65.85	53.81	77.93
voltage_datalogger_afe	trial_1	-	-	61.8	78.01
voltage_datalogger_afe	trial_2	-	50.6	48.48	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_2	31.81 ± 0.0 (1)	31.42 ± 0.38 (2)	46.22 ± 27.76 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682978327_2	16.35 ± 1.99 (3)	11.65 ± 1.38 (4)	11.58 ± 1.03 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682978327_2	65.85 ± 0.0 (1)	58.22 ± 7.62 (2)	54.7 ± 5.47 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1682978327_3

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	32.74	29.44	30.87
voltage_datalogger_adc0	trial_1	-	-	24.07	25.52
voltage_datalogger_adc0	trial_2	-	-	29.59	36.03
voltage_datalogger_adc0	trial_3	-	-	28.11	28.57
voltage_datalogger_adc2	trial_0	12.98	11.92	11.63	12.81
voltage_datalogger_adc2	trial_1	15.32	14.67	14.25	12.18
voltage_datalogger_adc2	trial_2	16.43	11.47	10.76	13.9
voltage_datalogger_adc2	trial_3	19.41	15.94	13.71	12.85
voltage_datalogger_afe	trial_0	48.31	48.31	46.72	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_3	nan ± nan (0)	32.74 ± 0.0 (1)	27.8 ± 2.23 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682978327_3	16.04 ± 2.31 (4)	13.5 ± 1.87 (4)	12.59 ± 1.44 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682978327_3	48.31 ± 0.0 (1)	48.31 ± 0.0 (1)	46.72 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	30.93	26.79	58.96
voltage_datalogger_adc0	trial_1	-	-	26.72	25.98
voltage_datalogger_adc0	trial_2	-	-	35.66	41.48
voltage_datalogger_adc0	trial_3	-	-	35.84	29.14
voltage_datalogger_adc2	trial_0	11.66	10.66	10.37	12.02
voltage_datalogger_adc2	trial_1	14.59	13.71	13.69	12.07
voltage_datalogger_adc2	trial_2	18.83	9.99	9.63	13.34
voltage_datalogger_adc2	trial_3	21.02	14.73	17.2	15.88
voltage_datalogger_afe	trial_0	67.14	67.14	56.85	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682978327_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682978327_3	nan ± nan (0)	30.93 ± 0.0 (1)	31.25 ± 4.5 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682978327_3	16.52 ± 3.64 (4)	12.27 ± 1.99 (4)	12.72 ± 3.0 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682978327_3	67.14 ± 0.0 (1)	67.14 ± 0.0 (1)	56.85 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682846455_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	42.11	41.89	41.87	30.87
voltage_datalogger_adc0	trial_1	39.38	38.43	37.82	25.52
voltage_datalogger_adc0	trial_2	36.08	36.08	31.78	36.03
voltage_datalogger_adc0	trial_3	37.23	37.23	36.81	28.57
voltage_datalogger_adc2	trial_0	14.08	13.99	13.99	12.81
voltage_datalogger_adc2	trial_1	13.95	13.91	13.91	12.18
voltage_datalogger_adc2	trial_2	14.85	14.85	14.85	13.9
voltage_datalogger_adc2	trial_3	14.22	14.22	14.22	12.85
voltage_datalogger_afe	trial_0	54.63	52.89	52.6	49.34
voltage_datalogger_afe	trial_1	64.24	64.17	60.22	49.26
voltage_datalogger_afe	trial_2	49.51	48.42	48.39	45.1
voltage_datalogger_afe	trial_3	-	55.16	54.29	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_0	38.7 ± 2.3 (4)	38.41 ± 2.18 (4)	37.07 ± 3.59 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846455_0	14.28 ± 0.35 (4)	14.24 ± 0.37 (4)	14.24 ± 0.37 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846455_0	56.13 ± 6.11 (3)	55.16 ± 5.74 (4)	53.87 ± 4.25 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	47.42	47.26	47.26	58.96
voltage_datalogger_adc0	trial_1	55.65	58.29	55.09	25.98
voltage_datalogger_adc0	trial_2	32.51	32.51	29.85	41.48
voltage_datalogger_adc0	trial_3	38.13	38.13	46.6	29.14
voltage_datalogger_adc2	trial_0	12.8	12.7	12.7	12.02
voltage_datalogger_adc2	trial_1	17.29	13.78	13.78	12.07
voltage_datalogger_adc2	trial_2	13.41	13.41	13.41	13.34
voltage_datalogger_adc2	trial_3	14.18	14.18	14.18	15.88
voltage_datalogger_afe	trial_0	54.95	55.76	60.73	77.93
voltage_datalogger_afe	trial_1	78.42	78.3	79.82	78.01
voltage_datalogger_afe	trial_2	55.86	55.15	55.23	76.72
voltage_datalogger_afe	trial_3	-	64.42	63.85	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_0	43.43 ± 8.84 (4)	44.05 ± 9.76 (4)	44.7 ± 9.2 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846455_0	14.42 ± 1.73 (4)	13.52 ± 0.54 (4)	13.52 ± 0.54 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846455_0	63.08 ± 10.86 (3)	63.41 ± 9.35 (4)	64.91 ± 9.15 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682846455_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	81.59	81.59	81.59	36.03
voltage_datalogger_adc0	trial_3	81.83	81.83	81.83	28.57
voltage_datalogger_adc2	trial_0	35.08	35.08	35.08	12.81
voltage_datalogger_adc2	trial_1	-	-	28.62	12.18
voltage_datalogger_adc2	trial_2	26.02	26.02	26.02	13.9
voltage_datalogger_adc2	trial_3	24.05	24.05	24.05	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	97.19	97.19	97.19	45.1
voltage_datalogger_afe	trial_3	97.25	97.25	97.25	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_1	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846455_1	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846455_1	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	92.68	92.68	92.68	41.48
voltage_datalogger_adc0	trial_3	96.93	96.93	96.93	29.14
voltage_datalogger_adc2	trial_0	28.52	28.52	28.52	12.02
voltage_datalogger_adc2	trial_1	-	-	34.5	12.07
voltage_datalogger_adc2	trial_2	21.81	21.81	21.81	13.34
voltage_datalogger_adc2	trial_3	30.96	30.96	30.96	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	120.97	120.97	120.97	76.72
voltage_datalogger_afe	trial_3	122.94	122.94	122.94	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_1	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846455_1	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846455_1	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682846455_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	35.7	31.96	31.2	30.87
voltage_datalogger_adc0	trial_1	40.09	35.3	34.73	25.52
voltage_datalogger_adc0	trial_2	45.41	43.52	43.46	36.03
voltage_datalogger_adc0	trial_3	42.94	41.45	39.25	28.57
voltage_datalogger_adc2	trial_0	13.26	13.0	12.43	12.81
voltage_datalogger_adc2	trial_1	15.37	15.11	15.11	12.18
voltage_datalogger_adc2	trial_2	14.18	14.18	14.01	13.9
voltage_datalogger_adc2	trial_3	16.01	15.17	14.9	12.85
voltage_datalogger_afe	trial_0	57.38	56.55	56.55	49.34
voltage_datalogger_afe	trial_1	56.52	54.76	54.61	49.26
voltage_datalogger_afe	trial_2	50.26	48.51	48.42	45.1
voltage_datalogger_afe	trial_3	-	59.02	51.91	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_2	41.04 ± 3.61 (4)	38.06 ± 4.64 (4)	37.16 ± 4.62 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846455_2	14.71 ± 1.06 (4)	14.36 ± 0.88 (4)	14.11 ± 1.06 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846455_2	54.72 ± 3.17 (3)	54.71 ± 3.89 (4)	52.87 ± 3.05 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	40.21	33.82	33.86	58.96
voltage_datalogger_adc0	trial_1	43.31	40.44	37.39	25.98
voltage_datalogger_adc0	trial_2	60.16	54.2	59.84	41.48
voltage_datalogger_adc0	trial_3	43.96	42.66	44.67	29.14
voltage_datalogger_adc2	trial_0	11.15	11.25	11.05	12.02
voltage_datalogger_adc2	trial_1	12.95	12.65	12.65	12.07
voltage_datalogger_adc2	trial_2	15.23	15.23	15.19	13.34
voltage_datalogger_adc2	trial_3	21.91	17.94	18.21	15.88
voltage_datalogger_afe	trial_0	62.85	62.0	62.0	77.93
voltage_datalogger_afe	trial_1	65.57	71.73	71.72	78.01
voltage_datalogger_afe	trial_2	62.24	73.56	68.64	76.72
voltage_datalogger_afe	trial_3	-	60.59	70.58	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_2	46.91 ± 7.78 (4)	42.78 ± 7.35 (4)	43.94 ± 9.97 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846455_2	15.31 ± 4.08 (4)	14.27 ± 2.56 (4)	14.28 ± 2.71 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846455_2	63.55 ± 1.45 (3)	66.97 ± 5.73 (4)	68.24 ± 3.76 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682846455_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	33.21	31.36	31.36	30.87
voltage_datalogger_adc0	trial_1	41.02	40.2	39.99	25.52
voltage_datalogger_adc0	trial_2	37.66	33.39	33.39	36.03
voltage_datalogger_adc0	trial_3	34.87	34.51	33.6	28.57
voltage_datalogger_adc2	trial_0	13.63	13.63	13.63	12.81
voltage_datalogger_adc2	trial_1	18.3	18.11	18.02	12.18
voltage_datalogger_adc2	trial_2	16.75	16.66	16.66	13.9
voltage_datalogger_adc2	trial_3	17.37	17.37	17.37	12.85
voltage_datalogger_afe	trial_0	60.17	48.82	48.16	49.34
voltage_datalogger_afe	trial_1	51.07	49.96	49.96	49.26
voltage_datalogger_afe	trial_2	62.06	54.03	51.25	45.1
voltage_datalogger_afe	trial_3	64.24	59.9	58.49	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_3	36.69 ± 2.96 (4)	34.86 ± 3.28 (4)	34.58 ± 3.24 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846455_3	16.51 ± 1.75 (4)	16.44 ± 1.7 (4)	16.42 ± 1.68 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846455_3	59.39 ± 5.01 (4)	53.18 ± 4.34 (4)	51.96 ± 3.92 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	33.27	32.36	32.36	58.96
voltage_datalogger_adc0	trial_1	40.57	41.28	40.84	25.98
voltage_datalogger_adc0	trial_2	46.8	35.15	35.15	41.48
voltage_datalogger_adc0	trial_3	44.86	44.6	33.62	29.14
voltage_datalogger_adc2	trial_0	12.94	12.94	12.94	12.02
voltage_datalogger_adc2	trial_1	21.97	16.24	21.41	12.07
voltage_datalogger_adc2	trial_2	17.42	17.32	17.32	13.34
voltage_datalogger_adc2	trial_3	20.02	20.02	20.02	15.88
voltage_datalogger_afe	trial_0	63.91	59.62	55.55	77.93
voltage_datalogger_afe	trial_1	64.94	71.11	71.11	78.01
voltage_datalogger_afe	trial_2	58.98	56.03	67.3	76.72
voltage_datalogger_afe	trial_3	70.03	69.29	77.21	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846455_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846455_3	41.38 ± 5.19 (4)	38.35 ± 4.84 (4)	35.49 ± 3.24 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846455_3	18.09 ± 3.38 (4)	16.63 ± 2.54 (4)	17.92 ± 3.23 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846455_3	64.46 ± 3.92 (4)	64.01 ± 6.35 (4)	67.79 ± 7.9 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682980882_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	35.44	35.43	30.87
voltage_datalogger_adc0	trial_1	45.45	44.5	44.37	25.52
voltage_datalogger_adc0	trial_2	30.74	30.29	29.84	36.03
voltage_datalogger_adc0	trial_3	59.76	54.08	54.08	28.57
voltage_datalogger_adc2	trial_0	17.45	17.44	17.44	12.81
voltage_datalogger_adc2	trial_1	11.99	11.99	11.99	12.18
voltage_datalogger_adc2	trial_2	14.17	12.88	12.87	13.9
voltage_datalogger_adc2	trial_3	15.14	13.72	13.1	12.85
voltage_datalogger_afe	trial_0	53.01	52.52	51.32	49.34
voltage_datalogger_afe	trial_1	-	51.74	51.74	49.26
voltage_datalogger_afe	trial_2	56.33	54.03	53.59	45.1
voltage_datalogger_afe	trial_3	62.47	61.5	60.8	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_0	45.32 ± 11.85 (3)	41.08 ± 9.07 (4)	40.93 ± 9.19 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980882_0	14.69 ± 1.96 (4)	14.01 ± 2.07 (4)	13.85 ± 2.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980882_0	57.27 ± 3.92 (3)	54.95 ± 3.87 (4)	54.36 ± 3.81 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	51.0	50.74	58.96
voltage_datalogger_adc0	trial_1	49.85	48.34	47.13	25.98
voltage_datalogger_adc0	trial_2	43.25	35.38	32.12	41.48
voltage_datalogger_adc0	trial_3	83.04	85.25	85.25	29.14
voltage_datalogger_adc2	trial_0	14.85	14.85	14.85	12.02
voltage_datalogger_adc2	trial_1	11.49	11.49	11.49	12.07
voltage_datalogger_adc2	trial_2	12.39	10.61	10.61	13.34
voltage_datalogger_adc2	trial_3	12.62	11.33	10.91	15.88
voltage_datalogger_afe	trial_0	57.76	58.67	51.71	77.93
voltage_datalogger_afe	trial_1	-	69.05	69.05	78.01
voltage_datalogger_afe	trial_2	68.16	69.14	66.08	76.72
voltage_datalogger_afe	trial_3	78.61	75.81	73.38	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_0	58.71 ± 17.41 (3)	54.99 ± 18.44 (4)	53.81 ± 19.45 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980882_0	12.84 ± 1.24 (4)	12.07 ± 1.64 (4)	11.96 ± 1.7 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980882_0	68.18 ± 8.51 (3)	68.17 ± 6.13 (4)	65.05 ± 8.13 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682980882_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	30.62	29.74	29.59	30.87
voltage_datalogger_adc0	trial_1	34.66	31.77	31.65	25.52
voltage_datalogger_adc0	trial_2	38.64	37.05	36.42	36.03
voltage_datalogger_adc0	trial_3	-	29.76	29.68	28.57
voltage_datalogger_adc2	trial_0	14.28	14.28	14.28	12.81
voltage_datalogger_adc2	trial_1	15.25	14.89	14.68	12.18
voltage_datalogger_adc2	trial_2	14.39	14.36	14.36	13.9
voltage_datalogger_adc2	trial_3	15.27	14.93	14.57	12.85
voltage_datalogger_afe	trial_0	58.66	56.55	56.55	49.34
voltage_datalogger_afe	trial_1	80.3	54.65	54.36	49.26
voltage_datalogger_afe	trial_2	52.16	50.53	49.73	45.1
voltage_datalogger_afe	trial_3	-	52.34	49.33	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_1	34.64 ± 3.27 (3)	32.08 ± 2.99 (4)	31.84 ± 2.77 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980882_1	14.8 ± 0.46 (4)	14.62 ± 0.3 (4)	14.47 ± 0.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980882_1	63.71 ± 12.03 (3)	53.52 ± 2.28 (4)	52.49 ± 3.07 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	41.32	40.33	38.05	58.96
voltage_datalogger_adc0	trial_1	37.09	49.83	37.41	25.98
voltage_datalogger_adc0	trial_2	45.52	45.23	39.84	41.48
voltage_datalogger_adc0	trial_3	-	29.71	33.75	29.14
voltage_datalogger_adc2	trial_0	16.03	16.03	16.03	12.02
voltage_datalogger_adc2	trial_1	17.64	14.79	14.51	12.07
voltage_datalogger_adc2	trial_2	15.6	15.6	15.6	13.34
voltage_datalogger_adc2	trial_3	17.53	18.82	13.97	15.88
voltage_datalogger_afe	trial_0	73.56	66.12	66.12	77.93
voltage_datalogger_afe	trial_1	96.5	66.0	68.38	78.01
voltage_datalogger_afe	trial_2	62.17	48.59	50.23	76.72
voltage_datalogger_afe	trial_3	-	75.89	60.44	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_1	41.31 ± 3.44 (3)	41.28 ± 7.47 (4)	37.26 ± 2.21 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980882_1	16.7 ± 0.9 (4)	16.31 ± 1.52 (4)	15.03 ± 0.82 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980882_1	77.41 ± 14.28 (3)	64.15 ± 9.84 (4)	61.29 ± 7.01 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682980882_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	36.86	34.05	34.05	30.87
voltage_datalogger_adc0	trial_1	33.96	33.31	32.19	25.52
voltage_datalogger_adc0	trial_2	41.36	39.73	39.4	36.03
voltage_datalogger_adc0	trial_3	39.41	37.29	35.46	28.57
voltage_datalogger_adc2	trial_0	13.91	13.8	13.62	12.81
voltage_datalogger_adc2	trial_1	15.09	14.93	14.93	12.18
voltage_datalogger_adc2	trial_2	13.56	13.54	13.54	13.9
voltage_datalogger_adc2	trial_3	14.57	14.47	14.47	12.85
voltage_datalogger_afe	trial_0	54.51	52.79	51.93	49.34
voltage_datalogger_afe	trial_1	54.33	52.65	52.39	49.26
voltage_datalogger_afe	trial_2	54.58	53.19	52.76	45.1
voltage_datalogger_afe	trial_3	-	54.45	50.29	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_2	37.9 ± 2.78 (4)	36.1 ± 2.58 (4)	35.28 ± 2.65 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980882_2	14.28 ± 0.59 (4)	14.18 ± 0.55 (4)	14.14 ± 0.58 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980882_2	54.47 ± 0.11 (3)	53.27 ± 0.71 (4)	51.84 ± 0.94 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	35.83	33.55	33.55	58.96
voltage_datalogger_adc0	trial_1	50.53	40.02	40.04	25.98
voltage_datalogger_adc0	trial_2	62.98	43.81	44.04	41.48
voltage_datalogger_adc0	trial_3	45.39	45.31	45.33	29.14
voltage_datalogger_adc2	trial_0	16.4	12.68	12.06	12.02
voltage_datalogger_adc2	trial_1	17.78	17.62	17.62	12.07
voltage_datalogger_adc2	trial_2	15.86	15.86	15.86	13.34
voltage_datalogger_adc2	trial_3	18.29	18.23	18.23	15.88
voltage_datalogger_afe	trial_0	57.36	56.35	56.38	77.93
voltage_datalogger_afe	trial_1	65.54	67.97	69.02	78.01
voltage_datalogger_afe	trial_2	60.29	57.36	56.27	76.72
voltage_datalogger_afe	trial_3	-	57.69	62.35	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_2	48.68 ± 9.8 (4)	40.67 ± 4.54 (4)	40.74 ± 4.59 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980882_2	17.08 ± 0.99 (4)	16.1 ± 2.16 (4)	15.94 ± 2.4 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980882_2	61.06 ± 3.38 (3)	59.84 ± 4.72 (4)	61.0 ± 5.24 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1682980882_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	35.4	33.09	33.09	30.87
voltage_datalogger_adc0	trial_1	-	25.91	25.91	25.52
voltage_datalogger_adc0	trial_2	42.23	40.63	40.63	36.03
voltage_datalogger_adc0	trial_3	34.02	33.17	32.23	28.57
voltage_datalogger_adc2	trial_0	14.0	13.78	13.78	12.81
voltage_datalogger_adc2	trial_1	15.19	14.89	14.62	12.18
voltage_datalogger_adc2	trial_2	13.21	12.8	12.72	13.9
voltage_datalogger_adc2	trial_3	15.14	13.9	13.72	12.85
voltage_datalogger_afe	trial_0	54.36	52.9	52.9	49.34
voltage_datalogger_afe	trial_1	56.91	54.81	52.88	49.26
voltage_datalogger_afe	trial_2	57.11	54.46	53.48	45.1
voltage_datalogger_afe	trial_3	62.97	61.78	60.97	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_3	37.22 ± 3.59 (3)	33.2 ± 5.2 (4)	32.96 ± 5.22 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682980882_3	14.38 ± 0.83 (4)	13.84 ± 0.74 (4)	13.71 ± 0.67 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682980882_3	57.84 ± 3.16 (4)	55.99 ± 3.42 (4)	55.06 ± 3.42 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	44.6	42.08	42.08	58.96
voltage_datalogger_adc0	trial_1	-	39.04	39.04	25.98
voltage_datalogger_adc0	trial_2	42.33	64.06	64.06	41.48
voltage_datalogger_adc0	trial_3	36.42	35.68	34.47	29.14
voltage_datalogger_adc2	trial_0	12.75	12.33	12.33	12.02
voltage_datalogger_adc2	trial_1	19.78	17.23	16.92	12.07
voltage_datalogger_adc2	trial_2	10.51	10.33	10.19	13.34
voltage_datalogger_adc2	trial_3	19.78	18.2	18.1	15.88
voltage_datalogger_afe	trial_0	58.81	58.17	58.17	77.93
voltage_datalogger_afe	trial_1	67.62	59.61	58.65	78.01
voltage_datalogger_afe	trial_2	76.23	72.81	71.35	76.72
voltage_datalogger_afe	trial_3	74.08	86.6	73.58	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682980882_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682980882_3	41.12 ± 3.45 (3)	45.22 ± 11.11 (4)	44.91 ± 11.38 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682980882_3	15.7 ± 4.15 (4)	14.52 ± 3.29 (4)	14.38 ± 3.24 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682980882_3	69.18 ± 6.78 (4)	69.3 ± 11.5 (4)	65.44 ± 7.07 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682846457_0

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	31.99	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	23.1	28.57
voltage_datalogger_adc2	trial_0	15.56	11.97	11.55	12.81
voltage_datalogger_adc2	trial_1	15.78	14.87	14.87	12.18
voltage_datalogger_adc2	trial_2	15.27	13.87	13.39	13.9
voltage_datalogger_adc2	trial_3	15.76	14.74	13.93	12.85
voltage_datalogger_afe	trial_0	44.81	44.81	44.81	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_0	nan ± nan (0)	nan ± nan (0)	27.54 ± 4.44 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846457_0	15.59 ± 0.21 (4)	13.86 ± 1.16 (4)	13.44 ± 1.21 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846457_0	44.81 ± 0.0 (1)	44.81 ± 0.0 (1)	44.81 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	40.3	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	22.77	29.14
voltage_datalogger_adc2	trial_0	13.92	10.7	10.57	12.02
voltage_datalogger_adc2	trial_1	18.5	17.62	17.62	12.07
voltage_datalogger_adc2	trial_2	15.89	14.62	14.07	13.34
voltage_datalogger_adc2	trial_3	14.14	16.06	12.37	15.88
voltage_datalogger_afe	trial_0	48.1	48.1	48.1	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_0	nan ± nan (0)	nan ± nan (0)	31.53 ± 8.76 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846457_0	15.61 ± 1.83 (4)	14.75 ± 2.57 (4)	13.66 ± 2.6 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846457_0	48.1 ± 0.0 (1)	48.1 ± 0.0 (1)	48.1 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682846457_1

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.84	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	13.27	12.48	12.06	12.81
voltage_datalogger_adc2	trial_1	15.2	14.4	13.69	12.18
voltage_datalogger_adc2	trial_2	15.03	13.11	13.11	13.9
voltage_datalogger_adc2	trial_3	15.46	13.43	13.08	12.85
voltage_datalogger_afe	trial_0	-	42.77	42.77	49.34
voltage_datalogger_afe	trial_1	-	-	45.24	49.26
voltage_datalogger_afe	trial_2	-	-	40.16	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_1	nan ± nan (0)	nan ± nan (0)	28.84 ± 0.0 (1)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846457_1	14.74 ± 0.86 (4)	13.36 ± 0.69 (4)	12.98 ± 0.59 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846457_1	nan ± nan (0)	42.77 ± 0.0 (1)	42.72 ± 2.07 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	27.98	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	10.82	9.98	9.82	12.02
voltage_datalogger_adc2	trial_1	13.72	13.39	13.02	12.07
voltage_datalogger_adc2	trial_2	16.98	10.78	10.78	13.34
voltage_datalogger_adc2	trial_3	14.6	11.32	11.06	15.88
voltage_datalogger_afe	trial_0	-	45.1	45.1	77.93
voltage_datalogger_afe	trial_1	-	-	50.3	78.01
voltage_datalogger_afe	trial_2	-	-	46.33	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_1	nan ± nan (0)	nan ± nan (0)	27.98 ± 0.0 (1)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846457_1	14.03 ± 2.2 (4)	11.37 ± 1.26 (4)	11.17 ± 1.16 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846457_1	nan ± nan (0)	45.1 ± 0.0 (1)	47.24 ± 2.22 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682846457_2

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	27.43	27.43	27.43	30.87
voltage_datalogger_adc0	trial_1	-	-	25.6	25.52
voltage_datalogger_adc0	trial_2	28.61	28.61	28.61	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	11.54	11.53	11.53	12.81
voltage_datalogger_adc2	trial_1	15.32	14.83	14.12	12.18
voltage_datalogger_adc2	trial_2	12.1	12.1	11.88	13.9
voltage_datalogger_adc2	trial_3	15.46	15.46	15.0	12.85
voltage_datalogger_afe	trial_0	-	-	49.89	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	44.88	44.88	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_2	28.02 ± 0.59 (2)	28.02 ± 0.59 (2)	27.21 ± 1.24 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846457_2	13.6 ± 1.8 (4)	13.48 ± 1.69 (4)	13.13 ± 1.47 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846457_2	nan ± nan (0)	44.88 ± 0.0 (1)	47.39 ± 2.5 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	37.98	37.98	37.98	58.96
voltage_datalogger_adc0	trial_1	-	-	31.78	25.98
voltage_datalogger_adc0	trial_2	39.52	39.52	39.52	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	10.19	10.25	10.25	12.02
voltage_datalogger_adc2	trial_1	20.93	14.13	13.12	12.07
voltage_datalogger_adc2	trial_2	10.29	10.29	9.85	13.34
voltage_datalogger_adc2	trial_3	15.14	15.14	16.11	15.88
voltage_datalogger_afe	trial_0	-	-	58.36	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	50.0	50.0	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_2	38.75 ± 0.77 (2)	38.75 ± 0.77 (2)	36.43 ± 3.35 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846457_2	14.14 ± 4.4 (4)	12.45 ± 2.21 (4)	12.33 ± 2.52 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846457_2	nan ± nan (0)	50.0 ± 0.0 (1)	54.18 ± 4.18 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682846457_3

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.34	30.87
voltage_datalogger_adc0	trial_1	-	-	26.24	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	11.22	11.22	11.22	12.81
voltage_datalogger_adc2	trial_1	15.47	14.7	14.41	12.18
voltage_datalogger_adc2	trial_2	17.11	11.41	11.01	13.9
voltage_datalogger_adc2	trial_3	-	14.85	14.58	12.85
voltage_datalogger_afe	trial_0	42.61	42.61	42.61	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_3	nan ± nan (0)	nan ± nan (0)	27.29 ± 1.05 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682846457_3	14.6 ± 2.48 (3)	13.04 ± 1.73 (4)	12.8 ± 1.69 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682846457_3	42.61 ± 0.0 (1)	42.61 ± 0.0 (1)	42.61 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	50.51	58.96
voltage_datalogger_adc0	trial_1	-	-	38.4	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	10.09	10.09	10.09	12.02
voltage_datalogger_adc2	trial_1	18.6	14.34	13.83	12.07
voltage_datalogger_adc2	trial_2	14.57	10.36	10.02	13.34
voltage_datalogger_adc2	trial_3	-	14.36	17.05	15.88
voltage_datalogger_afe	trial_0	49.69	49.69	49.69	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682846457_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682846457_3	nan ± nan (0)	nan ± nan (0)	44.46 ± 6.06 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682846457_3	14.42 ± 3.48 (3)	12.29 ± 2.06 (4)	12.75 ± 2.92 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682846457_3	49.69 ± 0.0 (1)	49.69 ± 0.0 (1)	49.69 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682981272_0

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	26.19	25.15	30.87
voltage_datalogger_adc0	trial_1	-	-	25.08	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	28.7	28.35	28.57
voltage_datalogger_adc2	trial_0	12.98	12.52	12.38	12.81
voltage_datalogger_adc2	trial_1	15.24	14.89	13.93	12.18
voltage_datalogger_adc2	trial_2	11.96	11.6	11.18	13.9
voltage_datalogger_adc2	trial_3	14.73	14.73	13.93	12.85
voltage_datalogger_afe	trial_0	-	-	44.33	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_0	nan ± nan (0)	27.44 ± 1.25 (2)	26.19 ± 1.53 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682981272_0	13.73 ± 1.32 (4)	13.43 ± 1.41 (4)	12.86 ± 1.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682981272_0	nan ± nan (0)	nan ± nan (0)	44.33 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	28.28	26.98	58.96
voltage_datalogger_adc0	trial_1	-	-	28.19	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	35.03	34.86	29.14
voltage_datalogger_adc2	trial_0	11.4	11.34	13.98	12.02
voltage_datalogger_adc2	trial_1	13.65	20.26	16.62	12.07
voltage_datalogger_adc2	trial_2	10.74	10.74	10.6	13.34
voltage_datalogger_adc2	trial_3	14.17	14.17	17.48	15.88
voltage_datalogger_afe	trial_0	-	-	40.69	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_0	nan ± nan (0)	31.66 ± 3.38 (2)	30.01 ± 3.46 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682981272_0	12.49 ± 1.45 (4)	14.13 ± 3.77 (4)	14.67 ± 2.68 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682981272_0	nan ± nan (0)	nan ± nan (0)	40.69 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682981272_1

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.53	30.87
voltage_datalogger_adc0	trial_1	-	-	32.96	25.52
voltage_datalogger_adc0	trial_2	-	-	26.97	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	17.36	12.75	11.55	12.81
voltage_datalogger_adc2	trial_1	15.56	14.72	13.99	12.18
voltage_datalogger_adc2	trial_2	12.92	11.81	10.87	13.9
voltage_datalogger_adc2	trial_3	15.42	14.2	14.02	12.85
voltage_datalogger_afe	trial_0	-	45.13	45.13	49.34
voltage_datalogger_afe	trial_1	-	44.55	44.55	49.26
voltage_datalogger_afe	trial_2	-	46.28	44.67	45.1
voltage_datalogger_afe	trial_3	-	52.02	49.5	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_1	nan ± nan (0)	nan ± nan (0)	29.49 ± 2.54 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682981272_1	15.32 ± 1.58 (4)	13.37 ± 1.15 (4)	12.61 ± 1.42 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682981272_1	nan ± nan (0)	47.0 ± 2.97 (4)	45.96 ± 2.05 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	27.12	58.96
voltage_datalogger_adc0	trial_1	-	-	32.95	25.98
voltage_datalogger_adc0	trial_2	-	-	35.08	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	13.81	11.61	10.8	12.02
voltage_datalogger_adc2	trial_1	19.58	19.16	12.75	12.07
voltage_datalogger_adc2	trial_2	11.79	10.94	9.61	13.34
voltage_datalogger_adc2	trial_3	20.38	23.16	19.01	15.88
voltage_datalogger_afe	trial_0	-	45.84	45.84	77.93
voltage_datalogger_afe	trial_1	-	46.63	46.63	78.01
voltage_datalogger_afe	trial_2	-	53.14	52.33	76.72
voltage_datalogger_afe	trial_3	-	62.02	63.67	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_1	nan ± nan (0)	nan ± nan (0)	31.72 ± 3.36 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682981272_1	16.39 ± 3.67 (4)	16.22 ± 5.15 (4)	13.04 ± 3.62 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682981272_1	nan ± nan (0)	51.91 ± 6.49 (4)	52.12 ± 7.12 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682981272_2

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	30.32	30.32	30.32	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	24.82	24.35	36.03
voltage_datalogger_adc0	trial_3	-	-	27.82	28.57
voltage_datalogger_adc2	trial_0	17.72	13.27	12.18	12.81
voltage_datalogger_adc2	trial_1	15.19	14.45	13.91	12.18
voltage_datalogger_adc2	trial_2	14.68	13.33	11.3	13.9
voltage_datalogger_adc2	trial_3	15.78	14.53	13.82	12.85
voltage_datalogger_afe	trial_0	-	45.64	45.64	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	43.01	43.01	45.1
voltage_datalogger_afe	trial_3	-	49.0	49.0	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_2	30.32 ± 0.0 (1)	27.57 ± 2.75 (2)	27.5 ± 2.45 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682981272_2	15.84 ± 1.15 (4)	13.9 ± 0.6 (4)	12.8 ± 1.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682981272_2	nan ± nan (0)	45.88 ± 2.45 (3)	45.88 ± 2.45 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	28.12	28.12	28.12	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	24.71	26.93	41.48
voltage_datalogger_adc0	trial_3	-	-	30.46	29.14
voltage_datalogger_adc2	trial_0	15.02	10.91	10.44	12.02
voltage_datalogger_adc2	trial_1	13.67	13.03	12.71	12.07
voltage_datalogger_adc2	trial_2	11.94	11.01	10.36	13.34
voltage_datalogger_adc2	trial_3	19.06	13.89	13.3	15.88
voltage_datalogger_afe	trial_0	-	46.59	46.59	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	49.87	49.87	76.72
voltage_datalogger_afe	trial_3	-	63.48	63.48	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_2	28.12 ± 0.0 (1)	26.42 ± 1.7 (2)	28.5 ± 1.47 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682981272_2	14.92 ± 2.63 (4)	12.21 ± 1.29 (4)	11.7 ± 1.32 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682981272_2	nan ± nan (0)	53.31 ± 7.31 (3)	53.31 ± 7.31 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1682981272_3

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	60.61	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	72.47	32.15	28.57
voltage_datalogger_adc2	trial_0	17.46	15.27	11.89	12.81
voltage_datalogger_adc2	trial_1	16.5	15.09	14.36	12.18
voltage_datalogger_adc2	trial_2	15.42	13.14	11.54	13.9
voltage_datalogger_adc2	trial_3	16.59	14.46	14.26	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_3	nan ± nan (0)	72.47 ± 0.0 (1)	46.38 ± 14.23 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682981272_3	16.49 ± 0.72 (4)	14.49 ± 0.84 (4)	13.01 ± 1.3 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682981272_3	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	61.02	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	84.58	33.06	29.14
voltage_datalogger_adc2	trial_0	16.23	14.79	10.35	12.02
voltage_datalogger_adc2	trial_1	23.22	13.93	13.59	12.07
voltage_datalogger_adc2	trial_2	16.16	11.05	9.63	13.34
voltage_datalogger_adc2	trial_3	19.63	17.16	12.96	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_expert_experiments/work/eval_testing_set/1682981272_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682981272_3	nan ± nan (0)	84.58 ± 0.0 (1)	47.04 ± 13.98 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682981272_3	18.81 ± 2.91 (4)	14.23 ± 2.19 (4)	11.63 ± 1.68 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682981272_3	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed