Experiment Report

Start of automated test report 2023-04-20 21:39:54
Author=UNKNOWN@workstation obo Luke Vassallo

Machine Information

sysname=Linux
nodename=workstation
release=5.19.0-38-generic
version=#39~22.04.1-Ubuntu SMP PREEMPT_DYNAMIC Fri Mar 17 21:16:15 UTC 2
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz
CPU cores : 8
CPU base clock : 3.8000 GHz
CPU boost clock : 3.7920 GHz
System Memory : 31.35GB
Nvidia driver version : 525.105.17
Device 0 : NVIDIA GeForce GTX 1080
Device 0 : 8.0GB

Library Information

python : 3.8.16
torch : 1.13.1+cu117
optuna : 3.1.0
numpy : 1.23.3
pandas : 1.5.3
matplotlib : 3.7.1
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

parameter_experiment_262:1681717898_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_0	nan ± nan (0)	25.49 ± 0.0 (1)	43.84 ± 22.7 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717898_0	14.74 ± 2.21 (4)	13.52 ± 2.0 (4)	12.77 ± 1.77 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717898_0	nan ± nan (0)	43.14 ± 0.58 (3)	43.14 ± 0.58 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_0	nan ± nan (0)	29.29 ± 0.0 (1)	57.15 ± 32.53 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717898_0	15.65 ± 5.58 (4)	14.06 ± 4.55 (4)	13.29 ± 3.99 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717898_0	nan ± nan (0)	50.37 ± 3.59 (3)	50.37 ± 3.59 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681717898_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_1	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717898_1	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717898_1	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_1	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717898_1	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717898_1	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681717898_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_2	nan ± nan (0)	28.04 ± 1.95 (2)	27.87 ± 1.92 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717898_2	15.43 ± 2.2 (4)	14.11 ± 1.17 (4)	12.46 ± 1.31 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717898_2	nan ± nan (0)	54.84 ± 0.0 (1)	54.84 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_2	nan ± nan (0)	33.24 ± 2.71 (2)	32.37 ± 2.83 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717898_2	17.03 ± 4.23 (4)	15.91 ± 4.18 (4)	12.51 ± 2.99 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717898_2	nan ± nan (0)	60.35 ± 0.0 (1)	60.35 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681717898_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_3	nan ± nan (0)	29.06 ± 0.0 (1)	28.79 ± 1.17 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717898_3	15.93 ± 0.5 (4)	14.71 ± 1.11 (4)	13.18 ± 1.04 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717898_3	nan ± nan (0)	46.93 ± 0.0 (1)	48.64 ± 2.83 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717898_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717898_3	nan ± nan (0)	27.71 ± 0.0 (1)	32.14 ± 3.54 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717898_3	16.84 ± 3.42 (4)	12.98 ± 1.7 (4)	11.94 ± 1.56 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717898_3	nan ± nan (0)	62.12 ± 0.0 (1)	55.5 ± 2.96 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681852441_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_0	27.41 ± 0.0 (1)	27.5 ± 3.38 (3)	26.08 ± 3.82 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852441_0	14.42 ± 3.34 (4)	11.62 ± 0.21 (4)	10.88 ± 0.27 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852441_0	nan ± nan (0)	nan ± nan (0)	43.51 ± 1.29 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_0	30.84 ± 0.0 (1)	31.87 ± 2.4 (3)	31.26 ± 2.33 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852441_0	13.64 ± 2.79 (4)	11.96 ± 1.41 (4)	11.47 ± 1.35 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852441_0	nan ± nan (0)	nan ± nan (0)	58.07 ± 7.07 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681852441_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_1	30.18 ± 0.0 (1)	30.18 ± 0.0 (1)	25.61 ± 4.28 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852441_1	18.45 ± 7.04 (4)	11.66 ± 0.52 (4)	10.76 ± 0.28 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852441_1	47.87 ± 0.0 (1)	45.98 ± 1.88 (2)	46.96 ± 2.17 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_1	34.53 ± 0.0 (1)	34.53 ± 0.0 (1)	29.1 ± 3.13 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852441_1	20.16 ± 9.54 (4)	10.58 ± 0.07 (4)	10.02 ± 0.24 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852441_1	55.2 ± 0.0 (1)	51.68 ± 3.52 (2)	61.21 ± 8.45 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681852441_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_2	nan ± nan (0)	42.96 ± 24.47 (3)	38.22 ± 19.47 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852441_2	13.98 ± 1.73 (4)	13.36 ± 1.77 (4)	12.48 ± 1.65 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852441_2	nan ± nan (0)	nan ± nan (0)	47.04 ± 0.41 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_2	nan ± nan (0)	51.42 ± 29.88 (3)	47.66 ± 23.73 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852441_2	13.17 ± 2.56 (4)	11.98 ± 1.66 (4)	13.34 ± 4.4 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852441_2	nan ± nan (0)	nan ± nan (0)	58.08 ± 3.96 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_262:1681852441_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_3	33.14 ± 0.0 (1)	29.75 ± 3.39 (2)	27.21 ± 1.58 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852441_3	14.11 ± 1.57 (4)	13.3 ± 1.5 (4)	12.78 ± 1.44 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852441_3	52.57 ± 0.0 (1)	49.28 ± 0.71 (2)	47.7 ± 0.87 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852441_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852441_3	39.81 ± 0.0 (1)	35.22 ± 4.59 (2)	29.75 ± 4.41 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852441_3	16.63 ± 5.45 (4)	13.64 ± 3.99 (4)	12.94 ± 3.3 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852441_3	58.1 ± 0.0 (1)	53.6 ± 0.6 (2)	52.44 ± 0.56 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681717896_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_0	nan ± nan (0)	29.85 ± 0.0 (1)	29.86 ± 0.0 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717896_0	18.56 ± 6.88 (4)	13.3 ± 1.32 (4)	12.9 ± 1.22 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717896_0	nan ± nan (0)	46.75 ± 1.52 (2)	46.75 ± 1.52 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_0	nan ± nan (0)	30.81 ± 0.0 (1)	34.0 ± 3.19 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717896_0	17.81 ± 5.25 (4)	13.38 ± 3.17 (4)	11.83 ± 1.38 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717896_0	nan ± nan (0)	54.77 ± 3.83 (2)	54.77 ± 3.83 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681717896_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_1	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717896_1	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717896_1	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_1	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717896_1	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717896_1	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681717896_2

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_2	nan ± nan (0)	27.72 ± 0.0 (1)	28.99 ± 3.32 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717896_2	19.43 ± 5.12 (4)	14.4 ± 0.39 (4)	13.46 ± 0.87 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717896_2	nan ± nan (0)	nan ± nan (0)	47.2 ± 2.48 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_2	nan ± nan (0)	27.54 ± 0.0 (1)	28.78 ± 2.13 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717896_2	18.05 ± 2.51 (4)	12.35 ± 0.71 (4)	11.88 ± 1.13 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717896_2	nan ± nan (0)	nan ± nan (0)	50.52 ± 3.8 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681717896_3

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_3	nan ± nan (0)	68.77 ± 0.0 (1)	37.73 ± 18.14 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717896_3	14.58 ± 1.04 (4)	14.0 ± 0.95 (4)	12.77 ± 1.47 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717896_3	nan ± nan (0)	53.82 ± 0.0 (1)	44.13 ± 4.43 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717896_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717896_3	nan ± nan (0)	86.5 ± 0.0 (1)	45.52 ± 23.82 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717896_3	14.54 ± 1.77 (4)	13.15 ± 1.59 (4)	13.88 ± 4.4 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717896_3	nan ± nan (0)	58.29 ± 0.0 (1)	52.6 ± 6.66 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681851168_0

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_0	nan ± nan (0)	31.33 ± 0.0 (1)	30.96 ± 0.38 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681851168_0	18.54 ± 3.98 (4)	14.32 ± 0.48 (4)	13.46 ± 0.92 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681851168_0	44.29 ± 0.0 (1)	44.29 ± 0.0 (1)	44.4 ± 1.49 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_0	nan ± nan (0)	30.85 ± 0.0 (1)	30.92 ± 0.07 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681851168_0	18.39 ± 3.08 (4)	13.9 ± 2.99 (4)	14.02 ± 2.17 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681851168_0	55.33 ± 0.0 (1)	55.33 ± 0.0 (1)	51.04 ± 5.28 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681851168_1

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_1	nan ± nan (0)	nan ± nan (0)	28.76 ± 3.15 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681851168_1	14.56 ± 0.96 (4)	13.15 ± 1.65 (4)	12.52 ± 1.54 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681851168_1	49.46 ± 0.0 (1)	47.11 ± 0.0 (1)	45.48 ± 1.93 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_1	nan ± nan (0)	nan ± nan (0)	30.6 ± 2.58 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681851168_1	15.98 ± 4.9 (4)	15.09 ± 4.81 (4)	11.32 ± 1.47 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681851168_1	54.31 ± 0.0 (1)	60.65 ± 0.0 (1)	51.66 ± 2.58 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681851168_2

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_2	nan ± nan (0)	27.42 ± 0.0 (1)	28.23 ± 1.9 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681851168_2	15.93 ± 1.5 (4)	15.04 ± 1.3 (4)	13.36 ± 0.86 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681851168_2	nan ± nan (0)	nan ± nan (0)	43.97 ± 0.3 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_2	nan ± nan (0)	38.4 ± 0.0 (1)	32.11 ± 4.36 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681851168_2	15.18 ± 2.97 (4)	14.52 ± 2.75 (4)	12.03 ± 2.1 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681851168_2	nan ± nan (0)	nan ± nan (0)	50.83 ± 1.49 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_622:1681851168_3

Steps per trial = 600

Euclidean wirelength (w) = 6

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_3	nan ± nan (0)	nan ± nan (0)	25.84 ± 3.67 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681851168_3	14.8 ± 1.61 (4)	11.93 ± 0.76 (4)	10.95 ± 0.41 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681851168_3	nan ± nan (0)	47.65 ± 0.0 (1)	47.65 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681851168_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681851168_3	nan ± nan (0)	nan ± nan (0)	30.08 ± 2.01 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681851168_3	14.98 ± 3.15 (4)	11.84 ± 1.04 (4)	10.76 ± 1.44 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681851168_3	nan ± nan (0)	56.83 ± 0.0 (1)	56.83 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681717900_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_0	35.26 ± 1.38 (4)	33.99 ± 2.79 (4)	33.74 ± 2.78 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717900_0	15.54 ± 0.29 (4)	15.28 ± 0.37 (4)	15.28 ± 0.37 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717900_0	nan ± nan (0)	51.39 ± 4.59 (4)	51.04 ± 4.33 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_0	39.26 ± 2.75 (4)	36.66 ± 2.86 (4)	39.91 ± 4.58 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717900_0	15.45 ± 2.31 (4)	16.18 ± 3.01 (4)	16.18 ± 3.01 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717900_0	nan ± nan (0)	63.77 ± 9.65 (4)	66.15 ± 7.42 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681717900_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_1	38.72 ± 7.69 (3)	36.1 ± 5.82 (4)	35.3 ± 5.73 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717900_1	14.04 ± 1.09 (4)	13.88 ± 0.93 (4)	13.82 ± 0.93 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717900_1	61.11 ± 9.84 (4)	58.38 ± 9.02 (4)	57.02 ± 8.35 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_1	39.29 ± 8.64 (3)	38.03 ± 8.29 (4)	40.72 ± 8.24 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717900_1	14.84 ± 4.11 (4)	14.17 ± 3.43 (4)	15.66 ± 2.97 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717900_1	71.16 ± 12.23 (4)	76.06 ± 11.72 (4)	70.59 ± 12.66 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681717900_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_2	33.24 ± 1.69 (3)	31.42 ± 2.73 (4)	31.15 ± 3.04 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717900_2	15.1 ± 1.19 (4)	13.99 ± 0.69 (4)	13.85 ± 0.57 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717900_2	53.83 ± 6.59 (3)	52.08 ± 4.79 (4)	50.93 ± 5.29 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_2	39.41 ± 6.91 (3)	37.52 ± 8.68 (4)	33.84 ± 4.01 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717900_2	14.78 ± 2.5 (4)	13.97 ± 2.38 (4)	13.63 ± 1.96 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717900_2	67.22 ± 13.7 (3)	65.73 ± 11.03 (4)	61.7 ± 9.38 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681717900_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_3	35.05 ± 3.01 (3)	37.76 ± 6.12 (4)	37.69 ± 6.14 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717900_3	14.27 ± 0.93 (4)	13.77 ± 0.89 (4)	13.7 ± 0.93 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717900_3	55.22 ± 7.51 (2)	56.42 ± 5.75 (4)	55.63 ± 6.24 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717900_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717900_3	39.03 ± 7.34 (3)	43.93 ± 11.9 (4)	43.68 ± 11.34 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717900_3	15.94 ± 2.94 (4)	15.27 ± 3.15 (4)	15.0 ± 3.34 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717900_3	69.53 ± 21.52 (2)	67.03 ± 14.53 (4)	78.35 ± 12.75 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681852463_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_0	36.33 ± 5.24 (4)	31.74 ± 3.35 (4)	31.4 ± 3.6 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852463_0	14.67 ± 0.68 (4)	14.06 ± 0.76 (4)	13.83 ± 0.93 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852463_0	54.5 ± 4.89 (2)	53.23 ± 4.16 (4)	52.37 ± 4.92 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_0	40.91 ± 8.34 (4)	36.29 ± 4.84 (4)	36.37 ± 4.61 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852463_0	15.63 ± 2.17 (4)	16.0 ± 1.73 (4)	15.36 ± 1.01 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852463_0	62.94 ± 15.11 (2)	60.04 ± 12.15 (4)	62.15 ± 14.63 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681852463_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_1	48.15 ± 2.46 (3)	42.49 ± 2.39 (4)	42.0 ± 2.64 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852463_1	14.49 ± 1.45 (4)	13.88 ± 1.28 (4)	13.56 ± 1.24 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852463_1	64.64 ± 2.25 (2)	60.28 ± 3.16 (4)	58.02 ± 3.45 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_1	64.58 ± 10.43 (3)	54.62 ± 6.39 (4)	54.05 ± 8.8 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852463_1	14.23 ± 2.06 (4)	16.11 ± 4.34 (4)	15.92 ± 4.3 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852463_1	87.58 ± 6.1 (2)	72.21 ± 5.3 (4)	81.38 ± 16.08 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681852463_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_2	41.12 ± 7.13 (3)	38.72 ± 5.05 (4)	38.0 ± 5.38 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852463_2	14.21 ± 0.86 (4)	13.5 ± 1.49 (4)	13.21 ± 1.39 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852463_2	56.78 ± 5.93 (4)	54.49 ± 5.62 (4)	53.34 ± 6.14 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_2	42.82 ± 7.81 (3)	41.08 ± 5.09 (4)	39.78 ± 6.38 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852463_2	15.57 ± 3.03 (4)	14.05 ± 3.73 (4)	13.21 ± 3.22 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852463_2	65.04 ± 10.85 (4)	59.98 ± 7.98 (4)	60.42 ± 9.72 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_226:1681852463_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 6.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_3	50.08 ± 4.94 (4)	47.36 ± 5.29 (4)	46.86 ± 5.68 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681852463_3	15.0 ± 0.41 (4)	14.38 ± 0.57 (4)	14.17 ± 0.63 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681852463_3	59.7 ± 4.63 (4)	57.46 ± 4.73 (4)	56.74 ± 4.54 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681852463_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681852463_3	66.8 ± 6.67 (4)	60.65 ± 8.72 (4)	57.89 ± 8.57 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681852463_3	16.1 ± 2.26 (4)	14.81 ± 1.95 (4)	13.91 ± 1.21 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681852463_3	77.0 ± 2.83 (4)	76.95 ± 6.28 (4)	75.44 ± 6.6 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681717902_0

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_0	nan ± nan (0)	29.06 ± 1.02 (2)	27.91 ± 0.87 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717902_0	19.88 ± 3.31 (3)	16.29 ± 3.01 (4)	13.0 ± 1.3 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717902_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_0	nan ± nan (0)	36.32 ± 5.37 (2)	30.19 ± 1.61 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717902_0	18.79 ± 1.37 (3)	17.3 ± 1.69 (4)	12.77 ± 1.44 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717902_0	nan ± nan (0)	nan ± nan (0)	nan ± nan (0)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681717902_1

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_1	nan ± nan (0)	28.27 ± 0.0 (1)	26.81 ± 1.65 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717902_1	15.57 ± 2.02 (3)	13.9 ± 0.8 (4)	12.38 ± 1.37 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717902_1	43.63 ± 0.0 (1)	43.63 ± 0.0 (1)	45.77 ± 1.66 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_1	nan ± nan (0)	27.95 ± 0.0 (1)	36.11 ± 6.49 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717902_1	14.59 ± 2.9 (3)	14.22 ± 2.48 (4)	11.29 ± 1.21 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717902_1	56.09 ± 0.0 (1)	56.09 ± 0.0 (1)	54.98 ± 0.82 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681717902_2

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_2	nan ± nan (0)	nan ± nan (0)	29.7 ± 1.21 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717902_2	17.76 ± 4.7 (4)	15.72 ± 2.41 (4)	13.18 ± 0.78 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717902_2	nan ± nan (0)	40.6 ± 0.0 (1)	40.6 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_2	nan ± nan (0)	nan ± nan (0)	38.64 ± 2.21 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717902_2	16.78 ± 2.59 (4)	15.3 ± 1.82 (4)	12.09 ± 1.62 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717902_2	nan ± nan (0)	43.88 ± 0.0 (1)	43.88 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681717902_3

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_3	nan ± nan (0)	nan ± nan (0)	27.22 ± 1.52 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681717902_3	17.7 ± 4.55 (4)	13.56 ± 1.52 (4)	13.07 ± 1.23 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681717902_3	nan ± nan (0)	46.1 ± 0.0 (1)	46.1 ± 0.0 (1)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681717902_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681717902_3	nan ± nan (0)	nan ± nan (0)	33.24 ± 3.49 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681717902_3	18.09 ± 3.63 (4)	12.28 ± 1.62 (4)	11.57 ± 1.26 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681717902_3	nan ± nan (0)	64.08 ± 0.0 (1)	64.08 ± 0.0 (1)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681853385_0

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_0	nan ± nan (0)	nan ± nan (0)	28.0 ± 3.53 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681853385_0	17.52 ± 0.12 (2)	13.66 ± 1.38 (4)	12.69 ± 1.17 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681853385_0	48.27 ± 0.0 (1)	48.18 ± 0.09 (2)	46.7 ± 2.11 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_0	nan ± nan (0)	nan ± nan (0)	30.04 ± 4.97 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681853385_0	18.7 ± 0.31 (2)	12.58 ± 1.67 (4)	12.2 ± 1.65 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681853385_0	46.91 ± 0.0 (1)	49.4 ± 2.49 (2)	49.38 ± 2.03 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681853385_1

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_1	35.16 ± 0.0 (1)	35.16 ± 0.0 (1)	27.92 ± 3.02 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681853385_1	20.01 ± 7.96 (4)	13.31 ± 1.67 (4)	12.87 ± 1.59 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681853385_1	56.63 ± 0.0 (1)	56.63 ± 0.0 (1)	49.56 ± 3.38 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_1	36.21 ± 0.0 (1)	36.21 ± 0.0 (1)	34.44 ± 1.01 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681853385_1	19.58 ± 5.78 (4)	12.02 ± 1.33 (4)	11.63 ± 1.4 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681853385_1	63.03 ± 0.0 (1)	63.03 ± 0.0 (1)	60.36 ± 5.03 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681853385_2

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_2	nan ± nan (0)	29.25 ± 0.0 (1)	28.4 ± 1.19 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681853385_2	16.91 ± 1.93 (4)	13.34 ± 1.21 (4)	12.47 ± 1.43 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681853385_2	nan ± nan (0)	47.16 ± 0.0 (1)	45.34 ± 0.77 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_2	nan ± nan (0)	43.56 ± 0.0 (1)	32.37 ± 6.32 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681853385_2	18.72 ± 2.15 (4)	11.74 ± 1.45 (4)	11.38 ± 1.87 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681853385_2	nan ± nan (0)	66.51 ± 0.0 (1)	59.28 ± 6.77 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

parameter_experiment_442:1681853385_3

Steps per trial = 600

Euclidean wirelength (w) = 4

Half perimeter wirelength (hpwl) = 4.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_3	nan ± nan (0)	29.57 ± 0.0 (1)	26.31 ± 0.0 (1)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1681853385_3	15.12 ± 0.68 (4)	13.78 ± 0.96 (4)	13.2 ± 1.15 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1681853385_3	nan ± nan (0)	43.43 ± 0.0 (1)	45.99 ± 2.15 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/luke/work/rl_pcb/experiments/01_parameter_exeperiments/work/eval_testing_set/1681853385_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1681853385_3	nan ± nan (0)	36.35 ± 0.0 (1)	38.47 ± 0.0 (1)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1681853385_3	14.78 ± 0.61 (4)	12.89 ± 1.25 (4)	14.04 ± 3.23 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1681853385_3	nan ± nan (0)	51.39 ± 0.0 (1)	62.54 ± 13.52 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed