Experiment Report

Start of automated test report 2023-04-30 00:10:59
Author=UNKNOWN@workstation obo Luke Vassallo

Machine Information

sysname=Linux
nodename=workstation
release=5.19.0-40-generic
version=#41~22.04.1-Ubuntu SMP PREEMPT_DYNAMIC Fri Mar 31 16:00:14 UTC 2
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz
CPU cores : 8
CPU base clock : 3.8000 GHz
CPU boost clock : 3.7920 GHz
System Memory : 31.35GB
Nvidia driver version : 525.105.17
Device 0 : NVIDIA GeForce GTX 1080
Device 0 : 8.0GB

Library Information

python : 3.8.16
torch : 1.13.1+cu117
optuna : 3.1.0
numpy : 1.23.3
pandas : 1.5.3
matplotlib : 3.7.1
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

ablation_experiment_055:1682487597_0

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	36.66	34.87	33.6	30.87
voltage_datalogger_adc0	trial_1	37.86	37.71	37.38	25.52
voltage_datalogger_adc0	trial_2	-	32.33	31.12	36.03
voltage_datalogger_adc0	trial_3	35.51	33.69	33.69	28.57
voltage_datalogger_adc2	trial_0	13.35	13.04	12.77	12.81
voltage_datalogger_adc2	trial_1	14.16	14.11	14.11	12.18
voltage_datalogger_adc2	trial_2	13.89	12.14	11.78	13.9
voltage_datalogger_adc2	trial_3	17.34	17.0	16.83	12.85
voltage_datalogger_afe	trial_0	57.42	53.42	51.9	49.34
voltage_datalogger_afe	trial_1	-	70.54	66.69	49.26
voltage_datalogger_afe	trial_2	56.38	53.23	52.55	45.1
voltage_datalogger_afe	trial_3	-	60.27	57.89	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_0	36.68 ± 0.96 (3)	34.65 ± 1.98 (4)	33.95 ± 2.23 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487597_0	14.68 ± 1.56 (4)	14.07 ± 1.83 (4)	13.87 ± 1.9 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487597_0	56.9 ± 0.52 (2)	59.36 ± 7.05 (4)	57.26 ± 5.92 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	39.75	41.2	38.11	58.96
voltage_datalogger_adc0	trial_1	50.9	50.52	51.88	25.98
voltage_datalogger_adc0	trial_2	-	33.8	31.53	41.48
voltage_datalogger_adc0	trial_3	44.35	42.45	42.45	29.14
voltage_datalogger_adc2	trial_0	12.07	12.89	12.65	12.02
voltage_datalogger_adc2	trial_1	18.73	18.37	18.37	12.07
voltage_datalogger_adc2	trial_2	10.85	10.87	10.76	13.34
voltage_datalogger_adc2	trial_3	21.77	22.38	21.5	15.88
voltage_datalogger_afe	trial_0	64.55	53.28	55.6	77.93
voltage_datalogger_afe	trial_1	-	83.06	83.04	78.01
voltage_datalogger_afe	trial_2	59.02	64.76	60.24	76.72
voltage_datalogger_afe	trial_3	-	66.03	63.29	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_0	45.0 ± 4.58 (3)	41.99 ± 5.93 (4)	40.99 ± 7.39 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487597_0	15.86 ± 4.55 (4)	16.13 ± 4.53 (4)	15.82 ± 4.31 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487597_0	61.78 ± 2.76 (2)	66.78 ± 10.63 (4)	65.54 ± 10.47 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682487597_1

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	31.99	31.99	31.84	30.87
voltage_datalogger_adc0	trial_1	40.22	39.21	39.1	25.52
voltage_datalogger_adc0	trial_2	-	36.15	35.92	36.03
voltage_datalogger_adc0	trial_3	81.66	29.56	29.05	28.57
voltage_datalogger_adc2	trial_0	12.12	12.0	12.0	12.81
voltage_datalogger_adc2	trial_1	15.92	15.7	15.21	12.18
voltage_datalogger_adc2	trial_2	15.25	15.25	14.61	13.9
voltage_datalogger_adc2	trial_3	15.7	15.65	15.65	12.85
voltage_datalogger_afe	trial_0	62.15	57.67	57.67	49.34
voltage_datalogger_afe	trial_1	-	59.87	59.87	49.26
voltage_datalogger_afe	trial_2	58.14	55.93	55.93	45.1
voltage_datalogger_afe	trial_3	55.71	55.71	55.71	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_1	51.29 ± 21.74 (3)	34.23 ± 3.72 (4)	33.98 ± 3.84 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487597_1	14.75 ± 1.54 (4)	14.65 ± 1.54 (4)	14.37 ± 1.42 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487597_1	58.67 ± 2.66 (3)	57.3 ± 1.67 (4)	57.3 ± 1.67 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	34.1	34.1	35.39	58.96
voltage_datalogger_adc0	trial_1	52.47	44.36	44.25	25.98
voltage_datalogger_adc0	trial_2	-	41.01	45.34	41.48
voltage_datalogger_adc0	trial_3	97.47	32.4	37.08	29.14
voltage_datalogger_adc2	trial_0	10.55	10.59	10.59	12.02
voltage_datalogger_adc2	trial_1	18.93	18.57	18.13	12.07
voltage_datalogger_adc2	trial_2	15.89	15.89	15.49	13.34
voltage_datalogger_adc2	trial_3	19.12	18.88	18.88	15.88
voltage_datalogger_afe	trial_0	67.7	65.92	65.92	77.93
voltage_datalogger_afe	trial_1	-	68.54	68.54	78.01
voltage_datalogger_afe	trial_2	65.65	62.97	62.97	76.72
voltage_datalogger_afe	trial_3	67.24	67.24	67.24	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_1	61.35 ± 26.62 (3)	37.97 ± 4.9 (4)	40.52 ± 4.34 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487597_1	16.12 ± 3.46 (4)	15.98 ± 3.32 (4)	15.77 ± 3.25 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487597_1	66.86 ± 0.88 (3)	66.17 ± 2.07 (4)	66.17 ± 2.07 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682487597_2

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	47.26	43.3	43.07	30.87
voltage_datalogger_adc0	trial_1	40.41	39.14	38.03	25.52
voltage_datalogger_adc0	trial_2	49.32	47.32	46.05	36.03
voltage_datalogger_adc0	trial_3	43.34	43.34	40.72	28.57
voltage_datalogger_adc2	trial_0	13.51	13.26	13.24	12.81
voltage_datalogger_adc2	trial_1	15.39	14.51	14.2	12.18
voltage_datalogger_adc2	trial_2	12.7	12.32	12.16	13.9
voltage_datalogger_adc2	trial_3	17.06	14.83	14.7	12.85
voltage_datalogger_afe	trial_0	-	54.44	53.12	49.34
voltage_datalogger_afe	trial_1	49.27	49.27	48.28	49.26
voltage_datalogger_afe	trial_2	56.13	49.7	46.98	45.1
voltage_datalogger_afe	trial_3	58.14	52.41	50.74	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_2	45.08 ± 3.45 (4)	43.28 ± 2.89 (4)	41.97 ± 2.96 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487597_2	14.66 ± 1.69 (4)	13.73 ± 1.0 (4)	13.58 ± 0.97 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487597_2	54.51 ± 3.8 (3)	51.46 ± 2.1 (4)	49.78 ± 2.35 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	53.56	52.03	52.15	58.96
voltage_datalogger_adc0	trial_1	48.0	39.28	37.55	25.98
voltage_datalogger_adc0	trial_2	60.31	57.73	73.64	41.48
voltage_datalogger_adc0	trial_3	54.93	54.93	65.02	29.14
voltage_datalogger_adc2	trial_0	10.91	10.92	10.88	12.02
voltage_datalogger_adc2	trial_1	19.02	16.94	13.49	12.07
voltage_datalogger_adc2	trial_2	11.54	11.22	11.26	13.34
voltage_datalogger_adc2	trial_3	26.05	13.11	13.38	15.88
voltage_datalogger_afe	trial_0	-	75.24	78.38	77.93
voltage_datalogger_afe	trial_1	53.1	53.1	50.5	78.01
voltage_datalogger_afe	trial_2	61.34	52.91	50.99	76.72
voltage_datalogger_afe	trial_3	74.61	64.18	66.27	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_2	54.2 ± 4.38 (4)	50.99 ± 7.06 (4)	57.09 ± 13.63 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487597_2	16.88 ± 6.18 (4)	13.05 ± 2.4 (4)	12.25 ± 1.19 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487597_2	63.02 ± 8.86 (3)	61.36 ± 9.22 (4)	61.54 ± 11.61 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682487597_3

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	38.49	37.41	36.75	30.87
voltage_datalogger_adc0	trial_1	47.32	45.81	45.81	25.52
voltage_datalogger_adc0	trial_2	-	35.51	35.45	36.03
voltage_datalogger_adc0	trial_3	54.39	36.61	36.61	28.57
voltage_datalogger_adc2	trial_0	13.59	13.58	13.58	12.81
voltage_datalogger_adc2	trial_1	14.51	14.27	14.27	12.18
voltage_datalogger_adc2	trial_2	14.76	14.76	14.76	13.9
voltage_datalogger_adc2	trial_3	17.09	16.98	16.78	12.85
voltage_datalogger_afe	trial_0	67.89	59.66	58.38	49.34
voltage_datalogger_afe	trial_1	58.3	51.97	51.43	49.26
voltage_datalogger_afe	trial_2	59.94	58.75	56.45	45.1
voltage_datalogger_afe	trial_3	56.49	53.47	52.79	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_3	46.73 ± 6.5 (3)	38.83 ± 4.08 (4)	38.66 ± 4.16 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487597_3	14.99 ± 1.29 (4)	14.9 ± 1.27 (4)	14.85 ± 1.19 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487597_3	60.66 ± 4.35 (4)	55.96 ± 3.3 (4)	54.76 ± 2.78 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	52.59	57.42	47.58	58.96
voltage_datalogger_adc0	trial_1	57.99	57.18	57.18	25.98
voltage_datalogger_adc0	trial_2	-	43.07	42.37	41.48
voltage_datalogger_adc0	trial_3	78.33	47.52	47.52	29.14
voltage_datalogger_adc2	trial_0	15.3	15.08	15.08	12.02
voltage_datalogger_adc2	trial_1	12.05	12.05	12.05	12.07
voltage_datalogger_adc2	trial_2	15.37	17.67	17.67	13.34
voltage_datalogger_adc2	trial_3	22.76	22.6	22.17	15.88
voltage_datalogger_afe	trial_0	70.05	66.85	57.57	77.93
voltage_datalogger_afe	trial_1	65.59	58.74	57.14	78.01
voltage_datalogger_afe	trial_2	70.4	73.59	65.78	76.72
voltage_datalogger_afe	trial_3	61.73	75.64	71.94	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487597_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487597_3	62.97 ± 11.08 (3)	51.3 ± 6.21 (4)	48.66 ± 5.35 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487597_3	16.37 ± 3.93 (4)	16.85 ± 3.87 (4)	16.74 ± 3.71 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487597_3	66.94 ± 3.56 (4)	68.7 ± 6.61 (4)	63.11 ± 6.15 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682619637_0

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	38.01	35.76	35.76	30.87
voltage_datalogger_adc0	trial_1	-	35.09	31.18	25.52
voltage_datalogger_adc0	trial_2	32.78	31.52	29.5	36.03
voltage_datalogger_adc0	trial_3	-	32.25	31.88	28.57
voltage_datalogger_adc2	trial_0	14.06	11.38	10.8	12.81
voltage_datalogger_adc2	trial_1	12.08	11.58	11.24	12.18
voltage_datalogger_adc2	trial_2	11.71	11.7	11.63	13.9
voltage_datalogger_adc2	trial_3	13.41	11.9	11.41	12.85
voltage_datalogger_afe	trial_0	-	55.22	49.93	49.34
voltage_datalogger_afe	trial_1	54.35	54.35	53.54	49.26
voltage_datalogger_afe	trial_2	-	-	72.34	45.1
voltage_datalogger_afe	trial_3	59.12	57.0	51.99	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_0	35.39 ± 2.61 (2)	33.66 ± 1.8 (4)	32.08 ± 2.29 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682619637_0	12.82 ± 0.96 (4)	11.64 ± 0.19 (4)	11.27 ± 0.3 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682619637_0	56.74 ± 2.38 (2)	55.52 ± 1.1 (3)	56.95 ± 8.98 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	35.72	35.93	35.93	58.96
voltage_datalogger_adc0	trial_1	-	46.23	42.61	25.98
voltage_datalogger_adc0	trial_2	40.96	37.92	36.96	41.48
voltage_datalogger_adc0	trial_3	-	56.0	52.01	29.14
voltage_datalogger_adc2	trial_0	17.33	13.57	10.54	12.02
voltage_datalogger_adc2	trial_1	11.41	10.89	10.7	12.07
voltage_datalogger_adc2	trial_2	14.64	14.58	13.46	13.34
voltage_datalogger_adc2	trial_3	12.52	11.07	10.39	15.88
voltage_datalogger_afe	trial_0	-	54.27	50.07	77.93
voltage_datalogger_afe	trial_1	73.82	73.82	71.26	78.01
voltage_datalogger_afe	trial_2	-	-	104.28	76.72
voltage_datalogger_afe	trial_3	64.93	65.31	57.08	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_0	38.34 ± 2.62 (2)	44.02 ± 7.92 (4)	41.88 ± 6.38 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682619637_0	13.97 ± 2.26 (4)	12.53 ± 1.59 (4)	11.27 ± 1.27 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682619637_0	69.38 ± 4.44 (2)	64.47 ± 8.0 (3)	70.67 ± 20.85 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682619637_1

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	32.57	31.83	30.87
voltage_datalogger_adc0	trial_1	43.56	41.24	41.24	25.52
voltage_datalogger_adc0	trial_2	51.36	34.77	33.86	36.03
voltage_datalogger_adc0	trial_3	30.96	27.52	26.62	28.57
voltage_datalogger_adc2	trial_0	12.06	11.46	11.37	12.81
voltage_datalogger_adc2	trial_1	14.89	14.58	14.05	12.18
voltage_datalogger_adc2	trial_2	12.5	11.35	11.23	13.9
voltage_datalogger_adc2	trial_3	17.27	16.99	16.58	12.85
voltage_datalogger_afe	trial_0	-	-	47.82	49.34
voltage_datalogger_afe	trial_1	-	-	50.12	49.26
voltage_datalogger_afe	trial_2	51.97	46.17	45.95	45.1
voltage_datalogger_afe	trial_3	47.23	47.23	46.43	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_1	41.96 ± 8.4 (3)	34.03 ± 4.93 (4)	33.39 ± 5.25 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682619637_1	14.18 ± 2.08 (4)	13.6 ± 2.35 (4)	13.31 ± 2.2 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682619637_1	49.6 ± 2.37 (2)	46.7 ± 0.53 (2)	47.58 ± 1.62 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	40.68	36.02	58.96
voltage_datalogger_adc0	trial_1	47.0	46.84	46.84	25.98
voltage_datalogger_adc0	trial_2	59.35	51.26	57.75	41.48
voltage_datalogger_adc0	trial_3	41.0	31.69	31.1	29.14
voltage_datalogger_adc2	trial_0	10.79	10.05	10.09	12.02
voltage_datalogger_adc2	trial_1	13.67	13.17	12.75	12.07
voltage_datalogger_adc2	trial_2	11.79	10.49	10.09	13.34
voltage_datalogger_adc2	trial_3	22.06	22.1	21.31	15.88
voltage_datalogger_afe	trial_0	-	-	51.81	77.93
voltage_datalogger_afe	trial_1	-	-	73.37	78.01
voltage_datalogger_afe	trial_2	63.48	55.98	53.19	76.72
voltage_datalogger_afe	trial_3	61.57	61.57	49.37	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_1	49.12 ± 7.64 (3)	42.62 ± 7.34 (4)	42.93 ± 10.28 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682619637_1	14.58 ± 4.44 (4)	13.95 ± 4.85 (4)	13.56 ± 4.6 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682619637_1	62.52 ± 0.95 (2)	58.78 ± 2.8 (2)	56.94 ± 9.59 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682619637_2

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	44.11	36.19	30.87
voltage_datalogger_adc0	trial_1	36.17	34.4	31.26	25.52
voltage_datalogger_adc0	trial_2	-	36.5	33.11	36.03
voltage_datalogger_adc0	trial_3	-	31.97	28.77	28.57
voltage_datalogger_adc2	trial_0	12.42	12.22	12.22	12.81
voltage_datalogger_adc2	trial_1	15.18	14.86	14.55	12.18
voltage_datalogger_adc2	trial_2	13.47	13.35	13.35	13.9
voltage_datalogger_adc2	trial_3	14.88	14.82	14.82	12.85
voltage_datalogger_afe	trial_0	49.98	47.9	47.55	49.34
voltage_datalogger_afe	trial_1	-	54.1	53.61	49.26
voltage_datalogger_afe	trial_2	-	54.86	51.91	45.1
voltage_datalogger_afe	trial_3	62.33	59.04	55.77	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_2	36.17 ± 0.0 (1)	36.74 ± 4.54 (4)	32.33 ± 2.71 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682619637_2	13.99 ± 1.11 (4)	13.81 ± 1.1 (4)	13.74 ± 1.04 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682619637_2	56.16 ± 6.18 (2)	53.98 ± 3.98 (4)	52.21 ± 3.02 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	53.57	38.79	58.96
voltage_datalogger_adc0	trial_1	38.12	35.69	49.26	25.98
voltage_datalogger_adc0	trial_2	-	34.39	35.12	41.48
voltage_datalogger_adc0	trial_3	-	59.55	34.85	29.14
voltage_datalogger_adc2	trial_0	11.09	10.83	10.83	12.02
voltage_datalogger_adc2	trial_1	17.75	18.48	17.47	12.07
voltage_datalogger_adc2	trial_2	15.29	12.84	12.84	13.34
voltage_datalogger_adc2	trial_3	18.14	17.94	17.79	15.88
voltage_datalogger_afe	trial_0	47.86	45.18	45.64	77.93
voltage_datalogger_afe	trial_1	-	70.22	57.39	78.01
voltage_datalogger_afe	trial_2	-	60.38	69.46	76.72
voltage_datalogger_afe	trial_3	71.25	71.32	68.77	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_2	38.12 ± 0.0 (1)	45.8 ± 10.98 (4)	39.5 ± 5.84 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682619637_2	15.57 ± 2.81 (4)	15.02 ± 3.27 (4)	14.73 ± 2.99 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682619637_2	59.56 ± 11.7 (2)	61.78 ± 10.49 (4)	60.32 ± 9.73 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_055:1682619637_3

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 5.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	41.69	40.46	39.23	30.87
voltage_datalogger_adc0	trial_1	44.97	43.47	43.11	25.52
voltage_datalogger_adc0	trial_2	39.37	35.33	35.01	36.03
voltage_datalogger_adc0	trial_3	-	48.72	48.14	28.57
voltage_datalogger_adc2	trial_0	12.21	12.21	12.18	12.81
voltage_datalogger_adc2	trial_1	15.65	15.43	14.81	12.18
voltage_datalogger_adc2	trial_2	14.19	13.48	12.98	13.9
voltage_datalogger_adc2	trial_3	17.19	17.18	17.18	12.85
voltage_datalogger_afe	trial_0	53.39	51.97	51.69	49.34
voltage_datalogger_afe	trial_1	54.98	49.66	49.66	49.26
voltage_datalogger_afe	trial_2	58.34	55.71	55.56	45.1
voltage_datalogger_afe	trial_3	67.82	51.18	50.02	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_3	42.01 ± 2.3 (3)	42.0 ± 4.85 (4)	41.37 ± 4.84 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682619637_3	14.81 ± 1.84 (4)	14.58 ± 1.89 (4)	14.29 ± 1.92 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682619637_3	58.63 ± 5.6 (4)	52.13 ± 2.23 (4)	51.73 ± 2.34 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	39.81	38.71	50.94	58.96
voltage_datalogger_adc0	trial_1	53.15	56.18	57.54	25.98
voltage_datalogger_adc0	trial_2	49.03	42.33	33.55	41.48
voltage_datalogger_adc0	trial_3	-	63.7	63.16	29.14
voltage_datalogger_adc2	trial_0	11.22	11.22	10.95	12.02
voltage_datalogger_adc2	trial_1	14.34	17.75	13.43	12.07
voltage_datalogger_adc2	trial_2	14.92	14.58	13.72	13.34
voltage_datalogger_adc2	trial_3	15.22	21.14	21.14	15.88
voltage_datalogger_afe	trial_0	57.21	56.78	49.02	77.93
voltage_datalogger_afe	trial_1	60.25	65.0	65.0	78.01
voltage_datalogger_afe	trial_2	55.33	75.96	67.99	76.72
voltage_datalogger_afe	trial_3	71.87	56.08	55.08	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682619637_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682619637_3	47.33 ± 5.58 (3)	50.23 ± 10.15 (4)	51.3 ± 11.12 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682619637_3	13.92 ± 1.59 (4)	16.17 ± 3.68 (4)	14.81 ± 3.81 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682619637_3	61.17 ± 6.43 (4)	63.46 ± 8.03 (4)	59.27 ± 7.61 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682487601_0

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	81.59	81.59	81.59	36.03
voltage_datalogger_adc0	trial_3	81.83	81.83	81.83	28.57
voltage_datalogger_adc2	trial_0	35.08	35.08	35.08	12.81
voltage_datalogger_adc2	trial_1	-	-	28.62	12.18
voltage_datalogger_adc2	trial_2	26.02	26.02	26.02	13.9
voltage_datalogger_adc2	trial_3	24.05	24.05	24.05	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	98.02	98.02	98.02	45.1
voltage_datalogger_afe	trial_3	97.25	97.25	97.25	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_0	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487601_0	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487601_0	97.64 ± 0.38 (2)	97.64 ± 0.38 (2)	97.64 ± 0.38 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	92.68	92.68	92.68	41.48
voltage_datalogger_adc0	trial_3	96.93	96.93	96.93	29.14
voltage_datalogger_adc2	trial_0	28.52	28.52	28.52	12.02
voltage_datalogger_adc2	trial_1	-	-	34.5	12.07
voltage_datalogger_adc2	trial_2	21.81	21.81	21.81	13.34
voltage_datalogger_adc2	trial_3	30.96	30.96	30.96	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	129.71	129.71	129.71	76.72
voltage_datalogger_afe	trial_3	122.94	122.94	122.94	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_0	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487601_0	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487601_0	126.32 ± 3.39 (2)	126.32 ± 3.39 (2)	126.32 ± 3.39 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682487601_1

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	81.59	81.59	81.59	36.03
voltage_datalogger_adc0	trial_3	81.83	81.83	81.83	28.57
voltage_datalogger_adc2	trial_0	35.08	35.08	35.08	12.81
voltage_datalogger_adc2	trial_1	-	-	28.62	12.18
voltage_datalogger_adc2	trial_2	26.02	26.02	26.02	13.9
voltage_datalogger_adc2	trial_3	24.05	24.05	24.05	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	97.19	97.19	97.19	45.1
voltage_datalogger_afe	trial_3	97.25	97.25	97.25	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_1	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487601_1	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487601_1	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	92.68	92.68	92.68	41.48
voltage_datalogger_adc0	trial_3	96.93	96.93	96.93	29.14
voltage_datalogger_adc2	trial_0	28.52	28.52	28.52	12.02
voltage_datalogger_adc2	trial_1	-	-	34.5	12.07
voltage_datalogger_adc2	trial_2	21.81	21.81	21.81	13.34
voltage_datalogger_adc2	trial_3	30.96	30.96	30.96	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	120.97	120.97	120.97	76.72
voltage_datalogger_afe	trial_3	122.94	122.94	122.94	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_1	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487601_1	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487601_1	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682487601_2

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	40.46	39.26	39.04	30.87
voltage_datalogger_adc0	trial_1	53.36	52.46	50.81	25.52
voltage_datalogger_adc0	trial_2	39.44	38.59	38.59	36.03
voltage_datalogger_adc0	trial_3	39.52	38.62	38.62	28.57
voltage_datalogger_adc2	trial_0	14.36	14.36	14.36	12.81
voltage_datalogger_adc2	trial_1	15.3	14.76	14.35	12.18
voltage_datalogger_adc2	trial_2	14.96	14.96	14.96	13.9
voltage_datalogger_adc2	trial_3	17.28	16.98	16.86	12.85
voltage_datalogger_afe	trial_0	60.15	57.85	57.43	49.34
voltage_datalogger_afe	trial_1	67.06	65.42	64.65	49.26
voltage_datalogger_afe	trial_2	69.27	62.48	61.55	45.1
voltage_datalogger_afe	trial_3	65.41	62.88	61.4	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_2	43.2 ± 5.88 (4)	42.23 ± 5.91 (4)	41.76 ± 5.23 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487601_2	15.48 ± 1.1 (4)	15.26 ± 1.01 (4)	15.13 ± 1.03 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487601_2	65.47 ± 3.36 (4)	62.16 ± 2.73 (4)	61.26 ± 2.56 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	41.57	39.8	40.01	58.96
voltage_datalogger_adc0	trial_1	54.62	65.96	53.17	25.98
voltage_datalogger_adc0	trial_2	43.16	42.31	42.31	41.48
voltage_datalogger_adc0	trial_3	40.2	42.06	42.06	29.14
voltage_datalogger_adc2	trial_0	11.3	11.3	11.3	12.02
voltage_datalogger_adc2	trial_1	13.81	13.33	13.04	12.07
voltage_datalogger_adc2	trial_2	15.72	15.72	15.72	13.34
voltage_datalogger_adc2	trial_3	21.37	21.18	23.59	15.88
voltage_datalogger_afe	trial_0	74.07	68.14	69.53	77.93
voltage_datalogger_afe	trial_1	87.83	82.32	82.27	78.01
voltage_datalogger_afe	trial_2	109.65	70.09	68.63	76.72
voltage_datalogger_afe	trial_3	72.46	82.44	77.12	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_2	44.89 ± 5.72 (4)	47.53 ± 10.68 (4)	44.39 ± 5.15 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487601_2	15.55 ± 3.71 (4)	15.38 ± 3.69 (4)	15.91 ± 4.7 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487601_2	86.0 ± 14.9 (4)	75.75 ± 6.67 (4)	74.39 ± 5.62 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682487601_3

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	35.33	33.59	33.59	30.87
voltage_datalogger_adc0	trial_1	44.96	44.96	44.51	25.52
voltage_datalogger_adc0	trial_2	42.54	39.61	39.61	36.03
voltage_datalogger_adc0	trial_3	44.13	43.05	42.43	28.57
voltage_datalogger_adc2	trial_0	14.44	14.43	14.43	12.81
voltage_datalogger_adc2	trial_1	16.5	16.5	16.5	12.18
voltage_datalogger_adc2	trial_2	16.75	16.75	16.75	13.9
voltage_datalogger_adc2	trial_3	15.51	14.41	14.41	12.85
voltage_datalogger_afe	trial_0	66.77	64.05	60.86	49.34
voltage_datalogger_afe	trial_1	71.98	71.4	71.4	49.26
voltage_datalogger_afe	trial_2	72.43	69.78	69.78	45.1
voltage_datalogger_afe	trial_3	61.23	60.7	60.22	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_3	41.74 ± 3.8 (4)	40.3 ± 4.32 (4)	40.03 ± 4.11 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487601_3	15.8 ± 0.91 (4)	15.52 ± 1.11 (4)	15.52 ± 1.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487601_3	68.1 ± 4.55 (4)	66.48 ± 4.31 (4)	65.56 ± 5.06 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	34.36	32.49	32.49	58.96
voltage_datalogger_adc0	trial_1	60.96	60.96	60.48	25.98
voltage_datalogger_adc0	trial_2	46.64	55.49	55.49	41.48
voltage_datalogger_adc0	trial_3	56.35	56.23	58.99	29.14
voltage_datalogger_adc2	trial_0	11.24	11.24	11.24	12.02
voltage_datalogger_adc2	trial_1	20.84	20.84	20.84	12.07
voltage_datalogger_adc2	trial_2	17.5	17.5	17.5	13.34
voltage_datalogger_adc2	trial_3	18.53	19.24	19.24	15.88
voltage_datalogger_afe	trial_0	91.17	76.75	71.68	77.93
voltage_datalogger_afe	trial_1	90.87	88.87	88.87	78.01
voltage_datalogger_afe	trial_2	87.43	78.17	78.17	76.72
voltage_datalogger_afe	trial_3	72.23	65.8	59.52	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487601_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487601_3	49.58 ± 10.19 (4)	51.29 ± 11.06 (4)	51.86 ± 11.33 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487601_3	17.03 ± 3.55 (4)	17.2 ± 3.64 (4)	17.2 ± 3.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487601_3	85.43 ± 7.76 (4)	77.4 ± 8.17 (4)	74.56 ± 10.63 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682622818_0

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	35.87	35.5	35.5	30.87
voltage_datalogger_adc0	trial_1	56.14	53.25	52.88	25.52
voltage_datalogger_adc0	trial_2	42.09	41.07	40.94	36.03
voltage_datalogger_adc0	trial_3	56.02	56.02	56.02	28.57
voltage_datalogger_adc2	trial_0	20.42	20.42	20.42	12.81
voltage_datalogger_adc2	trial_1	20.47	20.47	20.47	12.18
voltage_datalogger_adc2	trial_2	17.86	17.86	17.86	13.9
voltage_datalogger_adc2	trial_3	17.73	17.73	17.73	12.85
voltage_datalogger_afe	trial_0	55.48	54.72	54.72	49.34
voltage_datalogger_afe	trial_1	59.24	59.24	58.58	49.26
voltage_datalogger_afe	trial_2	62.81	62.81	61.37	45.1
voltage_datalogger_afe	trial_3	65.33	65.24	65.24	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_0	47.53 ± 8.83 (4)	46.46 ± 8.47 (4)	46.34 ± 8.41 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622818_0	19.12 ± 1.33 (4)	19.12 ± 1.33 (4)	19.12 ± 1.33 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622818_0	60.72 ± 3.72 (4)	60.5 ± 3.96 (4)	59.98 ± 3.85 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	36.46	35.85	35.85	58.96
voltage_datalogger_adc0	trial_1	69.32	54.89	55.06	25.98
voltage_datalogger_adc0	trial_2	52.13	50.02	52.28	41.48
voltage_datalogger_adc0	trial_3	67.75	67.75	67.75	29.14
voltage_datalogger_adc2	trial_0	21.26	21.26	21.26	12.02
voltage_datalogger_adc2	trial_1	25.12	25.12	25.12	12.07
voltage_datalogger_adc2	trial_2	18.49	18.49	18.49	13.34
voltage_datalogger_adc2	trial_3	20.49	20.49	20.49	15.88
voltage_datalogger_afe	trial_0	55.03	55.24	55.24	77.93
voltage_datalogger_afe	trial_1	67.58	67.58	67.34	78.01
voltage_datalogger_afe	trial_2	67.29	67.29	78.52	76.72
voltage_datalogger_afe	trial_3	79.12	78.58	78.58	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_0	56.42 ± 13.34 (4)	52.13 ± 11.41 (4)	52.74 ± 11.36 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622818_0	21.34 ± 2.41 (4)	21.34 ± 2.41 (4)	21.34 ± 2.41 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622818_0	67.26 ± 8.52 (4)	67.17 ± 8.26 (4)	69.92 ± 9.63 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682622818_1

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	60.6	34.87	34.7	30.87
voltage_datalogger_adc0	trial_1	45.75	43.48	43.26	25.52
voltage_datalogger_adc0	trial_2	36.9	36.05	36.05	36.03
voltage_datalogger_adc0	trial_3	45.75	41.77	41.77	28.57
voltage_datalogger_adc2	trial_0	15.03	14.97	14.97	12.81
voltage_datalogger_adc2	trial_1	16.28	15.5	15.5	12.18
voltage_datalogger_adc2	trial_2	12.77	12.62	12.62	13.9
voltage_datalogger_adc2	trial_3	16.41	16.38	16.38	12.85
voltage_datalogger_afe	trial_0	60.07	59.09	58.71	49.34
voltage_datalogger_afe	trial_1	57.76	55.12	54.13	49.26
voltage_datalogger_afe	trial_2	62.64	62.12	60.92	45.1
voltage_datalogger_afe	trial_3	91.69	83.8	77.04	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_1	47.25 ± 8.51 (4)	39.04 ± 3.66 (4)	38.94 ± 3.64 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622818_1	15.12 ± 1.46 (4)	14.87 ± 1.39 (4)	14.87 ± 1.39 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622818_1	68.04 ± 13.76 (4)	65.03 ± 11.12 (4)	62.7 ± 8.63 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	66.94	39.04	39.05	58.96
voltage_datalogger_adc0	trial_1	67.22	67.43	67.36	25.98
voltage_datalogger_adc0	trial_2	40.78	41.82	41.82	41.48
voltage_datalogger_adc0	trial_3	61.6	51.19	52.39	29.14
voltage_datalogger_adc2	trial_0	13.47	13.37	13.37	12.02
voltage_datalogger_adc2	trial_1	19.25	18.18	18.18	12.07
voltage_datalogger_adc2	trial_2	11.55	11.55	11.55	13.34
voltage_datalogger_adc2	trial_3	25.09	25.19	25.19	15.88
voltage_datalogger_afe	trial_0	78.66	79.98	79.64	77.93
voltage_datalogger_afe	trial_1	75.83	72.7	53.43	78.01
voltage_datalogger_afe	trial_2	90.82	78.93	81.41	76.72
voltage_datalogger_afe	trial_3	116.33	87.57	82.6	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_1	59.14 ± 10.83 (4)	49.87 ± 11.09 (4)	50.16 ± 11.11 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622818_1	17.34 ± 5.3 (4)	17.07 ± 5.28 (4)	17.07 ± 5.28 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622818_1	90.41 ± 15.99 (4)	79.8 ± 5.28 (4)	74.27 ± 12.08 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682622818_2

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	52.59	47.26	47.26	30.87
voltage_datalogger_adc0	trial_1	52.26	46.07	45.66	25.52
voltage_datalogger_adc0	trial_2	53.12	47.71	46.67	36.03
voltage_datalogger_adc0	trial_3	-	52.62	52.62	28.57
voltage_datalogger_adc2	trial_0	17.97	17.97	17.97	12.81
voltage_datalogger_adc2	trial_1	15.2	14.86	14.86	12.18
voltage_datalogger_adc2	trial_2	12.23	12.23	12.23	13.9
voltage_datalogger_adc2	trial_3	18.38	17.91	17.5	12.85
voltage_datalogger_afe	trial_0	60.18	51.16	51.11	49.34
voltage_datalogger_afe	trial_1	72.38	59.91	57.61	49.26
voltage_datalogger_afe	trial_2	52.83	48.74	47.98	45.1
voltage_datalogger_afe	trial_3	-	73.33	73.33	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_2	52.66 ± 0.35 (3)	48.42 ± 2.5 (4)	48.05 ± 2.7 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622818_2	15.94 ± 2.47 (4)	15.74 ± 2.39 (4)	15.64 ± 2.3 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622818_2	61.8 ± 8.06 (3)	58.28 ± 9.63 (4)	57.51 ± 9.77 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	68.91	53.37	53.37	58.96
voltage_datalogger_adc0	trial_1	69.93	54.69	55.8	25.98
voltage_datalogger_adc0	trial_2	54.33	70.25	64.88	41.48
voltage_datalogger_adc0	trial_3	-	73.11	73.11	29.14
voltage_datalogger_adc2	trial_0	16.98	16.98	16.98	12.02
voltage_datalogger_adc2	trial_1	18.44	18.32	18.32	12.07
voltage_datalogger_adc2	trial_2	11.49	11.49	11.49	13.34
voltage_datalogger_adc2	trial_3	22.83	23.6	22.76	15.88
voltage_datalogger_afe	trial_0	67.11	49.94	52.47	77.93
voltage_datalogger_afe	trial_1	75.4	73.76	63.44	78.01
voltage_datalogger_afe	trial_2	73.86	51.99	52.24	76.72
voltage_datalogger_afe	trial_3	-	90.04	90.04	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_2	64.39 ± 7.13 (3)	62.86 ± 8.89 (4)	61.79 ± 7.82 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622818_2	17.44 ± 4.05 (4)	17.6 ± 4.31 (4)	17.39 ± 4.02 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622818_2	72.12 ± 3.6 (3)	66.43 ± 16.52 (4)	64.55 ± 15.4 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_028:1682622818_3

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 2.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	45.29	45.03	45.03	30.87
voltage_datalogger_adc0	trial_1	45.97	43.17	43.17	25.52
voltage_datalogger_adc0	trial_2	41.88	41.75	41.75	36.03
voltage_datalogger_adc0	trial_3	63.03	60.21	59.77	28.57
voltage_datalogger_adc2	trial_0	15.28	15.28	15.28	12.81
voltage_datalogger_adc2	trial_1	16.61	16.59	16.59	12.18
voltage_datalogger_adc2	trial_2	13.04	13.03	13.03	13.9
voltage_datalogger_adc2	trial_3	16.99	16.99	16.99	12.85
voltage_datalogger_afe	trial_0	65.03	53.88	53.88	49.34
voltage_datalogger_afe	trial_1	54.2	53.81	53.81	49.26
voltage_datalogger_afe	trial_2	62.35	61.43	61.02	45.1
voltage_datalogger_afe	trial_3	63.03	60.86	60.31	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_3	49.04 ± 8.22 (4)	47.54 ± 7.41 (4)	47.43 ± 7.22 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622818_3	15.48 ± 1.55 (4)	15.47 ± 1.55 (4)	15.47 ± 1.55 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622818_3	61.15 ± 4.13 (4)	57.5 ± 3.66 (4)	57.26 ± 3.42 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	67.92	68.22	68.22	58.96
voltage_datalogger_adc0	trial_1	57.17	58.26	58.26	25.98
voltage_datalogger_adc0	trial_2	45.14	45.05	45.05	41.48
voltage_datalogger_adc0	trial_3	68.12	70.49	69.74	29.14
voltage_datalogger_adc2	trial_0	13.46	13.46	13.46	12.02
voltage_datalogger_adc2	trial_1	19.47	19.47	19.47	12.07
voltage_datalogger_adc2	trial_2	12.19	12.19	12.19	13.34
voltage_datalogger_adc2	trial_3	20.03	20.03	20.03	15.88
voltage_datalogger_afe	trial_0	74.03	71.32	71.32	77.93
voltage_datalogger_afe	trial_1	67.95	67.21	67.21	78.01
voltage_datalogger_afe	trial_2	76.65	75.85	75.51	76.72
voltage_datalogger_afe	trial_3	76.51	79.97	79.62	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622818_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622818_3	59.59 ± 9.44 (4)	60.5 ± 10.04 (4)	60.32 ± 9.86 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622818_3	16.29 ± 3.5 (4)	16.29 ± 3.5 (4)	16.29 ± 3.5 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622818_3	73.79 ± 3.53 (4)	73.59 ± 4.79 (4)	73.41 ± 4.63 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682487599_0

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	81.59	81.59	81.59	36.03
voltage_datalogger_adc0	trial_3	81.83	81.83	81.83	28.57
voltage_datalogger_adc2	trial_0	35.08	35.08	35.08	12.81
voltage_datalogger_adc2	trial_1	-	-	28.62	12.18
voltage_datalogger_adc2	trial_2	26.02	26.02	26.02	13.9
voltage_datalogger_adc2	trial_3	24.05	24.05	24.05	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	97.19	97.19	97.19	45.1
voltage_datalogger_afe	trial_3	97.25	97.25	97.25	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_0	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487599_0	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487599_0	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	92.68	92.68	92.68	41.48
voltage_datalogger_adc0	trial_3	96.93	96.93	96.93	29.14
voltage_datalogger_adc2	trial_0	28.52	28.52	28.52	12.02
voltage_datalogger_adc2	trial_1	-	-	34.5	12.07
voltage_datalogger_adc2	trial_2	21.81	21.81	21.81	13.34
voltage_datalogger_adc2	trial_3	30.96	30.96	30.96	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	120.97	120.97	120.97	76.72
voltage_datalogger_afe	trial_3	122.94	122.94	122.94	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_0	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487599_0	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487599_0	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682487599_1

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	29.79	28.4	27.67	30.87
voltage_datalogger_adc0	trial_1	-	34.78	33.69	25.52
voltage_datalogger_adc0	trial_2	-	-	29.51	36.03
voltage_datalogger_adc0	trial_3	-	33.73	32.72	28.57
voltage_datalogger_adc2	trial_0	12.17	11.43	10.94	12.81
voltage_datalogger_adc2	trial_1	16.93	14.89	14.71	12.18
voltage_datalogger_adc2	trial_2	13.72	13.39	13.39	13.9
voltage_datalogger_adc2	trial_3	16.79	16.01	15.31	12.85
voltage_datalogger_afe	trial_0	-	44.44	44.44	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	44.12	44.12	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_1	29.79 ± 0.0 (1)	32.3 ± 2.79 (3)	30.9 ± 2.42 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487599_1	14.9 ± 2.03 (4)	13.93 ± 1.72 (4)	13.59 ± 1.68 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487599_1	nan ± nan (0)	44.28 ± 0.16 (2)	44.28 ± 0.16 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	28.98	31.07	26.84	58.96
voltage_datalogger_adc0	trial_1	-	52.0	50.83	25.98
voltage_datalogger_adc0	trial_2	-	-	39.0	41.48
voltage_datalogger_adc0	trial_3	-	42.39	37.13	29.14
voltage_datalogger_adc2	trial_0	10.89	10.25	9.83	12.02
voltage_datalogger_adc2	trial_1	19.66	20.72	19.8	12.07
voltage_datalogger_adc2	trial_2	12.1	12.3	12.3	13.34
voltage_datalogger_adc2	trial_3	19.45	19.92	18.33	15.88
voltage_datalogger_afe	trial_0	-	47.03	47.03	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	44.89	44.89	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_1	28.98 ± 0.0 (1)	41.82 ± 8.55 (3)	38.45 ± 8.52 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487599_1	15.52 ± 4.05 (4)	15.8 ± 4.59 (4)	15.07 ± 4.13 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487599_1	nan ± nan (0)	45.96 ± 1.07 (2)	45.96 ± 1.07 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682487599_2

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	31.82	30.63	30.87
voltage_datalogger_adc0	trial_1	-	-	27.32	25.52
voltage_datalogger_adc0	trial_2	31.78	31.78	28.85	36.03
voltage_datalogger_adc0	trial_3	-	32.93	32.19	28.57
voltage_datalogger_adc2	trial_0	11.93	11.6	11.25	12.81
voltage_datalogger_adc2	trial_1	15.71	14.44	13.77	12.18
voltage_datalogger_adc2	trial_2	12.61	12.19	11.37	13.9
voltage_datalogger_adc2	trial_3	15.1	14.84	13.9	12.85
voltage_datalogger_afe	trial_0	47.92	47.92	47.92	49.34
voltage_datalogger_afe	trial_1	46.08	46.08	44.45	49.26
voltage_datalogger_afe	trial_2	-	-	42.63	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_2	31.78 ± 0.0 (1)	32.18 ± 0.53 (3)	29.75 ± 1.83 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487599_2	13.84 ± 1.6 (4)	13.27 ± 1.4 (4)	12.57 ± 1.26 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487599_2	47.0 ± 0.92 (2)	47.0 ± 0.92 (2)	45.0 ± 2.19 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	33.42	29.22	58.96
voltage_datalogger_adc0	trial_1	-	-	27.61	25.98
voltage_datalogger_adc0	trial_2	36.56	36.56	35.47	41.48
voltage_datalogger_adc0	trial_3	-	33.61	35.59	29.14
voltage_datalogger_adc2	trial_0	10.59	10.25	9.79	12.02
voltage_datalogger_adc2	trial_1	15.56	13.34	12.8	12.07
voltage_datalogger_adc2	trial_2	12.02	11.42	9.25	13.34
voltage_datalogger_adc2	trial_3	17.89	17.6	12.75	15.88
voltage_datalogger_afe	trial_0	48.63	48.63	48.63	77.93
voltage_datalogger_afe	trial_1	53.01	53.01	54.69	78.01
voltage_datalogger_afe	trial_2	-	-	49.14	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_2	36.56 ± 0.0 (1)	34.53 ± 1.44 (3)	31.97 ± 3.6 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487599_2	14.02 ± 2.88 (4)	13.15 ± 2.79 (4)	11.15 ± 1.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487599_2	50.82 ± 2.19 (2)	50.82 ± 2.19 (2)	50.82 ± 2.74 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682487599_3

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	81.59	81.59	81.59	36.03
voltage_datalogger_adc0	trial_3	81.83	81.83	81.83	28.57
voltage_datalogger_adc2	trial_0	35.08	35.08	35.08	12.81
voltage_datalogger_adc2	trial_1	-	-	28.62	12.18
voltage_datalogger_adc2	trial_2	26.02	26.02	26.02	13.9
voltage_datalogger_adc2	trial_3	24.05	24.05	24.05	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	97.19	97.19	97.19	45.1
voltage_datalogger_afe	trial_3	97.25	97.25	97.25	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_3	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	81.71 ± 0.12 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487599_3	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487599_3	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	97.22 ± 0.03 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	92.68	92.68	92.68	41.48
voltage_datalogger_adc0	trial_3	96.93	96.93	96.93	29.14
voltage_datalogger_adc2	trial_0	28.52	28.52	28.52	12.02
voltage_datalogger_adc2	trial_1	-	-	34.5	12.07
voltage_datalogger_adc2	trial_2	21.81	21.81	21.81	13.34
voltage_datalogger_adc2	trial_3	30.96	30.96	30.96	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	120.97	120.97	120.97	76.72
voltage_datalogger_afe	trial_3	122.94	122.94	122.94	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487599_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487599_3	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	94.8 ± 2.12 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487599_3	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487599_3	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	121.96 ± 0.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682622426_0

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	33.07	29.14	30.87
voltage_datalogger_adc0	trial_1	-	-	24.57	25.52
voltage_datalogger_adc0	trial_2	24.22	24.16	23.11	36.03
voltage_datalogger_adc0	trial_3	-	-	31.38	28.57
voltage_datalogger_adc2	trial_0	17.1	11.45	10.93	12.81
voltage_datalogger_adc2	trial_1	15.73	15.02	13.91	12.18
voltage_datalogger_adc2	trial_2	15.92	12.14	11.17	13.9
voltage_datalogger_adc2	trial_3	14.64	14.55	14.37	12.85
voltage_datalogger_afe	trial_0	-	50.79	50.79	49.34
voltage_datalogger_afe	trial_1	-	49.42	49.34	49.26
voltage_datalogger_afe	trial_2	-	-	49.75	45.1
voltage_datalogger_afe	trial_3	-	-	49.26	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_0	24.22 ± 0.0 (1)	28.62 ± 4.46 (2)	27.05 ± 3.35 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622426_0	15.85 ± 0.87 (4)	13.29 ± 1.52 (4)	12.6 ± 1.56 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622426_0	nan ± nan (0)	50.1 ± 0.68 (2)	49.78 ± 0.61 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	30.96	27.89	58.96
voltage_datalogger_adc0	trial_1	-	-	29.81	25.98
voltage_datalogger_adc0	trial_2	26.56	26.46	27.99	41.48
voltage_datalogger_adc0	trial_3	-	-	34.08	29.14
voltage_datalogger_adc2	trial_0	18.09	10.17	9.93	12.02
voltage_datalogger_adc2	trial_1	22.1	20.58	16.83	12.07
voltage_datalogger_adc2	trial_2	17.11	10.73	10.17	13.34
voltage_datalogger_adc2	trial_3	19.13	19.11	18.48	15.88
voltage_datalogger_afe	trial_0	-	52.38	52.38	77.93
voltage_datalogger_afe	trial_1	-	49.16	51.9	78.01
voltage_datalogger_afe	trial_2	-	-	72.6	76.72
voltage_datalogger_afe	trial_3	-	-	51.87	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_0	26.56 ± 0.0 (1)	28.71 ± 2.25 (2)	29.94 ± 2.51 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622426_0	19.11 ± 1.87 (4)	15.15 ± 4.73 (4)	13.85 ± 3.85 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622426_0	nan ± nan (0)	50.77 ± 1.61 (2)	57.19 ± 8.9 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682622426_1

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	34.31	33.79	30.87
voltage_datalogger_adc0	trial_1	-	45.66	45.66	25.52
voltage_datalogger_adc0	trial_2	-	-	29.0	36.03
voltage_datalogger_adc0	trial_3	-	34.13	31.66	28.57
voltage_datalogger_adc2	trial_0	14.67	14.4	14.4	12.81
voltage_datalogger_adc2	trial_1	17.34	16.64	15.99	12.18
voltage_datalogger_adc2	trial_2	11.79	11.65	11.65	13.9
voltage_datalogger_adc2	trial_3	16.25	15.84	15.51	12.85
voltage_datalogger_afe	trial_0	60.52	60.25	55.21	49.34
voltage_datalogger_afe	trial_1	69.41	56.57	53.27	49.26
voltage_datalogger_afe	trial_2	-	55.52	54.41	45.1
voltage_datalogger_afe	trial_3	-	61.81	52.23	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_1	nan ± nan (0)	38.03 ± 5.39 (3)	35.03 ± 6.37 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622426_1	15.01 ± 2.09 (4)	14.63 ± 1.9 (4)	14.39 ± 1.68 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622426_1	64.96 ± 4.44 (2)	58.54 ± 2.58 (4)	53.78 ± 1.13 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	42.78	42.62	58.96
voltage_datalogger_adc0	trial_1	-	44.17	44.17	25.98
voltage_datalogger_adc0	trial_2	-	-	29.37	41.48
voltage_datalogger_adc0	trial_3	-	31.56	32.61	29.14
voltage_datalogger_adc2	trial_0	16.77	16.77	16.77	12.02
voltage_datalogger_adc2	trial_1	22.47	20.93	21.66	12.07
voltage_datalogger_adc2	trial_2	10.25	10.29	10.29	13.34
voltage_datalogger_adc2	trial_3	15.47	19.78	14.23	15.88
voltage_datalogger_afe	trial_0	73.36	59.96	53.59	77.93
voltage_datalogger_afe	trial_1	79.82	58.23	65.14	78.01
voltage_datalogger_afe	trial_2	-	73.11	66.3	76.72
voltage_datalogger_afe	trial_3	-	79.47	77.92	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_1	nan ± nan (0)	39.5 ± 5.65 (3)	37.19 ± 6.33 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622426_1	16.24 ± 4.35 (4)	16.94 ± 4.13 (4)	15.74 ± 4.13 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622426_1	76.59 ± 3.23 (2)	67.69 ± 8.91 (4)	65.74 ± 8.61 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682622426_2

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	33.28	32.62	31.64	30.87
voltage_datalogger_adc0	trial_1	-	35.31	32.87	25.52
voltage_datalogger_adc0	trial_2	-	-	30.26	36.03
voltage_datalogger_adc0	trial_3	-	29.25	24.18	28.57
voltage_datalogger_adc2	trial_0	18.47	13.76	11.62	12.81
voltage_datalogger_adc2	trial_1	16.73	15.14	14.6	12.18
voltage_datalogger_adc2	trial_2	17.54	12.7	12.7	13.9
voltage_datalogger_adc2	trial_3	15.77	14.55	13.8	12.85
voltage_datalogger_afe	trial_0	48.33	48.33	48.33	49.34
voltage_datalogger_afe	trial_1	45.93	45.93	45.93	49.26
voltage_datalogger_afe	trial_2	-	-	49.95	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_2	33.28 ± 0.0 (1)	32.39 ± 2.48 (3)	29.74 ± 3.34 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622426_2	17.13 ± 1.0 (4)	14.04 ± 0.91 (4)	13.18 ± 1.13 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622426_2	47.13 ± 1.2 (2)	47.13 ± 1.2 (2)	48.07 ± 1.65 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	43.35	43.17	37.67	58.96
voltage_datalogger_adc0	trial_1	-	38.57	42.13	25.98
voltage_datalogger_adc0	trial_2	-	-	31.91	41.48
voltage_datalogger_adc0	trial_3	-	31.0	28.77	29.14
voltage_datalogger_adc2	trial_0	16.37	11.79	10.39	12.02
voltage_datalogger_adc2	trial_1	15.54	17.65	14.11	12.07
voltage_datalogger_adc2	trial_2	18.37	11.62	11.62	13.34
voltage_datalogger_adc2	trial_3	14.0	12.85	15.67	15.88
voltage_datalogger_afe	trial_0	62.53	62.53	62.53	77.93
voltage_datalogger_afe	trial_1	58.02	58.02	58.02	78.01
voltage_datalogger_afe	trial_2	-	-	69.8	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_2	43.35 ± 0.0 (1)	37.58 ± 5.02 (3)	35.12 ± 5.15 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622426_2	16.07 ± 1.58 (4)	13.48 ± 2.45 (4)	12.95 ± 2.07 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622426_2	60.28 ± 2.25 (2)	60.28 ± 2.25 (2)	63.45 ± 4.85 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_082:1682622426_3

Steps per trial = 600

Euclidean wirelength (w) = 0

Half perimeter wirelength (hpwl) = 8.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	41.73	37.59	30.87
voltage_datalogger_adc0	trial_1	-	32.83	32.26	25.52
voltage_datalogger_adc0	trial_2	-	29.13	26.62	36.03
voltage_datalogger_adc0	trial_3	-	29.71	25.67	28.57
voltage_datalogger_adc2	trial_0	15.15	14.49	13.89	12.81
voltage_datalogger_adc2	trial_1	15.32	14.62	13.93	12.18
voltage_datalogger_adc2	trial_2	15.79	12.84	12.0	13.9
voltage_datalogger_adc2	trial_3	16.62	15.78	14.9	12.85
voltage_datalogger_afe	trial_0	49.57	48.0	46.82	49.34
voltage_datalogger_afe	trial_1	-	50.12	47.92	49.26
voltage_datalogger_afe	trial_2	-	44.95	43.89	45.1
voltage_datalogger_afe	trial_3	-	50.32	48.61	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_3	nan ± nan (0)	33.35 ± 5.04 (4)	30.54 ± 4.79 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682622426_3	15.72 ± 0.57 (4)	14.43 ± 1.05 (4)	13.68 ± 1.05 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682622426_3	49.57 ± 0.0 (1)	48.35 ± 2.16 (4)	46.81 ± 1.8 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	43.12	42.04	58.96
voltage_datalogger_adc0	trial_1	-	45.51	46.28	25.98
voltage_datalogger_adc0	trial_2	-	39.7	30.31	41.48
voltage_datalogger_adc0	trial_3	-	31.52	38.15	29.14
voltage_datalogger_adc2	trial_0	22.32	16.41	15.63	12.02
voltage_datalogger_adc2	trial_1	20.83	16.27	13.29	12.07
voltage_datalogger_adc2	trial_2	22.78	13.93	10.09	13.34
voltage_datalogger_adc2	trial_3	20.09	16.1	15.53	15.88
voltage_datalogger_afe	trial_0	80.86	65.48	54.11	77.93
voltage_datalogger_afe	trial_1	-	57.02	57.28	78.01
voltage_datalogger_afe	trial_2	-	47.67	47.19	76.72
voltage_datalogger_afe	trial_3	-	65.93	54.56	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682622426_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682622426_3	nan ± nan (0)	39.96 ± 5.29 (4)	39.2 ± 5.88 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682622426_3	21.51 ± 1.09 (4)	15.68 ± 1.01 (4)	13.64 ± 2.25 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682622426_3	80.86 ± 0.0 (1)	59.03 ± 7.45 (4)	53.28 ± 3.72 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682487603_0

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	34.2	31.8	31.68	30.87
voltage_datalogger_adc0	trial_1	-	28.32	26.78	25.52
voltage_datalogger_adc0	trial_2	33.4	33.4	33.15	36.03
voltage_datalogger_adc0	trial_3	33.78	33.78	33.78	28.57
voltage_datalogger_adc2	trial_0	18.18	13.99	13.56	12.81
voltage_datalogger_adc2	trial_1	15.09	14.2	14.07	12.18
voltage_datalogger_adc2	trial_2	13.44	12.96	12.33	13.9
voltage_datalogger_adc2	trial_3	14.54	13.87	13.68	12.85
voltage_datalogger_afe	trial_0	49.98	48.33	47.7	49.34
voltage_datalogger_afe	trial_1	56.54	56.54	54.28	49.26
voltage_datalogger_afe	trial_2	-	53.38	52.78	45.1
voltage_datalogger_afe	trial_3	53.19	52.89	52.88	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_0	33.79 ± 0.33 (3)	31.83 ± 2.16 (4)	31.35 ± 2.74 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487603_0	15.31 ± 1.76 (4)	13.76 ± 0.47 (4)	13.41 ± 0.65 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487603_0	53.24 ± 2.68 (3)	52.78 ± 2.93 (4)	51.91 ± 2.5 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	37.75	32.23	32.43	58.96
voltage_datalogger_adc0	trial_1	-	32.6	38.01	25.98
voltage_datalogger_adc0	trial_2	33.51	33.51	35.76	41.48
voltage_datalogger_adc0	trial_3	35.24	35.24	35.24	29.14
voltage_datalogger_adc2	trial_0	15.24	11.11	10.85	12.02
voltage_datalogger_adc2	trial_1	18.42	17.52	17.08	12.07
voltage_datalogger_adc2	trial_2	15.62	15.53	15.29	13.34
voltage_datalogger_adc2	trial_3	18.48	17.83	17.24	15.88
voltage_datalogger_afe	trial_0	50.57	49.52	48.9	77.93
voltage_datalogger_afe	trial_1	61.91	61.91	70.4	78.01
voltage_datalogger_afe	trial_2	-	61.54	62.62	76.72
voltage_datalogger_afe	trial_3	80.72	80.7	80.7	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_0	35.5 ± 1.74 (3)	33.4 ± 1.16 (4)	35.36 ± 1.99 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487603_0	16.94 ± 1.52 (4)	15.5 ± 2.68 (4)	15.11 ± 2.58 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487603_0	64.4 ± 12.43 (3)	63.42 ± 11.15 (4)	65.66 ± 11.61 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682487603_1

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	35.45	33.73	33.52	30.87
voltage_datalogger_adc0	trial_1	38.73	38.73	37.38	25.52
voltage_datalogger_adc0	trial_2	38.76	27.01	27.01	36.03
voltage_datalogger_adc0	trial_3	43.71	43.71	40.47	28.57
voltage_datalogger_adc2	trial_0	25.72	14.37	13.68	12.81
voltage_datalogger_adc2	trial_1	16.14	15.35	13.98	12.18
voltage_datalogger_adc2	trial_2	13.44	12.95	12.64	13.9
voltage_datalogger_adc2	trial_3	14.72	14.44	13.52	12.85
voltage_datalogger_afe	trial_0	-	50.39	50.39	49.34
voltage_datalogger_afe	trial_1	-	-	51.82	49.26
voltage_datalogger_afe	trial_2	-	55.71	55.47	45.1
voltage_datalogger_afe	trial_3	61.0	61.0	61.0	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_1	39.16 ± 2.95 (4)	35.8 ± 6.18 (4)	34.6 ± 5.02 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487603_1	17.5 ± 4.84 (4)	14.28 ± 0.86 (4)	13.45 ± 0.5 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487603_1	61.0 ± 0.0 (1)	55.7 ± 4.33 (3)	54.67 ± 4.1 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	33.69	31.84	31.74	58.96
voltage_datalogger_adc0	trial_1	56.02	56.02	54.7	25.98
voltage_datalogger_adc0	trial_2	42.73	38.15	38.15	41.48
voltage_datalogger_adc0	trial_3	47.89	47.89	51.92	29.14
voltage_datalogger_adc2	trial_0	21.85	13.18	11.11	12.02
voltage_datalogger_adc2	trial_1	19.51	19.78	12.91	12.07
voltage_datalogger_adc2	trial_2	14.88	15.15	11.89	13.34
voltage_datalogger_adc2	trial_3	19.36	19.32	17.67	15.88
voltage_datalogger_afe	trial_0	-	48.45	48.45	77.93
voltage_datalogger_afe	trial_1	-	-	80.97	78.01
voltage_datalogger_afe	trial_2	-	52.1	52.48	76.72
voltage_datalogger_afe	trial_3	70.89	70.89	70.89	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_1	45.08 ± 8.11 (4)	43.47 ± 9.23 (4)	44.13 ± 9.51 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487603_1	18.9 ± 2.52 (4)	16.86 ± 2.79 (4)	13.4 ± 2.55 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487603_1	70.89 ± 0.0 (1)	57.15 ± 9.83 (3)	63.2 ± 13.3 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682487603_2

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	34.25	34.09	34.08	30.87
voltage_datalogger_adc0	trial_1	38.17	34.23	33.73	25.52
voltage_datalogger_adc0	trial_2	-	37.13	36.19	36.03
voltage_datalogger_adc0	trial_3	34.9	32.98	32.94	28.57
voltage_datalogger_adc2	trial_0	15.57	14.79	14.79	12.81
voltage_datalogger_adc2	trial_1	-	-	-	12.18
voltage_datalogger_adc2	trial_2	14.0	13.52	13.52	13.9
voltage_datalogger_adc2	trial_3	14.66	14.66	14.66	12.85
voltage_datalogger_afe	trial_0	57.61	57.61	54.06	49.34
voltage_datalogger_afe	trial_1	58.36	55.82	55.32	49.26
voltage_datalogger_afe	trial_2	54.23	53.35	52.31	45.1
voltage_datalogger_afe	trial_3	58.35	57.71	56.6	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_2	35.77 ± 1.72 (3)	34.61 ± 1.53 (4)	34.24 ± 1.2 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487603_2	14.74 ± 0.64 (3)	14.32 ± 0.57 (3)	14.32 ± 0.57 (3)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487603_2	57.14 ± 1.71 (4)	56.12 ± 1.77 (4)	54.57 ± 1.59 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	32.27	32.0	32.06	58.96
voltage_datalogger_adc0	trial_1	42.94	36.13	35.75	25.98
voltage_datalogger_adc0	trial_2	-	34.74	49.34	41.48
voltage_datalogger_adc0	trial_3	34.14	32.95	32.39	29.14
voltage_datalogger_adc2	trial_0	13.69	13.05	13.05	12.02
voltage_datalogger_adc2	trial_1	-	-	-	12.07
voltage_datalogger_adc2	trial_2	16.09	15.45	15.45	13.34
voltage_datalogger_adc2	trial_3	16.28	16.28	16.28	15.88
voltage_datalogger_afe	trial_0	54.56	54.56	52.92	77.93
voltage_datalogger_afe	trial_1	69.43	69.65	53.84	78.01
voltage_datalogger_afe	trial_2	64.36	63.33	54.7	76.72
voltage_datalogger_afe	trial_3	81.32	81.07	63.9	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_2	36.45 ± 4.65 (3)	33.96 ± 1.6 (4)	37.39 ± 7.05 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487603_2	15.35 ± 1.18 (3)	14.93 ± 1.37 (3)	14.93 ± 1.37 (3)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487603_2	67.42 ± 9.64 (4)	67.15 ± 9.66 (4)	56.34 ± 4.41 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682487603_3

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	34.3	31.58	31.58	30.87
voltage_datalogger_adc0	trial_1	34.96	31.6	30.67	25.52
voltage_datalogger_adc0	trial_2	36.75	29.54	29.54	36.03
voltage_datalogger_adc0	trial_3	-	28.07	27.28	28.57
voltage_datalogger_adc2	trial_0	13.3	11.59	11.58	12.81
voltage_datalogger_adc2	trial_1	15.46	14.71	14.16	12.18
voltage_datalogger_adc2	trial_2	13.74	13.73	13.73	13.9
voltage_datalogger_adc2	trial_3	13.67	13.36	13.35	12.85
voltage_datalogger_afe	trial_0	-	48.53	46.37	49.34
voltage_datalogger_afe	trial_1	53.28	49.67	48.67	49.26
voltage_datalogger_afe	trial_2	-	49.35	47.14	45.1
voltage_datalogger_afe	trial_3	-	-	50.67	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_3	35.34 ± 1.04 (3)	30.2 ± 1.49 (4)	29.77 ± 1.61 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487603_3	14.04 ± 0.84 (4)	13.35 ± 1.13 (4)	13.2 ± 0.98 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487603_3	53.28 ± 0.0 (1)	49.18 ± 0.48 (3)	48.21 ± 1.64 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	34.78	33.1	33.1	58.96
voltage_datalogger_adc0	trial_1	34.49	37.0	36.77	25.98
voltage_datalogger_adc0	trial_2	42.65	32.25	32.25	41.48
voltage_datalogger_adc0	trial_3	-	37.4	26.64	29.14
voltage_datalogger_adc2	trial_0	12.06	10.41	10.41	12.02
voltage_datalogger_adc2	trial_1	18.46	13.41	13.32	12.07
voltage_datalogger_adc2	trial_2	14.75	14.61	14.61	13.34
voltage_datalogger_adc2	trial_3	13.05	12.71	12.81	15.88
voltage_datalogger_afe	trial_0	-	52.79	56.69	77.93
voltage_datalogger_afe	trial_1	78.35	54.18	54.09	78.01
voltage_datalogger_afe	trial_2	-	51.32	45.78	76.72
voltage_datalogger_afe	trial_3	-	-	61.56	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487603_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487603_3	37.31 ± 3.78 (3)	34.94 ± 2.29 (4)	32.19 ± 3.63 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487603_3	14.58 ± 2.44 (4)	12.78 ± 1.53 (4)	12.79 ± 1.52 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487603_3	78.35 ± 0.0 (1)	52.76 ± 1.17 (3)	54.53 ± 5.72 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682623793_0

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	34.47	32.56	29.73	30.87
voltage_datalogger_adc0	trial_1	-	28.76	28.6	25.52
voltage_datalogger_adc0	trial_2	33.66	30.94	30.94	36.03
voltage_datalogger_adc0	trial_3	-	29.07	28.87	28.57
voltage_datalogger_adc2	trial_0	12.54	11.76	11.36	12.81
voltage_datalogger_adc2	trial_1	16.56	14.62	14.29	12.18
voltage_datalogger_adc2	trial_2	15.48	11.5	10.89	13.9
voltage_datalogger_adc2	trial_3	15.88	15.12	14.63	12.85
voltage_datalogger_afe	trial_0	53.48	49.22	48.39	49.34
voltage_datalogger_afe	trial_1	51.8	51.47	50.04	49.26
voltage_datalogger_afe	trial_2	55.46	55.46	53.82	45.1
voltage_datalogger_afe	trial_3	54.84	54.84	54.48	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_0	34.06 ± 0.41 (2)	30.33 ± 1.53 (4)	29.54 ± 0.91 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682623793_0	15.12 ± 1.54 (4)	13.25 ± 1.63 (4)	12.79 ± 1.68 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682623793_0	53.9 ± 1.41 (4)	52.75 ± 2.54 (4)	51.68 ± 2.55 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	31.39	30.82	29.21	58.96
voltage_datalogger_adc0	trial_1	-	29.56	26.07	25.98
voltage_datalogger_adc0	trial_2	38.66	35.18	35.18	41.48
voltage_datalogger_adc0	trial_3	-	34.83	31.79	29.14
voltage_datalogger_adc2	trial_0	11.51	11.15	10.91	12.02
voltage_datalogger_adc2	trial_1	15.57	13.59	13.42	12.07
voltage_datalogger_adc2	trial_2	17.72	10.15	9.67	13.34
voltage_datalogger_adc2	trial_3	17.06	14.93	14.55	15.88
voltage_datalogger_afe	trial_0	49.34	50.94	52.43	77.93
voltage_datalogger_afe	trial_1	78.93	61.22	61.18	78.01
voltage_datalogger_afe	trial_2	69.28	69.28	80.37	76.72
voltage_datalogger_afe	trial_3	62.24	62.24	66.5	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_0	35.02 ± 3.63 (2)	32.6 ± 2.45 (4)	30.56 ± 3.35 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682623793_0	15.46 ± 2.41 (4)	12.46 ± 1.9 (4)	12.14 ± 1.94 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682623793_0	64.95 ± 10.78 (4)	60.92 ± 6.54 (4)	65.12 ± 10.14 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682623793_1

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	34.78	34.78	34.73	30.87
voltage_datalogger_adc0	trial_1	36.54	35.08	30.97	25.52
voltage_datalogger_adc0	trial_2	-	37.26	35.36	36.03
voltage_datalogger_adc0	trial_3	-	32.06	32.06	28.57
voltage_datalogger_adc2	trial_0	12.13	11.95	11.82	12.81
voltage_datalogger_adc2	trial_1	15.48	14.98	14.33	12.18
voltage_datalogger_adc2	trial_2	15.23	12.2	11.8	13.9
voltage_datalogger_adc2	trial_3	15.42	14.93	14.24	12.85
voltage_datalogger_afe	trial_0	-	47.39	46.78	49.34
voltage_datalogger_afe	trial_1	62.18	50.34	48.88	49.26
voltage_datalogger_afe	trial_2	51.51	49.18	48.56	45.1
voltage_datalogger_afe	trial_3	56.63	55.03	54.32	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_1	35.66 ± 0.88 (2)	34.8 ± 1.85 (4)	33.28 ± 1.82 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682623793_1	14.57 ± 1.41 (4)	13.51 ± 1.44 (4)	13.05 ± 1.24 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682623793_1	56.77 ± 4.36 (3)	50.48 ± 2.83 (4)	49.64 ± 2.82 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	32.61	32.61	33.7	58.96
voltage_datalogger_adc0	trial_1	39.59	34.67	29.24	25.98
voltage_datalogger_adc0	trial_2	-	45.46	51.71	41.48
voltage_datalogger_adc0	trial_3	-	33.92	33.92	29.14
voltage_datalogger_adc2	trial_0	11.14	11.08	10.9	12.02
voltage_datalogger_adc2	trial_1	18.72	18.09	17.2	12.07
voltage_datalogger_adc2	trial_2	14.3	10.46	10.09	13.34
voltage_datalogger_adc2	trial_3	17.68	14.71	13.42	15.88
voltage_datalogger_afe	trial_0	-	61.73	60.81	77.93
voltage_datalogger_afe	trial_1	59.4	62.14	59.91	78.01
voltage_datalogger_afe	trial_2	58.12	58.16	56.83	76.72
voltage_datalogger_afe	trial_3	66.29	63.34	57.51	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_1	36.1 ± 3.49 (2)	36.67 ± 5.13 (4)	37.14 ± 8.62 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682623793_1	15.46 ± 2.98 (4)	13.58 ± 3.07 (4)	12.9 ± 2.77 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682623793_1	61.27 ± 3.59 (3)	61.34 ± 1.93 (4)	58.76 ± 1.64 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682623793_2

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	33.82	32.7	30.06	30.87
voltage_datalogger_adc0	trial_1	37.49	34.31	29.86	25.52
voltage_datalogger_adc0	trial_2	31.78	29.1	28.67	36.03
voltage_datalogger_adc0	trial_3	-	24.64	23.87	28.57
voltage_datalogger_adc2	trial_0	13.42	12.69	12.69	12.81
voltage_datalogger_adc2	trial_1	15.77	15.75	15.28	12.18
voltage_datalogger_adc2	trial_2	13.85	13.55	13.2	13.9
voltage_datalogger_adc2	trial_3	15.41	15.14	14.96	12.85
voltage_datalogger_afe	trial_0	-	53.98	51.73	49.34
voltage_datalogger_afe	trial_1	-	50.31	47.27	49.26
voltage_datalogger_afe	trial_2	-	46.41	45.63	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_2	34.36 ± 2.36 (3)	30.19 ± 3.72 (4)	28.12 ± 2.51 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682623793_2	14.61 ± 1.0 (4)	14.28 ± 1.22 (4)	14.03 ± 1.11 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682623793_2	nan ± nan (0)	50.23 ± 3.09 (3)	48.21 ± 2.58 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	30.62	33.09	41.84	58.96
voltage_datalogger_adc0	trial_1	40.2	35.69	35.36	25.98
voltage_datalogger_adc0	trial_2	43.05	32.57	35.01	41.48
voltage_datalogger_adc0	trial_3	-	36.34	26.28	29.14
voltage_datalogger_adc2	trial_0	11.5	10.75	10.75	12.02
voltage_datalogger_adc2	trial_1	17.89	18.02	17.64	12.07
voltage_datalogger_adc2	trial_2	16.0	15.5	11.89	13.34
voltage_datalogger_adc2	trial_3	19.25	19.04	18.8	15.88
voltage_datalogger_afe	trial_0	-	57.35	54.67	77.93
voltage_datalogger_afe	trial_1	-	54.56	48.35	78.01
voltage_datalogger_afe	trial_2	-	49.79	66.21	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_2	37.96 ± 5.32 (3)	34.42 ± 1.62 (4)	34.62 ± 5.53 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682623793_2	16.16 ± 2.93 (4)	15.83 ± 3.2 (4)	14.77 ± 3.5 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682623793_2	nan ± nan (0)	53.9 ± 3.12 (3)	56.41 ± 7.39 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_505:1682623793_3

Steps per trial = 600

Euclidean wirelength (w) = 5

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 5.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	35.8	33.73	30.71	30.87
voltage_datalogger_adc0	trial_1	38.1	37.51	35.43	25.52
voltage_datalogger_adc0	trial_2	-	29.99	29.65	36.03
voltage_datalogger_adc0	trial_3	34.66	31.77	29.75	28.57
voltage_datalogger_adc2	trial_0	12.32	12.19	11.49	12.81
voltage_datalogger_adc2	trial_1	15.57	14.86	14.52	12.18
voltage_datalogger_adc2	trial_2	14.38	14.35	13.97	13.9
voltage_datalogger_adc2	trial_3	15.24	15.24	14.8	12.85
voltage_datalogger_afe	trial_0	57.16	52.72	51.15	49.34
voltage_datalogger_afe	trial_1	-	48.26	47.91	49.26
voltage_datalogger_afe	trial_2	-	46.98	44.22	45.1
voltage_datalogger_afe	trial_3	-	45.45	45.45	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_3	36.19 ± 1.43 (3)	33.25 ± 2.79 (4)	31.38 ± 2.37 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682623793_3	14.38 ± 1.26 (4)	14.16 ± 1.18 (4)	13.7 ± 1.31 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682623793_3	57.16 ± 0.0 (1)	48.35 ± 2.71 (4)	47.18 ± 2.65 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	32.31	30.43	30.17	58.96
voltage_datalogger_adc0	trial_1	37.4	42.9	32.29	25.98
voltage_datalogger_adc0	trial_2	-	28.77	28.61	41.48
voltage_datalogger_adc0	trial_3	35.32	32.43	32.18	29.14
voltage_datalogger_adc2	trial_0	11.49	11.35	10.87	12.02
voltage_datalogger_adc2	trial_1	19.22	14.46	14.07	12.07
voltage_datalogger_adc2	trial_2	15.33	14.98	15.17	13.34
voltage_datalogger_adc2	trial_3	19.37	19.37	14.01	15.88
voltage_datalogger_afe	trial_0	72.9	58.18	61.41	77.93
voltage_datalogger_afe	trial_1	-	51.84	52.85	78.01
voltage_datalogger_afe	trial_2	-	52.85	50.58	76.72
voltage_datalogger_afe	trial_3	-	62.1	62.1	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682623793_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682623793_3	35.01 ± 2.09 (3)	33.63 ± 5.51 (4)	30.81 ± 1.53 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682623793_3	16.35 ± 3.24 (4)	15.04 ± 2.86 (4)	13.53 ± 1.6 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682623793_3	72.9 ± 0.0 (1)	56.24 ± 4.15 (4)	56.73 ± 5.09 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682487605_0

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	31.48	31.48	29.52	30.87
voltage_datalogger_adc0	trial_1	-	30.34	25.24	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	82.03	26.92	28.57
voltage_datalogger_adc2	trial_0	16.29	12.5	12.5	12.81
voltage_datalogger_adc2	trial_1	15.29	15.29	14.29	12.18
voltage_datalogger_adc2	trial_2	15.23	13.7	12.37	13.9
voltage_datalogger_adc2	trial_3	15.64	14.84	14.22	12.85
voltage_datalogger_afe	trial_0	52.49	52.49	52.49	49.34
voltage_datalogger_afe	trial_1	-	-	44.48	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_0	31.48 ± 0.0 (1)	47.95 ± 24.1 (3)	27.23 ± 1.76 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487605_0	15.61 ± 0.42 (4)	14.08 ± 1.08 (4)	13.34 ± 0.91 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487605_0	52.49 ± 0.0 (1)	52.49 ± 0.0 (1)	48.48 ± 4.01 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	37.79	37.79	31.17	58.96
voltage_datalogger_adc0	trial_1	-	32.0	25.97	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	98.02	32.07	29.14
voltage_datalogger_adc2	trial_0	15.85	10.74	10.74	12.02
voltage_datalogger_adc2	trial_1	13.39	13.39	12.98	12.07
voltage_datalogger_adc2	trial_2	15.39	14.42	10.47	13.34
voltage_datalogger_adc2	trial_3	17.93	13.21	13.32	15.88
voltage_datalogger_afe	trial_0	69.28	69.28	69.28	77.93
voltage_datalogger_afe	trial_1	-	-	59.33	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_0	37.79 ± 0.0 (1)	55.94 ± 29.85 (3)	29.74 ± 2.69 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487605_0	15.64 ± 1.61 (4)	12.94 ± 1.35 (4)	11.88 ± 1.28 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487605_0	69.28 ± 0.0 (1)	69.28 ± 0.0 (1)	64.31 ± 4.98 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682487605_1

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	29.84	29.84	30.87
voltage_datalogger_adc0	trial_1	-	-	33.19	25.52
voltage_datalogger_adc0	trial_2	35.2	35.2	35.2	36.03
voltage_datalogger_adc0	trial_3	-	72.45	25.45	28.57
voltage_datalogger_adc2	trial_0	12.72	11.59	11.06	12.81
voltage_datalogger_adc2	trial_1	15.13	14.96	14.73	12.18
voltage_datalogger_adc2	trial_2	13.71	13.61	13.61	13.9
voltage_datalogger_adc2	trial_3	15.67	13.72	13.3	12.85
voltage_datalogger_afe	trial_0	-	-	41.9	49.34
voltage_datalogger_afe	trial_1	-	45.99	45.99	49.26
voltage_datalogger_afe	trial_2	-	-	45.16	45.1
voltage_datalogger_afe	trial_3	-	48.95	47.39	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_1	35.2 ± 0.0 (1)	45.83 ± 18.95 (3)	30.92 ± 3.69 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487605_1	14.31 ± 1.16 (4)	13.47 ± 1.21 (4)	13.18 ± 1.33 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487605_1	nan ± nan (0)	47.47 ± 1.48 (2)	45.11 ± 2.02 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	33.06	33.06	58.96
voltage_datalogger_adc0	trial_1	-	-	34.85	25.98
voltage_datalogger_adc0	trial_2	62.78	62.78	62.78	41.48
voltage_datalogger_adc0	trial_3	-	87.7	27.9	29.14
voltage_datalogger_adc2	trial_0	11.54	10.51	10.57	12.02
voltage_datalogger_adc2	trial_1	18.24	17.93	17.25	12.07
voltage_datalogger_adc2	trial_2	14.31	11.12	11.12	13.34
voltage_datalogger_adc2	trial_3	13.94	12.51	12.06	15.88
voltage_datalogger_afe	trial_0	-	-	53.75	77.93
voltage_datalogger_afe	trial_1	-	58.53	58.53	78.01
voltage_datalogger_afe	trial_2	-	-	49.72	76.72
voltage_datalogger_afe	trial_3	-	57.01	69.61	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_1	62.78 ± 0.0 (1)	61.18 ± 22.34 (3)	39.65 ± 13.6 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487605_1	14.51 ± 2.4 (4)	13.02 ± 2.93 (4)	12.75 ± 2.65 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487605_1	nan ± nan (0)	57.77 ± 0.76 (2)	57.9 ± 7.44 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682487605_2

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	26.12	26.12	30.87
voltage_datalogger_adc0	trial_1	-	-	31.55	25.52
voltage_datalogger_adc0	trial_2	-	-	32.49	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	13.54	13.1	13.1	12.81
voltage_datalogger_adc2	trial_1	15.15	14.12	13.95	12.18
voltage_datalogger_adc2	trial_2	12.78	12.78	11.97	13.9
voltage_datalogger_adc2	trial_3	14.93	14.93	13.76	12.85
voltage_datalogger_afe	trial_0	38.16	38.16	38.16	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	48.28	45.1
voltage_datalogger_afe	trial_3	-	-	55.07	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_2	nan ± nan (0)	26.12 ± 0.0 (1)	30.05 ± 2.81 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487605_2	14.1 ± 0.98 (4)	13.73 ± 0.85 (4)	13.19 ± 0.77 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487605_2	38.16 ± 0.0 (1)	38.16 ± 0.0 (1)	47.17 ± 6.95 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	32.7	32.7	58.96
voltage_datalogger_adc0	trial_1	-	-	36.87	25.98
voltage_datalogger_adc0	trial_2	-	-	34.07	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	12.19	11.49	11.49	12.02
voltage_datalogger_adc2	trial_1	15.34	17.76	17.35	12.07
voltage_datalogger_adc2	trial_2	11.35	11.35	10.55	13.34
voltage_datalogger_adc2	trial_3	21.53	21.53	20.68	15.88
voltage_datalogger_afe	trial_0	42.65	42.65	42.65	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	53.0	76.72
voltage_datalogger_afe	trial_3	-	-	56.01	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_2	nan ± nan (0)	32.7 ± 0.0 (1)	34.55 ± 1.74 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487605_2	15.1 ± 4.0 (4)	15.53 ± 4.32 (4)	15.02 ± 4.18 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487605_2	42.65 ± 0.0 (1)	42.65 ± 0.0 (1)	50.55 ± 5.72 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682487605_3

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	32.65	32.65	31.5	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	-	-	27.74	36.03
voltage_datalogger_adc0	trial_3	-	27.88	27.3	28.57
voltage_datalogger_adc2	trial_0	12.4	11.86	11.44	12.81
voltage_datalogger_adc2	trial_1	15.49	14.64	14.0	12.18
voltage_datalogger_adc2	trial_2	17.35	12.16	11.17	13.9
voltage_datalogger_adc2	trial_3	16.18	14.64	13.85	12.85
voltage_datalogger_afe	trial_0	-	-	51.08	49.34
voltage_datalogger_afe	trial_1	-	-	47.86	49.26
voltage_datalogger_afe	trial_2	-	-	47.89	45.1
voltage_datalogger_afe	trial_3	-	-	47.58	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_3	32.65 ± 0.0 (1)	30.26 ± 2.38 (2)	28.85 ± 1.88 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487605_3	15.36 ± 1.83 (4)	13.32 ± 1.32 (4)	12.62 ± 1.31 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487605_3	nan ± nan (0)	nan ± nan (0)	48.6 ± 1.44 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	33.79	33.79	31.96	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	-	-	29.1	41.48
voltage_datalogger_adc0	trial_3	-	27.49	26.71	29.14
voltage_datalogger_adc2	trial_0	11.19	10.73	10.36	12.02
voltage_datalogger_adc2	trial_1	19.75	19.42	13.4	12.07
voltage_datalogger_adc2	trial_2	17.97	9.92	10.36	13.34
voltage_datalogger_adc2	trial_3	14.45	13.33	13.21	15.88
voltage_datalogger_afe	trial_0	-	-	59.25	77.93
voltage_datalogger_afe	trial_1	-	-	48.69	78.01
voltage_datalogger_afe	trial_2	-	-	69.09	76.72
voltage_datalogger_afe	trial_3	-	-	58.78	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487605_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487605_3	33.79 ± 0.0 (1)	30.64 ± 3.15 (2)	29.26 ± 2.15 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487605_3	15.84 ± 3.29 (4)	13.35 ± 3.72 (4)	11.83 ± 1.47 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487605_3	nan ± nan (0)	nan ± nan (0)	58.95 ± 7.21 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682624196_0

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.4	30.87
voltage_datalogger_adc0	trial_1	-	-	31.47	25.52
voltage_datalogger_adc0	trial_2	-	-	29.59	36.03
voltage_datalogger_adc0	trial_3	-	-	25.06	28.57
voltage_datalogger_adc2	trial_0	14.14	13.63	13.39	12.81
voltage_datalogger_adc2	trial_1	15.4	15.01	13.86	12.18
voltage_datalogger_adc2	trial_2	14.24	13.32	13.32	13.9
voltage_datalogger_adc2	trial_3	16.86	14.31	13.86	12.85
voltage_datalogger_afe	trial_0	-	-	56.08	49.34
voltage_datalogger_afe	trial_1	-	-	46.58	49.26
voltage_datalogger_afe	trial_2	-	46.84	46.84	45.1
voltage_datalogger_afe	trial_3	51.39	51.39	51.39	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_0	nan ± nan (0)	nan ± nan (0)	28.63 ± 2.33 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624196_0	15.16 ± 1.1 (4)	14.07 ± 0.65 (4)	13.61 ± 0.25 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624196_0	51.39 ± 0.0 (1)	49.12 ± 2.27 (2)	50.22 ± 3.89 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.47	58.96
voltage_datalogger_adc0	trial_1	-	-	29.42	25.98
voltage_datalogger_adc0	trial_2	-	-	40.93	41.48
voltage_datalogger_adc0	trial_3	-	-	25.37	29.14
voltage_datalogger_adc2	trial_0	16.76	15.95	11.36	12.02
voltage_datalogger_adc2	trial_1	14.69	19.24	16.77	12.07
voltage_datalogger_adc2	trial_2	13.16	12.25	12.25	13.34
voltage_datalogger_adc2	trial_3	24.87	17.58	12.78	15.88
voltage_datalogger_afe	trial_0	-	-	54.45	77.93
voltage_datalogger_afe	trial_1	-	-	51.09	78.01
voltage_datalogger_afe	trial_2	-	57.84	57.84	76.72
voltage_datalogger_afe	trial_3	88.37	88.37	88.37	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_0	nan ± nan (0)	nan ± nan (0)	31.05 ± 5.9 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624196_0	17.37 ± 4.51 (4)	16.26 ± 2.59 (4)	13.29 ± 2.07 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624196_0	88.37 ± 0.0 (1)	73.1 ± 15.26 (2)	62.94 ± 14.88 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682624196_1

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	27.95	30.87
voltage_datalogger_adc0	trial_1	-	30.74	30.06	25.52
voltage_datalogger_adc0	trial_2	-	-	25.44	36.03
voltage_datalogger_adc0	trial_3	-	-	26.71	28.57
voltage_datalogger_adc2	trial_0	16.21	14.35	12.89	12.81
voltage_datalogger_adc2	trial_1	15.45	14.87	14.65	12.18
voltage_datalogger_adc2	trial_2	18.87	16.03	12.37	13.9
voltage_datalogger_adc2	trial_3	15.46	13.82	13.06	12.85
voltage_datalogger_afe	trial_0	-	51.23	49.78	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	46.31	45.1
voltage_datalogger_afe	trial_3	-	-	44.03	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_1	nan ± nan (0)	30.74 ± 0.0 (1)	27.54 ± 1.7 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624196_1	16.5 ± 1.4 (4)	14.77 ± 0.82 (4)	13.24 ± 0.85 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624196_1	nan ± nan (0)	51.23 ± 0.0 (1)	46.71 ± 2.36 (3)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	28.61	58.96
voltage_datalogger_adc0	trial_1	-	29.26	28.81	25.98
voltage_datalogger_adc0	trial_2	-	-	27.02	41.48
voltage_datalogger_adc0	trial_3	-	-	30.03	29.14
voltage_datalogger_adc2	trial_0	13.97	12.56	10.25	12.02
voltage_datalogger_adc2	trial_1	18.39	17.6	17.32	12.07
voltage_datalogger_adc2	trial_2	20.04	17.0	9.76	13.34
voltage_datalogger_adc2	trial_3	14.57	13.19	12.41	15.88
voltage_datalogger_afe	trial_0	-	58.4	57.36	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	49.05	76.72
voltage_datalogger_afe	trial_3	-	-	65.17	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_1	nan ± nan (0)	29.26 ± 0.0 (1)	28.62 ± 1.07 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624196_1	16.74 ± 2.55 (4)	15.09 ± 2.23 (4)	12.43 ± 2.99 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624196_1	nan ± nan (0)	58.4 ± 0.0 (1)	57.19 ± 6.58 (3)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682624196_2

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	22.67	30.87
voltage_datalogger_adc0	trial_1	-	29.97	28.94	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	31.04	29.2	28.57
voltage_datalogger_adc2	trial_0	20.04	14.19	14.19	12.81
voltage_datalogger_adc2	trial_1	15.54	12.68	11.59	12.18
voltage_datalogger_adc2	trial_2	12.67	11.64	11.35	13.9
voltage_datalogger_adc2	trial_3	12.5	11.74	11.66	12.85
voltage_datalogger_afe	trial_0	-	57.09	53.62	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	-	-	40.08	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_2	nan ± nan (0)	30.5 ± 0.54 (2)	26.94 ± 3.02 (3)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624196_2	15.19 ± 3.05 (4)	12.56 ± 1.02 (4)	12.2 ± 1.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624196_2	nan ± nan (0)	57.09 ± 0.0 (1)	46.85 ± 6.77 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	25.36	58.96
voltage_datalogger_adc0	trial_1	-	28.11	27.36	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	31.2	35.36	29.14
voltage_datalogger_adc2	trial_0	18.37	15.05	15.05	12.02
voltage_datalogger_adc2	trial_1	14.76	11.68	11.29	12.07
voltage_datalogger_adc2	trial_2	15.06	13.18	12.98	13.34
voltage_datalogger_adc2	trial_3	13.82	12.75	12.75	15.88
voltage_datalogger_afe	trial_0	-	67.51	74.72	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	-	-	47.34	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_2	nan ± nan (0)	29.66 ± 1.54 (2)	29.36 ± 4.32 (3)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624196_2	15.5 ± 1.72 (4)	13.16 ± 1.22 (4)	13.02 ± 1.34 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624196_2	nan ± nan (0)	67.51 ± 0.0 (1)	61.03 ± 13.69 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_802:1682624196_3

Steps per trial = 600

Euclidean wirelength (w) = 8

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	30.98	27.74	30.87
voltage_datalogger_adc0	trial_1	-	32.24	28.82	25.52
voltage_datalogger_adc0	trial_2	-	-	-	36.03
voltage_datalogger_adc0	trial_3	-	-	-	28.57
voltage_datalogger_adc2	trial_0	20.57	14.73	12.6	12.81
voltage_datalogger_adc2	trial_1	-	12.18	11.69	12.18
voltage_datalogger_adc2	trial_2	16.25	14.01	12.55	13.9
voltage_datalogger_adc2	trial_3	13.16	12.28	12.14	12.85
voltage_datalogger_afe	trial_0	-	-	47.79	49.34
voltage_datalogger_afe	trial_1	53.99	53.99	53.47	49.26
voltage_datalogger_afe	trial_2	-	-	-	45.1
voltage_datalogger_afe	trial_3	-	-	-	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_3	nan ± nan (0)	31.61 ± 0.63 (2)	28.28 ± 0.54 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624196_3	16.66 ± 3.04 (3)	13.3 ± 1.1 (4)	12.24 ± 0.37 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624196_3	53.99 ± 0.0 (1)	53.99 ± 0.0 (1)	50.63 ± 2.84 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	31.38	35.72	58.96
voltage_datalogger_adc0	trial_1	-	37.81	28.64	25.98
voltage_datalogger_adc0	trial_2	-	-	-	41.48
voltage_datalogger_adc0	trial_3	-	-	-	29.14
voltage_datalogger_adc2	trial_0	16.13	12.34	12.6	12.02
voltage_datalogger_adc2	trial_1	-	11.13	11.05	12.07
voltage_datalogger_adc2	trial_2	17.02	11.02	10.29	13.34
voltage_datalogger_adc2	trial_3	14.98	11.35	10.44	15.88
voltage_datalogger_afe	trial_0	-	-	67.76	77.93
voltage_datalogger_afe	trial_1	69.98	69.98	63.67	78.01
voltage_datalogger_afe	trial_2	-	-	-	76.72
voltage_datalogger_afe	trial_3	-	-	-	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624196_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624196_3	nan ± nan (0)	34.6 ± 3.22 (2)	32.18 ± 3.54 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624196_3	16.04 ± 0.84 (3)	11.46 ± 0.52 (4)	11.1 ± 0.91 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624196_3	69.98 ± 0.0 (1)	69.98 ± 0.0 (1)	65.72 ± 2.05 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682487607_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	30.87
voltage_datalogger_adc0	trial_1	-	-	-	25.52
voltage_datalogger_adc0	trial_2	79.19	79.19	79.19	36.03
voltage_datalogger_adc0	trial_3	81.83	81.83	81.83	28.57
voltage_datalogger_adc2	trial_0	35.08	35.08	35.08	12.81
voltage_datalogger_adc2	trial_1	-	-	28.62	12.18
voltage_datalogger_adc2	trial_2	26.02	26.02	26.02	13.9
voltage_datalogger_adc2	trial_3	24.05	24.05	24.05	12.85
voltage_datalogger_afe	trial_0	-	-	-	49.34
voltage_datalogger_afe	trial_1	-	-	-	49.26
voltage_datalogger_afe	trial_2	95.85	95.85	95.85	45.1
voltage_datalogger_afe	trial_3	97.25	97.25	97.25	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_0	80.51 ± 1.32 (2)	80.51 ± 1.32 (2)	80.51 ± 1.32 (2)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487607_0	28.38 ± 4.8 (3)	28.38 ± 4.8 (3)	28.44 ± 4.16 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487607_0	96.55 ± 0.7 (2)	96.55 ± 0.7 (2)	96.55 ± 0.7 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	-	-	-	58.96
voltage_datalogger_adc0	trial_1	-	-	-	25.98
voltage_datalogger_adc0	trial_2	96.11	96.11	96.11	41.48
voltage_datalogger_adc0	trial_3	96.93	96.93	96.93	29.14
voltage_datalogger_adc2	trial_0	28.52	28.52	28.52	12.02
voltage_datalogger_adc2	trial_1	-	-	34.5	12.07
voltage_datalogger_adc2	trial_2	21.81	21.81	21.81	13.34
voltage_datalogger_adc2	trial_3	30.96	30.96	30.96	15.88
voltage_datalogger_afe	trial_0	-	-	-	77.93
voltage_datalogger_afe	trial_1	-	-	-	78.01
voltage_datalogger_afe	trial_2	120.23	120.23	120.23	76.72
voltage_datalogger_afe	trial_3	122.94	122.94	122.94	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_0	96.52 ± 0.41 (2)	96.52 ± 0.41 (2)	96.52 ± 0.41 (2)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487607_0	27.1 ± 3.87 (3)	27.1 ± 3.87 (3)	28.95 ± 4.64 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487607_0	121.58 ± 1.35 (2)	121.58 ± 1.35 (2)	121.58 ± 1.35 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682487607_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	50.6	50.6	50.6	30.87
voltage_datalogger_adc0	trial_1	38.79	38.2	38.2	25.52
voltage_datalogger_adc0	trial_2	40.52	40.41	40.39	36.03
voltage_datalogger_adc0	trial_3	41.28	34.54	34.54	28.57
voltage_datalogger_adc2	trial_0	27.46	27.46	27.46	12.81
voltage_datalogger_adc2	trial_1	-	19.74	19.74	12.18
voltage_datalogger_adc2	trial_2	15.59	15.33	15.33	13.9
voltage_datalogger_adc2	trial_3	18.16	17.51	17.51	12.85
voltage_datalogger_afe	trial_0	55.36	54.89	54.03	49.34
voltage_datalogger_afe	trial_1	47.02	46.49	46.49	49.26
voltage_datalogger_afe	trial_2	60.06	58.62	57.12	45.1
voltage_datalogger_afe	trial_3	64.69	64.34	63.64	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_1	42.8 ± 4.59 (4)	40.94 ± 5.96 (4)	40.93 ± 5.96 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487607_1	20.4 ± 5.1 (3)	20.01 ± 4.58 (4)	20.01 ± 4.58 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487607_1	56.78 ± 6.53 (4)	56.08 ± 6.48 (4)	55.32 ± 6.17 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	54.1	54.1	54.1	58.96
voltage_datalogger_adc0	trial_1	40.71	40.14	40.14	25.98
voltage_datalogger_adc0	trial_2	50.43	44.25	43.14	41.48
voltage_datalogger_adc0	trial_3	38.71	35.79	35.79	29.14
voltage_datalogger_adc2	trial_0	25.24	25.24	25.24	12.02
voltage_datalogger_adc2	trial_1	-	17.93	17.93	12.07
voltage_datalogger_adc2	trial_2	16.89	16.34	16.34	13.34
voltage_datalogger_adc2	trial_3	21.9	26.81	26.81	15.88
voltage_datalogger_afe	trial_0	63.94	61.08	59.67	77.93
voltage_datalogger_afe	trial_1	86.12	73.13	73.13	78.01
voltage_datalogger_afe	trial_2	68.78	63.09	56.16	76.72
voltage_datalogger_afe	trial_3	71.22	68.45	70.17	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_1	45.99 ± 6.45 (4)	43.57 ± 6.78 (4)	43.29 ± 6.76 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487607_1	21.34 ± 3.43 (3)	21.58 ± 4.51 (4)	21.58 ± 4.51 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487607_1	72.52 ± 8.28 (4)	66.44 ± 4.71 (4)	64.78 ± 7.06 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682487607_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	34.06	33.6	33.6	30.87
voltage_datalogger_adc0	trial_1	46.42	45.51	45.51	25.52
voltage_datalogger_adc0	trial_2	44.29	43.49	43.49	36.03
voltage_datalogger_adc0	trial_3	42.09	41.58	41.58	28.57
voltage_datalogger_adc2	trial_0	14.57	14.57	14.57	12.81
voltage_datalogger_adc2	trial_1	15.55	15.55	14.88	12.18
voltage_datalogger_adc2	trial_2	15.39	14.98	14.98	13.9
voltage_datalogger_adc2	trial_3	14.58	13.97	13.97	12.85
voltage_datalogger_afe	trial_0	55.07	53.72	53.12	49.34
voltage_datalogger_afe	trial_1	55.58	54.85	54.85	49.26
voltage_datalogger_afe	trial_2	61.17	60.51	58.89	45.1
voltage_datalogger_afe	trial_3	70.47	69.97	69.97	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_2	41.72 ± 4.68 (4)	41.04 ± 4.52 (4)	41.04 ± 4.52 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487607_2	15.02 ± 0.45 (4)	14.77 ± 0.58 (4)	14.6 ± 0.39 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487607_2	60.57 ± 6.2 (4)	59.76 ± 6.43 (4)	59.21 ± 6.56 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	37.44	36.88	36.88	58.96
voltage_datalogger_adc0	trial_1	54.02	54.16	54.16	25.98
voltage_datalogger_adc0	trial_2	50.84	50.97	50.97	41.48
voltage_datalogger_adc0	trial_3	43.69	48.65	48.65	29.14
voltage_datalogger_adc2	trial_0	13.2	13.2	13.2	12.02
voltage_datalogger_adc2	trial_1	17.03	17.03	19.69	12.07
voltage_datalogger_adc2	trial_2	13.99	13.49	13.49	13.34
voltage_datalogger_adc2	trial_3	15.86	18.48	18.48	15.88
voltage_datalogger_afe	trial_0	54.62	57.49	54.14	77.93
voltage_datalogger_afe	trial_1	83.94	59.66	59.66	78.01
voltage_datalogger_afe	trial_2	75.96	80.35	74.08	76.72
voltage_datalogger_afe	trial_3	100.26	98.56	98.56	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_2	46.5 ± 6.43 (4)	47.66 ± 6.53 (4)	47.66 ± 6.53 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487607_2	15.02 ± 1.51 (4)	15.55 ± 2.27 (4)	16.22 ± 2.9 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487607_2	78.69 ± 16.43 (4)	74.02 ± 16.75 (4)	71.61 ± 17.18 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682487607_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	33.96	33.85	33.85	30.87
voltage_datalogger_adc0	trial_1	50.64	50.48	50.43	25.52
voltage_datalogger_adc0	trial_2	38.3	37.98	37.98	36.03
voltage_datalogger_adc0	trial_3	37.33	36.9	36.9	28.57
voltage_datalogger_adc2	trial_0	12.17	11.71	11.68	12.81
voltage_datalogger_adc2	trial_1	14.5	14.27	14.27	12.18
voltage_datalogger_adc2	trial_2	13.46	13.15	13.08	13.9
voltage_datalogger_adc2	trial_3	16.07	15.13	14.86	12.85
voltage_datalogger_afe	trial_0	58.83	57.54	56.26	49.34
voltage_datalogger_afe	trial_1	58.84	58.5	58.5	49.26
voltage_datalogger_afe	trial_2	60.01	55.7	55.7	45.1
voltage_datalogger_afe	trial_3	66.35	65.51	65.51	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_3	40.06 ± 6.32 (4)	39.8 ± 6.35 (4)	39.79 ± 6.33 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682487607_3	14.05 ± 1.43 (4)	13.57 ± 1.28 (4)	13.47 ± 1.22 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682487607_3	61.01 ± 3.12 (4)	59.31 ± 3.72 (4)	58.99 ± 3.91 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	36.05	35.46	35.46	58.96
voltage_datalogger_adc0	trial_1	58.3	70.4	69.19	25.98
voltage_datalogger_adc0	trial_2	37.87	37.44	37.44	41.48
voltage_datalogger_adc0	trial_3	40.58	43.05	43.05	29.14
voltage_datalogger_adc2	trial_0	10.89	10.55	10.8	12.02
voltage_datalogger_adc2	trial_1	19.42	23.1	23.1	12.07
voltage_datalogger_adc2	trial_2	15.7	15.47	16.0	13.34
voltage_datalogger_adc2	trial_3	15.44	14.85	14.1	15.88
voltage_datalogger_afe	trial_0	75.55	73.69	58.98	77.93
voltage_datalogger_afe	trial_1	57.88	57.77	57.77	78.01
voltage_datalogger_afe	trial_2	76.36	74.82	74.82	76.72
voltage_datalogger_afe	trial_3	76.26	85.62	85.62	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682487607_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682487607_3	43.2 ± 8.87 (4)	46.59 ± 14.03 (4)	46.28 ± 13.51 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682487607_3	15.36 ± 3.02 (4)	15.99 ± 4.52 (4)	16.0 ± 4.5 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682487607_3	71.51 ± 7.88 (4)	72.97 ± 9.94 (4)	69.3 ± 11.58 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682624534_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	33.59	31.68	31.52	30.87
voltage_datalogger_adc0	trial_1	47.45	46.28	46.28	25.52
voltage_datalogger_adc0	trial_2	43.68	42.17	42.17	36.03
voltage_datalogger_adc0	trial_3	37.68	37.28	37.28	28.57
voltage_datalogger_adc2	trial_0	12.77	12.77	12.77	12.81
voltage_datalogger_adc2	trial_1	15.33	15.29	15.29	12.18
voltage_datalogger_adc2	trial_2	14.27	14.22	14.22	13.9
voltage_datalogger_adc2	trial_3	15.59	15.48	15.48	12.85
voltage_datalogger_afe	trial_0	57.22	54.36	54.17	49.34
voltage_datalogger_afe	trial_1	59.92	58.63	58.63	49.26
voltage_datalogger_afe	trial_2	-	55.0	54.76	45.1
voltage_datalogger_afe	trial_3	69.16	66.58	66.58	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_0	40.6 ± 5.34 (4)	39.35 ± 5.46 (4)	39.31 ± 5.51 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624534_0	14.49 ± 1.11 (4)	14.44 ± 1.08 (4)	14.44 ± 1.08 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624534_0	62.1 ± 5.11 (3)	58.64 ± 4.86 (4)	58.54 ± 4.95 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_0

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	33.49	34.81	31.87	58.96
voltage_datalogger_adc0	trial_1	65.25	57.86	57.86	25.98
voltage_datalogger_adc0	trial_2	60.06	60.94	60.94	41.48
voltage_datalogger_adc0	trial_3	40.95	40.39	40.39	29.14
voltage_datalogger_adc2	trial_0	10.77	10.77	10.77	12.02
voltage_datalogger_adc2	trial_1	14.13	17.52	17.52	12.07
voltage_datalogger_adc2	trial_2	16.99	13.69	13.69	13.34
voltage_datalogger_adc2	trial_3	13.87	13.84	13.84	15.88
voltage_datalogger_afe	trial_0	74.37	65.55	66.07	77.93
voltage_datalogger_afe	trial_1	72.9	65.11	65.11	78.01
voltage_datalogger_afe	trial_2	-	88.5	66.87	76.72
voltage_datalogger_afe	trial_3	81.94	80.99	80.99	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_0	49.94 ± 13.12 (4)	48.5 ± 11.13 (4)	47.76 ± 12.07 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624534_0	13.94 ± 2.2 (4)	13.95 ± 2.39 (4)	13.95 ± 2.39 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624534_0	76.4 ± 3.96 (3)	75.04 ± 10.07 (4)	69.76 ± 6.51 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682624534_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	47.93	47.52	47.52	30.87
voltage_datalogger_adc0	trial_1	43.82	40.5	39.96	25.52
voltage_datalogger_adc0	trial_2	34.8	32.85	32.85	36.03
voltage_datalogger_adc0	trial_3	61.87	61.87	61.87	28.57
voltage_datalogger_adc2	trial_0	15.2	15.2	15.2	12.81
voltage_datalogger_adc2	trial_1	15.65	15.65	15.52	12.18
voltage_datalogger_adc2	trial_2	14.9	13.2	12.98	13.9
voltage_datalogger_adc2	trial_3	16.36	15.92	15.92	12.85
voltage_datalogger_afe	trial_0	62.54	61.88	61.78	49.34
voltage_datalogger_afe	trial_1	69.14	66.28	64.33	49.26
voltage_datalogger_afe	trial_2	60.64	60.01	59.69	45.1
voltage_datalogger_afe	trial_3	77.98	76.78	76.78	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_1	47.1 ± 9.76 (4)	45.68 ± 10.69 (4)	45.55 ± 10.76 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624534_1	15.53 ± 0.55 (4)	14.99 ± 1.07 (4)	14.9 ± 1.14 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624534_1	67.58 ± 6.79 (4)	66.24 ± 6.5 (4)	65.65 ± 6.64 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_1

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	53.43	52.93	52.93	58.96
voltage_datalogger_adc0	trial_1	74.31	54.15	44.1	25.98
voltage_datalogger_adc0	trial_2	35.03	33.38	33.38	41.48
voltage_datalogger_adc0	trial_3	80.6	80.6	80.6	29.14
voltage_datalogger_adc2	trial_0	13.89	13.89	13.89	12.02
voltage_datalogger_adc2	trial_1	18.96	18.96	19.1	12.07
voltage_datalogger_adc2	trial_2	13.37	10.9	10.8	13.34
voltage_datalogger_adc2	trial_3	19.87	19.69	19.69	15.88
voltage_datalogger_afe	trial_0	78.24	78.74	76.93	77.93
voltage_datalogger_afe	trial_1	86.29	79.61	74.3	78.01
voltage_datalogger_afe	trial_2	84.35	63.53	66.32	76.72
voltage_datalogger_afe	trial_3	89.72	97.61	97.61	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_1	60.84 ± 17.98 (4)	55.26 ± 16.79 (4)	52.75 ± 17.5 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624534_1	16.52 ± 2.92 (4)	15.86 ± 3.63 (4)	15.87 ± 3.7 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624534_1	84.65 ± 4.17 (4)	79.87 ± 12.07 (4)	78.79 ± 11.55 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682624534_2

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	38.29	37.0	36.58	30.87
voltage_datalogger_adc0	trial_1	41.22	38.58	37.77	25.52
voltage_datalogger_adc0	trial_2	-	32.02	32.02	36.03
voltage_datalogger_adc0	trial_3	63.13	62.75	62.75	28.57
voltage_datalogger_adc2	trial_0	12.91	12.55	12.16	12.81
voltage_datalogger_adc2	trial_1	15.24	15.14	15.14	12.18
voltage_datalogger_adc2	trial_2	13.54	13.04	12.53	13.9
voltage_datalogger_adc2	trial_3	17.4	16.9	16.9	12.85
voltage_datalogger_afe	trial_0	54.95	53.28	53.28	49.34
voltage_datalogger_afe	trial_1	70.87	47.8	46.07	49.26
voltage_datalogger_afe	trial_2	60.46	58.84	58.63	45.1
voltage_datalogger_afe	trial_3	59.32	58.74	58.59	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_2	47.55 ± 11.08 (3)	42.59 ± 11.89 (4)	42.28 ± 12.01 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624534_2	14.77 ± 1.74 (4)	14.41 ± 1.74 (4)	14.18 ± 1.94 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624534_2	61.4 ± 5.84 (4)	54.67 ± 4.56 (4)	54.14 ± 5.14 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_2

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	42.73	37.42	36.82	58.96
voltage_datalogger_adc0	trial_1	49.89	47.42	45.6	25.98
voltage_datalogger_adc0	trial_2	-	34.75	34.75	41.48
voltage_datalogger_adc0	trial_3	74.85	80.57	80.57	29.14
voltage_datalogger_adc2	trial_0	11.11	10.53	10.39	12.02
voltage_datalogger_adc2	trial_1	16.69	16.61	16.61	12.07
voltage_datalogger_adc2	trial_2	16.34	14.21	15.05	13.34
voltage_datalogger_adc2	trial_3	23.92	25.41	25.41	15.88
voltage_datalogger_afe	trial_0	60.16	53.94	53.94	77.93
voltage_datalogger_afe	trial_1	81.93	51.01	48.72	78.01
voltage_datalogger_afe	trial_2	73.33	87.12	86.2	76.72
voltage_datalogger_afe	trial_3	81.23	79.49	79.8	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_2

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_2	55.82 ± 13.77 (3)	50.04 ± 18.25 (4)	49.44 ± 18.43 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624534_2	17.02 ± 4.56 (4)	16.69 ± 5.48 (4)	16.86 ± 5.44 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624534_2	74.16 ± 8.76 (4)	67.89 ± 15.68 (4)	67.17 ± 16.1 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

ablation_experiment_208:1682624534_3

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 0.0

Overlap (o) = 8.0

Estimated Wirelength (HPWL)

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	52.18	52.18	52.18	30.87
voltage_datalogger_adc0	trial_1	43.84	43.84	43.55	25.52
voltage_datalogger_adc0	trial_2	40.27	39.6	39.5	36.03
voltage_datalogger_adc0	trial_3	44.75	41.88	41.88	28.57
voltage_datalogger_adc2	trial_0	12.98	12.57	12.57	12.81
voltage_datalogger_adc2	trial_1	15.03	14.37	14.37	12.18
voltage_datalogger_adc2	trial_2	13.46	13.27	13.27	13.9
voltage_datalogger_adc2	trial_3	15.4	14.41	14.41	12.85
voltage_datalogger_afe	trial_0	59.52	59.31	59.22	49.34
voltage_datalogger_afe	trial_1	53.72	52.26	52.26	49.26
voltage_datalogger_afe	trial_2	57.54	55.92	55.18	45.1
voltage_datalogger_afe	trial_3	69.22	66.61	66.12	50.63

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_3	45.26 ± 4.33 (4)	44.38 ± 4.75 (4)	44.28 ± 4.78 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1682624534_3	14.22 ± 1.02 (4)	13.65 ± 0.78 (4)	13.65 ± 0.78 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1682624534_3	60.0 ± 5.72 (4)	58.53 ± 5.29 (4)	58.2 ± 5.2 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Raw trial data for run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_3

pcb name	trial	0% overlap	10% overlap	20% overlap	sa_pcb
voltage_datalogger_adc0	trial_0	63.61	63.61	63.61	58.96
voltage_datalogger_adc0	trial_1	43.21	43.21	56.46	25.98
voltage_datalogger_adc0	trial_2	38.95	38.42	38.31	41.48
voltage_datalogger_adc0	trial_3	47.42	58.7	58.7	29.14
voltage_datalogger_adc2	trial_0	11.71	11.36	11.36	12.02
voltage_datalogger_adc2	trial_1	19.19	18.13	18.13	12.07
voltage_datalogger_adc2	trial_2	16.18	12.74	12.74	13.34
voltage_datalogger_adc2	trial_3	18.33	18.61	18.61	15.88
voltage_datalogger_afe	trial_0	72.79	66.34	65.17	77.93
voltage_datalogger_afe	trial_1	55.47	53.32	53.32	78.01
voltage_datalogger_afe	trial_2	70.94	71.25	70.08	76.72
voltage_datalogger_afe	trial_3	87.73	74.19	76.08	68.54

Mean over all trials in run //home/luke/work/rl_pcb/experiments/02_ablation_experiments/work/eval_testing_set/1682624534_3

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1682624534_3	48.3 ± 9.33 (4)	50.98 ± 10.46 (4)	54.27 ± 9.57 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1682624534_3	16.35 ± 2.9 (4)	15.21 ± 3.2 (4)	15.21 ± 3.2 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1682624534_3	71.73 ± 11.43 (4)	66.28 ± 7.99 (4)	66.16 ± 8.36 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed