Experiment Report

Start of automated test report 2023-05-23 16:06:11
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Machine Information

sysname=Linux
nodename=workstation
release=5.19.0-41-generic
version=#42~22.04.1-Ubuntu SMP PREEMPT_DYNAMIC Tue Apr 18 17:40:00 UTC 2
machine=x86_64

CPU arch : X86_64
CPU bits : 64
CPU brand : Intel(R) Core(TM) i7-10700K CPU @ 3.80GHz
CPU cores : 8
CPU base clock : 3.8000 GHz
CPU boost clock : 3.7920 GHz
System Memory : 31.35GB
Nvidia driver version : 525.105.17
Device 0 : NVIDIA GeForce GTX 1080
Device 0 : 8.0GB

Library Information

python : 3.8.16
torch : 1.13.1+cu117
optuna : 3.1.1
numpy : 1.23.3
pandas : 2.0.1
matplotlib : 3.7.1
seaborn : 0.12.2

pcb library: generation of .pcb files.
Library version : 0.0.12
Library built with : C++14
Library built on : Mar 3 2023 23:10:31

netlist_graph: Graph pre-processing library for PCB component placement.
Library version : 0.1.16
Library built with : C++14
Library built on : Mar 3 2023 23:10:32

training_td3_cuda_262:1684831023_0

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/gitlab-runner/builds/TfLwHVT9/0/luke/rl_pcb/tests/05_training_td3_cuda_fast/work/eval_testing_set/1684831023_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1684831023_0	39.68 ± 0.0 (1)	49.11 ± 9.24 (3)	43.82 ± 8.67 (4)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1684831023_0	16.07 ± 2.55 (4)	15.11 ± 3.09 (4)	14.78 ± 3.3 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1684831023_0	59.0 ± 1.98 (2)	60.27 ± 3.64 (3)	58.82 ± 3.41 (4)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/gitlab-runner/builds/TfLwHVT9/0/luke/rl_pcb/tests/05_training_td3_cuda_fast/work/eval_testing_set/1684831023_0

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1684831023_0	46.82 ± 0.0 (1)	54.43 ± 7.58 (3)	51.07 ± 11.4 (4)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1684831023_0	13.88 ± 2.71 (4)	15.8 ± 1.88 (4)	14.52 ± 2.61 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1684831023_0	76.15 ± 1.81 (2)	74.28 ± 3.66 (3)	75.46 ± 7.13 (4)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

training_td3_cuda_262:1684831023_1

Steps per trial = 600

Euclidean wirelength (w) = 2

Half perimeter wirelength (hpwl) = 6.0

Overlap (o) = 2.0

Estimated Wirelength (HPWL)

Mean over all trials in run //home/gitlab-runner/builds/TfLwHVT9/0/luke/rl_pcb/tests/05_training_td3_cuda_fast/work/eval_testing_set/1684831023_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1684831023_1	nan ± nan (0)	nan ± nan (0)	40.33 ± 0.0 (1)	30.25 ± 3.84 (4)
voltage_datalogger_adc2	1684831023_1	16.86 ± 1.89 (4)	16.49 ± 1.74 (4)	15.48 ± 1.32 (4)	12.94 ± 0.62 (4)
voltage_datalogger_afe	1684831023_1	61.7 ± 0.0 (1)	61.7 ± 0.0 (1)	63.82 ± 2.12 (2)	48.58 ± 2.08 (4)

[1] # indicates the number of layouts over which the mean ± std was computed

Routed Wirelength

Mean over all trials in run //home/gitlab-runner/builds/TfLwHVT9/0/luke/rl_pcb/tests/05_training_td3_cuda_fast/work/eval_testing_set/1684831023_1

pcb name	run	0% overlap (#)[1]	10% overlap (#)[1]	20% overlap (#)[1]	simulated annealing
voltage_datalogger_adc0	1684831023_1	nan ± nan (0)	nan ± nan (0)	46.12 ± 0.0 (1)	38.89 ± 12.95 (4)
voltage_datalogger_adc2	1684831023_1	17.24 ± 4.14 (4)	17.33 ± 4.47 (4)	17.02 ± 4.29 (4)	13.33 ± 1.57 (4)
voltage_datalogger_afe	1684831023_1	68.62 ± 0.0 (1)	68.62 ± 0.0 (1)	72.16 ± 3.53 (2)	75.3 ± 3.94 (4)

[1] # indicates the number of layouts over which the mean ± std was computed