9) 105 MCQ
10) 60 MCQ

subject_code	unit_number	chapter_number	group_id	keyword	question_text	answer_text	marks	option1	option2	option3	option4	option 5	option 6
017013493	9	9	1	boooth's algorithm	Which of the following is used for binary multiplication ?	b	1	Restroing Multiplication	Booth's Algorithm	Pascal's Algorithm	Digit by Digit Multiplication		
017013493	9	9	2	boooth's algorithm	Booth’s Algorithm is applied on _____	b	1	decimal numbers	binary numbers	hexadecimal numbers	octal Numbers		
017013493	9	9	3	boooth's algorithm	If Booth’s Multiplication is performed on the numbers 22*3, then what is 3 referred to as _____	d	1	accumulator	multiplicand	quotient	multiplier		
017013493	9	9	4	boooth's algorithm	What is the value of n in multiplication of 110* 1000?	c	1	2	3	4	0		
017013493	9	9	5	boooth's algorithm	What will be the value obtained after multiplication of (-2) * (-3) using Booth’s Algorithm?	a	1	6	-6	-2	-3		
017013493	9	9	6	boooth's algorithm	What does the data transfer instruction STA stand for?	a	1	Store Accumulator	Send Accumulator	Send Action	Store Action		
017013493	9	9	7	boooth's algorithm	In Booth multiplication algorithm initially value for Q -1 ?	a	1	0	1	11	10		
017013493	9	9	8	boooth's algorithm	In Booth multiplication algorithm initially value for AC ?	a	1	0	1	11	10		
017013493	9	9	9	boooth's algorithm	In Booth multiplication algorithm if value of Q0 is 0 and value of Q-1 is 0 so what will be next step ?	a	1	ASR	A= A+M	N = N-1	A = A-M		
017013493	9	9	10	boooth's algorithm	In Booth multiplication algorithm if value of Q0 is 0 and value of Q-1 is 1 so what will be next step ?	a	1	A= A+M	ASR	A = A-M	N = N-1		
017013493	9	9	11	boooth's algorithm	In Booth multiplication algorithm if value of Q0 is 1 and value of Q-1 is 0 so what will be next step ?	c / B	1	N = N-1	A = A-M	ASR	A= A+M		
017013493	9	9	12	boooth's algorithm	In Booth multiplication algorithm if value of Q0 is 1 and value of Q-1 is 1 so what will be next step ?	d	1	A = A-M	N = N-1	A= A+M	ASR		
017013493	9	9	13	boooth's algorithm	In Booth Division algorithm if AC < 0 what will be next operation ?	b	1	Q0←1	Q0← 0, A←A+M	COUNT ← COUNT-1	A←A+M		
017013493	9	9	14	boooth's algorithm	In Booth Division algorithm if AC > 0 what will be next step ?	d	1	COUNT ← COUNT-1	A←A+M	Q0←1 , A←A+M	Q0←1		
017013493	9	9	15	boooth's algorithm	for (7)10 × (3)10 using booth's algorithm, what will be final data in binary in accumlator for sequence count 4?	c	1	1111	1001	1100	1010		
017013493	9	9	16	boooth's algorithm	for (-9)10 × (-13)10 using booth's algorithm, what will be final data in binary in accumlator for sequence count 4?	c	1	1011	1111	10	1010		
017013493	9	9	17	boooth's algorithm	for (-5)10 × (4)10 using booth's algorithm, what will be final data in binary in accumlator for sequence count 2?	c	1	1011	1111	10	10		
017013493	9	9	18	boooth's algorithm	for (13)10 × (9)10 using booth's algorithm, what will be final value in binary in Q for sequence count 4?	d	1	11011	1111	1011	1010		
017013493	9	9	19	boooth's algorithm	for (23)10 × (-7)10 using booth's algorithm, what will be final value in binary in Q for sequence count 6?	b	1	101110	111100	111	111001		
017013493	9	9	20	boooth's algorithm	for (-7)10 × (-3)10 using booth's algorithm, what will be final value in binary in Q for sequence count 4?	b	1	1100	1110	110	1010		
017013493	9	9	21	boooth's algorithm	for (7)10 / (3)10 using booth's algorithm, what will be final data in binary in accumlator for sequence count 4 ?	b	1	10	0	1101	1011		
017013493	9	9	22	boooth's algorithm	for (11)10 / (3)10 using booth's algorithm, what will be final data in binary in accumlator for sequence count 3 ?	c	1	101	1101	1	1100		
017013493	9	9	23	boooth's algorithm	for (23)10 / (5)10 using booth's algorithm, what will be final data in binary in accumlator for sequence count 5 ?	a	1	1	10101	110	11111		
017013493	9	9	24	boooth's algorithm	for (7)10 / (3)10 using booth's algorithm, hat will be final value in binary in Q for sequence count 4 ?	a	1	1110	101	1010	11		
017013493	9	9	25	boooth's algorithm	for (11)10 / (3)10 using booth's algorithm, hat will be final value in binary in Q for sequence count 3 ?	c	1	101	1101	1100	1111		
017013493	9	9	26	boooth's algorithm	for (10)10 / (3)10 using booth's algorithm, hat will be final value in binary in Q for sequence count 4 ?	d	1	1101	11	1010	100		
017013493	9	9	27	boooth's algorithm	Perform booth multiplication for given numbers having register size of four bits. Multiplicand : (2)10 Multiplier : (3)10 Convert final result in decimal.		5						

017013493	9	9	28	boooth's algorithm	Perform booth multiplication for given numbers having register size of four bits. Multiplicand : (7)10 Multiplier : (3)10 Convert final result in decimal.		5							
017013493	9	9	29	boooth's algorithm	Perform booth multiplication for given numbers having register size of four bits. Multiplicand : (7)10 Multiplier : (-3)10 Convert final result in decimal.		5							
017013493	9	9	30	boooth's algorithm	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (-7)10 Multiplier : (3)10 Convert final result in decimal.		5							
017013493	9	9	31	boooth's algorithm	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (-7)10 Multiplier : (-3)10 Convert final result in decimal.		5							
017013493	9	9	32	boooth's algorithm	Perform booth multiplication for given numbers having register size of four bits. Multiplicand : (-5)10 Multiplier : (-4)10 Convert final result in decimal.		5							
017013493	9	9	33	boooth's algorithm	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (9)10 Multiplier : (13)10 Convert final result in decimal.		5							
017013493	9	9	34	boooth's algorithm	Perform booth multiplication for given numbers having register size of five bits. Multiplicand : (9)10 Multiplier : (-13)10 Convert final result in decimal.		5							
017013493	9	9	35	boooth's algorithm	Perform booth multiplication for given numbers having register size of five bits. Multiplicand : (-9)10 Multiplier : (13)10 Convert final result in decimal.		5							
017013493	9	9	36	boooth's algorithm	Perform booth multiplication for given numbers having register size of five bits. Multiplicand : (-9)10 Multiplier : (-13)10 Convert final result in decimal.		5							
017013493	9	9	37	boooth's algorithm	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (23)10 Multiplier : (-5)10 Convert final result in decimal.		5							
017013493	9	9	38	boooth's algorithm	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (23)10 Multiplier : (-7)10 Convert final result in decimal.		5							
017013493	9	9	39	boooth's algorithm	Perform booth multiplication for given numbers having register size of six bits. Multiplicand : (25)10 Multiplier : (-7)10 Convert final result in decimal.		5							
017013493	9	9	40	boooth's algorithm	Perform booth division for given numbers having register size of Four bits. Dividend : (7)10 Divisor : (3)10 Convert final result in decimal.		5							
017013493	9	9	41	boooth's algorithm	Perform booth division for given numbers having register size of Four bits. Dividend : (10)10 Divisor : (3)10 Convert final result in decimal.		5							
017013493	9	9	42	boooth's algorithm	Perform booth division for given numbers having register size of Four bits. Dividend : (11)10 Divisor : (3)10 Convert final result in decimal.		5							
017013493	9	9	43	boooth's algorithm	Perform booth division for given numbers having register size of Four bits. Dividend : (14)10 Divisor : (4)10 Convert final result in decimal.		5							

017013493	9	9	44	boooth's algorithm	Perform booth division for given numbers having register size of Five bits. Dividend : (23)10 Divisor : (5)10 Convert final result in decimal.		5						
017013493	9	9	45	boooth's algorithm	Perform booth division for given numbers having register size of Five bits. Dividend : (23)10 Divisor : (7)10 Convert final result in decimal.		5						
017013493	9	9	46	boooth's algorithm	Perform booth division for given numbers having register size of Five bits. Dividend : (25)10 Divisor : (7)10 Convert final result in decimal.		5						
017013493	9	9	47	Hit miss ratio	What is the formula for Hit Ratio?	A	1	Hit/(Hit + Miss)	Miss/(Hit + Miss)	(Hit + Miss)/Miss	(Hit + Miss)/Hit		
017013493	9	9	48	Hit miss ratio	If cache has 51 hits and 3 misses over a period of time. What will be hit and miss ratio of cache ?	C	1	a) 10%, 90%	b) 6%, 94%	c) 94%, 6%	d) 90%, 10%		
017013493	9	9	49	Hit miss ratio	If cache has 55 hits and 45 misses over a period of time. What will be hit and miss ratio of cache ?	C	1	a) 55%, 65%	b) 45%, 55%	c) 55%, 45%	d) 55%, 55%		
017013493	9	9	50	Hit miss ratio	If cache has 89 hits and 71 misses over a period of time. What will be hit and miss ratio of cache ?	C	1	a) 55%, 65%	b) 45%, 55%	c) 55%, 45%	d) 55%, 55%		
017013493	9	9	51	Memory Hierarchy	Show memory interfacing with CPU along with memory address map for one 128*8 RAM and one 512*8 ROM using chip select pins. Take starting address map as 0840 H.		3						
017013493	9	9	52	Memory Hierarchy	Show memory interfacing with CPU along with memory address map for four 128*8 RAM and one 512*8 ROM using chip select pins. Take starting address map as 0000 H.		3						
017013493	9	9	53	Memory Hierarchy	Given RAM of 64KB byte size having starting address 00000 H find ending address.		3						
017013493	9	9	54	Memory Hierarchy	Given RAM of 32KB byte size having starting address 00000 H find ending address.		3						
017013493	9	9	55	Memory Hierarchy	Given RAM of 64KB byte size having starting address FFFF H find ending address.		3						
017013493	9	9	56	Memory Hierarchy	Given RAM of 32KB byte size having starting address FFFF H find ending address.		3						
017013493	9	9	57	Memory Hierarchy	If starting address of ROM is 3000 H having 1K size find ending address .		3						
017013493	9	9	58	Memory Hierarchy	Given RAM of 4K byte size having starting address 0000 H find ending address.		3						
017013493	9	9	59	Memory Hierarchy	Given RAM of 1K byte size having starting address 2000 H find ending address.		3						
017013493	9	9	60	Memory Hierarchy	Given RAM of 32KB byte size having starting address 8000 H find ending address.		3						
017013493	9	9	61	Memory Hierarchy	The memory unit that communicates directly with CPU is called the _____.	A	1	a) Main mamory	b) secondary memory	c) cache memory	d) auxilary memory		
017013493	9	9	62	Memory Hierarchy	the typical access time ratio between cache and main memory is about _____?	C	1	a) 1 to 9	B)1 to 10	c) 1 to 7	d) 10 to 15		
017013493	9	9	63	Memory Hierarchy	Which of the following statements is/are correct ? 1. The CPU has direct access to main memory. 2. The CPU has direct access to cache memory. 3. The CPU has direct access to auxillary memory.	d	1	a) only 1 and 3	b) only 2 and 3	c) only 1	d) only 1 and 2		
017013493	9	9	64	Memory Hierarchy	Block size in auxillary memory typically ranges from _____?	b	1	a) 248 to 256 words	b) 256 to 2048 words	c) 148 to 248 words	d) 256 to 278 words		
017013493	9	9	65	Memory Hierarchy	Block size in cache memory typically ranges from _____?	a	1	a) 1 to 16 words	b) 8 to 16 words	c) 16 to 24 words	d) 7 to 15 words		
017013493	9	9	66	Memory Hierarchy	Device that provide back-up storage are called _____?	d	1	a) Main mamory	b) secondary memory	c) cache memory	d) auxilary memory		
017013493	9	9	67	Memory Hierarchy	A very special high speed memory called a_____?	c	1	a) Main mamory	b) secondary memory	c) cache memory	d) auxilary memory		
017013493	9	9	68	Memory Hierarchy	in which memory design highest memory capacity and access time ?	a	1	a) Magnatics tapes	b) auxilary memory	c) secondary memory	d) cache memory		
017013493	9	9	69	Memory Hierarchy	in which memory design lowest memory capacity and access time ?	b	1	a) Magnatics tapes	b) CPU Register	c) secondary memory	d) cache memory		
017013493	9	9	70	Memory Hierarchy	Average acces time of auxillary memory is usually _____ than of main memory.	c	1	a) 10 times	b) 100 times	c) 1000 times	d) 10000 times		

017013493	9	9	71	Memory Hierarchy	which RAM is design with flip-flop ?	b	1	a) Dynamic RAM	b) Static RAM	c) ROM	d) None of above		
017013493	9	9	72	Memory Hierarchy	which type of memory have a highest storage capacity in single memory chip?	a	1	a) Dynamic RAM	b) Static RAM	c) ROM	d) None of above		
017013493	9	9	73	Memory Hierarchy	_____ is shortest read and write time ?	b	1	a) Dynamic RAM	b) Static RAM	c) ROM	d) None of above		
017013493	9	9	74	Memory Hierarchy	which program is use to start computer software operating when power turn on ?	a	1	a) bootstrap loader	b) Static RAM	c) ROM	d) Dynamic RAM		
017013493	9	9	75	Memory Hierarchy	_____is non-volatile memory.	b	1	a) RAM	b) ROM	c) CPU	d) None of above		
017013493	9	9	76	Memory Hierarchy	_____is volatile memory.	a	1	a) RAM	b) ROM	c) CPU	d) None of above		
017013493	9	9	77	Memory Hierarchy	which device is used to provide backup storage ?	b	1	a) Virtual memory	b) Auxillary memory	c) Cache memory	d) Associative memory		
017013493	9	9	78	Memory Hierarchy	the tracks are divided into sections is called ?	c	1	a) Seek time	b) latency time	c) Sectors	d) Sub-operation		
017013493	9	9	79	Memory Hierarchy	bitas are stored in megnatize surface is called ?	b	1	a) Seek time	b) Read write head	c) ROM	d) cache memory		
017013493	9	9	80	Memory Hierarchy	which memory search time is short and critical ?	a	1	a) Associate memory	b) Auxillary memory	c) Cache memory	d) Virtual memory		
017013493	9	9	81	Memory Hierarchy	cache memory access time is _____times lesser than main memory.	c	1	a) 15 to 20	b) 22 to 27	c) 5 to 10	d) 20 to 28		
017013493	9	9	82	Memory Hierarchy	fast and small memory is referred as ?	c	1	a) Virtual memory	b) Auxillary memory	c) Cache memory	d) Associative memory		
017013493	9	9	83	Memory Hierarchy	_____ is placed between memory and CPU.	c	1	a) Virtual memory	b) Auxillary memory	c) Cache memory	d) Associative memory		
017013493	9	9	84	Memory Hierarchy	performance of cache memory is measured in terms of quantity callled ?	a	1	a) Hit ratio	b) Miss ratio	c) Seek ratio	d) None of above		
017013493	9	9	85	Memory Hierarchy	CPU refers memory, if the word is in cache, it will produce a _____ if word not found in cache and it is in main memory then it counts as a _____.	b	1	a) Hit, Hit	b) hit,miss	c) Miss, Hit	d) Miss, Miss		
017013493	9	9	86	Memory Hierarchy	The time taken to move the read write head to the desired track is known as _____.	b	1	a) latency time	b) seek time	c) data transfer rate	d) access time		
017013493	9	9	87	Memory Hierarchy	_____ is the time required to bring the starting position of the address sector of the track to come under read/write head.	a	1	a) latency time	b) seek time	c) data transfer rate	d) access time		
017013493	9	9	88	Memory Hierarchy	The rate at which data is written to disk or read from disk is known as ?	c	1	a) latency time	b) seek time	c) data transfer rate	d) access time		
017013493	9	9	89	Memory Hierarchy	Memory Access time is given by ?	b	1	a) seek time * latency time	b) seek time + latency time	c) seek time - latency time	d) seek time / latency time		
017013493	9	9	90	Memory Hierarchy	Every word stored in cache there is duplicate copy in _____?	a	1	a) Main mamory	b) secondary memory	c) cache memory	d) auxilary memory		
017013493	9	9	91	Memory Hierarchy	in associative mapping pair replace is determine from which algorithm.	a	1	a) Replacement	b) displacement	c) location	d) None of above		
017013493	9	9	92	Memory Hierarchy	Which of the given procedure is used to replace cell of cache ?	a	1	a) Round-robin	b) Robin-round	c) Robin-Robin	d) Round-Round		
017013493	9	9	93	Memory Hierarchy	Word is requested from main memory it constitutes a _____ replacement policy.	d	1	a) LIFO	b) PIFO	c) SIFO	d) FIFO		
017013493	9	9	94	Memory Hierarchy	In direct mapping, n-bit memory address is divided into _____ part.	b	1	a) 1	b) 2	c) 3	d) 4		
017013493	9	9	95	Memory Hierarchy	The n-bits divided into 2 fields k bits for _____ and n-k bits for _____.	c	1	a) index field , index field	b) Tag field , Tag field	c) index field , Tag field	d) None of above		
017013493	9	9	96	Memory Hierarchy	Direct mapping 2^k words in _____ and 2^n words in _____.	a	1	a) cache memory, Main memory	b) main Memory, Cache memory	c) SRAM	d) DRAM		
017013493	9	9	97	Memory Hierarchy	In Direct mapping, ___ words in cache memory and _____words in main memory.	c	1	a) 2^x, 2^y	b) 2^n, 2^k	c) 2^k, 2^n	d) 2^s, 2^{kt}		
017013493	9	9	98	Memory Hierarchy	Direct Mapping the CPU address of ___bits is divided in _____ parts.	a	1	a) 15, 2	b) 14, 2	c) 20, 3	d) 15, 1		
017013493	9	9	99	Memory Hierarchy	In Direct mapping ____ bits constitute the index field and remaining _____ bits from the tag field.	b	1	a) nine, four	b) nine, six	c) six, nine	d) nine,six		
017013493	9	9	100	Memory Hierarchy	Direct mapping nine bits constitute the _____ and remaining six bits from the _____.	c	1	a) index field , index field	b) Tag field , Tag field	c) index field , Tag field	d) None of above		

017013493	9	9	101	Memory Hierarchy	Which of the following techniques are used in associative mapping. 1) random replacement 2) first in frist out 3) last in first out 4) least recently used 5) last in last out	d	1	a) Only 3),4) and 5)	b) Only 1),2)	c) Only 1),2) and 5)	d) Only 1),2) and 4)		
017013493	9	9	102	Memory Hierarchy	Main memory always contains same data as _____.	d	1	a) Associative Memory	b) Magnatic disc	c) Auxillary Memory	d) Cache Memory		
017013493	9	9	103	Memory Hierarchy	_____ location is updated during write operation in write back.	b	1	a) Auxillary	b) Cache	c) Main	d) None of above		
017013493	9	9	104	Memory Hierarchy	To overcome the slow operating speeds of the secondary memory we make use of faster flash drives.	A	1	TRUE	FALSE	-	-		
017013493	9	9	105	Memory Hierarchy	The fastest data access is provided using _____.	D	1	Caches	DRAM's	SRAM's	Registers		
017013493	9	9	106	Memory Hierarchy	What is true about memory unit?	C	1	A memory unit is the collection of storage units or devices together.	The memory unit stores the binary information in the form of bits.	Both A and B	None of the above		
017013493	9	9	107	Memory Hierarchy	When when power is switched off which memory loses its data?	B	1	Non-Volatile Memory	Volatile Memory	Both A and B	None of the above		
017013493	9	9	108	Memory Hierarchy	Auxillary memory access time is generally _____ times that of the main memory.	C	1	10	100	1000	10000		
017013493	9	9	109	Memory Hierarchy	Which of the following is correct example for Auxiliary Memory?	D	1	Magnetic disks	Tapes	Flash memory.	Both A and B		
017013493	9	9	110	Memory Hierarchy	Which of the following is correct refreshed rate for DRAM?	C	1	10-1000 ms	10-50 ms	10-100 ms	10-500 ms		
017013493	9	9	111	Memory Hierarchy	Which of the following is true?	A	1	To overcome the slow operating speeds of the secondary memory we make use of faster flash drives.	If we use the flash drives instead of the harddisks, then the secondary storage can go above primary memory in the hierarchy.	In the memory hierarchy, as the speed of operation increases the memory size also increases.	Both A and C		
017013493	9	9	112	Memory Hierarchy	____ number of lines are required to select _____ memory locations.	A	1	10, 1024	2, 2	5, 1024	5, 5K		
017013493	9	9	113	Memory Hierarchy	Calculate the address lines required for 8 Kilobyte memory chip?	B	1	8	13	16	24		
017013493	9	9	114	Memory Hierarchy	1 gigabyte is equal to ?	C	1	1391 megabytes	1024 kilobytes	1024 megabytes	1150 megabytes		
017013493	9	9	115	Memory Hierarchy	_____ is the fastest to read from and write to than the other kinds of storage in a computer.	D	1	Floppy disk	Hard disk	CD-ROM	RAM		
017013493	9	9	116	Memory Hierarchy	Which of the following is a volatile memory?	A	1	Cache memory	Hard Disk	DVD	CD		
017013493	9	9	117	Memory Hierarchy	The CPU clock speed refers to the number of:	D	1	CPUs it can have	RAMs it can have	Clocks it can have	Number of cycles CPU executes per second		
017013493	9	9	118	Memory Hierarchy	A 26-bit address bus has maximum accessible memory capacity of _____.	A	1	64 MB	16 MB	1 GB	4 GB		
017013493	9	9	119	Memory Hierarchy	Which of the following memory improves the speed of execution of a program?	B	1	Primary memory	Cache memory	Secondary memory	Virtual memory		
017013493	9	9	120	Memory Hierarchy	Which of the following is not a valid category of Read Only Memory (ROM)?	D	1	PROM	EPROM	EEPROM	EEEPROM		
017013493	9	9	121	Memory Hierarchy	A byte is a group of ?	C	1	2 bits	4 bits	8 bits	16 bits		
017013493	9	9	122	Secondary Memory	Static RAM (SRAM) is faster than Dynamic RAM (DRAM) because _____.	C	1	SRAM uses capacitors	SRAM is costlier	SRAM does not require refreshing	SRAM is cheaper		
017013493	9	9	123	Secondary Memory	_____ refers to the amount of time required to position the read - white head of a hard disk on appropriate sector.	A	1	Seek time	Rotational latency	Access time	Load time		
017013493	9	9	124	Secondary Memory	A hard disk is divided into tracks which are further subdivided into ?	B	1	clusters	sectors	vectors	heads		
017013493	9	9	125	Type of RAMS	How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes?	D	1	2	8	4	16		

017013493	9	9	126	Type of RAMS	Which of the following sets of words best describes the characteristics of a primary storage device, like RAM.	C	1	Cheap, non-volatile, fast access	Volatile, expensive, slow access	Expensive, volatile, fast access	Fast access, non-volatile, cheap		
017013493	9	9	127	Type of RAMS	Which of the following memories must be refreshed many times per second?	B	1	Static RAM	Dynamic RAM	EPROM	ROM		
017013493	9	9	128	Type of RAMS	A computer uses RAM chips of 1024 × 1 capacity. How many chips are needed to provide memory capacity of 16K bytes?	D	1	8	16	1024	128		
017013493	9	9	129	Type of RAMS	How many 32 K × 1 RAM chips are needed to provide a memory capacity of 256 K-bytes ?	C	1	8	32	64	128		
017013493	9	9	130	Type of RAMS	Among the following the volatile memory is	B	1	Bubble memory	RAM	ROM	Magnetic disc		
017013493	9	9	131	Type of RAMS	How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes?	D	1	2	8	4	16		
017013493	9	9	132	Type of RAMS	Which of the following technology can give high speed RAM?	B	1	TTL	CMOS	ECL	NMOS		
017013493	9	9	133	Type of RAMS	Which of the following sets of words best describes the characteristics of a primary storage device, like RAM.	A	1	Cheap, non-volatile, fast access	Volatile, expensive, slow access	Expensive, volatile, fast access	Fast access, non-volatile, cheap		

017013493	9	9	134	Type of RAMS	Consider the following statements regarding memory: 1. Integrated circuit RAM chips are available in both static and dynamic modes. 2. The dynamic RAM stores the binary information in the form of electric charges that are applied to capacitors. 3. The static RAM is easier to use and has shorter read and write cycles. 4. RAM and ROM chips are not available in a variety of physical sizes. Which of the above statements are correct ?	A	1	1 and 2 only	1, 3 and 4 only	2, 3 and 4 only	1, 2, 3 and 4		
017013493	9	9	135	Associative Mapping	Which of the following refers to the associative memory?	B	1	the address of the data is generated by the CPU	the address of the data is supplied by the users	there is no need for an address i.e. the data is used as an address	the data are accessed sequentially		
017013493	10	10	136	I/O devices	Input or output devices that are connected to computer are called _____	b	1	Input/Output Subsystem	Peripheral Devices	Interfaces	Interrupt		
017013493	10	10	137	Modes of transfer	How many types of modes of I/O Data Transfer?	d	1	2	4	5	3		
017013493	10	10	138	Peripheral devices	Which of the following statement/s is/are correct? (a) Keyboard and Mouse Comes under output periferal devices. (b) The method which offers higher speeds of I/O transfers is DMA (c) The data transfer rate of peripherals is usually slower than the transfer rate of the CPU	b	1	Only a and b	only b and c	only a	only c		
017013493	10	10	139	DMA	Which of the following is true about DMA? 1.DMA is an approach of performing data transfers in bulk between memory and the external device without the intervention of the processor 2. The DMA controller acts as a processor for DMA transfers and overlooks the entire process 3.The DMA controller has 3 registers.	a	1	All 1, 2 and 3	only 1 and 2	only 2	only 1 and 3		
017013493	10	10	140	Memory mapped I/O	In memory-mapped I/O _____	a	1	The I/O devices and the memory share the same address space	The I/O devices have a separate address space	The memory and I/O devices have an associated address space	A part of the memory is specifically set aside for the I/O operation		
017013493	10	10	141	DMA	The CPU activities the ..... output to inform the external DMA that the buses are in the high-impedance state.	b	1	Bus request	bus grant	cycle stealing	none of these		
017013493	10	10	142	I/O Interface	The main functions of input-output interface circuits is / are -	d	1	Data conversion	synchronization	device selection	all a,b and c		
017013493	10	10	143	I/O Interface	The process of matching of operating speeds of CPU and other peripherals is known as -	b	1	Data conversion	synchronization	device selection	cycle stealing		
017013493	10	10	144	I/O Bus	I/O bus consists of -	d	1	data lines	address lines	control lines	all a,b and c		
017013493	10	10	145	I/O Bus	Which of the following is/are correct regarding I/O bus? (a) The I/O bus from the processor is attached to all peripheral interfaces. (b) I/O bus consists of data lines and control lines only (c) I/O bus is used for the selection of I/O devices by CPU	c	1	only 1 and 2	only 2	only 1	All 1, 2 and 3		
017013493	10	10	146	I/O Bus	How many types of commands that an interface may receive?	c	1	2	3	4	5		
017013493	10	10	147	I/O Bus	Which of the given command is not a valid command for I/O interface?	d	1	Status command	control command	Data output command	Interrupt command		
017013493	10	10	148	I/O Bus	Which I/O command is issued to rewind the magnetic tape or to start the tape moving in the forward direction?	b	1	Status command	control command	Data output command	Data input command		
017013493	10	10	149	DMA	In which mode, the I/O module and main memory exchange data directly, without processor involvement ?	a	1	DMA	Programmed I/O	Interrupt I/O	both b and c		
017013493	10	10	150	I/O Bus	In which case the interface receives an item of data from the peripheral and places it in its buffer register?	d	1	Status command	control command	Data output command	Data input command		
017013493	10	10	151	I/O Bus	The control lines which are enabled during a memory transfer are -	a	1	memory read and memory write	I/O read and I/O write	Interrupt enable and disable	both a and b		
017013493	10	10	152	I/O Bus	In which configuration only one set of read and write signals employed ?	a	1	Memory mapped I/O	Isolated I/O	Interrupt Initiated I/O	both a and b		
017013493	10	10	153	Memory mapped I/O	Which type of instructions are used by Computers with memory-mapped I/0 to access I/0 data?	b	1	Register type	Memory type	I/O type	none of the above		
017013493	10	10	154	I/O Interface	What is the difference between isolated and memory-mapped I/O?		2						
017013493	10	10	155	I/O Bus	Match the following: 1. Skip next instruction if flag is set. P - Data input command 2. Read interface status register. Q - Control command 3. Move printer paper to beginning of next page. R - Status command	C	1	1-P, 2-Q, 3-R	1-Q, 2-P, 3-R	1-R, 2-P, 3-Q	1-P, 2-R, 3-Q		
017013493	10	10	156	Asynchronous data transfer	If the registers in the interface share a common clock with the CPU registers, the transfer between the two units is said to be -	a	1	Synchronous data transfer	Asynchronous data transfer	Common data transfer	None of these		
017013493	10	10	157	Asynchronous data transfer	Which of the given methods are asynchronous data transfer method?	d	1	Handshaking Method	Strobe Pulse Method	cycle stealing	both a and b		
017013493	10	10	158	DMA	During DMA transfer, the DMA controller takes over the buses to manage the transfer -	d	1	Directly from CPU to memory	Directly from memory to CPU	Directly between the memory and registers	Directly between the I/O device and memory		

017013493	10	10	159	I/O processing	Priority is provided by _____ for access to memory by various I/O channels and processors.	c	1	a register	a counter	a controller	the processor scheduler		
017013493	10	10	160	I/O devices	Which device is used for taking care of all data transfers between I/O units and the memory while the CPU is processing another program?	b	1	I/O Channel	IOP	RAM	Priority encoder		
017013493	10	10	161	DMA	The term “cycle stealing” refers to:	c	1	Interrupt-based data transfer	Polling mode data transfer	DMA-based data transfer	Clock cycle overriding		
017013493	10	10	162	Memory mapped I/O	Which of the given mapping technique will provide simpler hardware, simple instruction set and provides all addressing modes? (i) Memory mapped I/O (ii) Isolated I/O	c	1	Both (i) and (ii)	Only (ii)	only (i)	Neither (i) nor (ii)		
017013493	10	10	163	Memory mapped I/O	Which of the following is not an advantage of memory mapped technique? (i) Simple hardware (ii) Simple Instruction Size (iii) All address modes available (iv) More memory address space	b	1	(i), (iv) only	(iv) only	(i), (ii), (iii) only	(iii), (iv) only		
017013493	10	10	164	Programmed I/O	In which mode of transfer, each data transfer is initiated by an instruction in the program?	a	1	Programmed I/O	DMA	Interrupt initiated I/O	None		
017013493	10	10	165	Programmed I/O	Choose the correct option/s from the following regarding programmed I/O mode of transfer. (i) CPU stays in a program loop until the I/O unit indicates that it is ready for data transfer. (ii) Processor keeps busy needlessly in programmed I/O mode (iii) An interrupt facility is used to issue an interrupt request when data is available from the device.	a	1	All 1, 2 and 3	only 1 and 2	only 2	only 1 and 3		

017013493	10	10	166	DMA	Why are the read and write control lines in a DMA controUer bidirectional? Under what condition and for what purpose are they used as inputs? Under what condition and for what purpose are they used as outputs?		2						
017013493	10	10	167	DMA	Which type of register specifies the mode of transfer in DMA controller?	b	1	Address register	control register	word count register	Status register		
017013493	10	10	168	Interface	A special synchronization hardware which is required between CPU and peripherals called _____	a	1	Interface Unit	Memory Unit	Processor	Accumulator		
017013493	10	10	169	Interface	Which of the given function is not considered as a main functions of I/O interface?	d	1	Data conversion	Synchronization	device selection	all of the given functions		
017013493	10	10	170	Command	Identify the type of command if user starts moving a magnetic tape in forward direction	b	1	status command	control command	data output command	data input command		
017013493	10	10	171	strobe method	Draw the timimg signals of source initiated strobe for data transfer.		2						
017013493	10	10	172	strobe method	Draw the timimg signals of destination initiated strobe for data transfer.		2						
017013493	10	10	173	strobe method	In which method there is no acknowlegement received for placing the data on bus by source?		1	Strobe method	Asynchronous data transferring	Handshaking	synchronous data transferring		
017013493	10	10	174	handshaking	Enlist the sequence of events occured in source initiated transfer using handshaking.		2						
017013493	10	10	175	handshaking	Draw the timimg diagram of destination initiated handshaking for data transfer.		2						
017013493	10	10	176	handshaking	Draw the timimg diagram of source initiated handshaking for data transfer.		2						
017013493	10	10	177	peripherals	Which mode of tranfer has time consuming transfer process as CPU monitors peripheral devices constantly?	a	1	Programmed I/O	Interrupt I/O	DMA	Both a and b		
017013493	10	10	178	mode of transfer	In which mode of transfer, interrupt request is initiated when the data is available from the device?	b		Programmed I/O	Interrupt I/O	DMA	Both a and b		
017013493	10	10	179	data transfer	In case of Data transfer between two independent units, where internal timing in each unit is independent from the other is known as_____data transfer.	b		Synchronous	Asynchronous	Control	None		
017013493	10	10	180	mode of transfer	Choose the correct statement/s: 1. The strobe may be activated by either the source or the destination unit 2. The source removes the data from the bus before that it disables its strobe pulse. 3. One of the Disadvantages of the strobe method is Source unit that initiates the transfer has no way of knowing whether the destination unit has actually received the data item that was placed in the bus.	d		Only 1	Only 3	All 1, 2, 3	Both 1 and 3		
017013493	10	10	181	mode of transfer	By the help of_____ method we can solve the problem of strobe method.	c		IOP	Direct	handshaking	Indirect		
017013493	10	10	182	mode of transfer	In the programmed I/O method, the I/O device does not have direct access to _____	b		CPU	Memory	register	none		
017013493	10	10	183	mode of transfer	The method which offers higher speeds of I/O transfers is _____	d		Interrupt	Memory mapping	Programmed Control I/O	DMA		
017013493	10	10	184	mode of transfer	The DMA transfers are performed by a control circuit called as _____	a		DMA Controller	Memory unit	Control unit	CPU		
017013493	10	10	185	mode of transfer	Which register is not a part of DMA controller?	d		Address register	control register	word count register	Status register		
017013493	10	10	186	mode of transfer	Which of the following I/O transfer mode uses polling method?	a		Programmed I/O	Interrupt I/O	DMA initiated	priority interrupt		
017013493	10	10	187	mode of transfer	Which of the following value will be passed to (PI, PO) of each device in sequence if interrupt request is generated by third device in a daisy chain priority arrangement?	c		(1,0),(0,0),(0,0)...	(1,1),(1,1),(0,1),...	(1,1),(1,1),(1,0),...	(0,0),(0,0),(0,1),...		
017013493	10	10	188	mode of transfer	Removing the CPU from the path and letting the peripheral device manage the memory buses directly would improve the speed of transfer. This technique is known as _____	d		Programmed I/O	Interrupt I/O	priority interrupt	DMA		
017013493	10	10	189	mode of transfer	Which of the register of DMA controller is incremented after transferring each word to memory?	a		Address register	control register	word count register	Status register		
017013493	10	10	190	mode of transfer	Which of the register of DMA controller is decremented after transferring each word to memory?	c		Address register	control register	word count register	Status register		
017013493	10	10	191	mode of transfer	In which mode of transfer CPU is idle and has no control of the memory buses?	c		Programmed I/O	Interrupt I/O	DMA transfer	priority interrupt		
017013493	10	10	192	mode of transfer	The method of accessing the I/O devices by repeatedly checking the status flags is _____	a		Programmed I/O	Memory mapped I/O	I/O Mapped	None		
017013493	10	10	193	mode of transfer	The process wherein the processor constantly checks the status flags is called as _____	a		Polling	Inspection	Reviewing	Echoing		
017013493	10	10	194	mode of transfer	Match the columns: Units: a) Input unit; b) Output unit; c) Memory unit; d) Processing unit Activities: i) Executes instructions; ii) Receives data for processing; iii) Displays computed result; iv) Stores programs and computed values	d		(a,ii), (b,iv), (c,iii), (d,i)	(a,ii), (b,iii), (c,i), (d,iv)	(a,iii), (b,ii), (c,iv), (d,i)	(a,ii), (b,iii), (c,iv), (d,i)		
017013493	10	10	195	mode of transfer	On receiving an interrupt from an I/O device, the CPU _____	b		halts for predetermined time	branches off to the interrupt service routine after completion of the current instruction	branches off to the interrupt service routine immediately.	hands over control of address bus and data bus to the interrupting device		
017013493	10	10	196	mode of transfer	Which of the following is not considered as a peripheral device?	a		CPU	Key board	Mouse	all of the given		