KS8721BL/SL

3.3V Sinlge Power Supply 10/100BaseTX/FX MII Physical Layer Transceiver

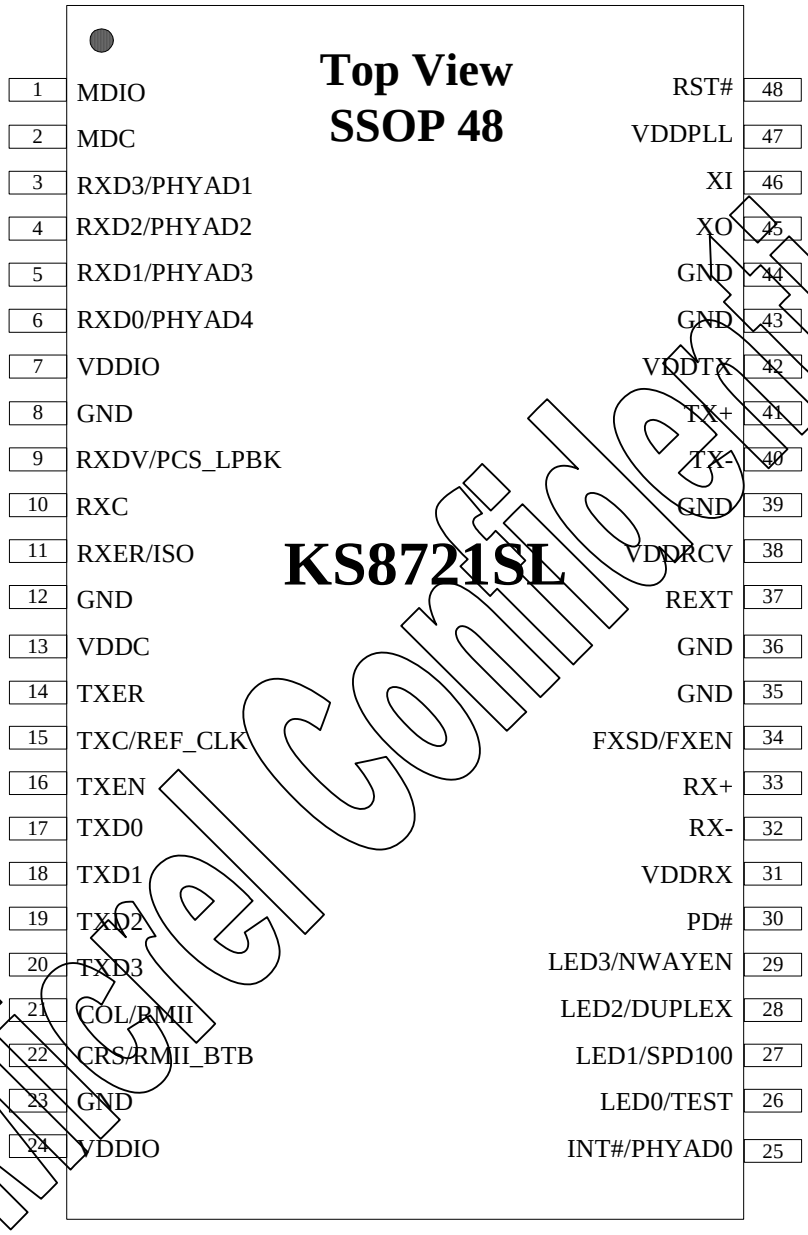
HIGHLIGHTS

- Single 3.3V power supply with built-in 2.5V regulator.
- Single chip 100BaseTX/100BaseFX/10BaseT physical layer solution
- 2.5V CMOS design, Power Consumption<200 mW (excluding output driver current)
- Fully compliant to IEEE 802.3u standard
- Supports Media Independent Interface (MII) and Reduced MII (RMII)
- Supports 10BaseT, 100BaseTX and 100Base-FX with Far_End_Fault Detection
- Supports power down mode and power saving mode
- Configurable through MII serial management ports or via external control pins
- Supports auto-negotiation and manual selection for 10/100Mbps speed and full / half-duplex mode
- On-chip built-in analog front end filtering for both 100BaseTX and 10BaseT
- LED outputs for link, activity, full/half duplex, collision and speed
- Supports back to back, FX to TX for media converter applications
- Supports MDI/MDI-X auto crossover
- 2.5V / 3.3V tolerance on I/O
- 48 Pin SSOP and LQFP
- KS8721BL is a drop in replacement for the KS8721BT in the same footprint.
- KS8721SL is a drop in replacement for the KS8721B in the same footprint.

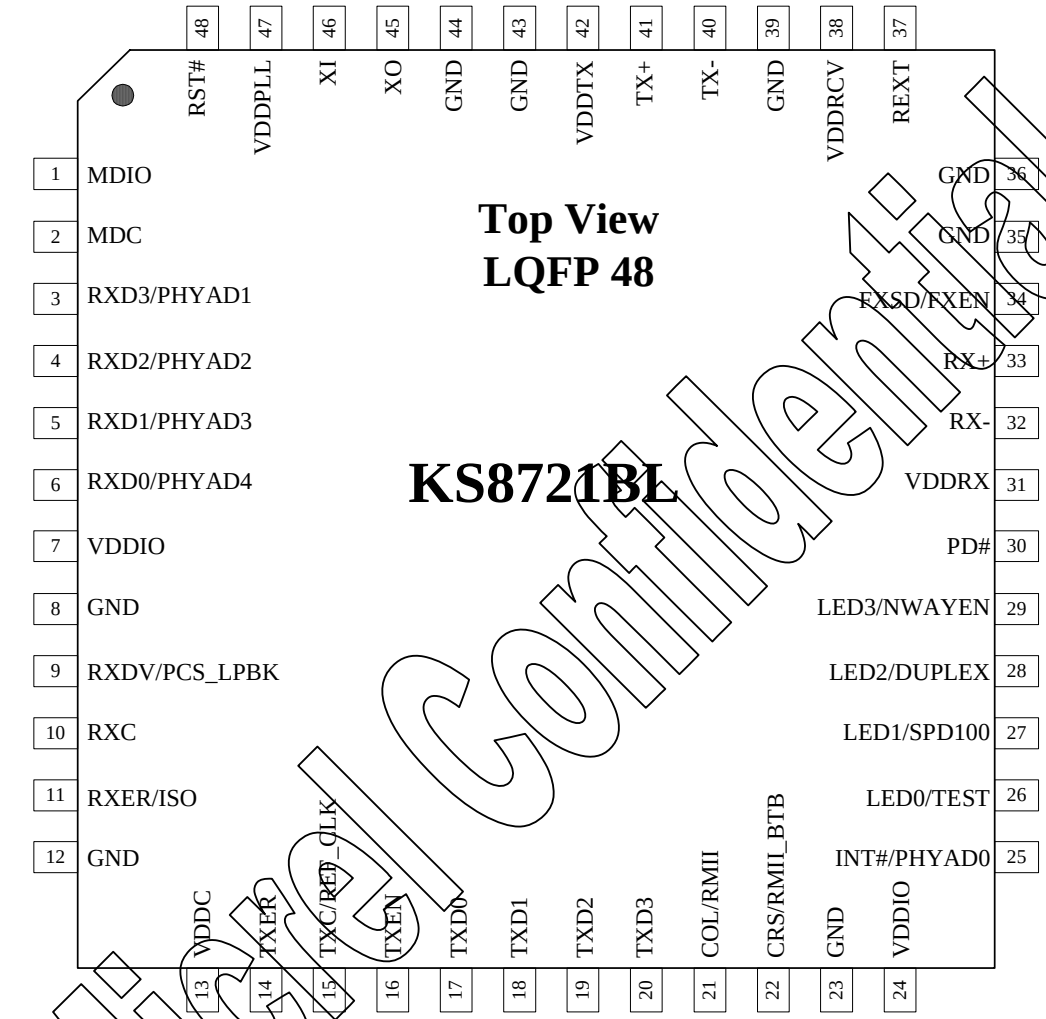
Operating at 2.5 volts to meet low voltage and low power requirements, the KS8721BL/SL are a 10BaseT/100BaseTX/FX Physical Layer Transceiver, which provides an MII to transmit and receive data. It contains the 10BaseT Physical Medium Attachment (PMA), Physical Medium Dependent (PMD), and Physical Coding Sub-layer (PCS) functions. Moreover, the KS8721BL/SL have on-chip 10BaseT output filtering, which eliminates the need for external filters and allows a single set of line magnetics to be used to meet requirements for both 100BaseTX and 10BaseT.

The KS8721BL/SL can automatically configure itself for 100 or 10 Mbps and full or half duplex operation, using on-chip Auto-Negotiation algorithm. It is an ideal choice of physical layer transceiver for 100BaseTX/10BaseT applications.

PINOUT 48 SSOP



PINOUT 48 LQFP



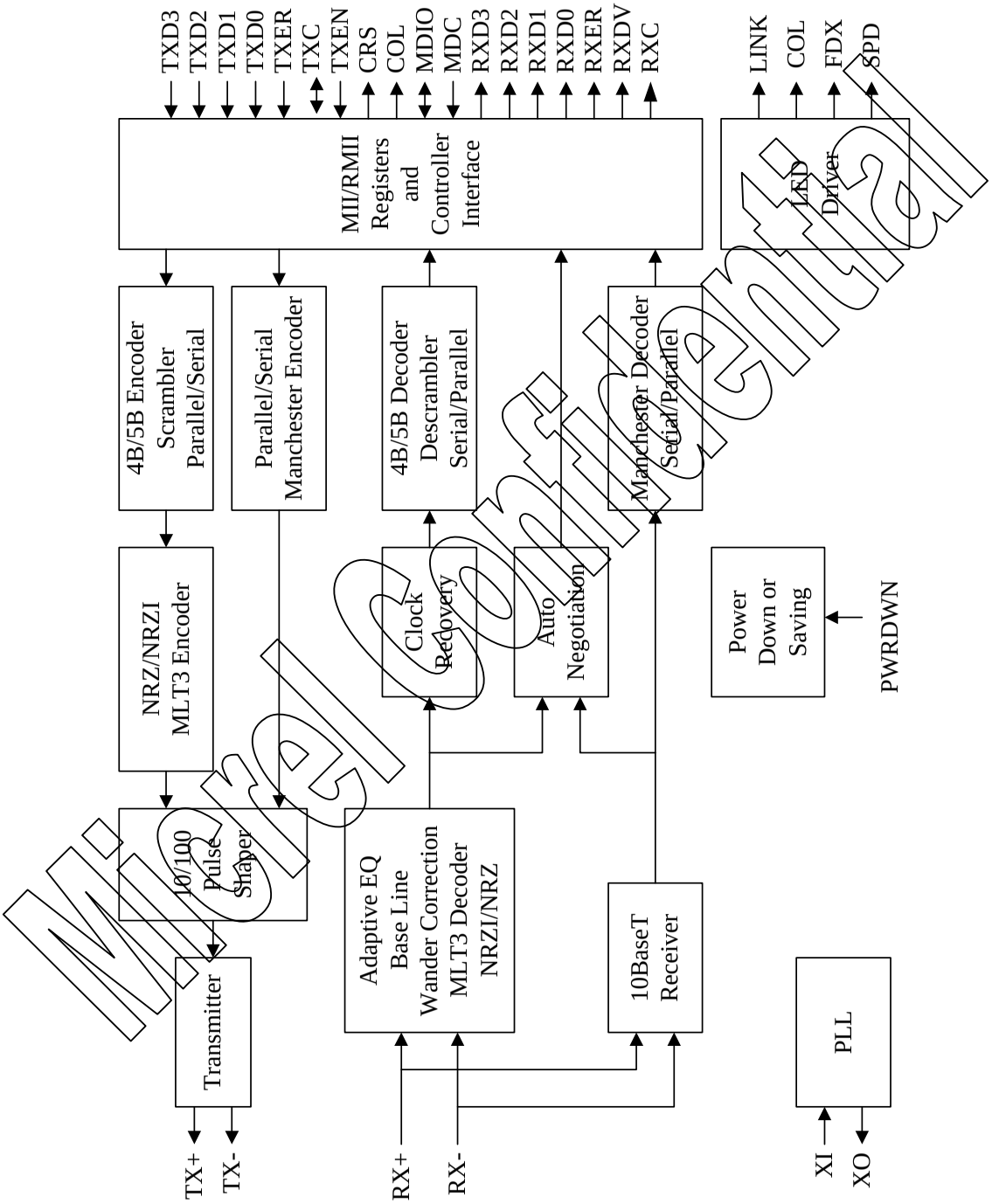
DOCUMENT REVISION HISTORY

Revision	Date	Change
0.90	8/22/03	• Document Origination (Preliminary)

ORDERING INFORMATION

Part Number	Package Type	Description
KS8721SL	48 Pin SSOP	Single 3.3V Power Supply 10/100BaseTX/FX MII Physical Layer Transceiver – Commercial Temperature
KS8721BL	48 Pin LQFP	Single 3.3V Power Supply 10/100BaseTX/FX MII Physical Layer Transceiver – Commercial Temperature
KS8721BL-EVAL	N/A	KS8721BL Evaluation Kit

BLOCK DIAGRAM



PIN DESCRIPTIONS

Signal Name	Pin No.	I/O	Description
MDIO	1	I/O	**Management Interface (MII) Data I/O** This pin requires an external 10K pull-up resistor.
MDC	2	I	**Management Interface (MII) Clock Input** This pin is synchronous to the MDIO data interface
RXD3 / PHYAD1	3	Ipd/O	**MII Receive Data Output** RXD [3..0], these bits are synchronous with RXCLK. When RXDV is asserted, RXD [3..0] presents valid data to MAC through the MII. RXD [3..0] is invalid when RXDV is de-asserted. The pull-up/pull-down value is latched as PHYADDR [1] during reset. See "Strapping Options" section for details.
RXD2 / PHYAD2	4	Ipd/O	**MII Receive Data Output** The pull-up/pull-down value is latched as PHYADDR [2] during reset. See "Strapping Options" section for details.
RXD1 / PHYAD3	5	Ipd/O	**MII Receive Data Output** The pull-up/pull-down value is latched as PHYADDR [3] during reset. See "Strapping Options" section for details.
RXD0 / PHYAD4	6	Ipd/O	**MII Receive Data Output** The pull-up/pull-down value is latched as PHYADDR [4] during reset. See "Strapping Options" section for details.
VDDIO	7	Pwr	Digital IO 2.5 /3.3V tolerance power supply (See "Circuit design ref for power supply" section for details)
GND	8	Gnd	Ground
RXDV / **CRSDV /** PCS_LPBK	9	Ipd/O	**MII Receive Data Valid Output** The pull-up/pull-down value is latched as pcs_lpbk during reset. See "Strapping Options" section for details.
RXC	10	O	**MII Receive Clock Output** Operating at: 25 MHz = 100 Mbps 2.5 MHz = 10 Mbps

RXER / ISO	11	Ipd/O	**MII Receive Error Output** The pull-up/pull-down value is latched as ISOLATE during reset. See "Strapping Options" section for details.
GND	12	Gnd	Ground
VDDC	13	Pwr	Digital core 2.5 V only power supply (See "Circuit design ref for power supply" section for details)
TXER	14	Ipd	**MII Transmit Error Input**
TXC / REFCLK	15	I/O	**MII Transmit Clock Output** RMII Reference Clock Input
TXEN	16	Ipd	**MII Transmit Enable Input**
TXD0	17	Ipd	**MII Transmit Data Input**
TXD1	18	Ipd	**MII Transmit Data Input**
TXD2	19	Ipd	**MII Transmit Data Input**
TXD3	20	Ipd	**MII Transmit Data Input**
COL / RMII	21	Ipd/O	**MII Collision Detect Output** The pull-up/pull-down value is latched as RMII select during reset. See "Strapping Options" section for details.
CRS / RMII_BTB	22	Ipd/O	**MII Carrier Sense Output** The pull-up/pull-down value is latched as RMII Loop-back during reset when RMII mode is selected. See "Strapping Options section" for details.
GND	23	Gnd	Ground
VDDIO	24	Pwr	Digital IO 2.5 / 3.3V tolerance power supply (See "Circuit design ref for power supply" section for details)
INT# / PHYAD0	25	Ipu/O	**Management Interface (MII) Interrupt Out.** Latched as PHYAD[0] during power up / reset. See "Strapping Options" Section for details.
LED0 / TEST	26	Ipu/O	**Link/Activity LED Output** The external pull down enable test mode and only used for the factory test. Active Low

Link/Act	Pin State	LED Definition
No Link	H	Off
Link	L	On
Activity	-	Toggle

LED1 / SPD100/ noFEF	27	Ipu/O	**Speed LED Output** Latched as SPEED (Register 0, bit 13) during power up / reset. See "Strapping Options" Section for details. Active Low

Speed	Pin State	LED Definition

			10BT	H	Off
			100BT	L	On
LED2 / DUPLEX	28	Ipu/O	**Full-duplex LED Output** Latched as DUPLEX (register 0h, bit 8) during power up / reset. See "Strapping Options" Section for details. Active Low		
			Duplex	Pin State	LED Definition
			Half	H	Off
			Full	L	On
LED3 / NWAYEN	29	Ipu/O	**Collision LED Output** Latched as ANEG_EN (register 0h, bit 12) during power up / reset. See "Strapping Options" Section for details. Active Low		
			Collision	Pin State	LED Definition
			No Collision	H	Off
			Collision	L	On
PD#	30	Ipu	**Power Down.** 1=Normal operation, 0=Power down, Active low		
VDDRX	31	Pwr	Analog 2.5 V power supply (See "Circuit design ref for power supply" section for details)		
RX-	32	I	**Receive Input** Differential receive input pins for FX, 100BaseTX or 10BaseT		
RX+	33	I	**Receive Input** Differential receive input pin for FX, 100BaseTX or 10BaseT		
FXSD / FXEN	34	Ipd/O	**Fiber Mode Enable / Signal Detect in Fiber Mode** If FXEN=0, FX mode is disable. The default is "0". See "100BT FX Mode" section for more details.		
GND	35	Gnd	Ground		
GND	36	Gnd	Ground		
REXT	37	I	**External resistor (6.49K Ω) connects to REXT and GNDRX**		
VDDRCV	38	Pwr	Analog 2.5 V power supply (See "Circuit design ref for power supply" section for details)		
GND	39	Gnd	Ground		
TX-	40	O	**Transmit Outputs** Differential transmit output for 100BaseTX/FX or 10BaseT		
TX+	41	O	**Transmit Outputs** Differential transmit output for FX, 100BaseTX/FX or 10BaseT		

VDDTX	42	Pwr	Transmitter 2.5 V power supply (See “Circuit design ref for power supply” section for details)
GND	43	Gnd	Ground
GND	44	Gnd	Ground
XO	45	O	**XTAL feedback** Used with XI for Xtal application.
XI	46	I	**Crystal Oscillator Input** Input for a crystal or an external 25 MHz clock
VDDPLL	47	Pwr	Analog PLL 2.5 V power supply (See “Circuit design ref for power supply” section for details)
RST#	48	Ipu	**Chip Reset** Active low, minimum of 50 us pulse is required

Note:

Pwr = power supply;
Gnd = ground;
I = input;
O = output;
I/O = bi-directional
Ipu = input w/ internal pull up;
Ipd = input w/ internal pull down;
Ipu/O = input w/ internal pull up during reset, output pin otherwise;
Ipd/O = input w/ internal pull down during reset, output pin otherwise;
PD = strap pull down;
PU = strap pull up;

STRAPPING OPTIONS

Signal Name	Pin No.	I/O	Description
PHYAD[4:1] / RXD[0:3]	6,5, 4,3	Ipd/O	PHY Address latched at power-up / reset. The default PHY address is 00001.
PHYAD0/ INT#	25	Ipu/O	
PCS_LPBK / RXDV	9	Ipd/O	Enables PCS_LPBK mode at power-up / reset. PD (default) = Disable, PU = Enable
ISO / RXER	11	Ipd/O	Enables ISOLATE mode at power-up /reset. PD (default) = Disable, PU = Enable
RMII / COL	21	Ipd/O	Enables RMII mode at power-up / reset. PD (default) = Disable, PU = Enable
RMII_BTB / CRS	22	Ipd/O	Enable RMII_BTB mode at power-up / reset. PD (default) = Disable, PU = Enable
SPD100 / No FEF / LED1	27	Ipu/O	Latched into Register 0h bit 13 during power-up / reset. PD = 10Mb/s, PU (default) = 100Mb/s. If SPD100 is asserted during power-up / reset, this pin also latched as the Speed Support in register 4h. (If FXEN is pulled up, the latched value 0 means no Far _End _Fault.)
DUPLEX / LED2	28	Ipu/O	Latched into Register 0h bit 8 during power-up / reset. PD = Half Duplex, PU (default) = Full duplex. If Duplex is pulled up during reset, this pin also latched as the Duplex support in register 4h.
NWAYEN / LED3	29	Ipu/O	Nway (auto-=Negotiation) Enable Latched into Register 0h bit 12 during power-up / reset. PD = Disable Auto-Negotiation, PU (default) = Enable Auto-Negotiation
PD#	30	Ipu	Power Down Enable PU (default) = Normal operation, PD = Power down mode

Note: Strap-in is latched during power up or reset.

REGISTER MAP

Register No.	Description
0h	Basic Control Register
1h	Basic Status Register
2h	PHY Identifier I
3h	PHY Identifier II
4h	Auto-Negotiation Advertisement Register
5h	Auto-Negotiation Link Partner Ability Register
6h	Auto-Negotiation Expansion Register
7h	Auto-Negotiation Next Page Register
8h	Link Partner Next Page Ability
15h	RXER Counter Register
1bh	Interrupt Control/Status Register
1fh	100BaseTX PHY Control Register

Note: RW: Read/Write, RO: Read Only, SC: Self Clear, LH: Latch High, LL: Latch Low

Some of the default values are set by strap-in defined on page 8

Address	Name	Description	Mode	Default
Register 0h – Basic Control				
0.15	Reset	1 = software reset. Bit is self-clearing	RW/ SC	0
0.14	Loop-back	1 = loop-back mode 0 = normal operation	RW	0
0.13	Speed Select (LSB)	1 = 100Mb/s 0 = 10Mb/s Ignored if Auto-Negotiation is enabled (0.12 = 1)	RW	Set by SPD100
0.12	Auto-Negotiation Enable	1 = enable auto-negotiation process (override 0.13 and 0.8) 0 = disable auto-negotiation process	RW	Set by NWAYEN

Address	Name	Description	Mode	Default
0.11	Power Down	1 = power down mode 0 = normal operation	RW	0
0.10	Isolate	1 = electrical isolation of PHY from MII and TX+/TX- 0 = normal operation	RW	Set by ISO
0.9	Restart Auto-Negotiation	1 = restart auto-negotiation process 0 = normal operation. Bit is self-clearing	RW/ SC	0
0.8	Duplex Mode	1 = full duplex 0 = half duplex	RW	Set by DUPLEX
0.7	Collision Test	1 = enable COL test 0 = disable COL test	RW	0
0.6:1	Reserved		RO	0
0.0	Disable Transmitter	0 = enable transmitter 1 = disable transmitter	R/W	0
Register 1h – Basic Status				
1.15	100BaseT4	1 = T4 capable 0 = not T4 capable	RO	0
1.14	100BaseTX Full Duplex	1 = capable of 100BaseX full duplex 0 = not capable of 100BaseX full duplex	RO	1
1.13	100BaseTX Half Duplex	1 = capable of 100BaseX half duplex 0 = not capable of 100BaseX half duplex	RO	1
1.12	10BaseT Full Duplex	1 = 10Mbps with full duplex 0 = no 10Mbps with full duplex capability	RO	1
1.11	10BaseT Half Duplex	1 = 10Mbps with half duplex 0 = no 10Mbps with half duplex capability	RO	1
1.10:7	Reserved		RO	0

Address	Name	Description	Mode	Default
1.6	No Preamble	1 = preamble suppression 0 = normal preamble	RO	1
1.5	Auto-Negotiation Complete	1 = auto-negotiation process completed 0 = auto-negotiation process not completed	RO	0
1.4	Remote Fault	1 = remote fault 0 = no remote fault	RO/LH	0
1.3	Auto-Negotiation Ability	1 = capable to perform auto-negotiation 0 = unable to perform auto-negotiation	RO	1
1.2	Link Status	1 = link is up 0 = link is down	RO/LL	0
1.1	Jabber Detect	1 = jabber detected 0 = jabber not detected. Default is Low	RO/LH	0
1.0	Extended Capability	1 = supports extended capabilities registers	RO	1
Register 2h – PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	0022h
Register 3h – PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	000101
3.9:4	Model Number	Six bit manufacturer's model number	RO	100001
3.3:0	Revision Number	Four bit manufacturer's model number	RO	1001

Address	Name	Description	Mode	Default
Register 4h – Auto-Negotiation Advertisement				
4.15	Next Page	1 = next page capable 0 = no next page capability.	RW	0
4.14	Reserved		RO	0
4.13	Remote Fault	1 = remote fault supported 0 = no remote fault	RW	0
4.12 : 11	Reserved		RO	0
4.10	Pause	1 = pause function supported 0 = no pause function	RW	0
4.9	100BaseT4	1 = T4 capable 0 = no T4 capability	RO	0
4.8	100BaseTX Full Duplex	1 = TX with full duplex 0 = no TX full duplex capability	RW	Set by SPD100 & DUPLEX
4.7	100BaseTX	1 = TX capable 0 = no TX capability	RW	Set by SPD100
4.6	10BaseT Full Duplex	1 = 10Mbps with full duplex 0 = no 10Mbps full duplex capability	RW	Set by DUPLEX
4.5	10BaseT	1 = 10Mbps capable 0 = no 10Mbps capability	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	00001
Register 5h – Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = next page capable 0 = no next page capability	RO	0
5.14	Acknowledge	1 = link code word received from partner 0 = link code word not yet received	RO	0
5.13	Remote Fault	1 = remote fault detected 0 = no remote fault	RO	0
5.12	Reserved		RO	0

Address	Name	Description	Mode	Default
5.11:10	Pause	5.10 5 .11 0 0 No PAUSE 0 1 Asymmetric PAUSE (link partner) 1 0 Symmetric PAUSE 1 1 Symmetric & Asymmetric PAUSE (local device)	RO	0
5.9	100 BaseT4	1 = T4 capable 0 = no T4 capability	RO	0
5.8	100BaseTX Full Duplex	1 = TX with full duplex 0 = no TX full duplex capability	RO	0
5.7	100BaseTX	1 = TX capable 0 = no TX capability	RO	0
5.6	10BaseT Full Duplex	1 = 10Mbps with full duplex 0 = no 10Mbps full duplex capability	RO	0
5.5	10BaseT	1 = 10Mbps capable 0 = no 10Mbps capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	00001
Register 6h – Auto-Negotiation Expansion				
6.15:5	Reserved		RO	0
6.4	Parallel Detection Fault	1 = fault detected by parallel detection 0 = no fault detected by parallel detection.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = link partner has next page capability 0 = link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = local device has next page capability 0 = local device does not have next page capability	RO	1

Address	Name	Description	Mode	Default
6.1	Page Received	1 = new page received 0 = new page not yet received	RO/ LH	0
6.0	Link Partner Auto-Negotiation Able	1 = link partner has auto-negotiation capability 0 = link partner does not have auto-negotiation capability	RO	0
Register 7h – Auto-Negotiation Next Page				
7.15	Next Page	1 = additional next page(s) will follow 0 = last page	RW	0
7.14	Reserved		RO	0
7.13	Message Page	1 = message page 0 = unformatted page	RW	1
7.12	Acknowledge 2	1 = will comply with message 0 = cannot comply with message	RW	0
7.11	Toggle	1 = previous value of the transmitted link code word equaled logic One 0 = logic Zero	RO	0
7.10:0	Message Field	11-bit wide field to encode 2048 messages	RW	001
Register 8h – Link Partner Next Page Ability				
8.15	Next Page	1 = additional Next Page(s) will follow 0 = last page	RO	0
8.14	Acknowledge	1 = successful receipt of link word 0 = no successful receipt of link word	RO	0
8.13	Message Page	1 = Message Page 0 = Unformatted Page	RO	0
8.12	Acknowledge 2	1 = able to act on the information 0 = not able to act on the information	RO	0

Address	Name	Description	Mode	Default
8.11	Toggle	1 = previous value of transmitted Link Code Word equal to logic zero 0 = previous value of transmitted Link Code Word equal to logic one	RO	0
8.10:0	Message Field		RO	0
Register 15h – RXER Counter				
15.15:0	RXER Counter	RX Error counter for the RX_ER in each package	RO	0000
Register 1bh – Interrupt Control/Status Register				
1b.15	Jabber Interrupt Enable	1=Enable Jabber Interrupt 0=Disable Jabber Interrupt	RW	0
1b.14	Receive Error Interrupt Enable	1=Enable Receive Error Interrupt 0=Disable Receive Error Interrupt	RW	0
1b.13	Page Received Interrupt Enable	1=Enable Page Received Interrupt 0=Disable Page Received Interrupt	RW	0
1b.12	Parallel Detect Fault Interrupt Enable	1= Enable Parallel Detect Fault Interrupt 0= Disable Parallel Detect Fault Interrupt	RW	0
1b.11	Link Partner Acknowledge Interrupt Enable	1= Enable Link Partner Acknowledge Interrupt 0= Disable Link Partner Acknowledge Interrupt	RW	0
1b.10	Link Down Interrupt Enable	1= Enable Link Down Interrupt 0= Disable Link Down Interrupt	RW	0

Address	Name	Description	Mode	Default
1b.9	Remote Fault Interrupt Enable	1= Enable Remote Fault Interrupt 0= Disable Remote Fault Interrupt	RW	0
1b.8	Link Up Interrupt Enable	1= Enable Link Up Interrupt 0= Disable Link Up Interrupt	RW	0
1b.7	Jabber Interrupt	1= Jabber Interrupt Occurred 0= Jabber Interrupt Does Not Occurred	RO	0
1b.6	Receive Error Interrupt	1= Receive Error Occurred 0= Receive Error Does Not Occurred	RO	0
1b.5	Page Receive Interrupt	1= Page Receive Occurred 0= Page Receive Does Not Occurred	RO	0
1b.4	Parallel Detect Fault Interrupt	1= Parallel Detect Fault Occurred 0= Parallel Detect Fault Does Not Occurred	RO	0
1b.3	Link Partner Acknowledge Interrupt	1= Link Partner Acknowledge Occurred 0= Link Partner Acknowledge Does Not Occurred	RO	0
1b.2	Link Down Interrupt	1= Link Down Occurred 0= Link Down Does Not Occurred	RO	0
1b.1	Remote Fault Interrupt	1= Remote Fault Occurred 0= Remote Fault Does Not Occurred	RO	0
1b.0	Link Up Interrupt	1= Link Up Interrupt Occurred 0= Link Up Interrupt Does Not Occurred	RO	0
Register 1fh – 100BaseTX PHY Controller				
1f.15:14	reserved			
1f:13	Pairswap disable	1 = disable MDI/MDIX 0 = enable MDI/MDIX	R/W	0

Address	Name	Description	Mode	Default
1f.12	Energy detect	1 = presence of signal on RX+/- analog wire pair 0 = no signal detected on RX+/-	RO	0
1f.11	Force link	1 = force link pass 0 = normal link operation ***This bit bypasses the control logic and allow transmitter to send pattern even if there is no link.***	R/W	0
1f.10	Power Saving	1 = enable power saving 0 = disable	RW	1
1f.9	Interrupt Level	1 = interrupt pin active high 0 = active low	RW	0
1f.8	Enable Jabber	1 = enable jabber counter 0 = disable	RW	1
1f.7	Auto-Negotiation Complete	1 = auto-negotiation complete 0 = not complete	RW	0
1f.6	Enable Pause (Flow-Control Result)	1 = flow control capable 0 = no flow control	RO	0
1f.5	PHY Isolate	1 = PHY in isolate mode 0 = not isolated	RO	0
1f.4:2	Operation Mode Indication	[000] = still in auto-negotiation [001] = 10BaseT half duplex [010] = 100BaseTX half duplex [011] = default [101] = 10BaseT full duplex [110] = 100BaseTX full duplex [111] = PHY/MII isolate	RO	0
1f.1	Enable SQE test	1 = enable SQE test 0 = disable	RW	0
1f.0	Disable Data Scrambling	1 = disable scrambler 0 = enable	RW	0

SELECTION OF ISOLATION TRANSFORMER

One simple 1:1 isolation transformer is needed at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. The following table gives recommended transformer characteristics.

Characteristics Name	Value	Test Condition
Turns Ratio	1 CT : 1 CT	
Open-Circuit Inductance (min.)	350 uH	100 mV, 100 KHz, 8 mA
Leakage Inductance (max.)	0.4 uH	1 MHz (min.)
Inter-Winding Capacitance (max.)	12 pF	
D.C. Resistance (max.)	0.9 ohm	
Insertion Loss (max.)	1.0 dB	0 – 65 MHz
HIPOT (min.)	1500 Vrms	

Note: The IEEE 802.3u standard for 100BaseTX assumes a transformer loss of 0.5 dB. For the transmit line transformer, insertion loss of up to 1.3 dB can be compensated by increasing the line drive current by means of reducing the REXT resistor value.

SELECTION OF REFERENCE CRYSTAL

A crystal with the following typical characteristics is recommended.

Characteristics Name	Value	Units
Frequency	25.00000	MHz
Frequency Tolerance (max.)	+/- 100	ppm
Load Capacitance (max.)	20	pF
Series Resistance (max.)	25	ohm

FUNCTIONAL DESCRIPTION

100BaseTX Transmit

The 100BaseTX transmit function performs parallel to serial conversion, NRZ to NRZI conversion, MLT-3 encoding and transmission. The circuitry starts with a parallel to serial conversion, which converts the 25 MHz, 4-bit nibbles into a 125 MHz serial bit stream. The incoming data is clocked in at the positive edge of the TXC signal. The serialized data is further converted from NRZ to NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 6.49 KΩ resistor for the 1: 1 transformer ratio. It has a typical rise/fall times of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitters. The wave-shaped 10BaseT output driver is also incorporated into the 100BaseTX driver.

100BaseTX Receive

The 100BaseTX receive function performs adaptive equalization, DC restoration, MLT-3 to NRZI conversion, data and clock recovery, NRZI to NRZ conversion, and serial to parallel conversion. The receiving side starts with the equalization filter to compensate inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion are a function of the length of the cable, the equalizer has to adjust its characteristic to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and can self adjust against the environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate effect of base line wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. Finally, the NRZ serial data is converted to 4-bit parallel 4B nibbles. A synchronized 25 MHz RXC is generated so that the 4B nibbles is clocked out at the negative edge of RCK25 and is valid for the receiver at the positive edge. When no valid data is present, the clock recovery circuit is locked to the 25 MHz reference clock and both TXC and RXC clocks continue to run.

PLL Clock Synthesizer

The KS8721BL/SL generates 125 MHz, 25 MHz and 20 MHz clocks for system timing. An internal crystal oscillator circuit provides the reference clock for the synthesizer.

Scrambler/De-scrambler (100BaseTX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander.

10BaseT Transmit

When TXEN (transmit enable) goes high, data encoding and transmission will begin. The KS8721BL/SL will continue to encode and transmit data as long as TXEN remains high. The data transmission will end when TXEN goes low. The last transition occurs at the boundary of the bit cell if the last bit is zero, or at the center of the bit cell if the last bit is one. The output driver is incorporated into the 100Base driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.5 V amplitude. The harmonic contents are at least 27 dB below the fundamental when driven by an all-ones Manchester-encoded signal.

10BaseT Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths in order to prevent noises at the RX+ or RX- input from falsely trigger the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KS8721BL/SL decodes a data frame. This activates the carrier sense (CRS) ad RXDV signals and makes the receive data (RXD) available. The receive clock is maintained active during idle periods in between data reception.

SQE and Jabber Function (10BaseT only)

In 10BaseT operation, a short pulse will be put out on the COL pin after each packet is transmitted. This is required as a test of the 10BaseT transmit/receive path and is called SQE test. The 10BaseT transmitter will be disabled and COL will go high if TXEN is High for more than 20 ms (Jabbering). If TXEN then goes low for more than 250 ms, the 10BaseT transmitter will be re-enabled and COL will go Low.

Auto-negotiation

The KS8721BL/SL performs auto-negotiation by hardware strapping option (pin 29) or software (Register 0.12). It will automatically choose its mode of operation by advertising its abilities and comparing them with those received from its link partner whenever auto-negotiation is enabled. It can also be configured to advertise 100BaseTX or 10BaseT in either full- or half-duplex mode (please refer to page 11 and 12 for setting). The auto-negotiation is disabled in the FX mode.

During auto-negotiation, the contents of Register 4, coded in Fast Link Pulse (FLP), will be sent to its link partner under the conditions of power-on, link-loss or re-start. At the same time, the KS8721BL/SL will monitor incoming data to determine its mode of operation. Parallel detection circuit will be enabled as soon as either 10BaseT NLP (Normal Link Pulse) or 100BaseTX idle is detected. The operation mode is configured based on the following priority:

Priority 1: 100BaseTX, full-duplex
Priority 2: 100BaseTX, half-duplex
Priority 3: 10BaseT, full-duplex
Priority 4: 10BaseT, half-duplex

When the KS8721BL/SL receives a burst of FLP from its link partner with 3 identical link code words (ignoring acknowledge bit), it will store these code words in Register 5 and wait for the next 3 identical code words. Once the KS8721BL/SL detects the second code words, it then configures itself according to above-mentioned priority. In addition, the KS8721BL/SL also checks 100BaseTX idle or 10BaseT NLP symbol. If either is detected, the KS8721BL/SL automatically configures to match the detected operating speed.

MII Management Interface

The KS8721BL/SL supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the KS8721BL/SL. The MDIO interface consists of the following:

- A physical connection including a data line (MDIO), a clock line (MDC) and an optional interrupt line (INTRPT)
- A specific protocol that runs across the above-mentioned physical connection and it also allows one controller to communicate with multiple KS8721BL/SL devices. Each

KS8721BL/SL assigned an MII address between 0 and 31 by the PHYAD inputs.

- An internal addressable set of fourteen 16-bit MDIO registers. Register [0:6] are required and their functions are specified by the IEEE 802.3 specifications. Additional registers are provided for expanded functionality.

The INTPRT pin functions as a management data interrupt in the MII. An active Low or High in this pin indicates a status change on the KS8721BL/SL based on 1fh.9 level control. Register bits at 1bh[15:8] are the interrupt enable bits. Register bits at 1bh[7:0] are the interrupt condition bits. This interrupt is cleared by reading Register 1bh.

MII Data Interface

The data interface consists of separate channels for transmitting data from a 10/100 802.3 compliant Media Access Controller (MAC) to the KS8721BL/SL, and for receiving data from the line. Normal data transmission is implemented in 4B Nibble Mode (4-bit wide nibbles).

Transmit Clock (TXC): The transmit clock is normally generated by the KS8721BL/SL from an external 25MHz reference source at the X1 input. The transmit data and control signals must always be synchronized to the TXC by the MAC. The KS8721BL/SL normally samples these signals on the rising edge of the TXC.

Receive Clock (RXC): For 100BaseTX links, the receive clock is continuously recovered from the line. If the link goes down, and auto-negotiation is disabled, the receive clock operates off the master input clock (X1 or TXC). For 10BaseT links, the receive clock is recovered from the line while carrier is active, and operates from the master input clock when the line is idle. The KS8721BL/SL synchronizes the receive data and control signals on the falling edge of RXC in order to stabilize the signals at the rising edge of the clock with 10ns setup and hold times.

Transmit Enable: The MAC must assert TXEN at the same time as the first nibble of the preamble, and de-assert TXEN after the last bit of the packet.

Receive Data Valid: The KS8721BL/SL asserts RXDV when it receives a valid packet. Line operating speed and MII mode will determine timing changes in the following way:

- For 100BaseTX link with the MII in 4B mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the data packet.
- For 10BaseT links, the entire preamble is truncated. RXDV is asserted with the first nibble of the SFD " 5D" and remains asserted until the end of the packet.

Error Signals: Whenever the KS8721BL/SL receives an error symbol from the network, it asserts RXER and drives "1110" (4B) on the RXD pins. When the MAC asserts TXER, the KS8721BL/SL will drive "H" symbols (a Transmit Error define in the IEEE 802.3 4B/5B code group) out on the line to force signaling errors.

Carrier Sense (CRS): For 100TX links, a start-of-stream delimiter, or /J/K symbol pair causes assertion of Carrier Sense (CRS). An end-of-stream delimiter, or /T/R symbol pair causes de-assertion of CRS. The PMA layer will also de-assert CRS if IDLE symbols are received without /T/R, yet in this case RXER will be asserted for one clock cycle when CRS is de-asserted. For 10T links, CRS assertion is based on reception of valid preamble, and de-assertion on reception of an end-of-frame (EOF) marker.

Collision: Whenever the line state is half-duplex and the transmitter and receiver are active at the same time, the KS8721BL/SL asserts its collision signal, which is asynchronous to any clock.

RMII (Reduced MII) Data Interface

RMII interface specifies a low pin count (Reduced) Media Independent Interface (RMII) intended for use between Ethernet PHYs and Switch or Repeater ASICs. It is fully compliant with IEEE 802.3u [2].

This interface has the following characteristics:

1. It is capable of supporting 10Mb/s and 100Mb/s data rates
2. A single clock reference is sourced from the MAC to PHY (or from an external source)
3. It provides independent 2 bit wide (di-bit) transmit and receive data paths
4. It uses TTL signal levels, compatible with common digital CMOS ASIC processes

RMII Signal Definition

Signal Name	Direction (with respect to the PHY)	Direction (with respect to the MAC)	Use
REF_CLK	Input	Input or Output	Synchronous clock reference for receive, transmit and control interface
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data
TX_EN	Input	Output	Transit Enable
TXD[1:0]	Input	Output	Transit Data
RX_ER	Output	Input (Not Required)	Receive Error

Note: Unused MII signals, TXD[3:2], TXER need to tie to GND when RMII is using.

Reference Clock (REF_CLK)

REF_CLK is a continuous 50 MHz clock that provides the timing reference for CRS_DV, RXD[1:0], TX_EN, TXD[1:0], and RX_ER. REF_CLK is sourced by the MAC or an external source. Switch implementations may choose to provide REF_CLK as an input or an output depending on whether they provide a REF_CLK output or rely on an external clock distribution device. Each PHY device shall have an input corresponding to this clock but may use a single clock input for multiple PHYs implemented on a single IC.

Carrier Sense/Receive Data Valid (CRS_DV)

CRS_DV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. That is, in 10BASE-T mode, when squelch is passed or in 100BASE-X mode when 2 non-contiguous zeroes in 10 bits are detected carrier is said to be detected.

Loss of carrier shall result in the de-assertion of CRS_DV synchronous to REF_CLK. So long as carrier criteria are being met, CRS_DV shall remain asserted continuously from the first recovered di-bit of the frame through the final recovered di-bit and shall be negated prior to the first REF_CLK that follows the final di-bit.

The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] shall be "00" until proper receive signal decoding takes place (see definition of RXD[1:0] behavior).

Receive Data [1:0] (RXD[1:0])

RXD[1:0] shall transition synchronously to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY. In some cases (e.g. before data recovery or during error conditions) a pre-determined value for RXD[1:0] is transferred instead of recovered data. RXD[1:0] shall be "00" to indicate idle when CRS_DV is de-asserted. Values of RXD[1:0] other than "00" when CRS_DV is de-asserted are reserved for out-of-band signaling (to be defined). Values other than "00" on RXD[1:0] while CRS_DV is de-asserted shall be ignored by the MAC/repeater. Upon assertion of CRS_DV, the PHY shall ensure that RXD[1:0]=00 until proper receive decoding takes place.

Transmit Enable (TX_EN)

Transmit Enable TX_EN indicates that the MAC is presenting di-bits on TXD[1:0] on the RMII for trans-mission. TX_EN shall be asserted synchronously with the first nibble of the preamble and shall remain asserted while all di-bits to be transmitted are presented to the RMII. TX_EN shall be negated prior to the first REF_CLK following the final di-bit of a frame. TX_EN shall transition synchronously with respect to REF_CLK.

Transmit Data [1:0] (TXD[1:0])

Transmit Data TXD[1:0] shall transition synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the PHY. TXD[1:0] shall be "00" to indicate idle when TX_EN is de-asserted. Values of TXD[1:0] other than "00" when TX_EN is de-asserted are reserved for out-of-band signaling (to be defined). Values other than "00" on TXD[1:0] while TX_EN is disserted shall be ignored by the PHY.

Collision Detection

Since the definition of CRS_DV and TX_EN both contain an accurate indication of the start of frame, the MAC can reliably regenerate the COL signal of the MII by Ending TX_EN and CRS_DV.

During the IPG time following the successful transmission of a frame, the COL signal is asserted by some transceivers as a self-test. The Signal Quality Error (SQE) function will not be supported by the reduced MII due to the lack of the COL signal. Historically, SQE was present to indicate that a transceiver located physically remote from the MAC was functioning. Since the reduced MII only supports chip-to-chip connections on a PCB, SQE functionality is not required.

RX_ER

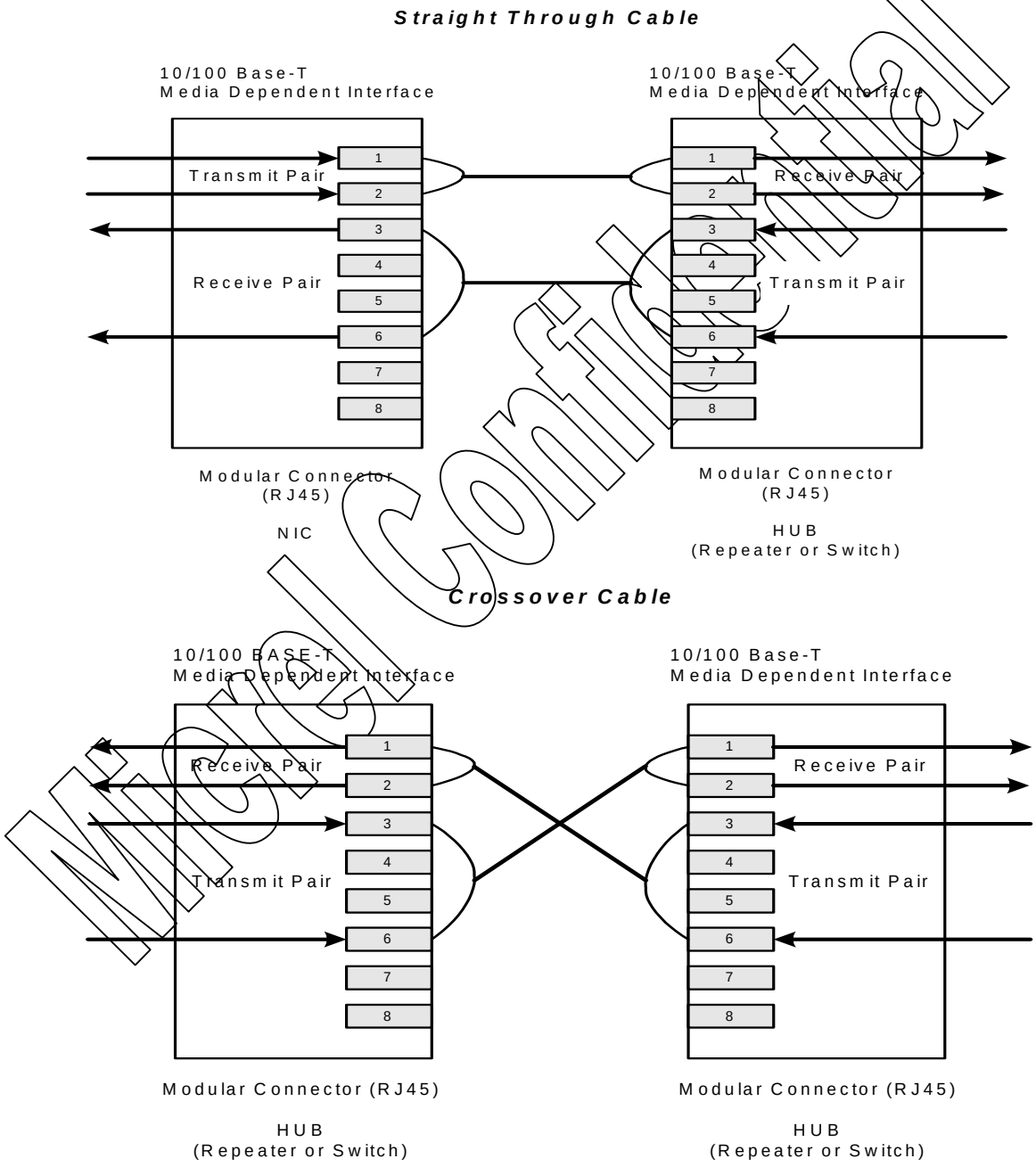
The PHY shall provide RX_ER as an output according to the rules specified in IEEE 802.3u [2] (see Clause 24, Figure 24-11 - Receive State Diagram). RX_ER shall be asserted for one or more REF_CLK periods to indicate that an error (e.g. a coding error or any error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY. RX_ER shall transition synchronously with respect to REF_CLK. While CRS_DV is de-asserted, RX_ER shall have no effect on the MAC.

RMII AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
	REF_CLK Frequency		50		MHz
	REF_CLK Duty Cycle	35		65	%
Tsu	TXD[1:0], TX_EN, RXD[1:0], CRS_DV, RX_ER Data Setup to REF_CLK rising edge	4			ns
Thold	TXD[1:0], TX_EN, RXD[1:0], CRS_DV, RXER Data hold from REF_CLK rising edge	2			ns

Auto Crossover (Auto MDI/MDI-X)

Automatic MDI/MDI-X configuration is intended to eliminate the need for crossover cables between similar devices. The assignment of pin-outs for a 10/100 BASE-T crossover function cable is shown below.
This feature can eliminate the confusion in real applications so both straight cable and crossover cable can be used. This feature is controlled by register 1f:13, see the “Register 1fh” section for details.



Power Management

The KS8721BL/SL offers the following modes for power management:

- Power Down Mode: This mode can be achieved by writing to Register 0.11 or pulling pin 30 PD# Low.
- Power Saving Mode: writing to register 1fh.10 can disable this mode. The KS8721BL/SL will then turn off everything except for the Energy Detect and PLL circuits when the cable is not installed. In other words, the KS8721BL/SL will shutdown most of the internal circuits to save power if there is no link. Power Saving mode will be in his most effective state when Auto-Negotiation Mode is enable.

100BT FX Mode

100BT FX mode is activated when FXSD/FXEN is higher 0.6V (This pin has a default pull down). Under this mode, the auto-negotiation and auto-MDIX features are disabled.
In fiber operation FXSD pin should connect to the SD (signal detect) output of the fiber module. The internal threshold of FXSD is around ½ Vdd +/- 50mV (1.25V+/-0.05V). Above this level, it is considered Fiber signal detected, and the operation is summarized in the following table:

FXSD/FXEN	Condition
Less than 0.6V	100TX mode
Less than 1.25V, but greater than 0.6V	FX mode No signal detected FEF generated
Greater than 1.25	FX mode Signal detected

To ensure a proper operation, the swing of fiber module SD should cover the threshold variation. A resistive voltage divider is recommended to adjust the SD voltage range.

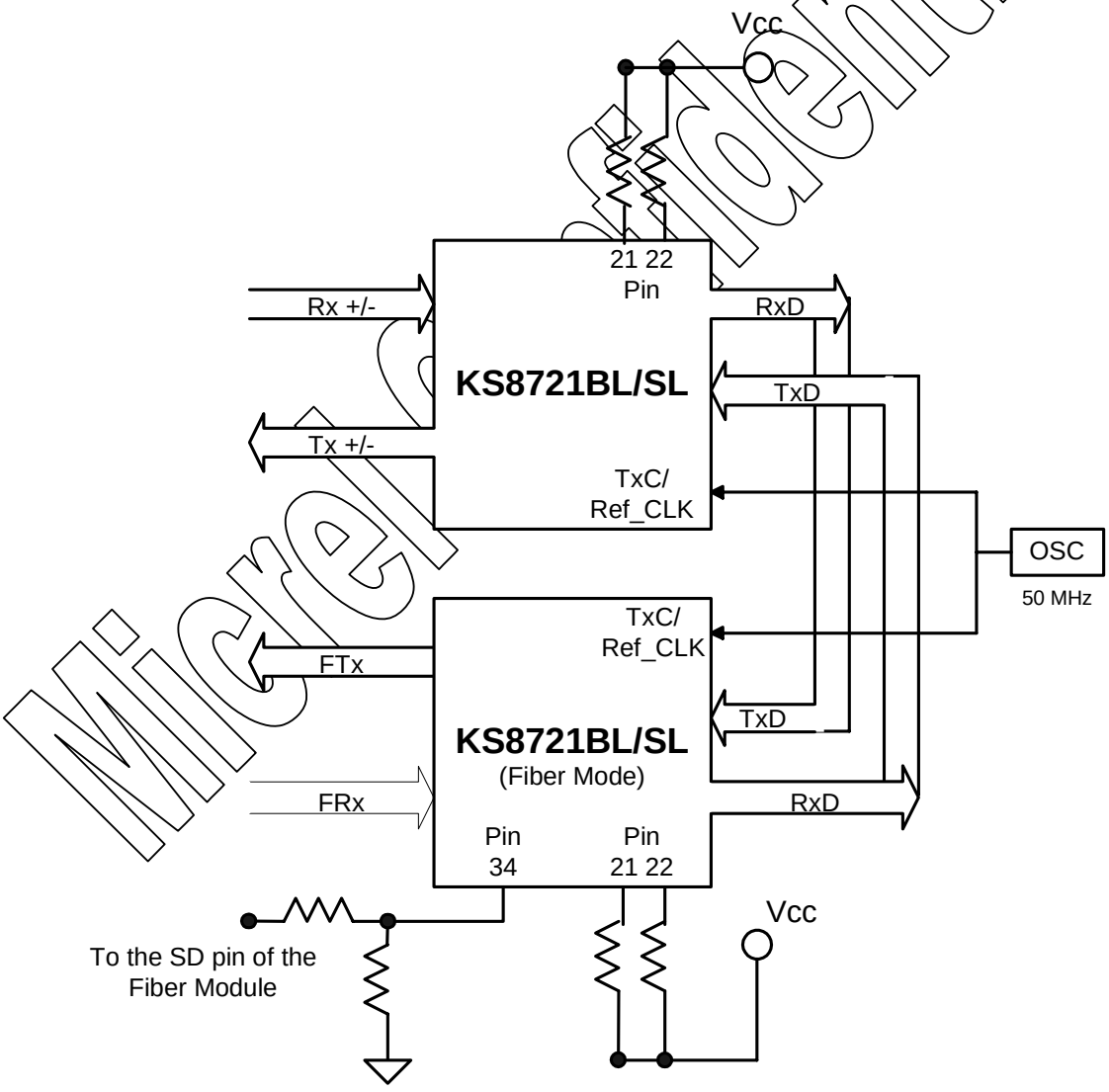
FEF (Far End Fault), repetition of a special pattern, which consists of 84-one and 1-zero, is generated under “FX mode with no signal detected”. The purpose of FEF is to notify the sender of a faulty link. When receiving a FEF, the LINK will go down to indicate a fault, even with fiber signal detected. The transmitter does not affect by receiving a FEF and still sends out its normal transmit pattern from MAC. FEF can be disabled by strapping pin27 low, please refer to “Strapping Options” section.

Media converter operation

KS8721BL/SL is capable of performing media conversion with 2 parts in a back-to-back RMII mode as indicated in the diagram. Both parts are in RMII mode and with RMII_BTB asserted (pin21 & 22 strapped high). One part is operating at TX mode and the other in FX mode. Both parts can share a common 50MHz oscillator.

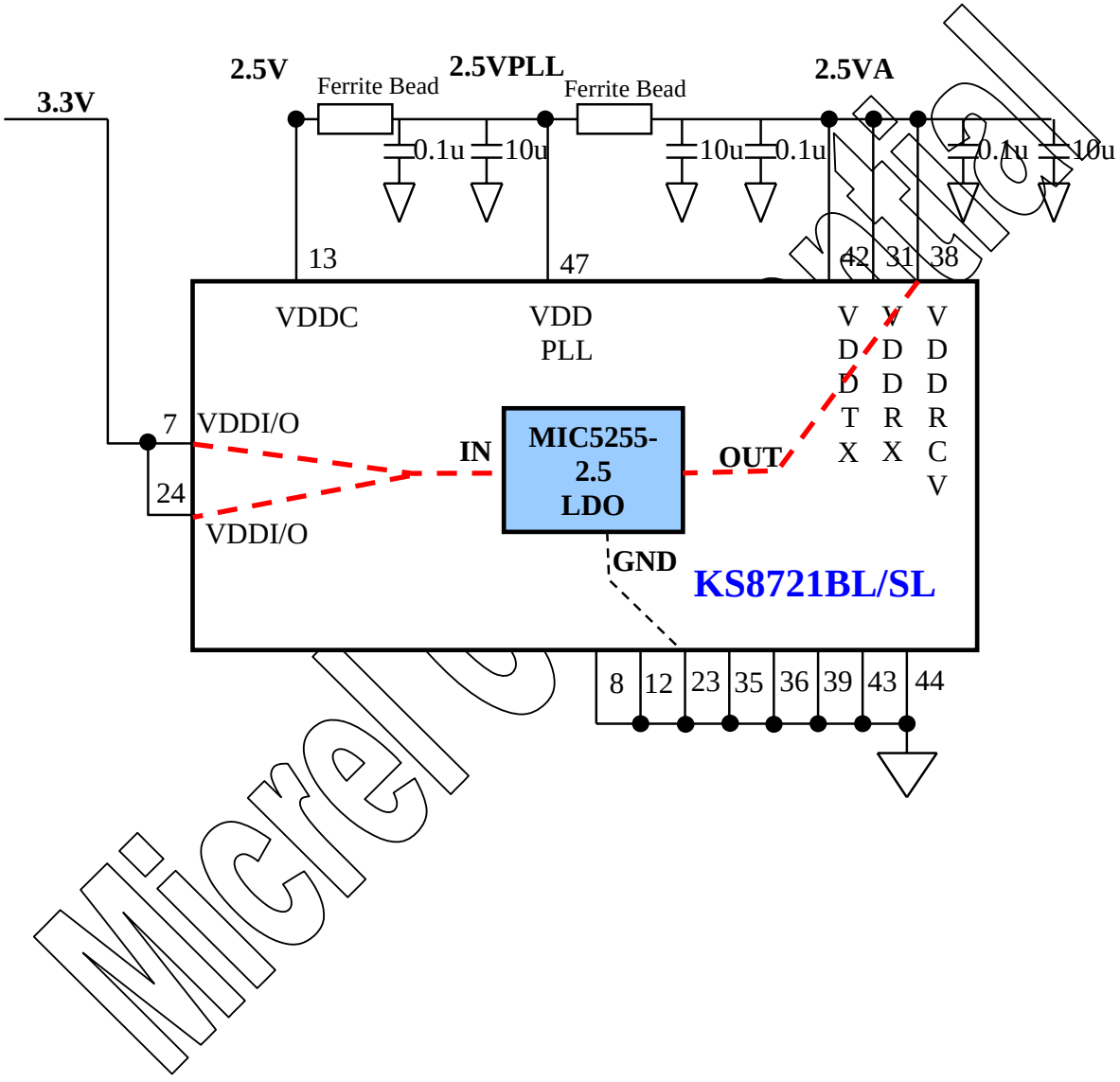
Under this operation, auto-Negotiation on the TX side will prohibit 10baseT link up. TXD2, active High, can disable transmitter and set it at tri-state. RXD2 serves as energy detection can indicate if there is line signal detected. TXD3 should tied low and RXD3 let float.

Please contact Micrel FAE for Application Note.



Circuit Design Reference for Power Supply

Micrel's integrated LDO technology, and thoughtful implementation allows the user to save BOM cost on both existing and future designs with the use of the new KS8721BL/SL single supply, single port 10/100 Ethernet PHY.



Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Storage Temperature:	- 55 °C to 150 °C
Supply Referenced to GND:	- 0.5 V to 5.0 V
All Pins	- 0.5 V to 5.0 V

Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply Voltages	VDDPLL, VDDTX, VDDRXC, VDDRCV, VDDC		2.5		V
	VDDIO		3.3		V
Ambient Operating Temperature Commercial	T_A	0		70	°C
Ambient Operating Temperature Industrial	T_A	-40		85	°C

Themal Data

	Thermal Resistance, θ_{JA} (℃/W)	Thermal Resistance, θ_{JA} (℃/W)	Thermal Resistance, θ_{JA} (℃/W)	Thermal Resistance, θ_{JC} (℃/W)	Remarks
Velocity (m/s)	**0**	**1**	**2**	**0**	
KS8721BL	83.56	77.08	72.36	13.3	No Heat Spreader
KS8721SL	42.43	36.19	34.24	6.75	No Heat Spreader

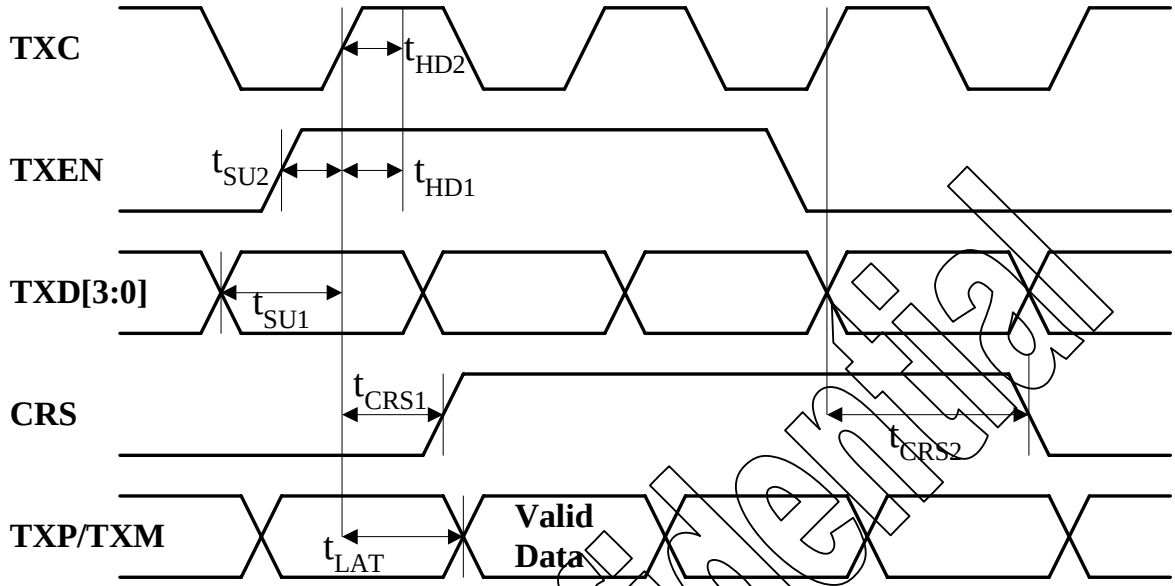
Electrical Characteristics (V_{dd} = 3.3 V +/- 10%)

Parameter	Sym	Test Condition	Min	Typ	Max	Unit
Total Supply Current (including TX output driver current)						
Normal 100BaseTX	I_{dd1}	Including 40mA output current		129		mA
Normal 10BaseT (Independent of utilization)	I_{dd2}	Including 90mA output current		159		mA
Power Saving mode 1	I_{dd3}	Auto-Negotiation is enable		TBD		mA
Power Down Mode	I_{dd5}			TBD		mA
TTL Inputs						
Input High Voltage	V_{ih}		Vdd (I/O) - 0.8			V
Input Low Voltage	V_{il}				0.8	V
Input Current	Iin	Vin = GND ~ VDD	-10		10	µA
TTL Outputs						
Output High Voltage	Voh	Ioh = - 4 mA	Vdd (I/O) - 0.4			V
Output Low Voltage	Vol	Iol = 4 mA			0.4	V
Output Tri-state Leakage	|Ioz|				10	µA

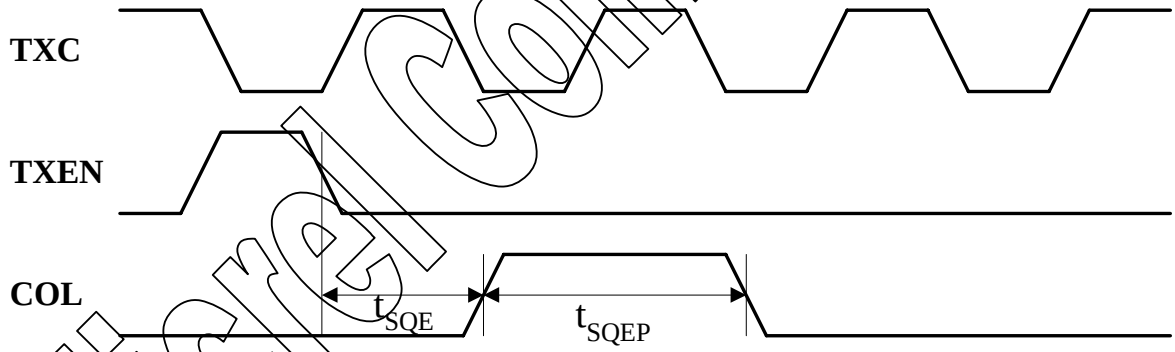
100BaseTX Receive						
RX+/RX- Differential Input Resistance	Rin			8		KΩ
Propagation Delay		from magnetics to RDTX		50	110	ns
100BaseTX Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	Vo	50 Ω from each output to Vdd	0.95		1.05	V
Output Voltage Imbalance	Vimb	50 Ω from each output to Vdd			2	%
Rise/Fall time	Tr/Tf		3		5	ns
Rise/Fall time Imbalance			0		0.5	ns
100BaseTX Transmit (measured differentially after 1:1 transformer)						
Duty Cycle Distortion					± 0.5	ns
Overshoot					5	%
Reference Voltage of ISET	Vset			0.75		V
Propagation Delay		from TDTX to magnetics		45	60	ns
Jitters				0.7	1.4	ns pk-pk
10BaseT Receive						
RX+/RX- Differential Input Resistance	Rin			8		KΩ
Squelch Threshold	Vsq	5 MHz square wave		400		mV

10BaseT Transmit (measured differentially after 1:1 transformer)						
Peak Differential Output Voltage	Vp	50 Ω from each output to Vdd	2.2		2.8	V
Jitters Added		50 Ω from each output to Vdd			± 3.5	ns
Rise/Fall time				25		ns
Clock Outputs						
Crystal Oscillator	X1, X2			25		MHz
Receive Clock, 100TX	RXC_{100}			25		MHz
Receive Clock, 10T	RXC_{10}			2.5		MHz
Receive Clock jitters				3.0		ns $_{pk-pk}$
Transmit Clock, 100TX	TXC_{100}			25		MHz
Transmit Clock, 10T	TXC_{10}			2.5		MHz
Transmit Clock jitters				1.8		ns $_{pk-pk}$

10BaseT MII Transmit Timing

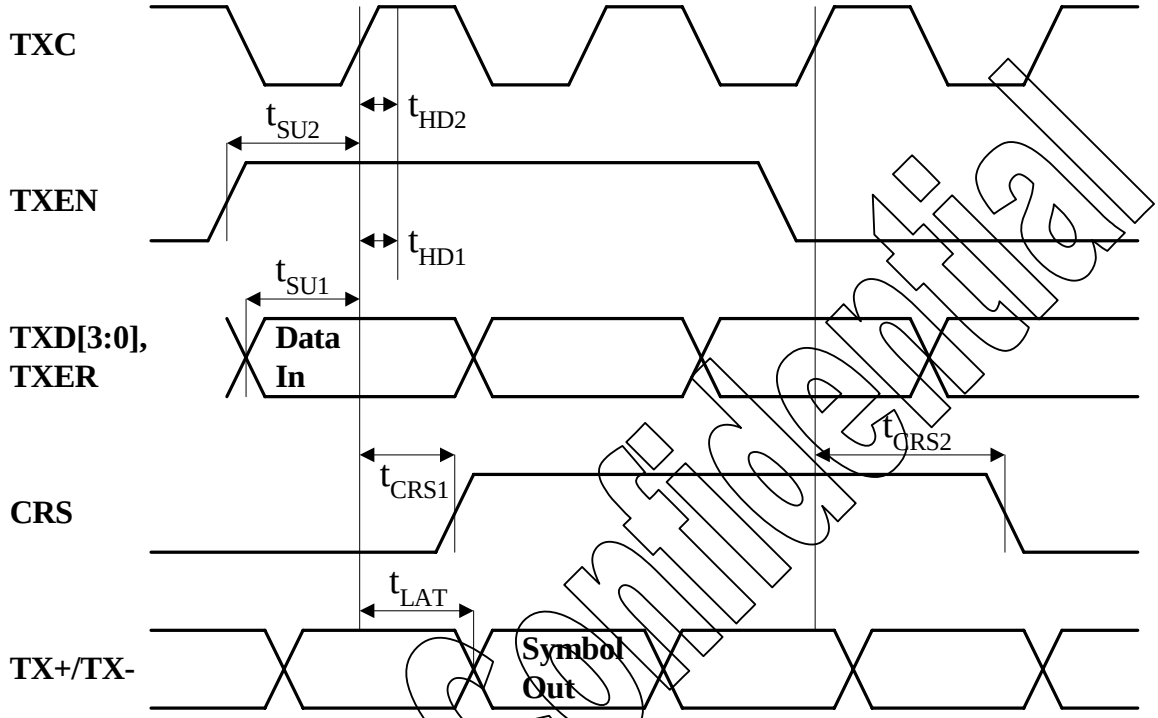


SQE Timing



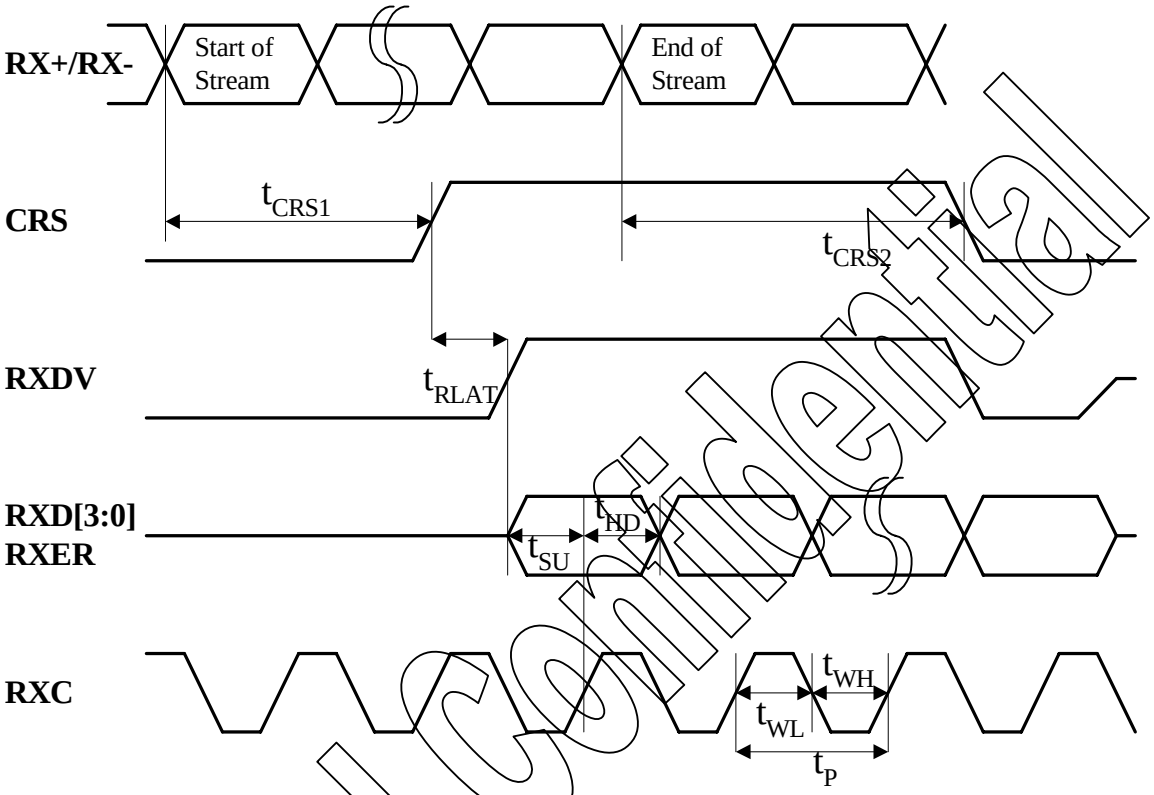
		min.	typ.	max.
t_{SU1}	TXD[3:0] Setup to TXC High	10ns		
t_{SU2}	TXEN Setup to TXC High	10ns		
t_{HD1}	TXD[3:0] Hold after TXC High	0ns		
t_{HD2}	TXEN Hold after TXC High	0ns		
t_{CRS1}	TXEN High to CRS asserted latency		4BT	
t_{CRS2}	TXEN Low to CRS de-asserted latency		8BT	
t_{LAT}	TXEN High to TXP/TXM output (TX latency)		4BT	
t_{SQE}	COL (SQE) Delay after TXEN de-asserted		2.5us	
t_{SQEP}	COL (SQE) Pulse Duration		1.0us	

100BaseTX MII Transmit Timing



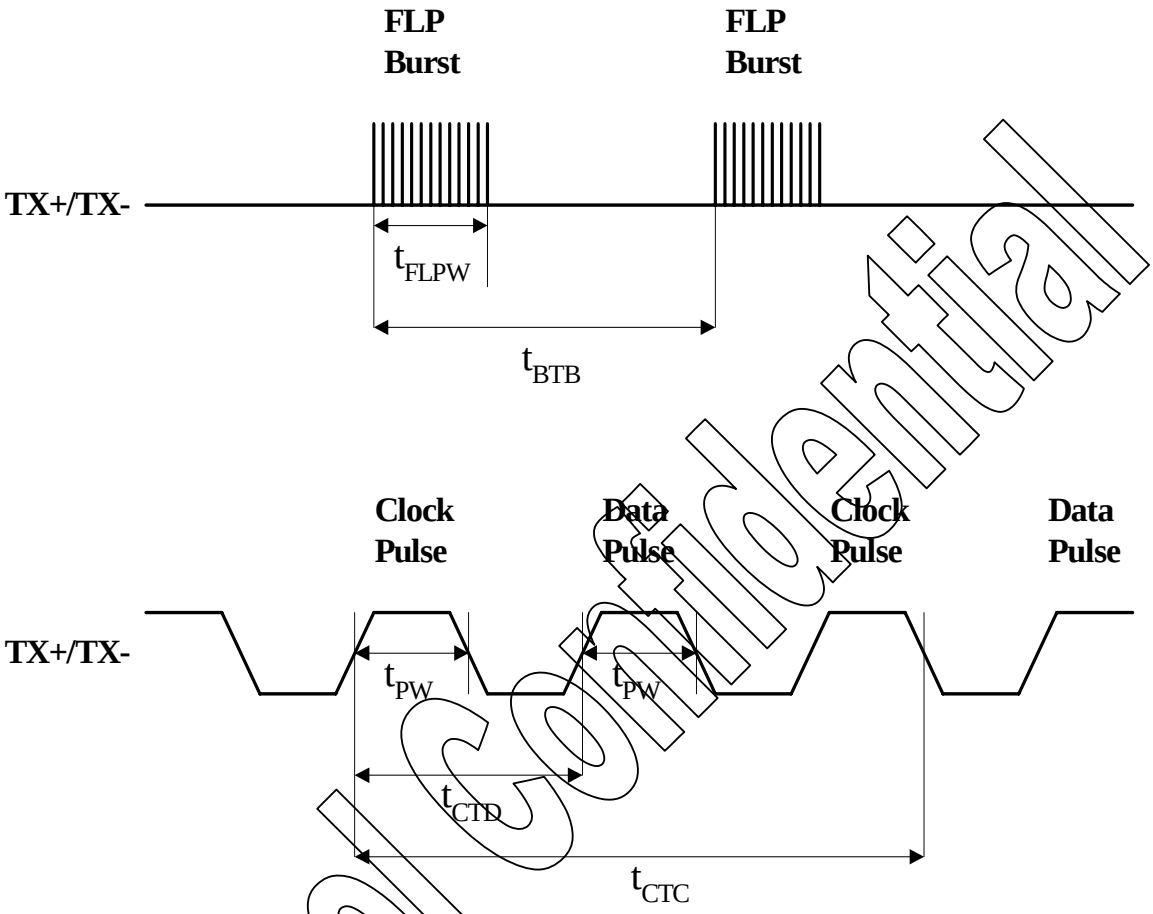
		min.	typ.	max.
t_{SU1}	TXD[3:0] Setup to TXC High	10ns		
t_{SU2}	TX_ER Setup to TXC High	10ns		
t_{HD1}	TXD[3:0] Hold after TXC High	0ns		
t_{HD2}	TXER Hold after TXC High	0ns		
t_{HD3}	TXEN Hold after TXC High	0ns		
t_{CRS1}	TXEN High to CRS asserted latency		4BT	
t_{CRS2}	TXEN Low to CRS de-asserted latency		4BT	
t_{LAT}	TXEN High to TX+/TX- output (TX latency)		7BT	

100BaseTX MII Receive Timing



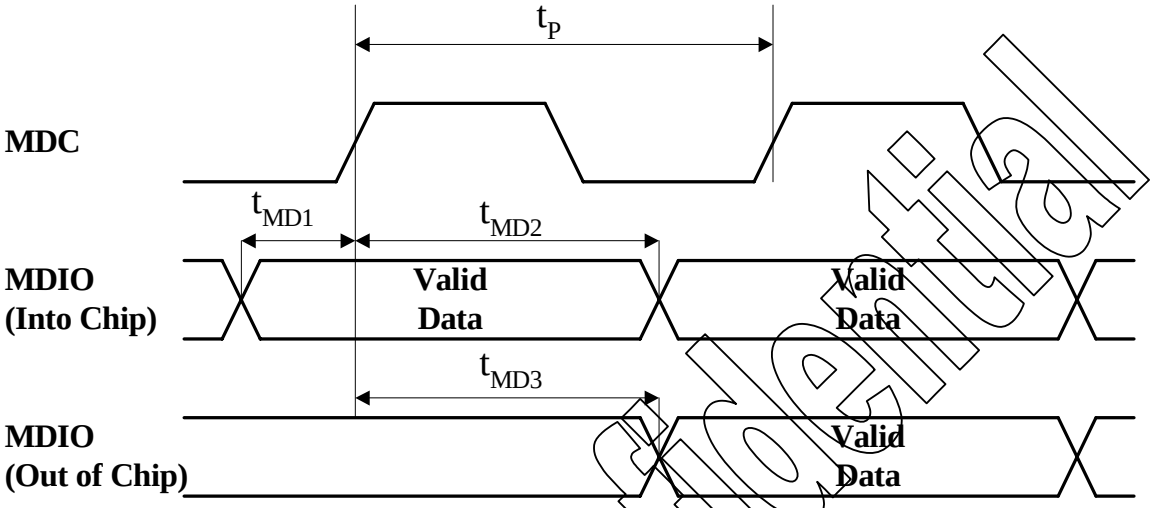
		min.	typ.	max.
t_P	RXC period		40ns	
t_{WL}	RXC pulse width	20ns		
t_{WH}	RXC pulse width	20ns		
t_{SU}	RXD[3:0], RXER, RXDV setup to rising edge of RXC		20ns	
t_{HD}	RXD[3:0], RXER, RXDV hold from rising edge of RXC		20ns	
t_{RLAT}	CRS to RXD latency, 4B or 5B aligned	1BT	2BT	3BT
t_{CRS1}	"Start of Stream" to CRS asserted		140ns	
t_{CRS2}	"End of Stream" to CRS de-asserted		170ns	

Auto Negotiation / Fast Link Pulse Timing



		min.	typ.	max.
t_{BTB}	FLP burst to FLP burst	8ms	16ms	24ms
t_{FLPW}	FLP burst width		2ms	
t_{PW}	Clock/Data pulse width		100ns	
t_{CTD}	Clock pulse to data pulse		69us	
t_{CTC}	Clock pulse to clock pulse		136us	
	Number of Clock/Data pulses per burst	17		33

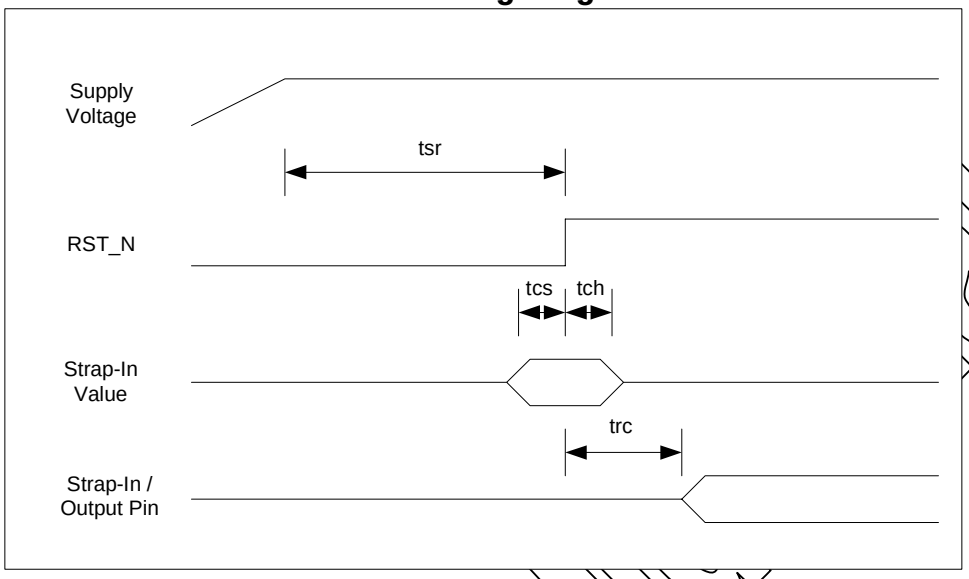
Serial Management Interface Timing



		min.	typ.	max.
t_P	MDC period		400 ns	
t_{MD1}	MDIO Setup to MDC (MDIO as input)	10ns		
t_{MD2}	MDIO Hold after MDC (MDIO as input)	10ns		
t_{MD3}	MDC to MDIO Valid (MDIO as output)		222ns	

Reset Timing

Reset Timing Diagram



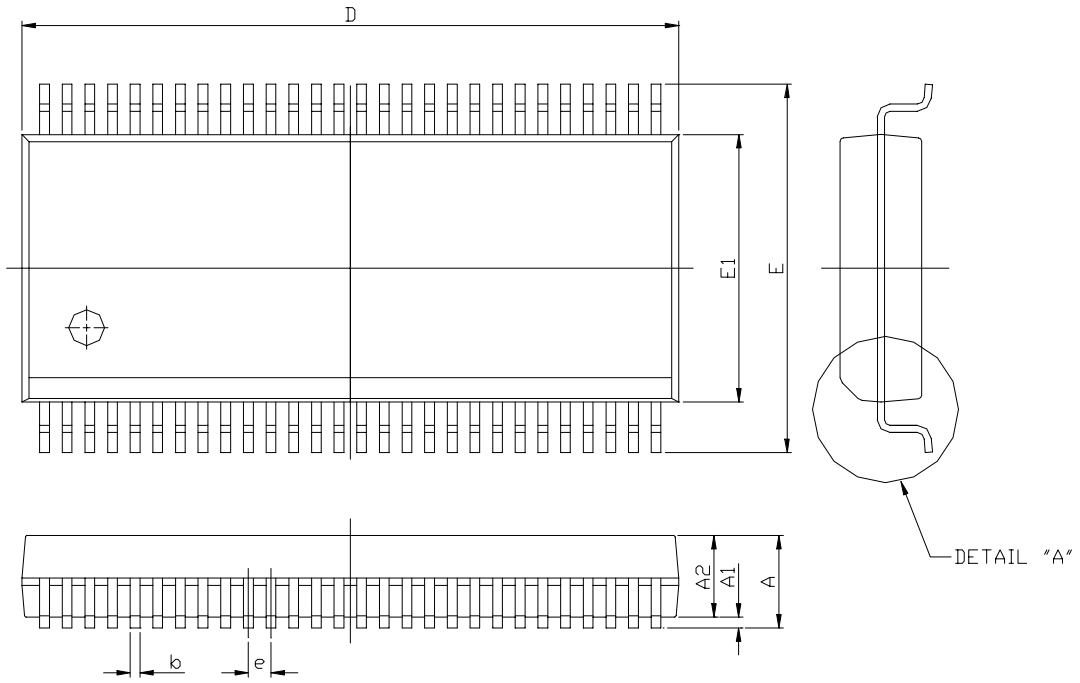
Reset Timing Parameters

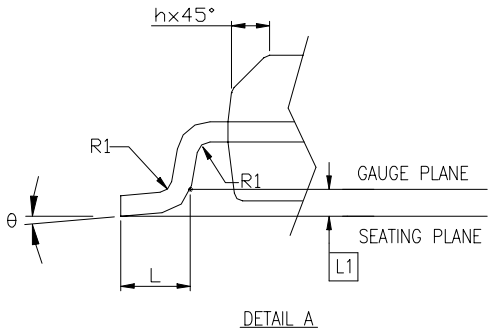
Parameter	Description	Min	Max	Units
t_{sr}	Stable supply voltages to reset high	10		ms
t_{cs}	Configuration setup time	50		ns
t_{ch}	Configuration hold time	50		ns
t_{rc}	Reset to Strap-In pin output	50		us

Magnetic Vendor Selection Lists

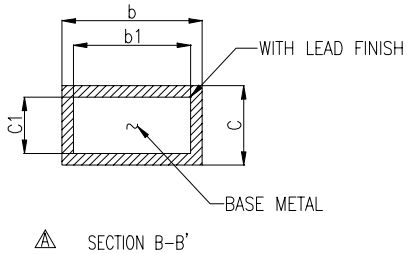
Single Port			
Magnetic manufacturer	Part number	AUTO MDIX	Number of port
Pulse	H1102	Yes	1
Bel Fuse	S558-5999-U7	Yes	1
YCL	PT163020	Yes	1
Transpower	HB726	Yes	1
Delta	LF8505	Yes	1
LanKom	LF-H41S	Yes	1

48 PIN SSOP PACKAGE OUTLINE





DETAIL A

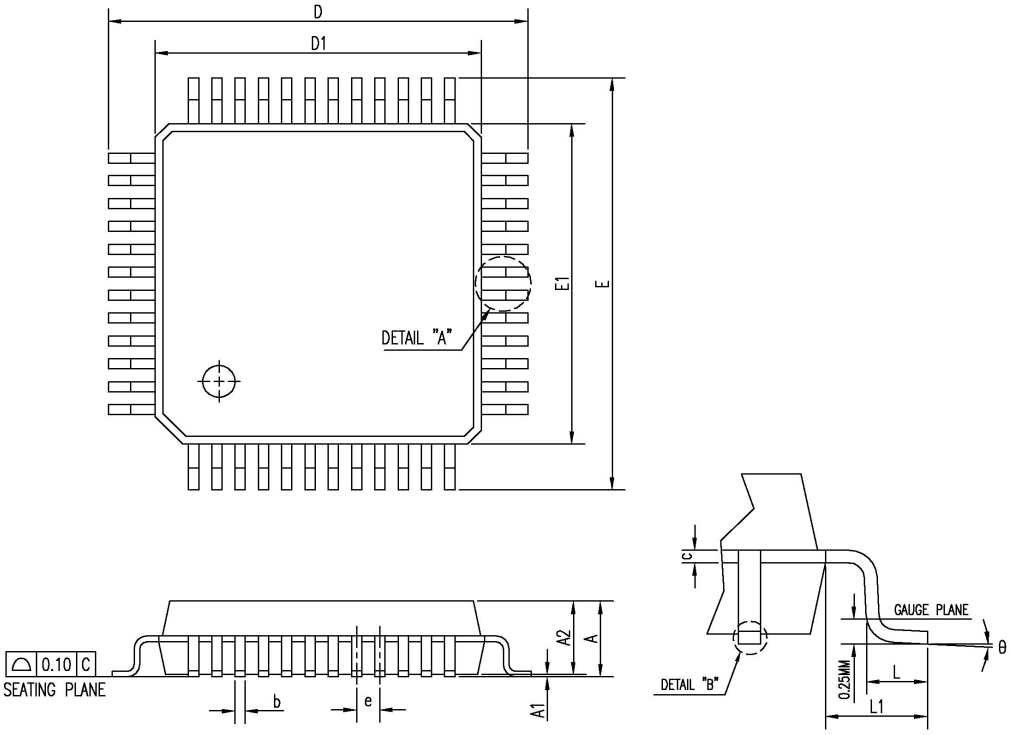


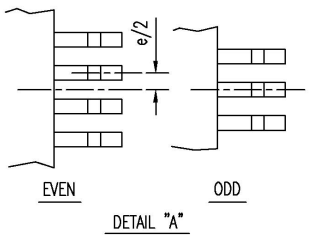
⚠ SECTION B-B'

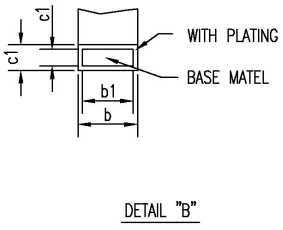
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	2.413	2.591	2.794	0.095	0.102	0.110
A1	0.203	0.305	0.406	0.008	0.012	0.016
b	0.203		0.343	0.008		0.014
b1	0.203	0.254	0.305	0.008	0.010	0.012
c	0.127		0.254	0.005		0.010
c1	0.127		0.216	0.005		0.009
E	10.058	10.312	10.566	0.396	0.406	0.416
E1	7.391	7.493	7.595	0.291	0.295	0.299
e	0.635 BASIC			0.025 BASIC		
h	0.381		0.635	0.015		0.025
L	0.508		1.016	0.020		0.040
L1	0.254 BASIC			0.010 BASIC		
R1						
θ	0		5	0		5

	D (MM)			JEDEC
N	MIN.	NOM	MAX.	
48	15.748	15.875	16.002	MO-118AA
56	18.288	18.415	18.542	MO-118AB

48 PIN LQFP PACKAGE OUTLINE







SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
c	0.129 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						

	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.19	0.22	0.25	0.17	0.20	0.23	0.50 BSC.			
64L	0.13	0.16	0.19	0.13	0.16	0.19	0.40 BSC.			

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