Team meeting 2/26/2025

* new microcontroller

esp32-s3-wroom-1-n16

2/27/2025

Signal list

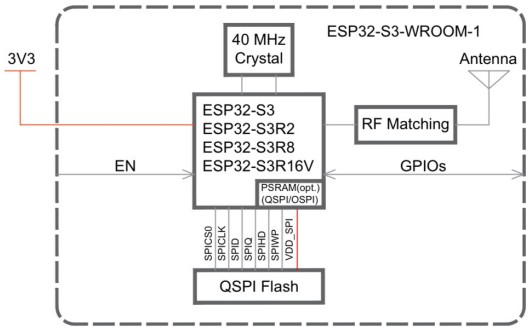


Figure 1: ESP32-S3-WROOM-1 Block Diagram

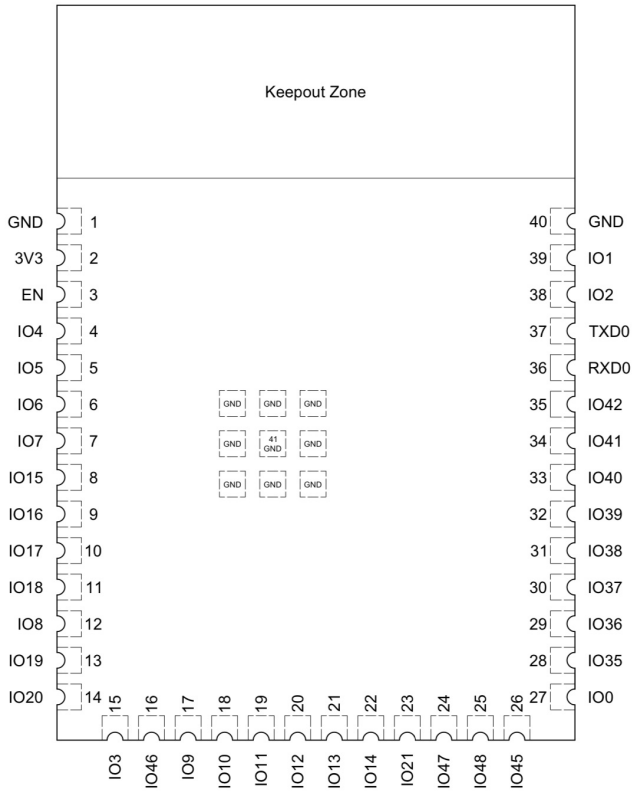


Figure 3: Pin Layout (Top View)

Table 3: Pin Definitions

used for programming screen leds

Name	No.	Type [a]	Function
GND	1	P	GND
3V3	2	P	Power supply
EN	3	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.
IO4	4	I/O/T	RTC_GPIO4, **GPIO4**, TOUCH4, ADC1_CH3
IO5	5	I/O/T	RTC_GPIO5, **GPIO5**, TOUCH5, ADC1_CH4
IO6	6	I/O/T	RTC_GPIO6, **GPIO6**, TOUCH6, ADC1_CH5
IO7	7	I/O/T	RTC_GPIO7, **GPIO7**, TOUCH7, ADC1_CH6
IO15	8	I/O/T	RTC_GPIO15, **GPIO15**, UORTS, ADC2_CH4, XTAL_32K_P
IO16	9	I/O/T	RTC_GPIO16, **GPIO16**, UOCTS, ADC2_CH5, XTAL_32K_N
IO17	10	I/O/T	RTC_GPIO17, **GPIO17**, U1TXD, ADC2_CH6
IO18	11	I/O/T	RTC_GPIO18, **GPIO18**, U1RXD, ADC2_CH7, CLK_OUT3
IO8	12	I/O/T	RTC_GPIO8, **GPIO8**, TOUCH8, ADC1_CH7, SUBSPICS1
IO19	13	I/O/T	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, **USB_D-**
IO20	14	I/O/T	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, **USB_D+**
IO3	15	I/O/T	RTC_GPIO3, **GPIO3**, TOUCH3, ADC1_CH2
IO46	16	I/O/T	**GPIO46**
IO9	17	I/O/T	RTC_GPIO9, **GPIO9**, TOUCH9, ADC1_CH8, FSPIHD, SUBSPIHD
IO10	18	I/O/T	RTC_GPIO10, **GPIO10**, TOUCH10, ADC1_CH9, FSPICS0, FSPIIO4, SUBSPICS0
IO11	19	I/O/T	RTC_GPIO11, **GPIO11**, TOUCH11, ADC2_CH0, FSPID, FSPIIO5, SUBSPID
IO12	20	I/O/T	RTC_GPIO12, **GPIO12**, TOUCH12, ADC2_CH1, FSPICLK, FSPIIO6, SUBSPICLK
IO13	21	I/O/T	RTC_GPIO13, **GPIO13**, TOUCH13, ADC2_CH2, FSPIQ, FSPIIO7, SUBSPIQ
IO14	22	I/O/T	RTC_GPIO14, **GPIO14**, TOUCH14, ADC2_CH3, FSPIWP, FSPIDQS, SUBSPIWP
IO21	23	I/O/T	RTC_GPIO21, **GPIO21**
IO47 [c]	24	I/O/T	SPICLK_P_DIFF,**GPIO47**, SUBSPICLK_P_DIFF
IO48 [c]	25	I/O/T	SPICLK_N_DIFF,**GPIO48**, SUBSPICLK_N_DIFF
IO45	26	I/O/T	**GPIO45**
IO0	27	I/O/T	RTC_GPIO0, **GPIO0**
IO35 [b]	28	I/O/T	SPIIO6, **GPIO35**, FSPID, SUBSPID
IO36 [b]	29	I/O/T	SPIIO7, **GPIO36**, FSPICLK, SUBSPICLK
IO37 [b]	30	I/O/T	SPIDQS, **GPIO37**, FSPIQ, SUBSPIQ
IO38	31	I/O/T	**GPIO38**, FSPIWP, SUBSPIWP
IO39	32	I/O/T	**MTCK**, GPIO39, CLK_OUT3, SUBSPICS1
IO40	33	I/O/T	**MTDO**, GPIO40, CLK_OUT2
IO41	34	I/O/T	**MTDI**, GPIO41, CLK_OUT1
IO42	35	I/O/T	**MTMS**, GPIO42
RXD0	36	I/O/T	**U0RXD**, GPIO44, CLK_OUT2
TXD0	37	I/O/T	**U0TXD**, GPIO43, CLK_OUT1
IO2	38	I/O/T	RTC_GPIO2, **GPIO2**, TOUCH2, ADC1_CH1
IO1	39	I/O/T	RTC_GPIO1, **GPIO1**, TOUCH1, ADC1_CH0
GND	40	P	GND
EPAD	41	P	GND

input
input
input
output

rotary encoder A
rotary encoder B
clear button
vibration motor

→ button/RC circuit

used for debugging, can connect directly to micro USB

white/blue led indicator

already pulled down for programming. do not use!

FSPI HD
FSPICS0
FSPI D
FSPI CLK
FSPI Q
FSPI WP

~ may be 1.8V
~ may be 1.8V

0: VDD_SPI powered from VDD3P3_RTC, 1: 1.8V

-> button/RC circuit

EFUSE_PIN_POWER_SELECTION	1	N	18	Represents the power supply for GPIO33 ~ GPIO37, GPIO47, and GPIO48.

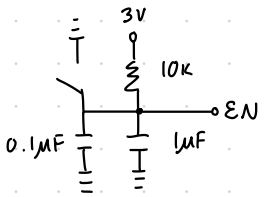
-> TXD on programmer
-> RXD on programmer

[a] P: power supply; I: input; O: output; T: high impedance. Pin functions in bold font are the default pin functions. For pin 28 ~ 30, the default function is decided by eFuse bit.

[b] For modules with Octal SPI PSRAM, i.e., modules embedded with ESP32-S3R8 or ESP32-S3R16V, pins IO35, IO36, and IO37 are connected to the Octal SPI PSRAM and are not available for other uses.

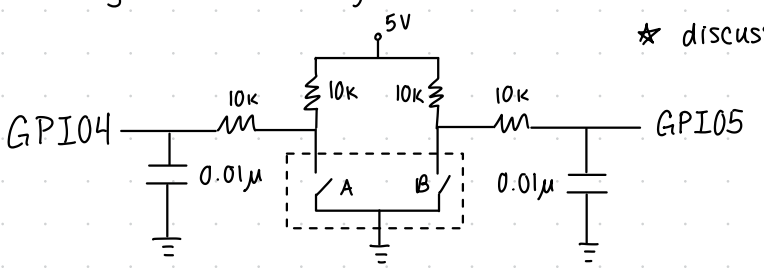
★ not our chip

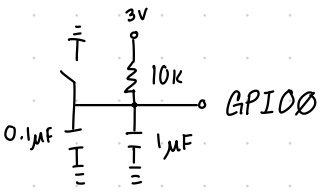
[c] For modules embedded with ESP32-S3R16V, as the VDD_SPI voltage of the ESP32-S3R16V chip is set to 1.8 V, the working voltage for GPIO47 and GPIO48 is also 1.8 V, which is different from other GPIOs.



★ rotary encoder needs ground, debounced (2 caps)

★ discuss using internal pullups





★ SPI2 + SPI3 are general purpose, 0 + 1 are used by esp32
↳ pins can be chosen from any GPIOs via GPIO matrix
↳ interface 4c recommended via IO MUX

https://www.espressif.com/sites/default/files/documentation/esp32-s3_datasheet_en.pdf#cd-pins-io-mux-gpio

Table 4: Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO0	Weak pull-up	1
GPIO3	Floating	–
GPIO45	Weak pull-down	0
GPIO46	Weak pull-down	0

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

GPIO0 and GPIO46 control the boot mode after the reset is released. See Table 6 *Chip Boot Mode Control*.

Table 6: Chip Boot Mode Control

Boot Mode	GPIO0	GPIO46
SPI Boot	1	Any value
Joint Download Boot [2]	0	0

★ 46 comes pulled down to 0

[1] **Bold** marks the default value and configuration.

[2] Joint Download Boot mode supports the following download methods:

- USB Download Boot:
  - USB-Serial-JTAG Download Boot
  - USB-OTG Download Boot
- UART Download Boot

In SPI Boot mode, the ROM bootloader loads and executes the program from SPI flash to boot the system.

In Joint Download Boot mode, users can download binary files into flash using UART0 or USB interface. It is also possible to download binary files into SRAM and execute it from SRAM.

9 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

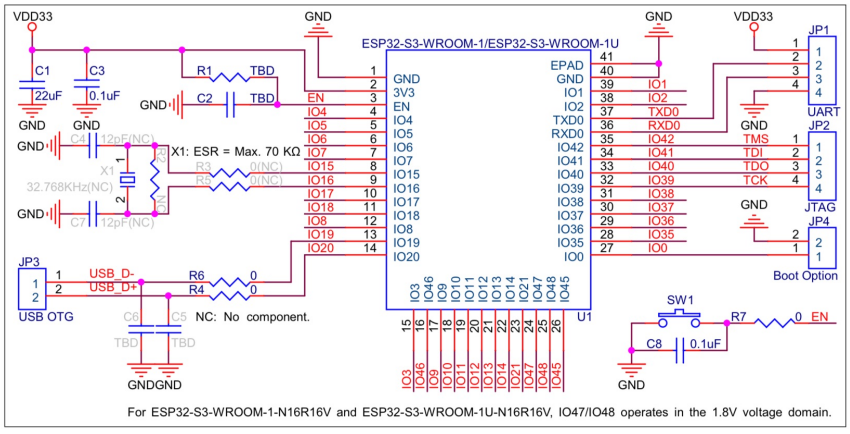


Figure 7: Peripheral Schematics