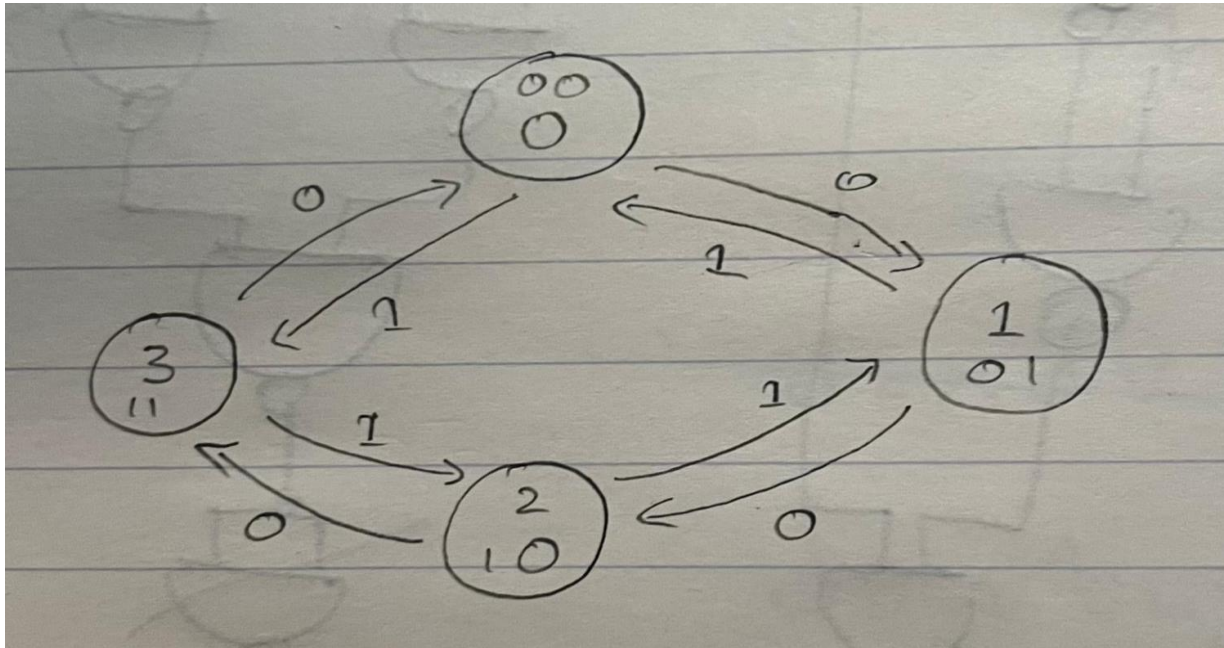


Exercise 4

(Design the cyclic counter using D or JK flip-flops, which counts clock pulses modulo 4)

State Diagram:

First, we make a diagram for the clock pulses to get a better understanding to create our state transition table



State Transition Table:

Now we make state transition table to find D1 and D2

Sates	Present State	Input	Next State	D1	D2
0	00	0	01	0	1
1	01	0	10	1	0
2	10	0	11	1	1
3	11	0	00	0	0
0	00	1	11	1	1
1	01	1	10	1	0
2	10	1	01	0	1
3	11	1	00	0	0

Karnaugh Map:

Now we make the Karnaugh Map for D1 and D2 to find the functions to make our circuit.

		<i>BC</i>			
<i>I</i>		<i>00</i>	<i>01</i>	<i>11</i>	<i>10</i>
	<i>0</i>	0	1	0	1
	<i>1</i>	1	1	0	0

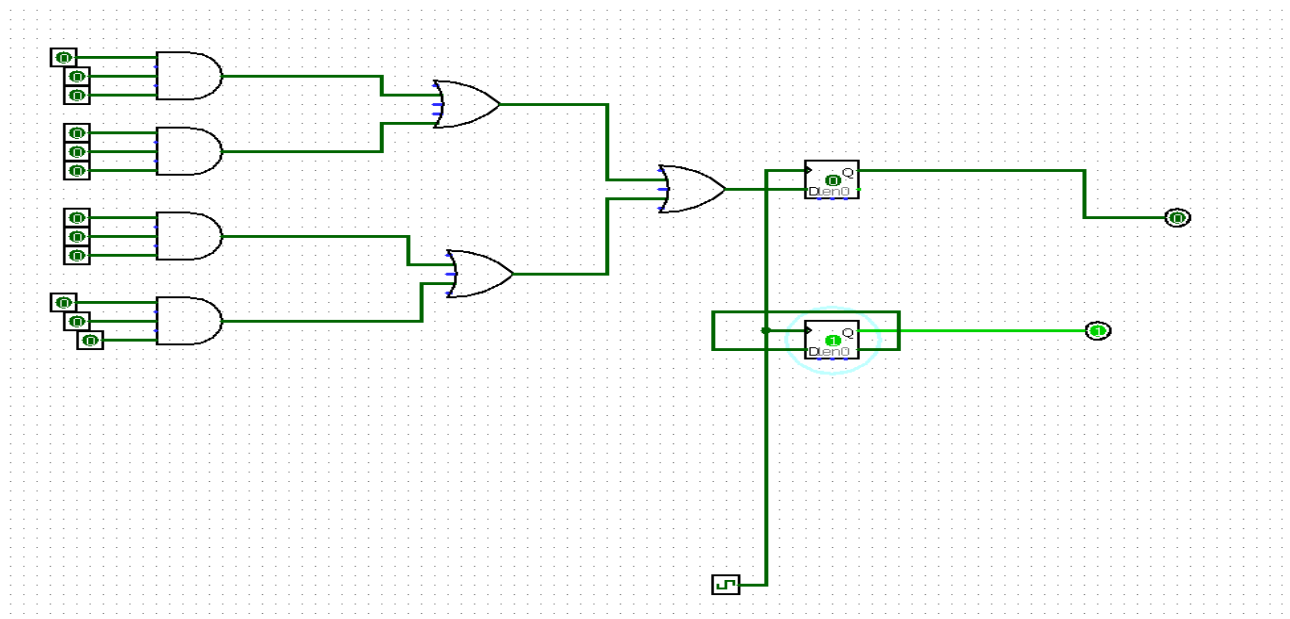
$$D1 = \sim bc + \sim ab \sim c + a \sim b$$

		<i>BC</i>			
<i>I</i>		<i>00</i>	<i>01</i>	<i>11</i>	<i>10</i>
	<i>0</i>	1	0	0	1
	<i>1</i>	1	0	0	1

$$D2 = \sim c$$

Circuit (OR, AND, D-Flip flops):

By using the function we can now create the circuit where its accurate to our table values.



Conclusion:

Asynchronous counter that can store data and count up or down based on input using either D flip-flops or J-K flip-flops in this project. When the input $x = 1$, the counter will count up: 0, 1, 2, 3, 0, 1, 2, 3,..., and when the input $x = 0$, the counter will count down: 0, 1, 2, 3, 0, 1, 2, 3,...

As a result, the flip-flop can count pulses and synchronize variable-timed input signals with a fundamental reference signal [1].