The synchronous system

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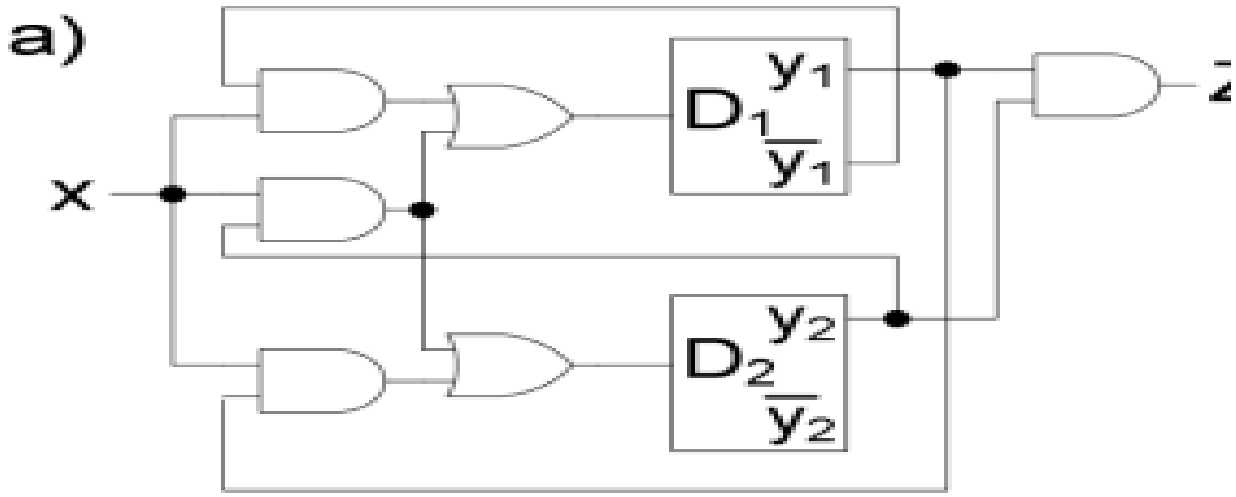
Excerise: 5

Introduction:

A synchronous system is a system whose value depends on time. In the interpretation of this task, sometimes there is a clock speed (changes in the value on the set of logical values), which causes changes in the values on the outputs of the flip-flops. The second flip-flop in this task is a flip-flop of the JK type.



Tranformation Circuit(NAND GATES):

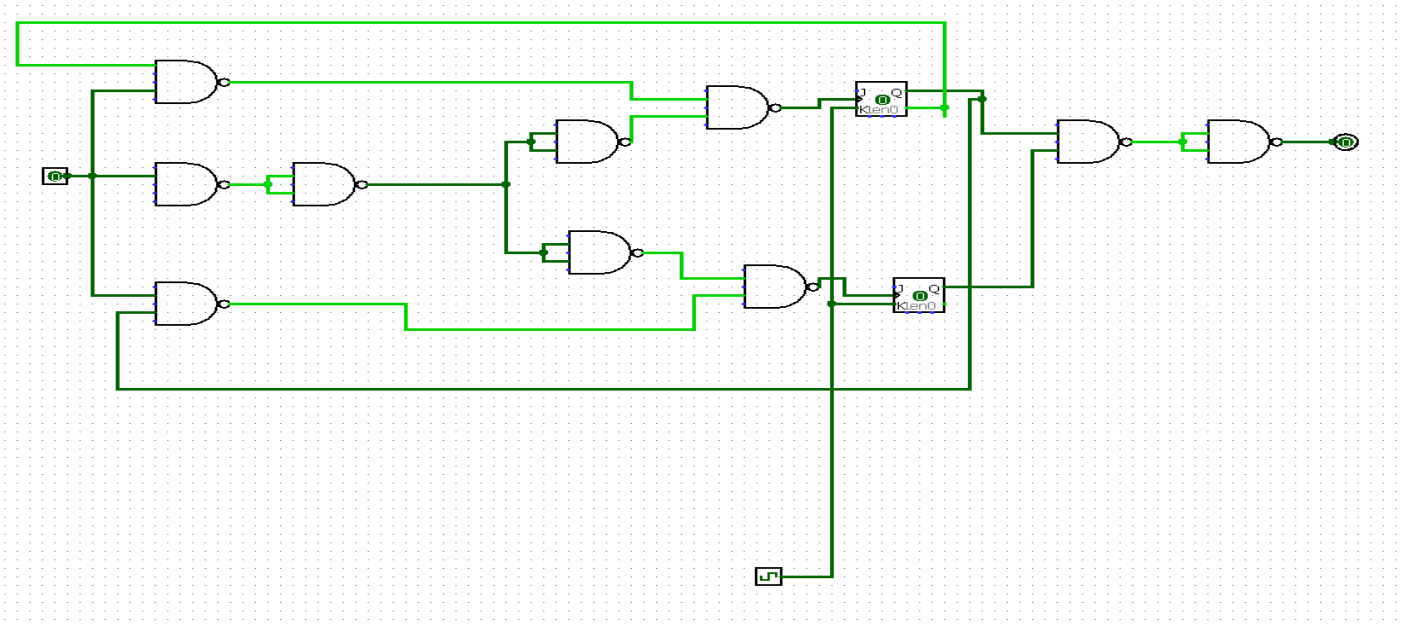


Table (JK flip flops included):

x	y_1	y_2	D_1	D_2	J_1	K_1	J_2	K_2
0	0	0	0	0	0	X	0	X
0	0	1	0	0	0	X	X	1
0	1	0	0	0	X	1	0	X
0	1	1	0	0	X	1	X	1
1	0	0	1	0	1	X	0	X
1	0	1	1	1	1	X	X	0
1	1	0	0	1	X	1	1	X
1	1	1	1	1	X	0	X	0

Now we are building a Karnaugh map for each of the JK Flip-Flops inputs:

J_1	x=0	x=1
y_1y_2=00	0	1
y_1y_2=01	0	1
y_1y_2=11	×	×
y_1y_2=10	×	×

J1 = x

K_1	x=0	x=1
y_1y_2=00	×	×
y_1y_2=01	×	×
y_1y_2=11	1	0
y_1y_2=10	1	1

K1 = $\overline{x}$+ $\overline{\overline{y}}_2$

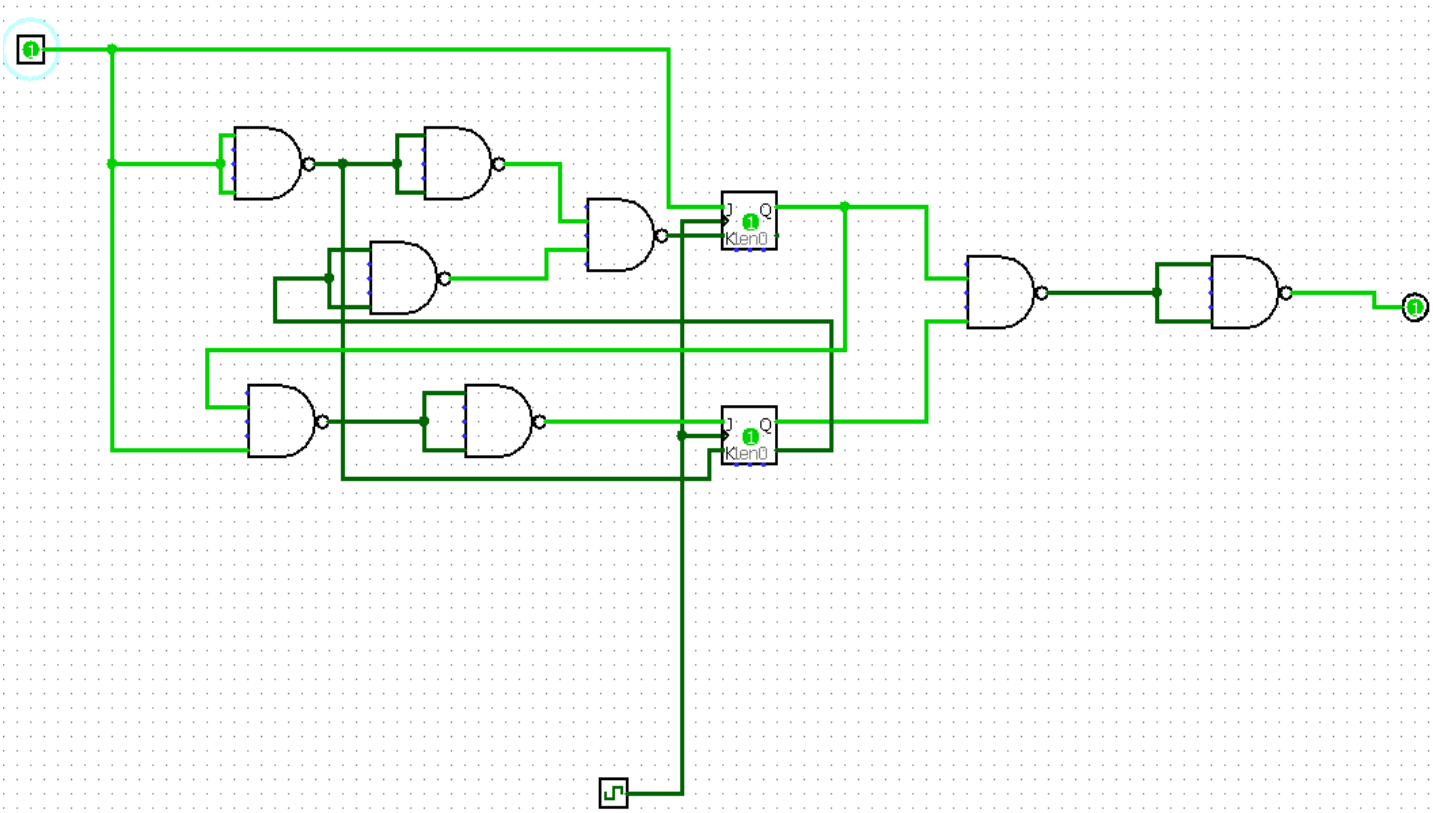
J_2	x=0	x=1
y_1y_2=00	0	0
y_1y_2=01	×	×
y_1y_2=11	×	×
y_1y_2=10	0	1

J2 = xy_1

K_2	x=0	x=1
y_1y_2=00	×	×
y_1y_2=01	1	0
y_1y_2=11	1	0
y_1y_2=10	×	×

$K_2 = \overline{x}$

Final circuit:



The measurement results shown on circuit:

Step	t_0	t_1	t_2	t_3	t_4	t_5
x	1	1	1	1	0	0
y1, y2	10	01	11	11	00	00
Z	0	0	1	1	0	0

Summary:

After the transformation of The initial synchronous circuit and by performation correct state transformations using D flip flops and Jk flip flops we achived a circuit that gave us output 1 only when the input are 1 and y1y2 11 other then that it gave us 0 as result even when our y1y2 were 10 01.