Verification Report

[Verification of AHB-Lite Memory]

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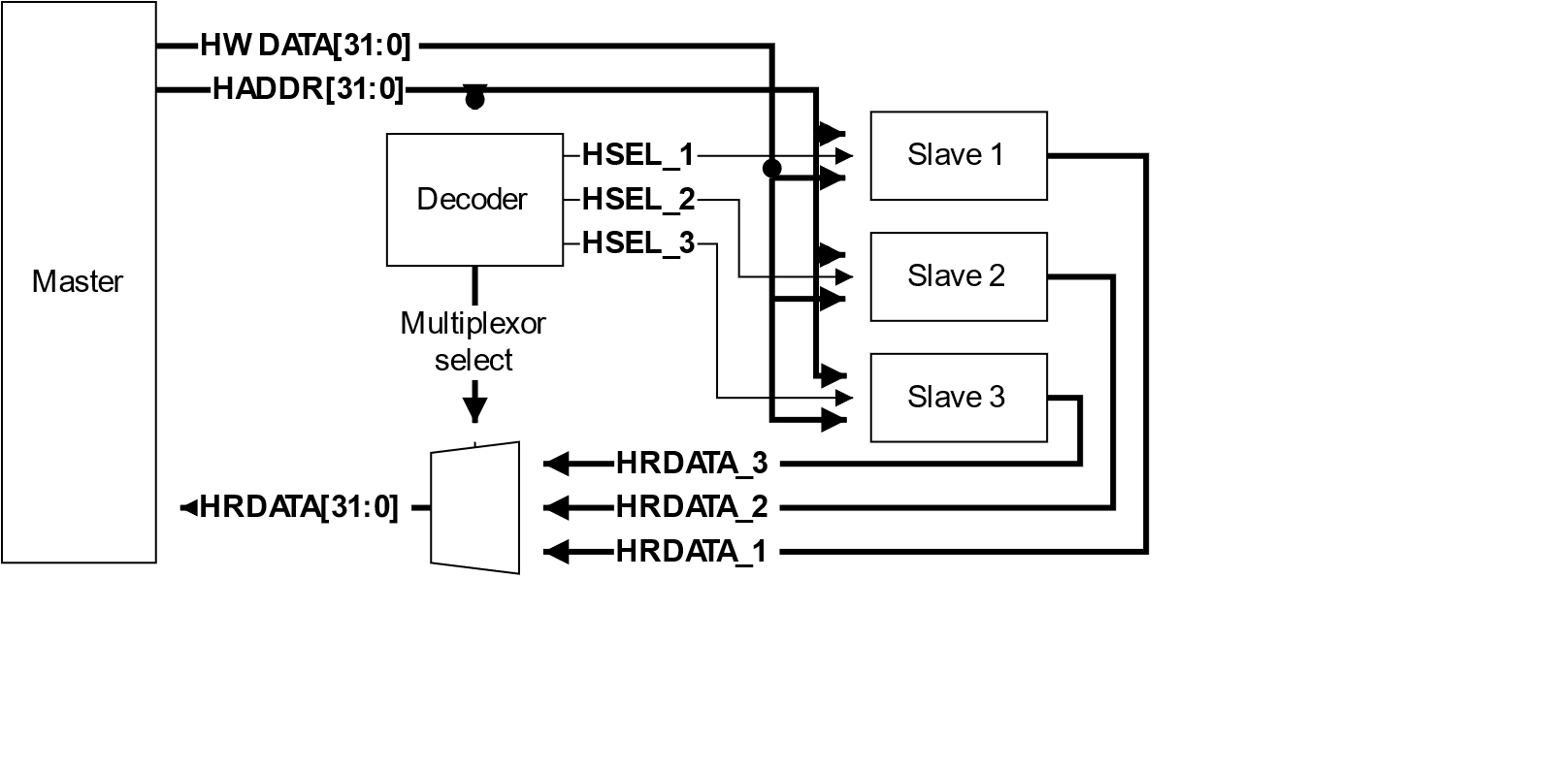
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# Introduction to the Device-Under-Test (DUT)

The DUT is AMBA (Advanced Microcontroller Bus Architecture) 3(3rd version) AHB-Lite (Advanced High-performance Bus), which is the interface used for communication between different on-chip IPs. AHB ensures high-performance of systems on chip (SOC) designs, because of its various features such as burst transfer, single clock edge operations, non-tristate implementation and wide data bus configurations, 64, 128, 256, and 1024 bits.

This is a Lite version of AHB hence it is a single master system. There is only one source of address, control, and write data, so no master-to-slave multiplexor is required.  When implemented on a chip, it must be attached with some memory module. And the master/controlling IP would be sending/receiving data to/from this memory, which is the slave. The master and slave interact with data and control signals.

Below is given the block diagram of AHB-Lite block. It has single master and three slaves and a decoder with multiplexer from slave to master.



# Verification Plan

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **No.** | **Feature** | **Test Description** | **Ref.** | **Type** | **Result** | **Comments** |
| 1 | Enable/Disable the value of **HWRITE** | HWRITE controls the direction of data transfer to or from the master, HWRITE is HIGH, it indicates a write transfer and the master broadcasts data on the write data bus, HWDATA [31:0] HWRITE is LOW, a read transfer is performed and the slave must generate the data on the read data bus, HRDATA [31:0]. | IHI0033.pdf/Sec 3.1/pg3-2 | TR |  |  |
| 2 | **HTRANS [1:0]** set to BUSY | Slaves must always provide a zero-wait state OKAY response to BUSY transfers and the transfer must be ignored by the slave. | IHI0033.pdf/Sec 3.2/pg3-5 | TR |  |  |
| 3 | **HTRANS [1:0]** set to IDLE | Slaves must always provide a zero-wait state OKAY response to IDLE transfers and the transfer must be ignored by the slave. | IHI0033.pdf/Sec 3.2/pg3-5 | TR |  |  |
| 4 | **HTRANS [1:0]** set to NONSEQ/SEQ | Indicates a single transfer or the first transfer of a burst for NONSEQ.  The remaining transfers in a burst are SEQUENTIAL and the address is related to the previous transfer. | IHI0033.pdf/Sec 3.2/pg3-5 | TR |  |  |
| 5 | Use **HBURST [2:0]** at different values b000-b111 | Bursts of 4, 8, and 16-beats, undefined length bursts, and single transfers are defined in this protocol. The number of beats is controlled by HBURST and the transfer size is controlled by HSIZE. | IHI0033.pdf/Sec 3.5/pg3-9 | TR |  |  |
| 6 | **HTRANS [1:0]** set to BUSY transfer type, to end a burst of fixed length | The protocol does not permit a master to end a burst with a BUSY transfer for fixed length bursts of type:  • incrementing INCR4, INCR8, and INCR16  • or wrapping WRAP4, WRAP8, and WRAP16.  These fixed lengths burst types must terminate with a SEQ transfer | IHI0033.pdf/Sec 3.5.1/pg3-10 | A |  |  |
| 7 | **HTRANS [1:0]** set to SEQ transfer type, to end a burst of fixed length from state BUSY | When the HTRANS transfer type changes to SEQ the master must keep HTRANS constant, until HREADY is HIGH. | IHI0033.pdf/Sec 3.6.1/pg3-17 | A |  |  |
| 8 | **HTRANS [1:0]** set to BUSY transfer type after a single burst (HBURST [2:0] = b000) | The master is not permitted to perform a BUSY transfer immediately after a SINGLE burst. SINGLE bursts must be followed by an IDLE transfer or a NONSEQ transfer. | IHI0033.pdf/Sec 3.5.1/pg3-10 | A |  |  |
| 9 | Enable/Disable **HMASTLOCK** | This signal indicates to any slave that the current transfer sequence is indivisible and must therefore be processed before any other transactions are processed | IHI0033.pdf/Sec 3.3/pg3-7 | A |  |  |
| 10 | Check **HRESP** state by making transfer at non-existent address | If a NONSEQUENTIAL or SEQUENTIAL transfer is attempted to a non-existent address location then the slave provides an ERROR response. IDLE or BUSY transfers to non-existent locations result in a zero-wait state OKAY response. | IHI0033.pdf/Sec 4.1.1/pg4-2 | TR |  |  |
| 11 | Check **HRESP** state by extending data transfer, keeping **HREADY** at LOW | HREADY signal when set LOW, causes wait states to be inserted into the transfer and enables the slave to have extra time to provide the data. HRESP must also be LOW with HREADY. | IHI0033.pdf/Sec 5.1.3/pg5-3 | A |  |  |
| 12 | Check **HRESP** state by extending data transfer, keeping **HREADY** at HIGH | HREADY signal when set HIGH, master must hold the data valid until the transfer completes and enables the slave to have extra time to sample the data. HRESP must also be HIGH and HTRANS stay IDLE. | IHI0033.pdf/Sec 5.1.3/pg5-3 | A |  |  |
| 13 | Attempt a transfer where the width, as indicated by **HSIZE**, is wider than the data bus that it connects to | The master must never attempt a transfer where the width, as indicated by HSIZE, is wider than the data bus that it connects to.  slave can use the ERROR transfer response. | IHI0033.pdf/Sec 6.2.3/pg6-2 | TR |  |  |
| 14 | Implementing a wide slave on a narrow bus | Replicate the data on both halves of the wide bus | IHI0033.pdf/Sec 6.2.2/pg6-2 | TR |  |  |
| 15 | Implementing a master on a wide bus | • multiplexing the input bus • replicating the output bus. | IHI0033.pdf/Sec 6.2.3/pg6-2 | TR |  |  |
| 16 | Enable the value of **HRESETn** | During reset all masters must ensure the address and control signals are at valid levels and that HTRANS [1:0] indicates IDLE. During reset all slaves must ensure that HREADYOUT is HIGH. | IHI0033.pdf/Sec 7.1.2/pg7-2 | A |  |  |

## Explanation of Different Fields

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| **No.** | The serial number of the test. |
| **Feature** | The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level of a user. |
| **Test Description** | A detailed description of the test case being performed. You can be as verbose as you want. |
| **Ref.** | Reference to the section in the related standard document. The section number as well as page numbers should be described here. |
| **Type** | Type of the test. Whether the test is an assertion (A) or a transaction (T) type. |
| **Result** | Pass (P) or Fail (F). |
| **Comments** | Any other comments about the test or its results that you want to mention. |