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UNIVERSITY OF TECHNOLOGY
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LOGIC DESIGN PROJECT - CO3091

Final report
Group 2

Assignment

TRAFFIC LIGHT SYSTEM

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1 Introduction

1.1 Introduction to Traffic light system

1.1.1 The origin of the traffic lights

Traffic lights have been playing a crucial and indispensable role in regulating the road traffic and ensuring safety. Nowadays, red, amber, green,... are typically a signal to almost every person when it comes to participating in traffic whether they should stop, go or get ready to either stop or go at intersections and pedestrian crossings. The journey of the traffic lights dates back to 1868, when the first manually operated signal was installed outside the British Houses of Parliament to manage horse-drawn traffic.

1.1.2 The early concept of controlling the flow of traffic in intersection

The very first traffic signal signal was invented in London, England, in 1968. Designed by a British railway manager, John Peake Knight, who suggested adopting a railway method for controlling traffic, as railroads used a semaphore system with a small arms extending from a pole to represent the signal for a train to pass or not. According to Knight's adaptation, The mechanism used arms that extended horizontally to indicate "Stop" and at a 45-degree angle for "Go" during daytime. At night, to ensure visibility and also maintain the functionality, a gas-lit semaphore red and green light would be used at the top of the post. A police officer would be positioned under the signals to operate them. However, this method was disastrous and short-lived. Less than two months later, a gas explosion occurred, killing the police officer operating it. Due to high safety concerns at that time, the project was quickly abandoned.

This first attempt revealed the necessity of traffic flow control in cities. However, the evolution of traffic control had to wait more than 4 more decades until the introduction of a new type of energy, now widely used, electricity. At the same time, the rise of motor vehicles brought back the question of modern traffic lights systems.

1.1.3 The Pre-Completed Three-Color System and Early Improvements

The breakthrough that redefined the traffic lights layout as we have always been using these days came in 1920. William Potts, a Detroit police officer, who is credited for inventing the three-lens traffic lights. As the driver did not manage to respond in time with the signal at a certain speed, Potts added in one more signal, the yellow light, which logically means "Caution". The yellow is placed after the green light in the priority, which tells the driver that the red light is about to light up and they would have to lower the speed to stop before the light.

He also came up with the design of the three-light, four-way traffic signal tower although he was not able to patent the system as of this major.

Shortly after that, an African-American inventor Garrett Morgan brought to the world a "T-shaped" traffic signal design that also has a caution signal. Morgan's traffic lights was more advanced as it allowed for an all-stop phase, vehicles from all directions would come to a halt before any change in direction. His design later solved the safety concerns, which had peaked since the gas-lit traffic system and complex traffic flow problem that all those previous models overlooked and laid the groundwork for future developments.

1.2 Introduction to Project

1.2.1 Specification

This report will have 4 intersections - each has its own time counter and traffic lights (red, green, amber/yellow).

In mode 1, the user can input the number of seconds for green and amber (in binary), red timer will be the addition of the twos. The maximum for any timer is 99 seconds. The intersection will use a 2 phase control system, as shown in the picture below.

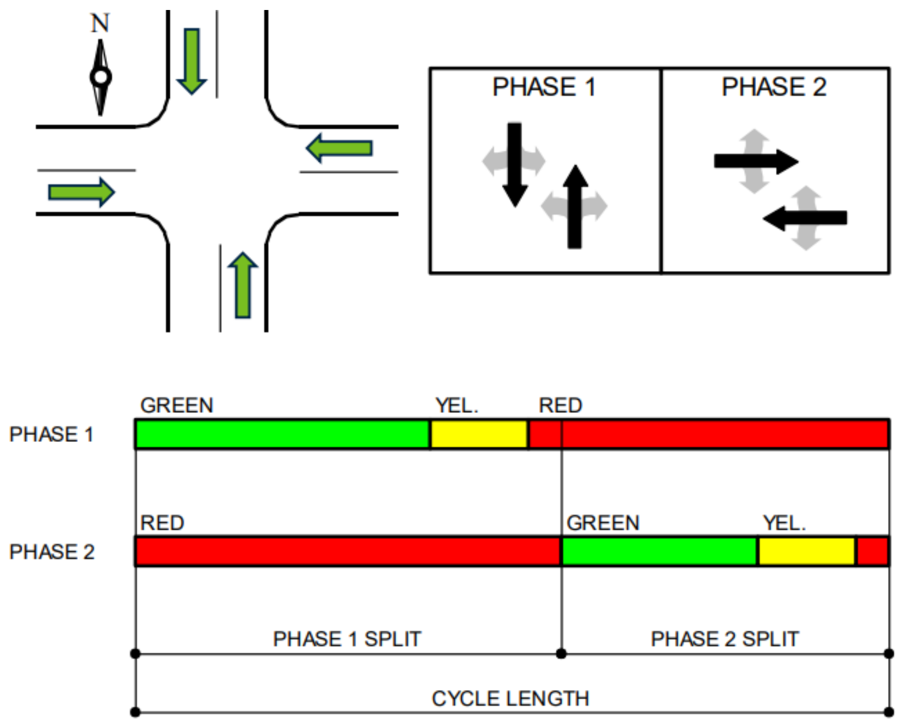


Figure 1: 2 phases system, (Source: Traffic Signals 101 Course Manual)

In mode 2 (manual), user will control lights for each intersections (independent from each other).

1.2.2 Technical resources

Proteus, developed by LabCenter Electronics Ltd, is without doubt the best schematic entry, known for its handy and forceful simulation capabilities, gives us an ability to rebuild a realistic concept of a traffic intersection with visual indicators for red, yellow, and green lights and LED display for the timing system integrated with signals.

2 Components

2.1 Logic gates: AND, OR, NOT

Logic gates are fundamental building blocks to day to day circuit, in this project we use logic gates to deal with various things like check ouput,etc.

AND Gate

Theory: An AND gate is a basic digital logic gate that implements logical conjunction. It has two or more inputs and one output. The output of the AND gate is HIGH (1) only when all its inputs are HIGH (1). If any input is LOW (0), the output is LOW (0).

The logical operation can be expressed as, where "A" and "B" are the inputs, and "Q" is the output:

Table 1: Truth Table

Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

Applications: AND gates are used in circuits where multiple conditions must be true for an action to occur, such as enabling a device only when multiple signals are active.

OR Gate

Theory: An OR gate is a fundamental logic gate that implements logical disjunction. It has two or more inputs and one output. The output of the OR gate is HIGH (1) if at least one input is HIGH (1). The output is LOW (0) only when all inputs are LOW (0).

The logical operation can be expressed as, where "A" and "B" are the inputs, and "Q" is the output:

Table 2: Truth Table

Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	1

Applications: OR gates are commonly used in circuits where an action occurs if any one of multiple conditions is true, such as in alarms or error detection systems.

NOT Gate

Theory: A NOT gate is a simple digital logic gate that implements logical negation. It has one input and one output. The output is the inverse of the input; it is HIGH (1) if the input is LOW (0), and LOW (0) if the input is HIGH (1).

The logical operation can be expressed as, where "A" is are the inputs, and "Q" is the output:

Table 3: Truth Table

Input A	Output Q
0	1
1	0

Applications: NOT gates are used in circuits where signal inversion is required, such as in control logic or toggling states.

2.2 Resistor

Theory: A resistor is a passive electronic component that limits or regulates the flow of electrical current in a circuit. It achieves this by providing a specific amount of resistance to the current, which is measured in ohms (Ω). Resistors are critical components in nearly all electronic devices, ensuring the appropriate voltage and current levels for various circuit elements. Resistors follow Ohm's Law:

$$R = \frac{V}{I}$$

Where V is voltage, I is current, and R is resistance. This equation establishes the relationship between the voltage drop across the resistor, the current flowing through it, and its resistance value.

Applications:

- **Limiting current to protect components:** Resistors are used to control the flow of current in circuits, preventing sensitive components such as LEDs and transistors from being damaged by excessive current.
- **Dividing voltage in circuits:** By connecting resistors in series or parallel, a portion of the input voltage can be dropped across specific resistors, creating a desired output voltage for use in various parts of the circuit.
- **Pull-up or pull-down resistors in digital circuits:** These resistors are used to ensure that a digital input pin is at a defined logic level (high or low) when no active signal is driving it, avoiding erratic behavior or floating states.

2.3 7-segment Display

Theory: A 7-segment display is an electronic device used for visually displaying numerical values and limited alphanumeric characters. It is composed of seven individual LEDs (segments), arranged in a pattern resembling the number '8'. By selectively activating specific segments, various numbers and characters can be displayed.

Working:

- **Common Anode:** In this configuration, all anodes of the segments are connected together and tied to a high voltage (e.g., $+V$). Individual cathodes are connected to ground through controlling circuits. By sinking current from specific cathodes, corresponding segments light up.
- **Common Cathode:** In this configuration, all cathodes of the segments are connected together and tied to ground. Individual anodes are connected to a positive voltage through controlling circuits. By sourcing current to specific anodes, corresponding segments light up.

  Applications:

- **Digital clocks:** Used for displaying time in a simple and efficient manner, where segments are controlled to represent the numbers for hours, minutes, and seconds.
- **Calculators:** Provides a clear numerical display for performing and showing arithmetic calculations, making them intuitive and user-friendly.
- **Counters:** Commonly used in industrial and consumer electronics to visually represent count values, such as the number of items produced in a manufacturing line or a person's score in a game.

2.4 LED Lights

Theory: A Light Emitting Diode (LED) is a semiconductor device that emits light when an electric current flows through it. This phenomenon, known as electroluminescence, occurs when electrons recombine with holes within the material of the LED, releasing energy in the form of photons. The color of the emitted light depends on the energy band gap of the semiconductor material. LEDs are widely used due to their efficiency, long lifespan, and low power consumption compared to traditional light sources.

Applications:

- **Indicators in circuits:** LEDs are commonly used as visual indicators to display the operational status of electronic devices, such as power-on signals, error alerts, or activity indicators.
- **Illumination in displays:** LEDs serve as the primary source of light in devices like LED screens, digital billboards, and backlit panels, providing bright and vivid displays.
- **Status signaling in devices:** From consumer electronics like smartphones and computers to industrial machinery, LEDs are utilized for conveying operational or error states to users through visual signals.

2.5 Capacitor

Theory: A capacitor is an essential passive electronic component that stores and releases energy in the form of an electric field. It comprises two conductive plates separated by an insulating material known as a dielectric. When a voltage is applied across the plates, an electric charge accumulates on them. The capacitance, measured in farads (F), determines the amount of charge the capacitor can store, which depends on the surface area of the plates, the distance between them, and the properties of the dielectric material.

Applications:

- **Smoothing voltage in power supplies:** Capacitors are often used in power supply circuits to filter and stabilize the voltage output, reducing fluctuations and providing a smooth DC voltage for devices.

- **Coupling and decoupling signals in circuits:** Capacitors enable the transfer of AC signals between different parts of a circuit (coupling) while blocking DC components. They are also used to isolate sensitive components from noise (decoupling).
- **Timing circuits:** In combination with resistors, capacitors form RC circuits that create precise time delays or oscillations, used in applications such as clocks, timers, and frequency generators.

2.6 ICS Part

2.6.1 IC555

The 555 timer IC is well-known as an compact, versatile integrated circuit that is widely used in timer, delay, pulse generation and also oscillator products.

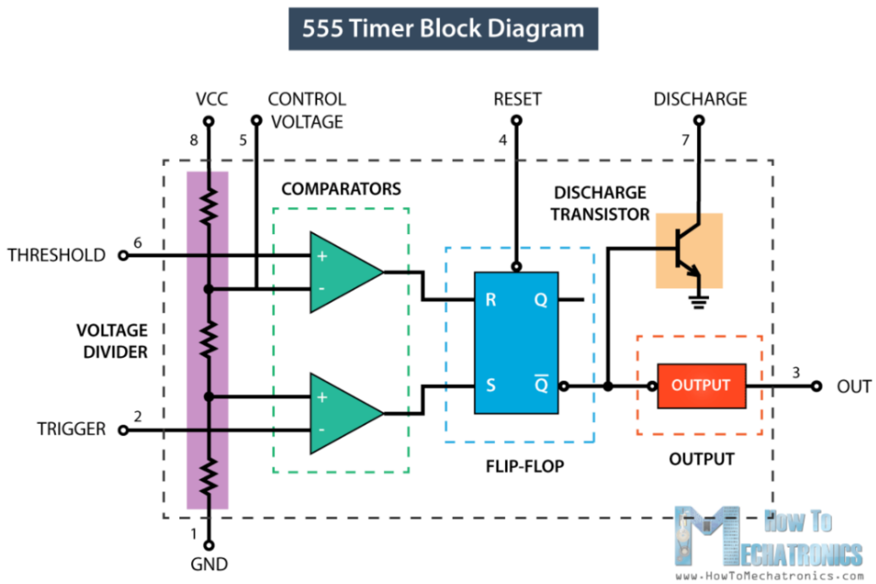


Figure 2: Block Diagram of the 555 Timer IC

The block diagram above provides an overview of the 555 Timer IC's internal components and signal flow:

- **Pin 1 (GND)**: Ground, connects to the negative side of the power supply.
- **Pin 2 (Trigger)**: Activates the timer when the voltage falls below 1/3 Vcc.
- **Pin 3 (Output)**: Provides the output signal.
- **Pin 4 (Reset)**: Resets the timer when pulled low.
- **Pin 5 (Control Voltage)**: Adjusts the reference voltages of the comparators.
- **Pin 6 (Threshold)**: Ends the timing interval when voltage exceeds 2/3 Vcc.
- **Pin 7 (Discharge)**: Connects to the capacitor for timing adjustments.
- **Pin 8 (Vcc)**: Power supply pin, typically between 4.5V and 15V.

The 555 Timer IC operates by charging and discharging an external capacitor through external resistors. Depending on its structures, the IC can work in 3 different modes, which are monostable, astable and bistable, determining its role as a pulse generator, oscillator or flip-flop. The timing cycle is handled by monitoring the capacitor's voltage and comparing it to reference voltage of one-third and two-third of the supply voltage (Vcc).

Monostable Mode

In this mode, the 555 timer serves as a one-shot pulse generator. When an external trigger pulse is signaled, the output goes high for a specified duration configured by an external resistor and capacitor, then returns to its normal state. This is often used for timers, delay circuits, or pulse-width modulation. The internal circuit includes a flip-flop that controls the output, which is triggered by the "threshold" and "discharge" pins. The output pulse duration is defined by the equation:

$t = 1.1 \times R \times C$ where R is the resistance and C is the capacitance

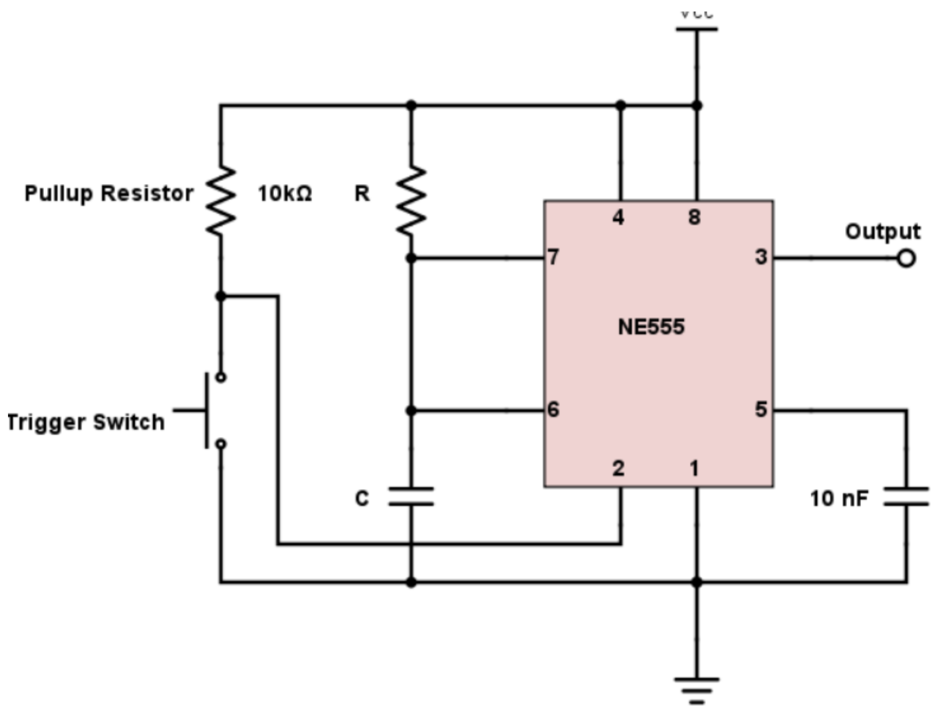


Figure 3: 555 Timer IC, source: allaboutcircuits

Astable Mode

The 555 will function as an oscillator and generate a continuous square wave without needing an external signal. It switches between high and low states indefinitely, making it a good choice for applications like clock pulses, LED flashers and tone generators. The timing components R1, R2, and C control the frequency and duty cycle of the output waveform, which are formulated below:

Frequency = 1.44(R1+2R2)

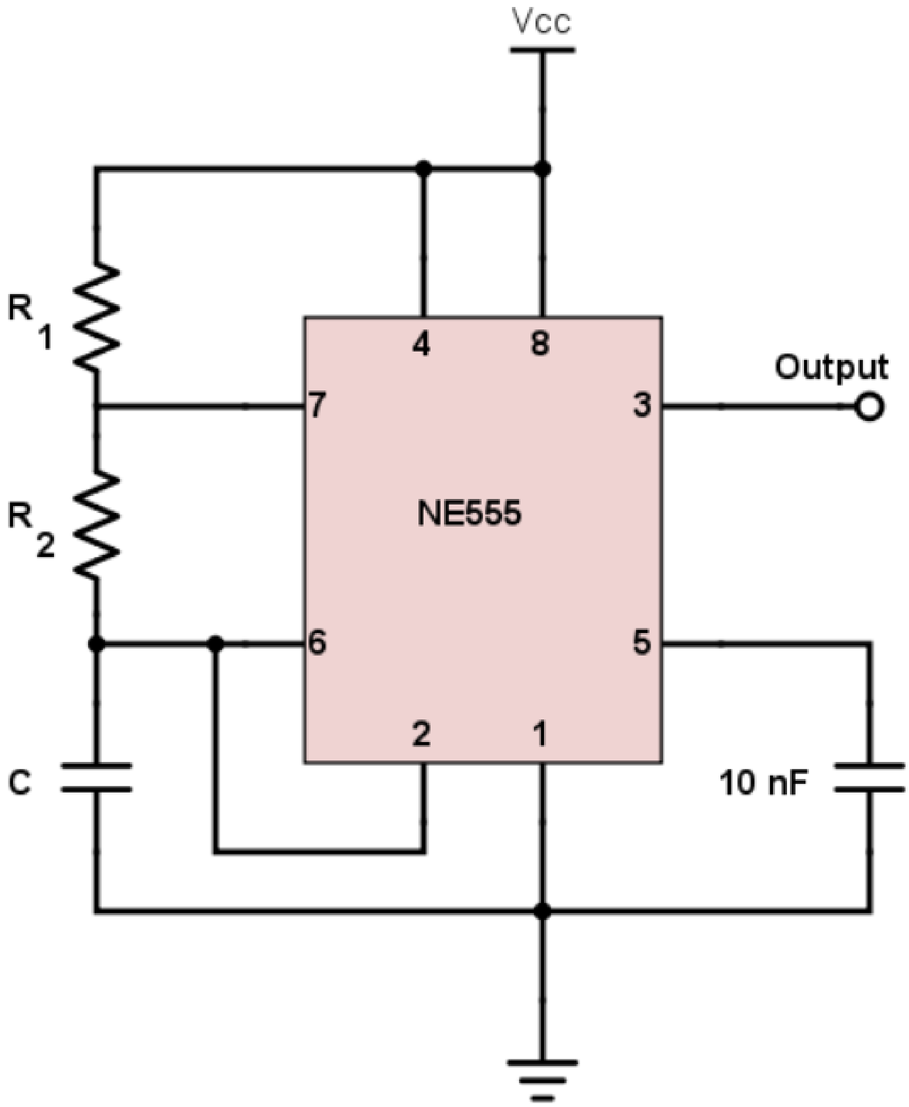


Figure 4: 555 Timer IC, source: allaboutcircuits

In this mode, the capacitor alternatively charges and discharges between the “threshold” and “trigger” levels (2/3 and 1/3 of the supply voltage), which flips the state of the internal flip-flop one after another, creating a repetitive signal at the output.

Bistable Mode

The Bistable mode is essentially a flip-flop operation, where the 555 timer is triggered to latch in either high or low states until another external trigger signal. This is often used in toggle switches and memory storage circuits, as it maintains its output until reset or triggered by another signal. The external reset pin can be used to manually control the output state, enabling or disabling the output as desired.

2.6.2 74LS247: BCD to 7-segments

BCD is binary encoding decimal to present decimal in binary base. It is different to usual when translate the value directly to binary, with BCD we translate only the digits (0 to 9) to corresponding

(0000 to 1010). To see more clearly, we can view the table below, which show difference between BCD vs binary.

Decimal	BCD	Binary
11	0001 0001	1011
20	0010 0000	1010

Table 4: Decimal, BCD, and Binary Representation

Decimal	Binay (BCD) 8 4 2 1
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1

Figure 5: Decimal and BCD

Any other is 4 bits binary is invalid. In this project, we only use 2 digits numbers, hence the BCD will be constraint to be 8 bits, 2 4 bits each for 1 digit.

BCD counter is an IC that take pulses, and for each pulse it increases (or decreases) the value of the output by 1. The specific value here is 0 (0000) and 9 (1010).

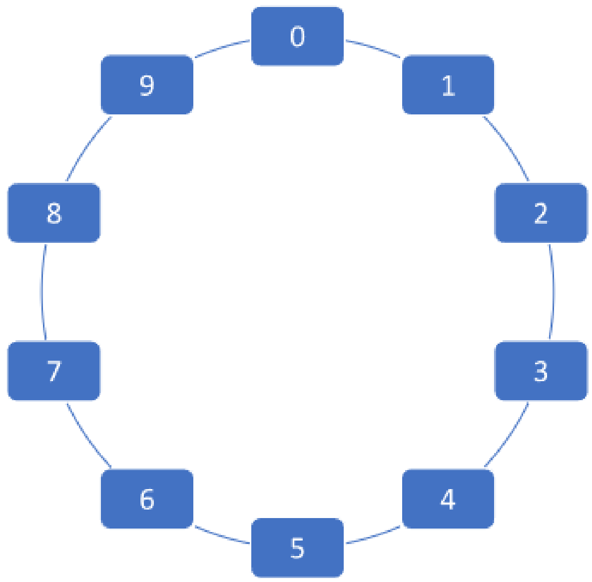


Figure 6: BCD values in cỉcle

2.6.3 74LS273: Flip flop

Flip flop is a circuit that can memorize previous bit(s). There are many type of flip flop such as SR, JK, etc. But in this project, we use D flip flop (74LS273).

Simple logic gate:

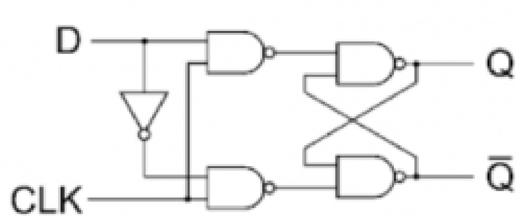


Figure 7: Circuit diagram

Truth table:

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

Figure 8: Truth table for D flip flop

2.6.4 4008: Full Adder:

An adder is a circuit that adds two binary numbers. An adder is either a half adder or a full adder. The difference is that the full adder also has a Carry-In bit, while the half adder does not.

The 4008 ICs (e.g., U60, U61) perform 4-bit binary addition. They take two 4-bit binary numbers (A0-A3 and B0-B3) as inputs and generate a sum (S0-S3) along with a carry-out (Cout).

These adders are configured to process the input values provided and calculate the resulting sum.

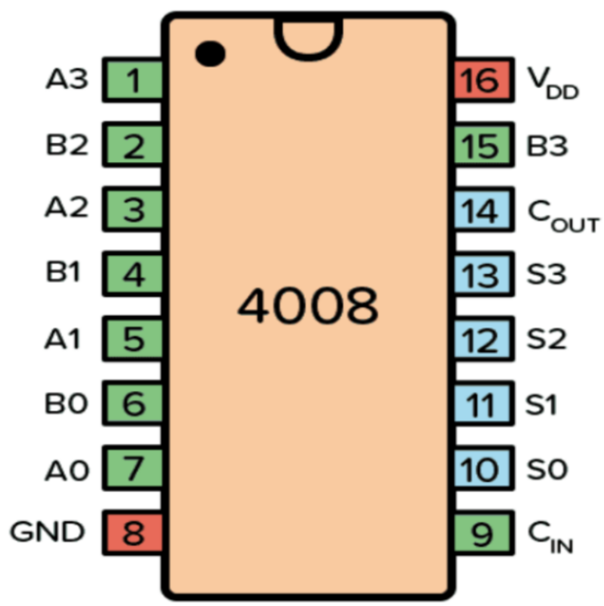


Figure 9: 4008 pins

The full adder is made off logic gates as the image below:

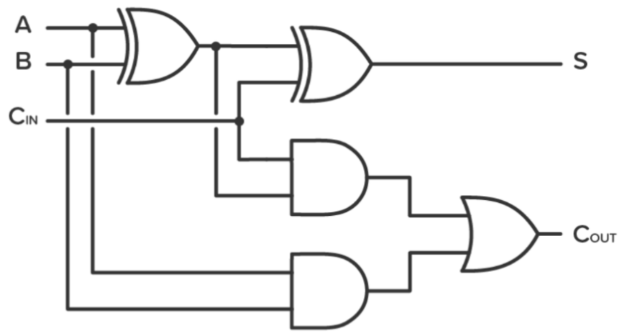


Figure 10: Full adder logic gates

2.6.5 74192: BCD decade counter

Take a input, and count down every clock cycle. It working can be seen below:

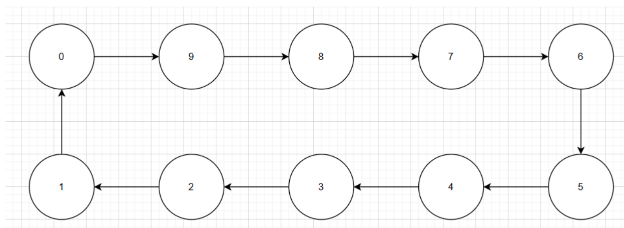


Figure 11: Full adder logic gates

2.6.6 4017: Ring counter

Ring counter is an example of shift register, and is consist of d flip flop connect to each other. In its begin state, the output will be 10. . . 0, and for each clock cycle (to be more specific clock edge) the 1 will shifted to right 1 place and loop back if it in the end.

Logic gate (source geeksforgeeks):

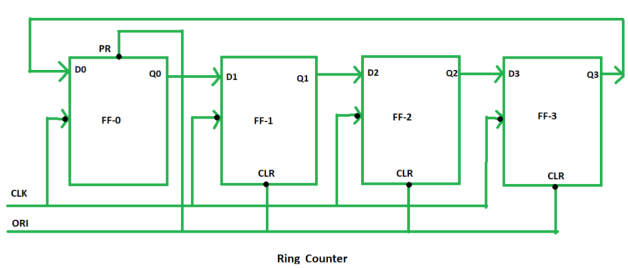


Figure 12: Circuit diagram

Truth table

ORI	Clk	Q_0	Q_1	Q_2	Q_3
low	X	1	0	0	0
high	low	0	1	0	0
high	low	0	0	1	0
high	low	0	0	0	1
high	low	1	0	0	0

Figure 13: Logic table for ring counter

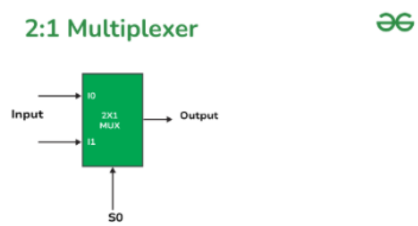
Application:

- Ring counter can be used to frequency division application, store memory (in this project is store the state/light of traffic).

2.6.7 4019: Multiplexer

Multiplexer is an IC which help us to choose between different inputs and output only 1 of them.

Mux takes multiple input lines, and also a selector lines to choose 1 of many input lines to a single output line.



Truth Table

S_0	I_0	I_1	Y
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Figure 14: Mutiplexer (Source:geeksforgeeks)

Application:

- Mutiplexer has a lot of application such as data selction/routing, and also in some circuit (such as ADC-Analog-to-Digital).

3 Design

The project will be simplified to different blocks, and can be shown as figure below

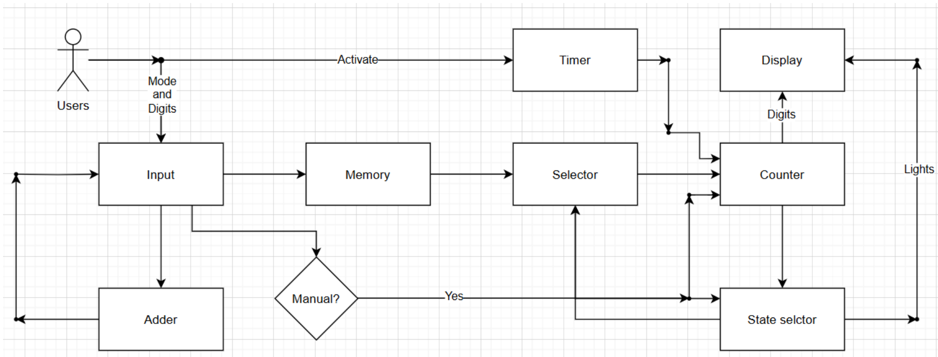


Figure 15: Overall interaction between blocks

In this section, we will discuss each block purpose and functionality specified in an active-mode operation.

3.1 Mode 1 (Auto):

3.1.1 Input block (mode 1)

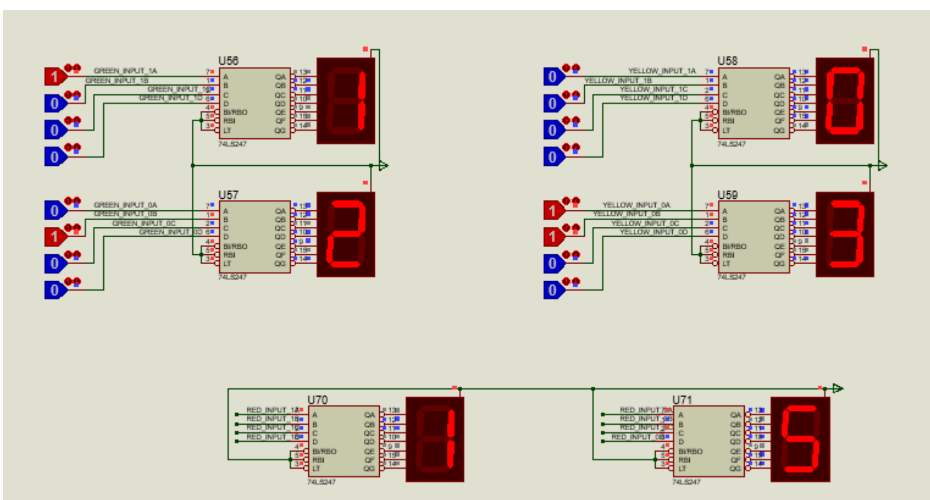


Figure 16: Input block

General purpose:

The input blocks will take input from user (to be more specific green and yellow time) and display them out by 7-seg leds (also display red time).

As the figure above show, green time is 12, yellow is 3, and red is 15. The user input through logic gates in BCDs.

Functionality:

Take users' inputs and display it through BCD converter and 7-seg leds. In addition, green time and yellow time will be passed to adder block. The adder block will return time for red and display it for user to check.

3.1.2 Adder block

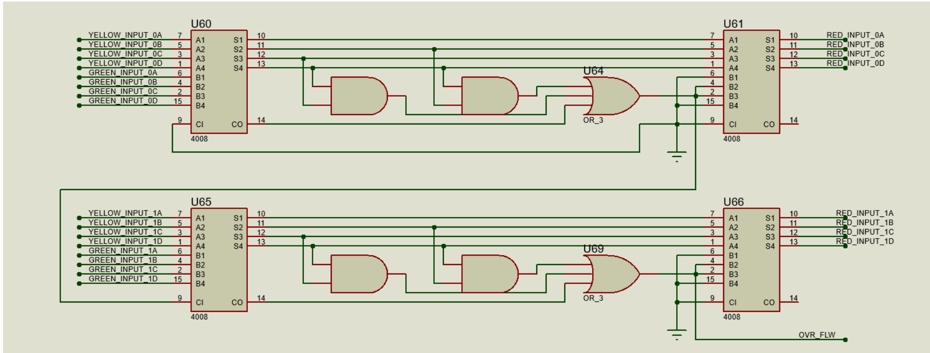


Figure 17: Adder block

General purpose:
Take time of green and yellow, return time of red as sum.
Functionality:
Return red to input block to display, overflow bit is transfer to memory block.

3.1.3 Memory block

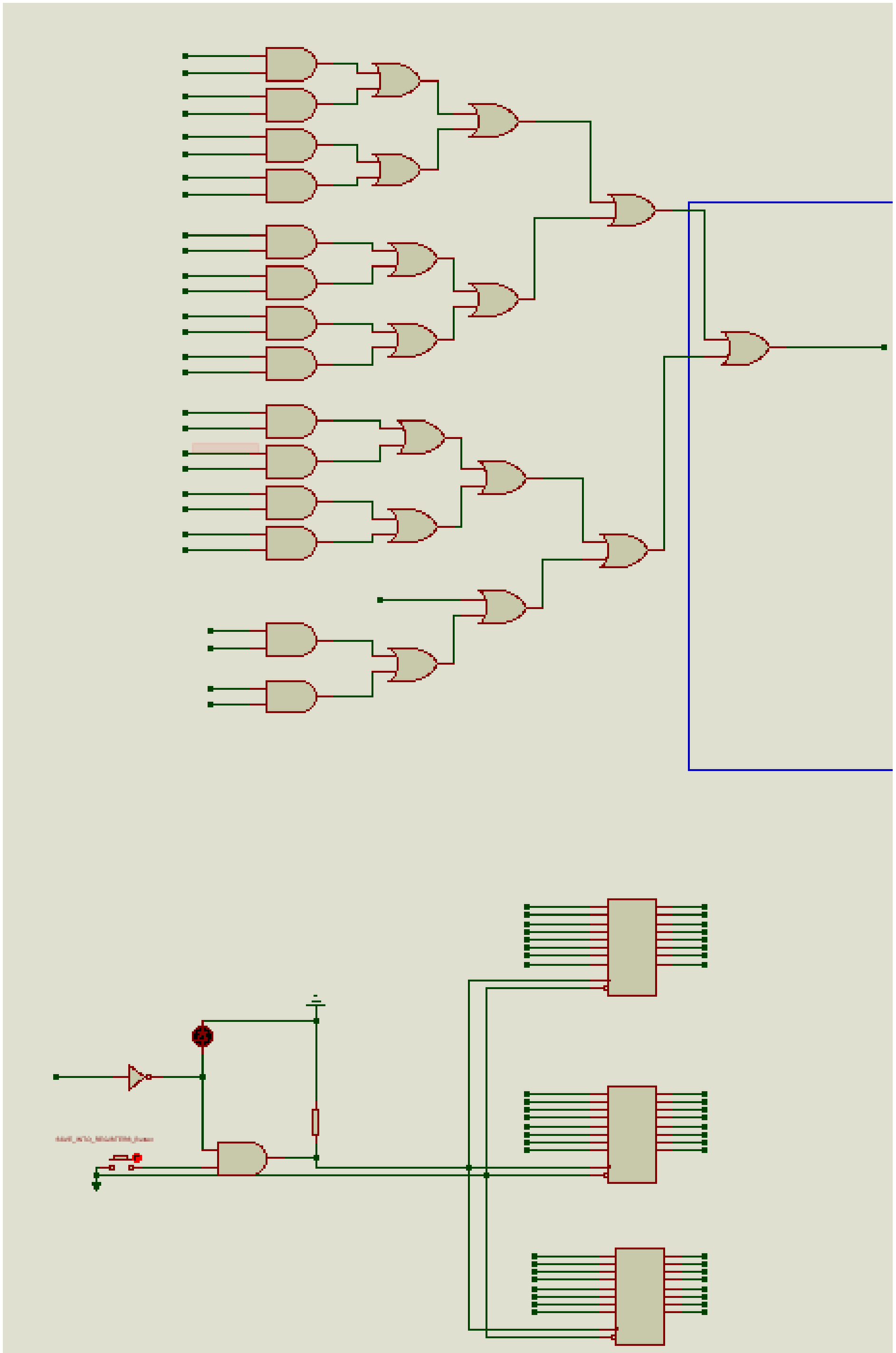


Figure 18: Memory block

General purpose:
Its general purpose is to store user inputs (time for red, yellow, and green).

Take user's input for time of red, yellow, and green lights and store it (only when user hit a button), and its output will be the selector input.

Functionality:

Take users input and put into memory. Users have to hit the button to store it into memory. However, the memory will store new data only when the light is lit.

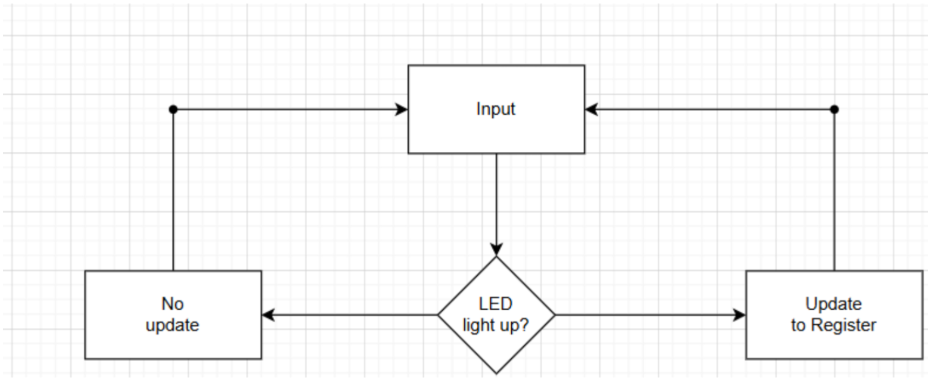


Figure 19: Simple flow chart

Why do we need protection?

The value of green and yellow is not in BCD format.

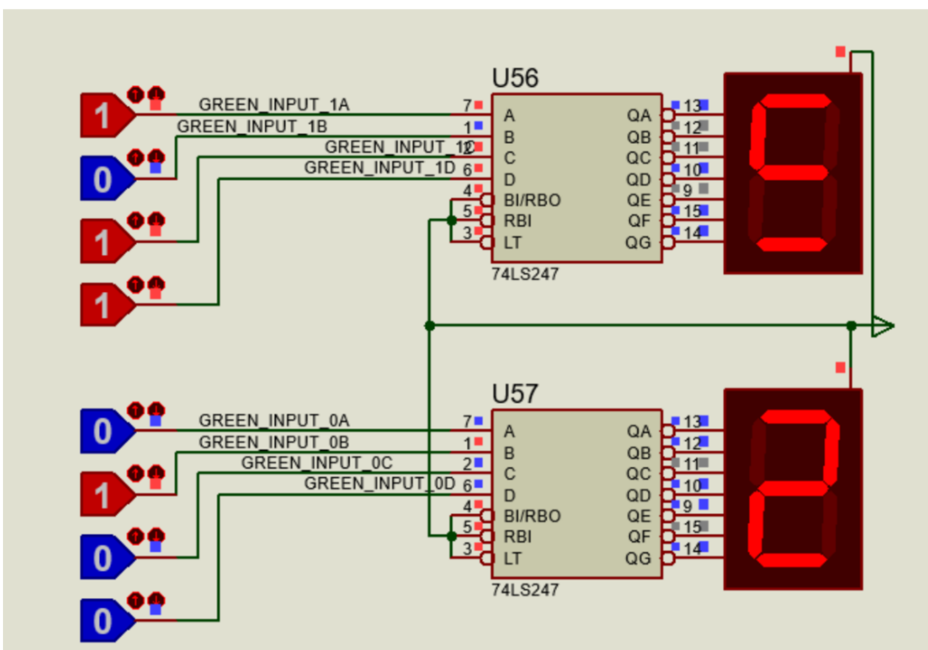


Figure 20: Input block (mode 1) input wrong format

So, how does we know if user input at wrong format. Recall that, BCD single digit only work from 0000 to 1001, which mean 1010 is invalid. An interesting hint has show up, any input that has the value of 1x1x (where we don't care what value x is) is invalid.

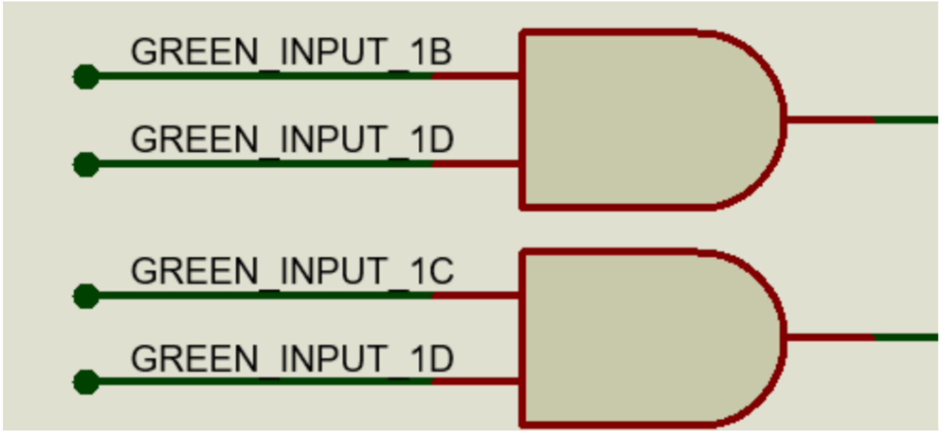


Figure 21: Logic gates check condition

Moreover, it can also be say to 11xx. That why, we use AND gate to detect invalid (1 for invalid).

2. The sum of green and yellow (which is red) is greater than 99 (our max possible value).

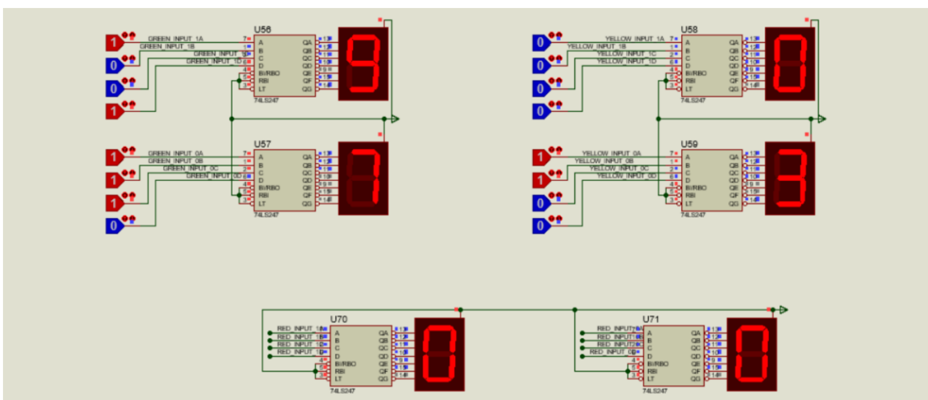


Figure 22: Red timer value overflow

We can know if red is overflow, by using overflow output from the adder.

3. Avoid race condition when transition. To be more specific, when the cycle is in red-yellow, and we hit change memories, the next cycle we be green-red.

Let's look at an example, old time(green=5, yellow = 3, red = 8), new time(green=5,yellow=5,red=10). We hit update memory when the cycle in red-green.

RED-8	RED-3	GREEN-5 (wrong timing)
GREEN-5	YELLOW-5	YELLOW-2 (wrong timing)

To sum of all of that we have circuit as follow

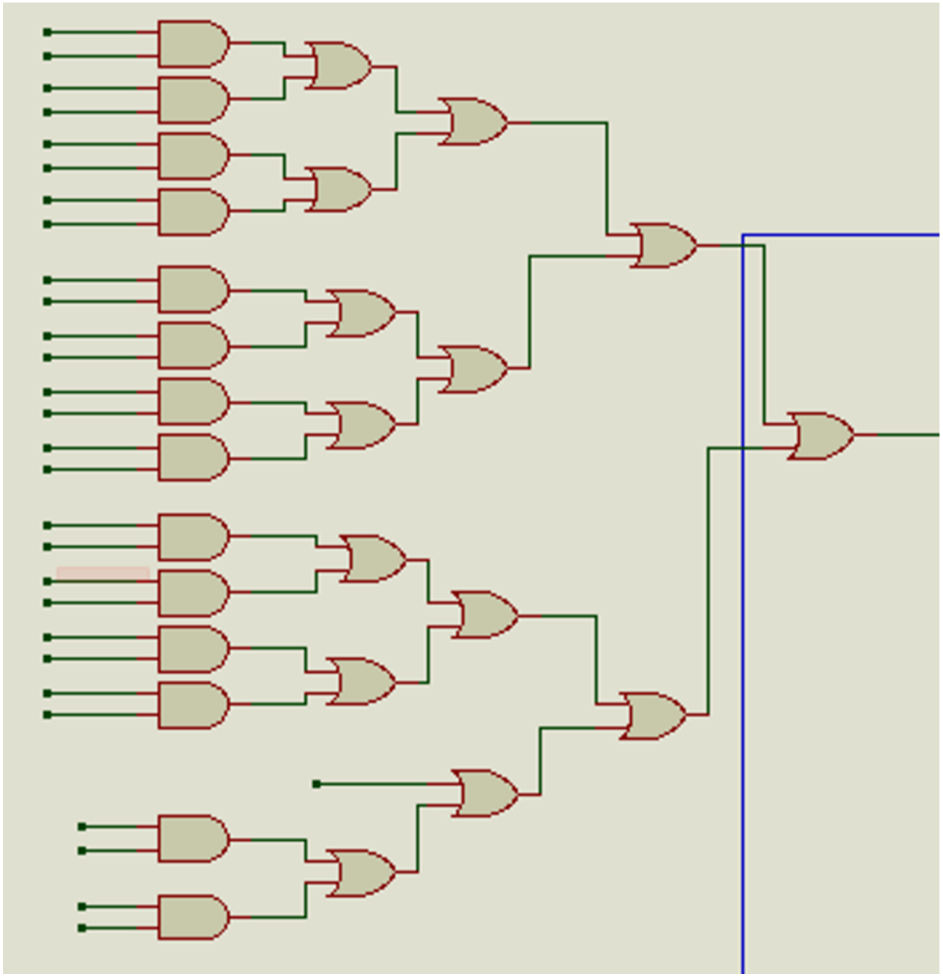


Figure 23: Logic circuit check conditions

Where each and gate output a 1 if we need to block update the memory, all the or gates will output 1 if at least 1 binary bit is produced.

After that, the 1 (1 when there's at least a condition to block updating) turn to 0 through inverse gate. The 0 will block the output from the button (button & 0 = 0 for all button states).

What happened when the light is on, and we hit update values. When button is pressed, the clock input will be high and then low, create a edge activate flip flop and store the values.

3.1.4 Selector block

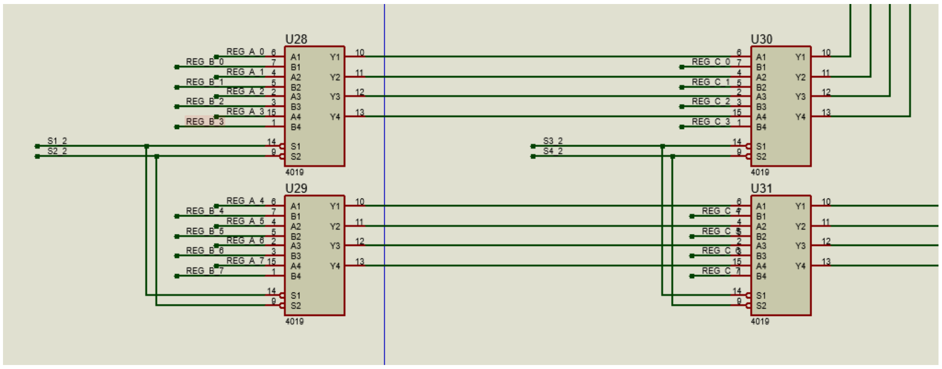


Figure 24: Selector block for 1 intersection

General purpose:
Will take input from both block selector and block memory, output to block counter.

Functionality:
The working is basing on multiplexer, in this project we use 4 mutiplexers, which take 2 4-bits input and base on chosen bits will choose the according outputs.

Table 5: Truth Table

S1	S2	Output
0	0	A & B (binary operator)
0	1	A
1	0	B
1	1	0

As you can see, the input of S1 and S2 when they are the same value does not choose a single A or B. Hence. In the project, S_1 and S_2 (both control by state selector block) will be exclusive different, which mean only S_1=1 and S_2 = 0 or S_1 =0 and S_2 = 1 is valid.

As you can see on the above figure, there will be 4 multiplexer work together. Furthermore, there are 2 sets of 2 multiplexers use the same selector inputs. The working of above circuit can be shown as the below table (as has be told above; pair S1_1 and S2_1, S3_1 and S4_1 will be exclusive different):

Table 6: Truth Table

S1_1(Inverse of S2_1)	S3_1(Inverse of S4_1)	Output
0	0	Reg_A
0	1	Reg_C
1	0	Reg_B
1	1	Reg_C

3.1.5 Counter block

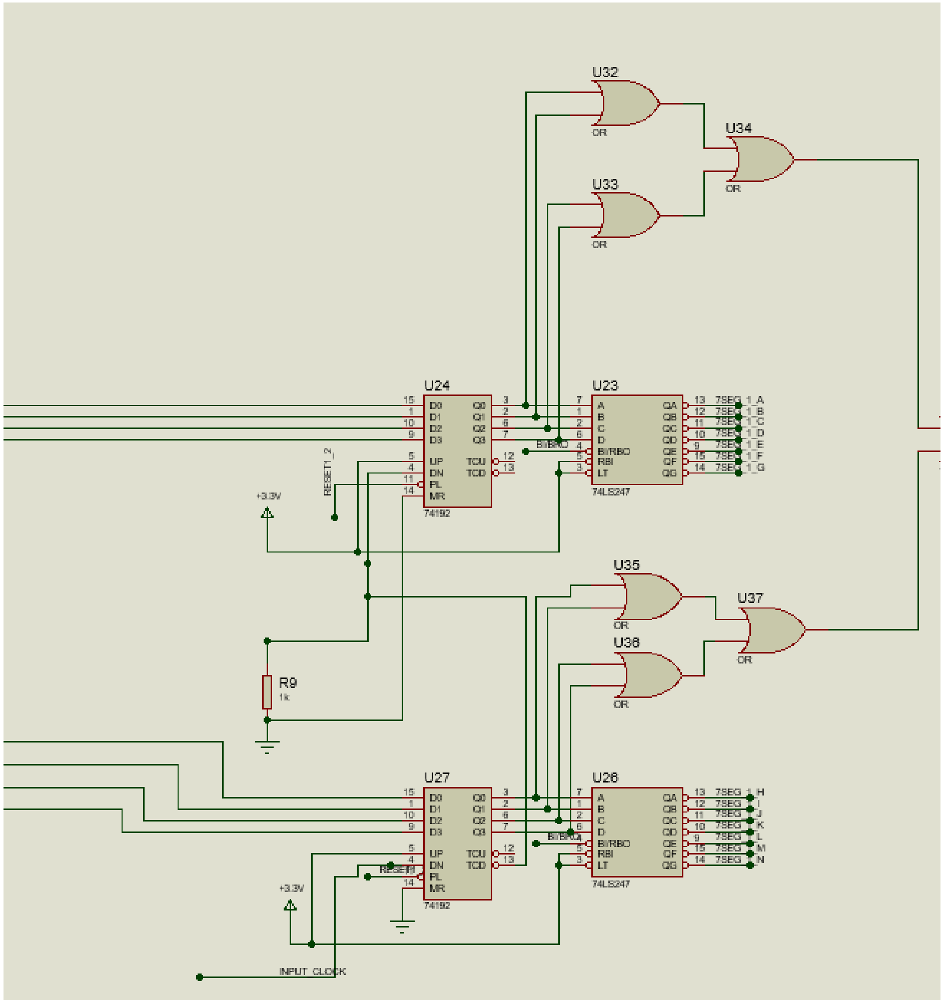


Figure 25: Counter block for 1 intersection

General purpose:
Take value from selector and count down until hit 00, and will be reset with the next value.

Functionality:
Get value from selector block, clock from clock block, and output the counting value to intersection. Moreover, there will be also 6 OR gates, the outputs are only 0s when counting value is 00. At which time, the 0 will reset the count down from the next value from selector block (via PL pins).

3.1.6 State Selector block

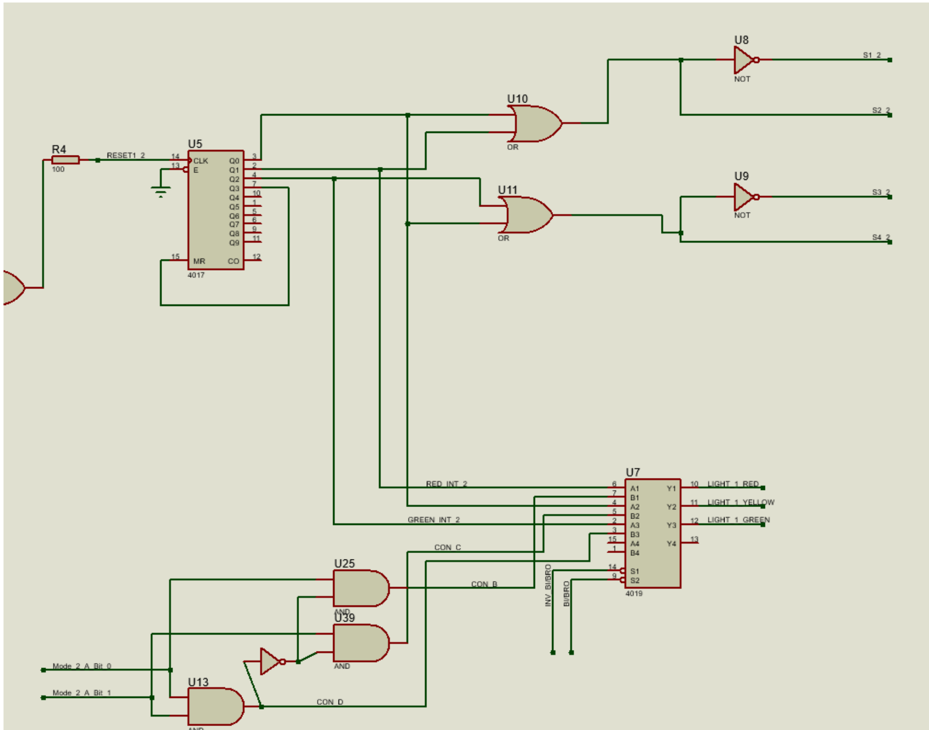


Figure 26: State selector block for 1 intersection

General purpose:

Take input from counter block and mode selector button, then update accordingly. the outputs will be input of selector block, and lights in display block.

Functionality:

If the mode is in manual, output for display modes will be switches to manual input light by multiplexer.

If the mode is in auto, all output will be from ring counter IC. Ring counter IC will take 0 (Reset from counter) and update the output (with no ouput larger than 00001000 hence the connection between fourth output pin to reset pin).

3.1.7 Timer block

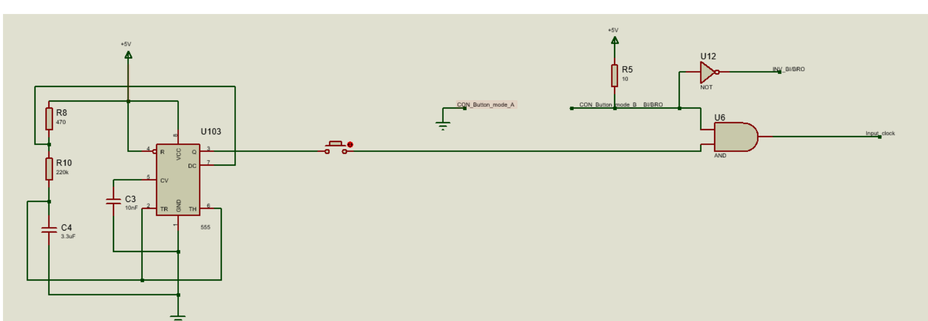


Figure 27: Timer block

General purpose:

The timer block is designed to generate and control periodic signals that are used to synchronize operations within the circuit (1 Hz). Its general purpose is to act as the timing engine for driving transitions between each traffic light state. The mode switch allows user to switch between counting and non- counting light mode

Functionality: Signal Generation:

- The 555 Timer IC is configured in astable mode, meaning it continuously produces a square wave signal.
- The frequency and duty cycle of this signal are determined by the external resistors (RB, R10) and capacitor (C4), which set the RC time constants.

Mode Selection:

- The mode switches (CON_Button_mode_A and CON_Button_mode_B) allow users to select different operational modes for the timer block.
- The NOT gate (U12) inverts one of the mode signals, ensuring that the AND gate (U8) receives complementary inputs from the switches. Conditional Timing Control:
- The AND gate (U8) combines the timer's output with the mode signals, enabling or disabling the timer's signal based on the selected mode.
- This ensures that the timer's output is only active under certain conditions, adding flexibility to the circuit's behavior. Output and Signal Flow:
- The processed signal from the AND gate is sent to the next stage of the circuit, which likely controls the LED-based traffic lights.
- Depending on the mode and timer configuration, the traffic lights will transition states (e.g., green to yellow to red) at varying intervals. Execution Flow: The timer generates a continuous pulse signal (oscillates HIGH and LOW based on the RC time constants).

The mode switches (Button_mode_A and Button_mode_B) alter the signal flow depending on their state. The logic gates (AND and NOT) modify the timer's signal based on the selected mode, providing conditional control. The resulting signal is used to drive the traffic light LEDs, changing states based on the timer and mode configuration.

3.1.8 Display block

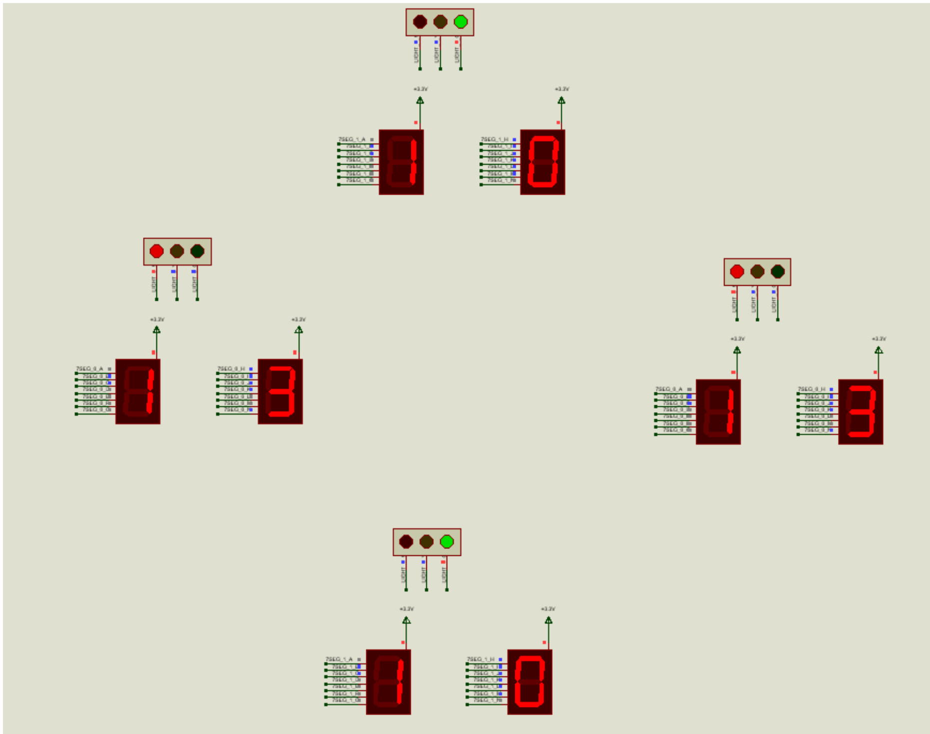


Figure 28: Display block

General Purpose

The display block in the traffic light system serves a dual purpose:

1. Traffic Light Status Indicator: When the mode switch from the timer block is closed, the display block only shows which light (Red, Yellow, or Green) is currently active in the traffic signal system. No numerical counting is displayed in this mode.
2. Countdown Timer Display: When the mode switch is open, the display block shows a countdown timer corresponding to the active traffic light. This countdown informs users how much time remains for the current light before transitioning to the next.

Functionality

1. Mode-Dependent Behavior:
   - ☐ Mode 1 (Mode Switch Closed):
     - Only the active light (Red, Yellow, or Green) is illuminated on the 7-segment display.
     - The system uses a direct connection to the light control logic to turn on/off the appropriate 7-segment display for the current active light.
   - ☐ Mode 2 (Mode Switch Open):
     - The block displays a countdown timer for the active light on the respective 7- segment display.
     - The timer value is driven by the timer block, and the 7-segment display is dynamically updated to reflect the countdown in real-time.
2. Integration with Timer Block:

  - The timer block provides the signal to control the countdown value during Mode 2.
  - The mode switch determines whether the timer signal or a static light-on signal is passed to the display block.

3. Traffic Light Representation:
  - Each traffic light (Red, Yellow, Green) is associated with its respective 7-segment display.
  - LEDs are used to reinforce the status of the lights visually alongside the numerical countdown.

4. User Guidance:
  - During Mode 1, users only see which light is active, simplifying the information for easy understanding.
  - During Mode 2, users receive additional information about the time left for the current light, enhancing the system's usability in scenarios where countdowns are beneficial.

3.2 Mode 2 (manual):

3.2.1 Input block (mode 2)

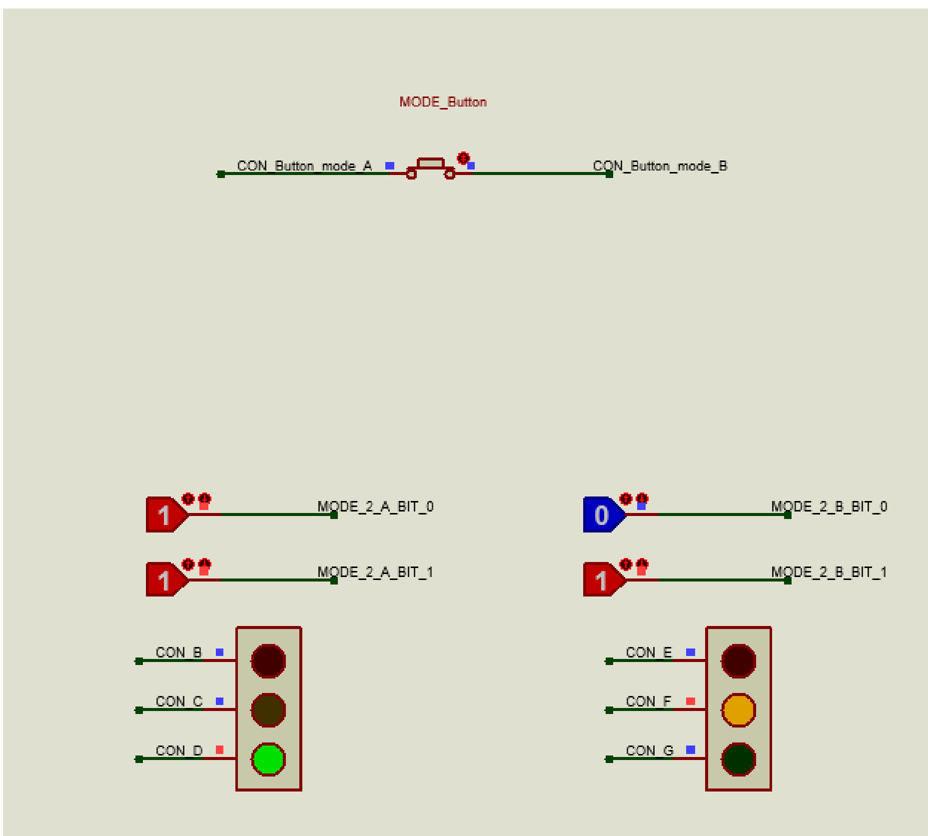


Figure 29: Input for mode 2 block

For mode 2, mode button has to be pushed down. Moreover, there are 4 logic gates for 2 intersection (2 for each) and each has 1 traffic light.

That mean, when in mode 2, lights have to be from the output, not the counter block (if we in mode 1). We choose using the mutiplexer.

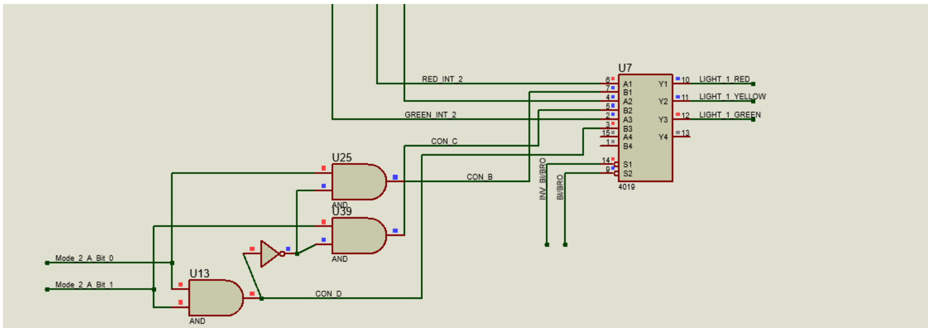


Figure 30: Mutiplexer choose lights

Moreover, we need to disable clock to save current mode 1 state - counter block will not count down because not have clock (in addition BI/BRO will be off which mean no digits are shown on display block). Timer clock will not output the clock because is connected direct to ground through button, and can be shown below

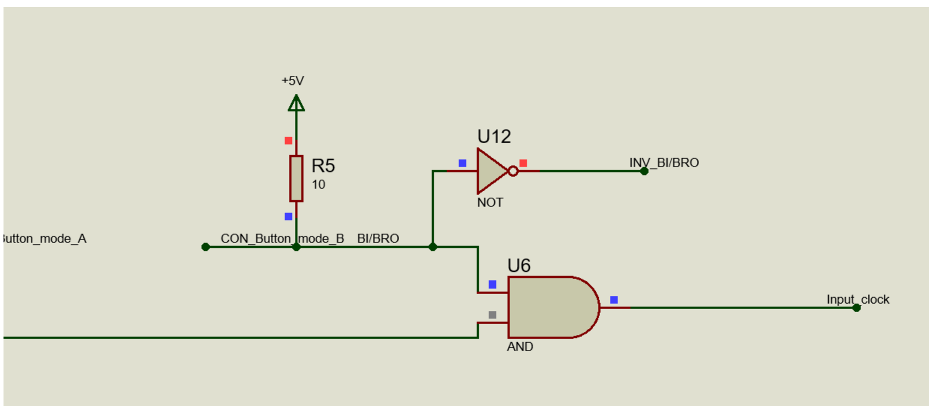


Figure 31: Timer block in mode 2

Intersection can be shown as below

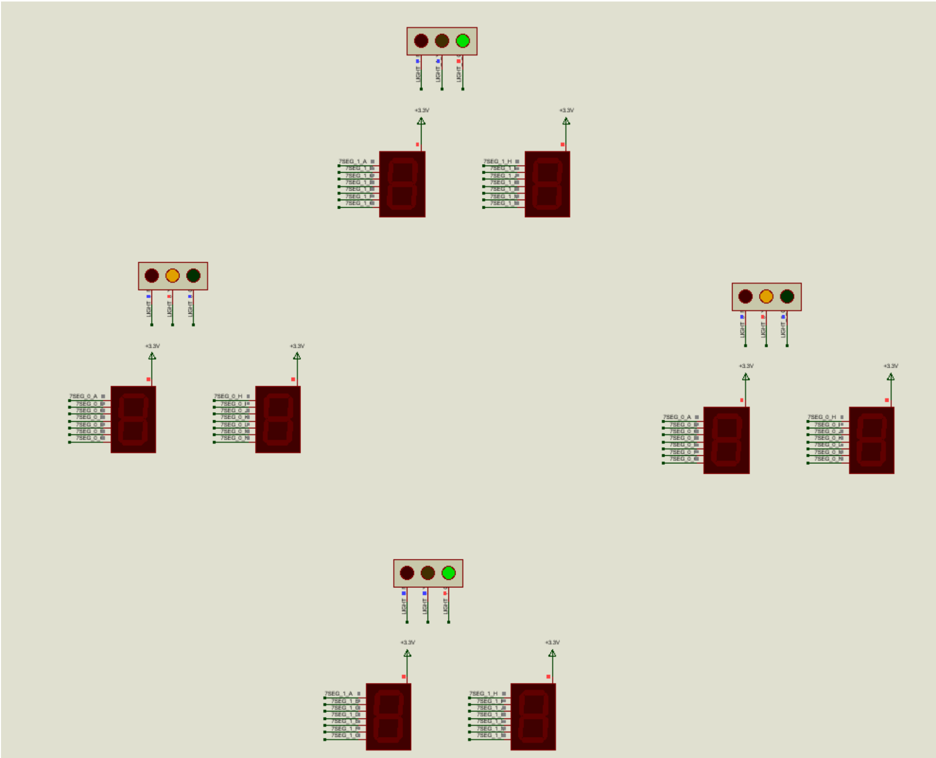


Figure 32: Intersection in mode 2 - Manual

3.3 Conclusion for block

The working of project can be summarize by the below UML.

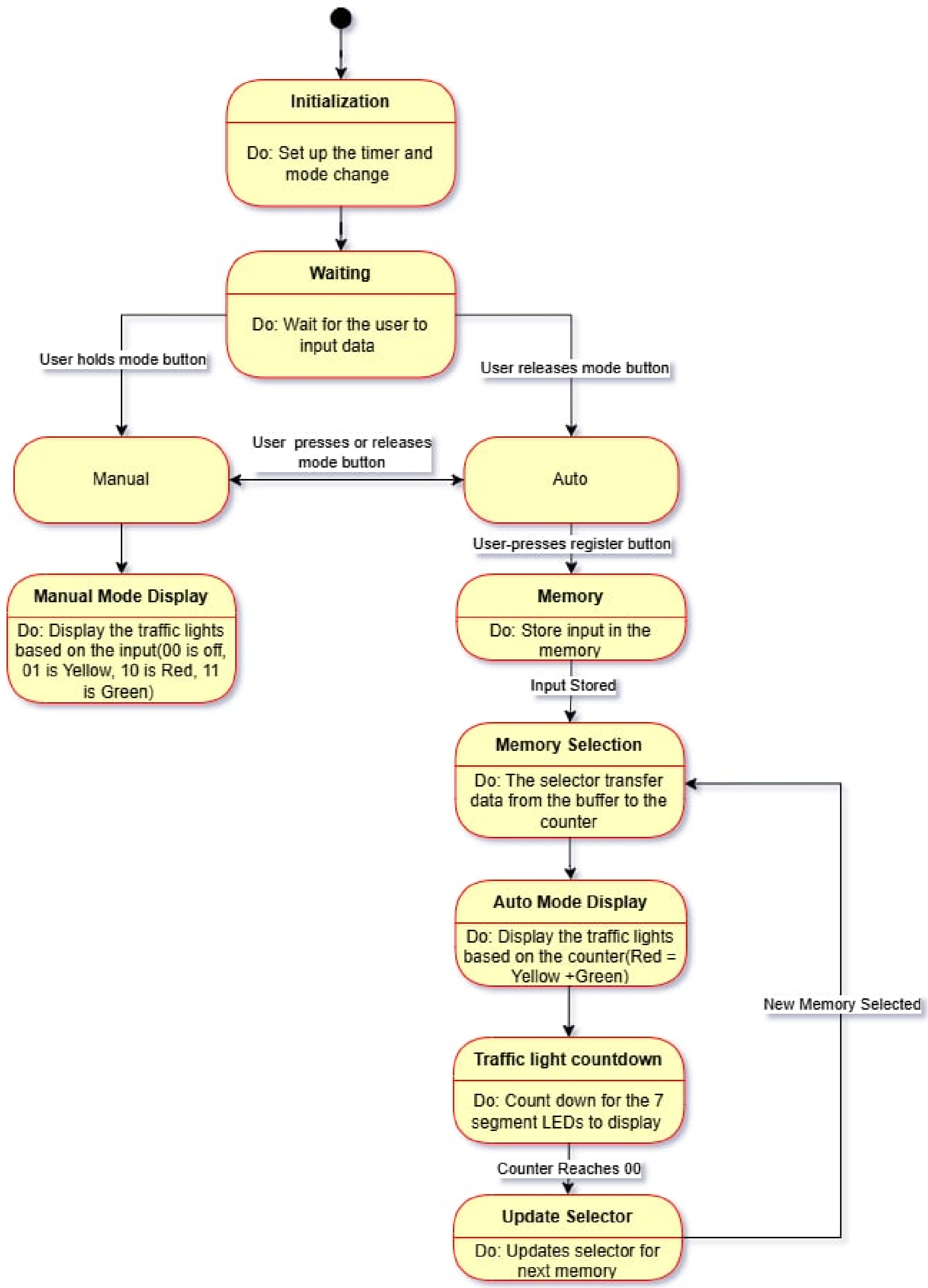


Figure 33: State diagram

To be noted, when first simulate, the timer button need to be open, then need to be closed.

4 Conclusion

4.1 Project

The project has been implemented and tested thoroughly by our team before making this report. All functions were meticulously verified and found to operate reliably within the defined project scope. This project also meets the requirements of the traffic system in reality, where it needs to be the guide for all who participate on the road.

One of the standout features of this system is its robustness and adaptability. It is capable of handling diverse road scenarios, such as dynamically adjusting to extended timings during rush hours or operating non-counting lights for prolonged vehicle queues. Additionally, the inclusion of a caution light for warnings enhances safety, particularly in complex or high-risk situations.

Beyond consistent performance, the system's customizability underscores its value. By enabling tailored configurations for various traffic patterns, it provides a scalable solution adaptable to different urban layouts and traffic conditions. This versatility makes it a strong candidate for integration into broader intelligent traffic management systems.

The implementation of the above traffic light system has demonstrated the effective application of logic design principles in creating a practical and functional model. The project incorporates modern digital components such as IC555 timers, logic gates, and multiplexers, which were meticulously assembled and programmed to achieve a reliable and accurate operation.

Moreover, the project aligns with contemporary urban traffic management trends, providing a foundational framework that could be scaled for broader applications. By adhering to systematic methodologies and addressing design challenges, we achieved a prototype that balances functionality, efficiency, and user interaction.

In summary, this project has successfully met its objectives by delivering a traffic light system that is functional, reliable, and adaptable, offering a viable model for modern urban traffic control. It not only fulfills its role as a traffic regulator but also sets a foundation for future advancements in intelligent transportation systems.

4.2 Future development

Looking ahead, the following enhancements can be considered to improve and expand the capabilities of the traffic light system:

- **Integration to real life**: The project has only on software only, we can implement it onto real life.
- **Integration of Smart Features**: Incorporating sensors to detect real-time traffic density and adapt the signal timings accordingly, enhancing traffic flow efficiency.
- **Wireless Communication**: Adding IoT modules for remote monitoring and control, allowing for centralized traffic management.
- **Pedestrian Safety Features**: Introducing audio signals or tactile indicators for visually impaired pedestrians to ensure inclusive safety.
- **Scalability for Complex Intersections**: Expanding the system to manage multi-lane and multi-directional intersections, ensuring its applicability in diverse urban settings.

- **Improved User Interfaces**: Designing intuitive interfaces for configuration and manual control, aimed at traffic operators and city planners.

By addressing these potential areas, the project could evolve into a sophisticated solution for intelligent traffic management, contributing to safer and more efficient urban transportation systems.

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