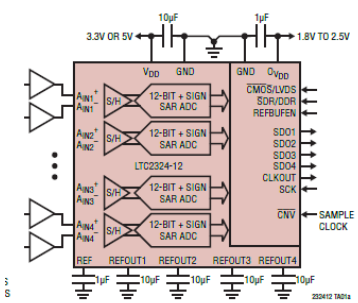
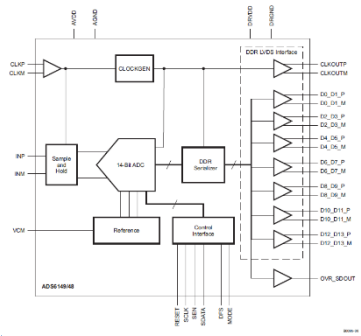
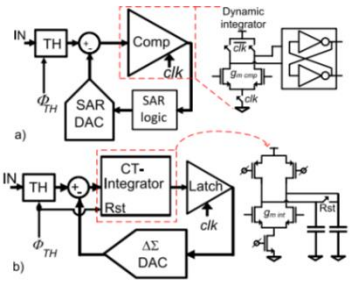
W2022 Siemens ADCs

Lab 3

Data Converters Specifications

POC	ADI(LTC2324-12)	TI(ADS6129)	From paper
Architecture	SAR	pipelined	SAR
Block diagram			
Price ($)	220	109.3	_____
Min power supply (V)	3.3	3.3	1.5
Peak-to-peak input range (V)	8	4.2	1.25
Power consumption at 1 MSps (mW)	40	687	26.5
Max DNL (LSB)	0.25	1	0.45
Max INL (LSB)	1	1	0.9
ENOB (bit)	11.66	11.2	9.8
SNR (dB)	78.5dB	73.4	57
SINAD (dB)	78dB	73.2	60.7
SFDR (dB)	93dB	92	66.0
Digital output format	serial	parallel	parallel
Internal reference	yes	yes	yes
Internal sampling clock	yes	yes	yes
Walden FoM	6.18 fJ/step	1.168 fJ/step	49.9
Schreier FoM	152dB	156	161.2