W2022 Siemens ADCs

SAR ADC Project

Contents

Part I:verifying the proper operation of the behavioral models :

- NAND Gate :

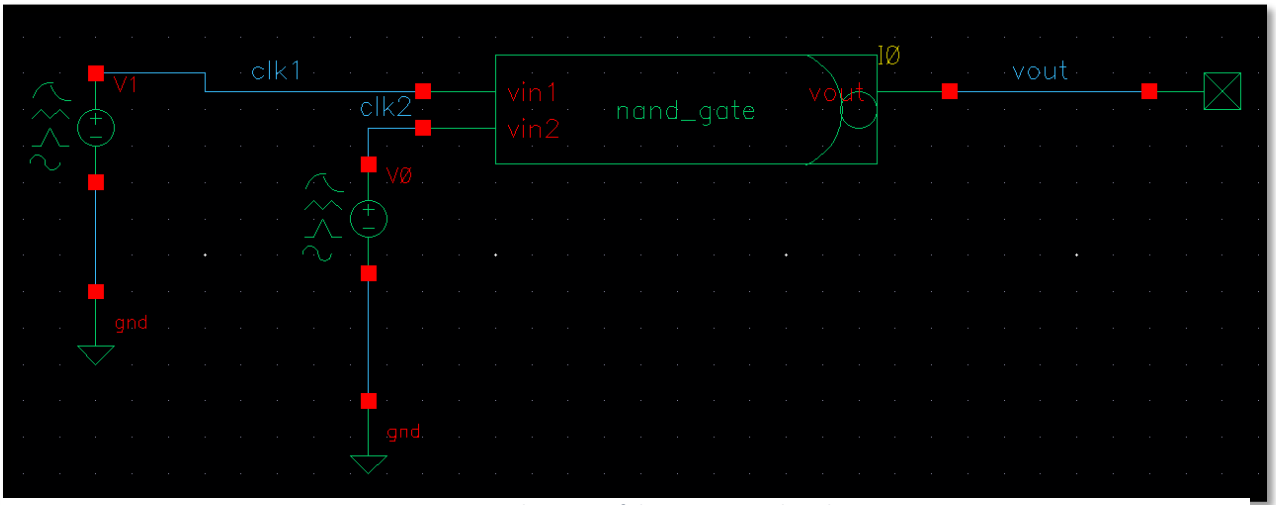

Figure 1-schematic of the NAND test bench

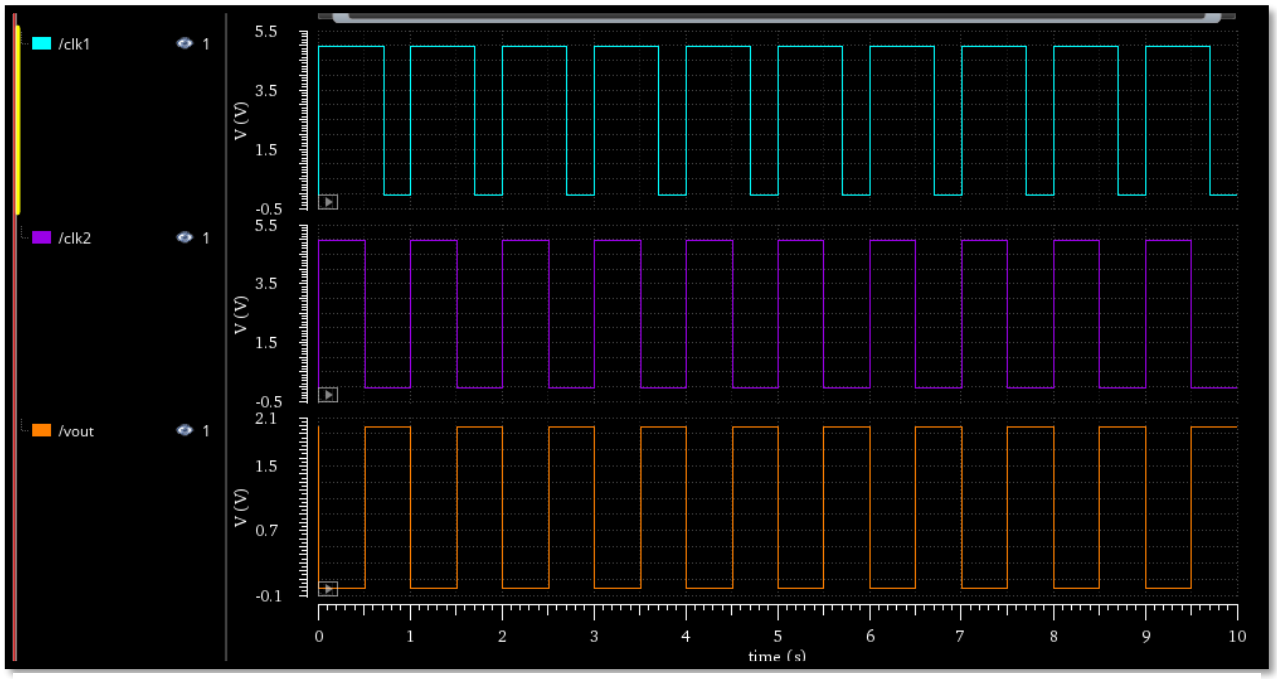

Figure 2-Transient analysis

Comment: We clearly see the proper operation of the NAND Gate as the output is only “Low” when the 2 inputs are “High” and is “Low” elsewhere.

- NOR Gate :

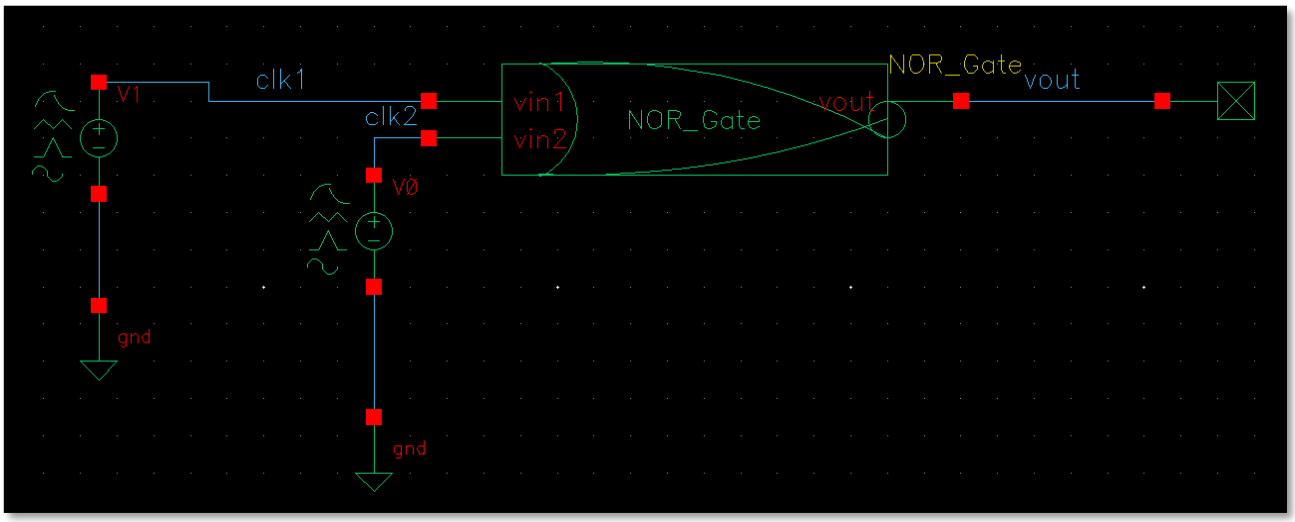

Figure 3-schematic of the NOR test bench

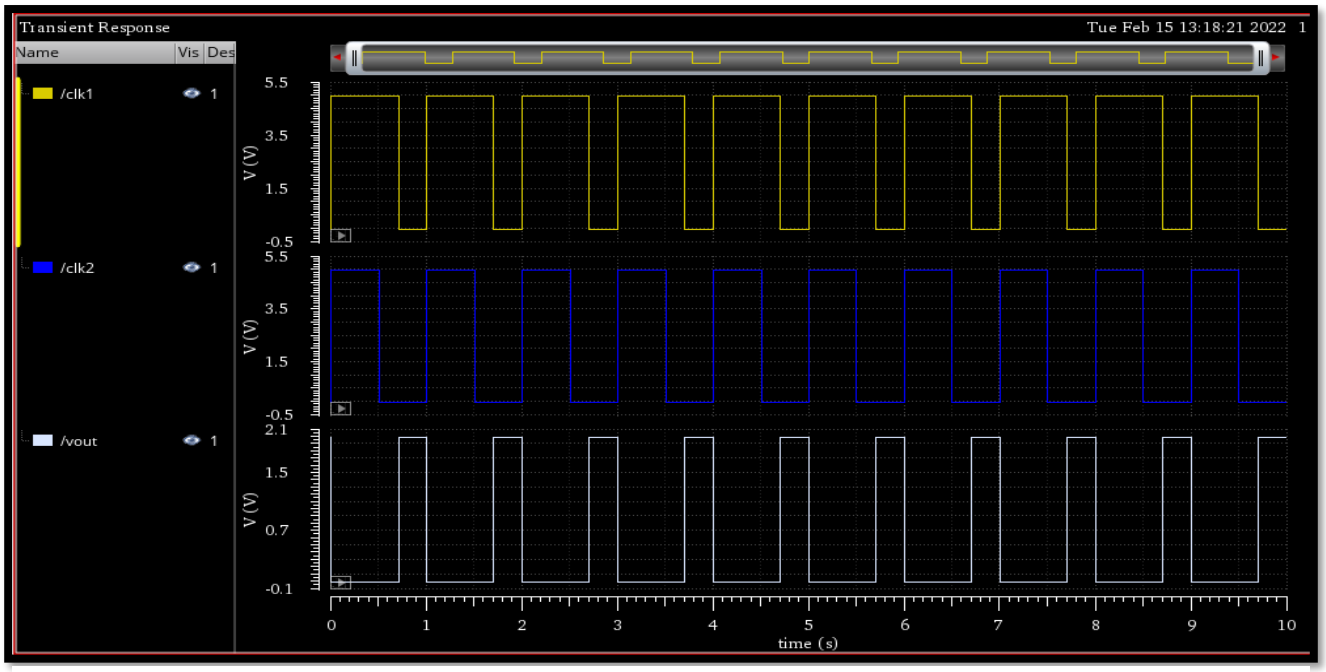

Figure 4-Transient analysis

Comment: We clearly see the proper operation of the NOR Gate as the output is only “HIGH” when the 2 inputs are “LOW” and is “Low” elsewhere.

- Inverter Gate:

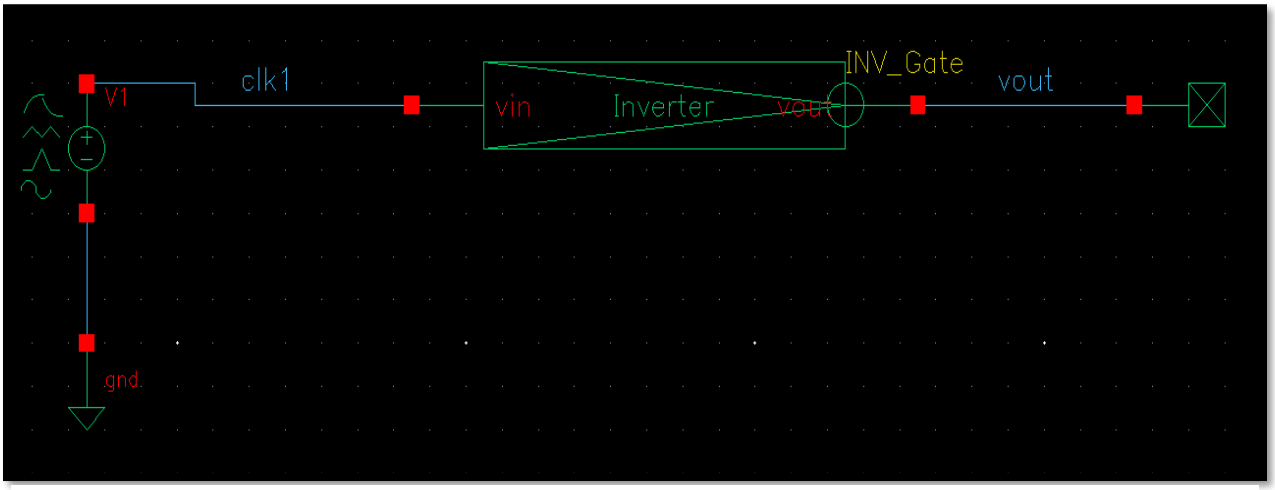

Figure 5-schematic of the INVERTER test bench

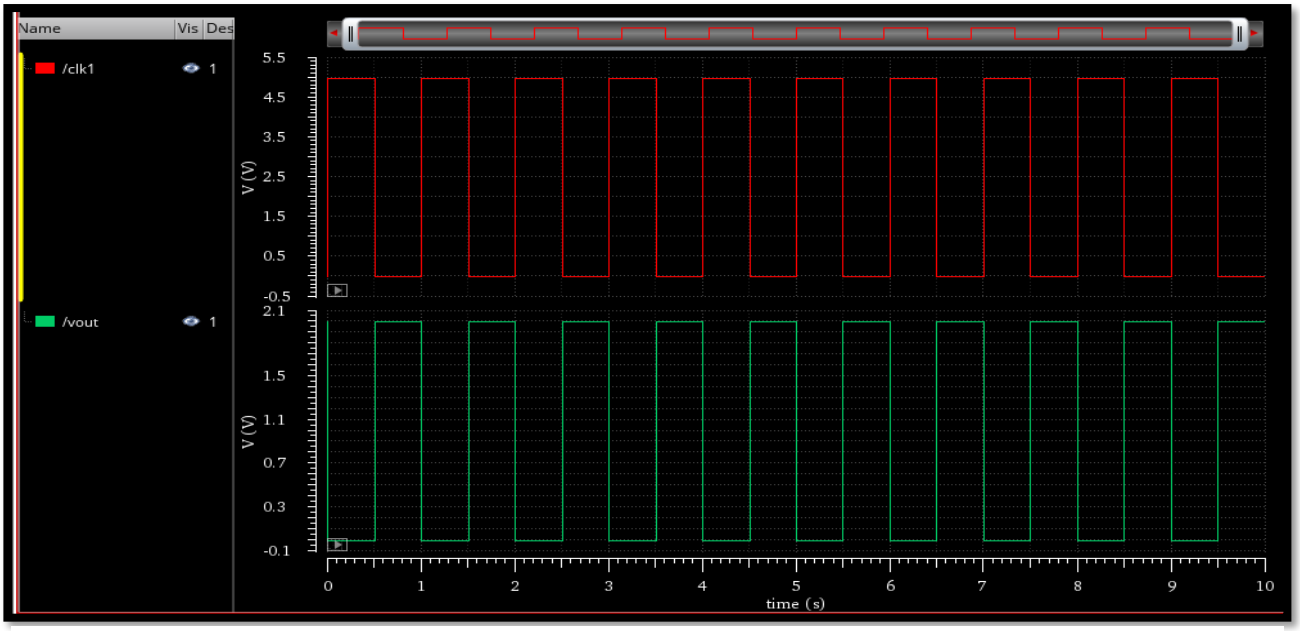

Figure 6-Transient analysis

Comment: We clearly see the proper operation of the Inverter Gate as the output is the complement of the input .

- Comparator:

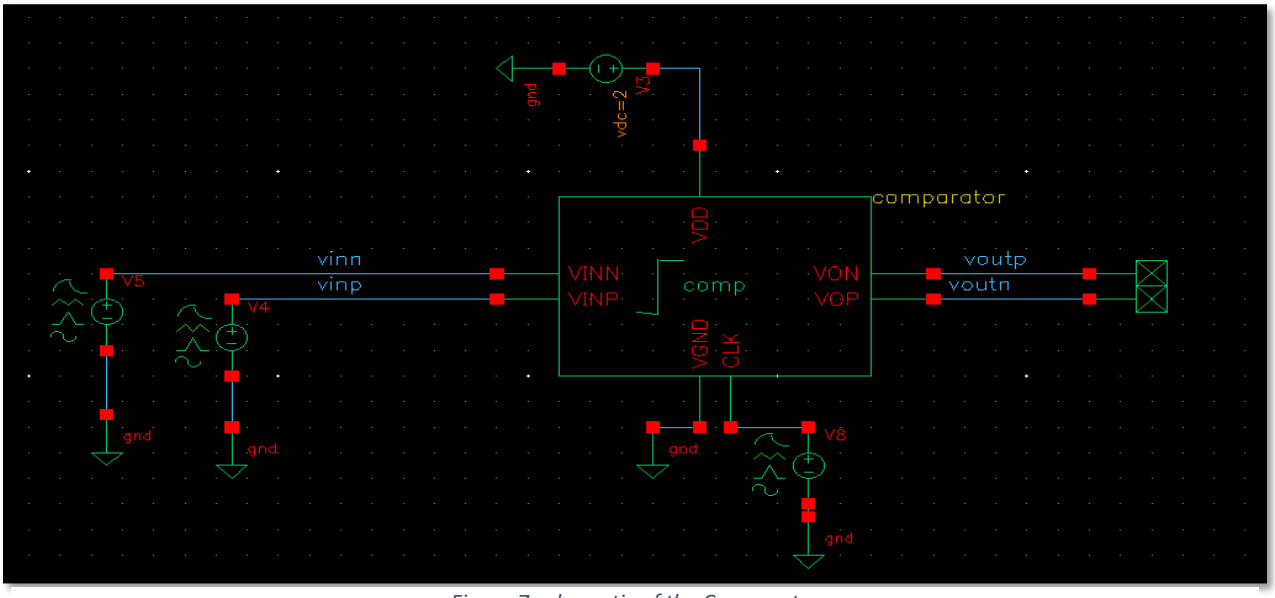

Figure 7-schematic of the Comparator

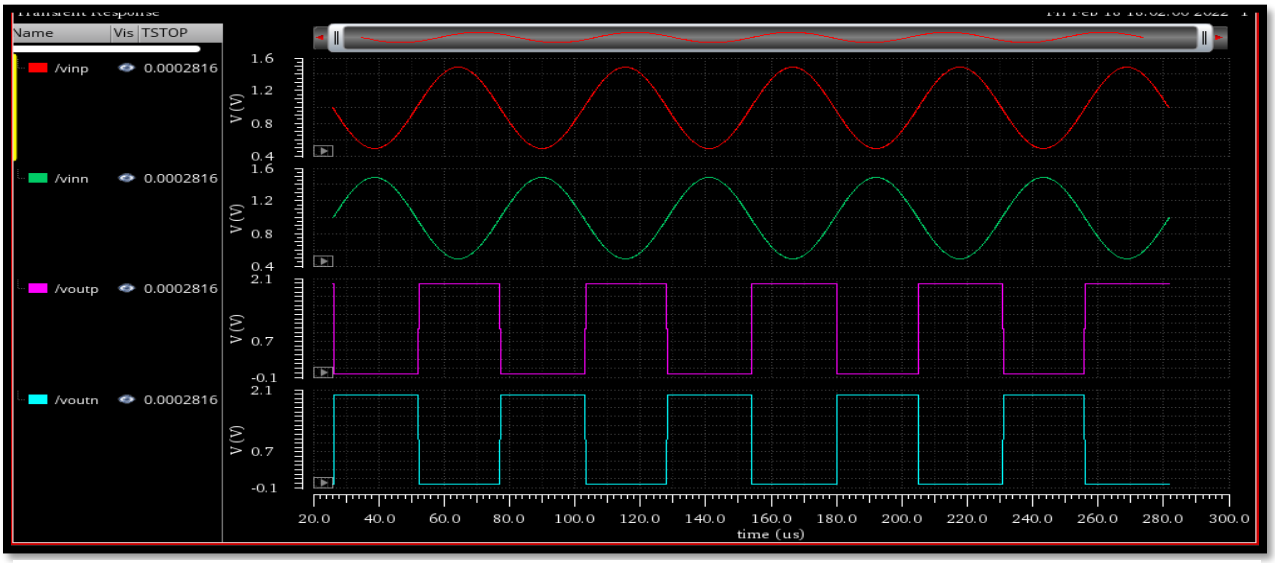

Figure 8-Transient analysis

Comment: We clearly see the proper operation of the Comparator as the $V_{onn}$is High if $V_{inn}$is larger than V_{inp} , and $V_{onp}$is High if $V_{inp}$is larger than V_{inn}.

- DFF with set & reset:

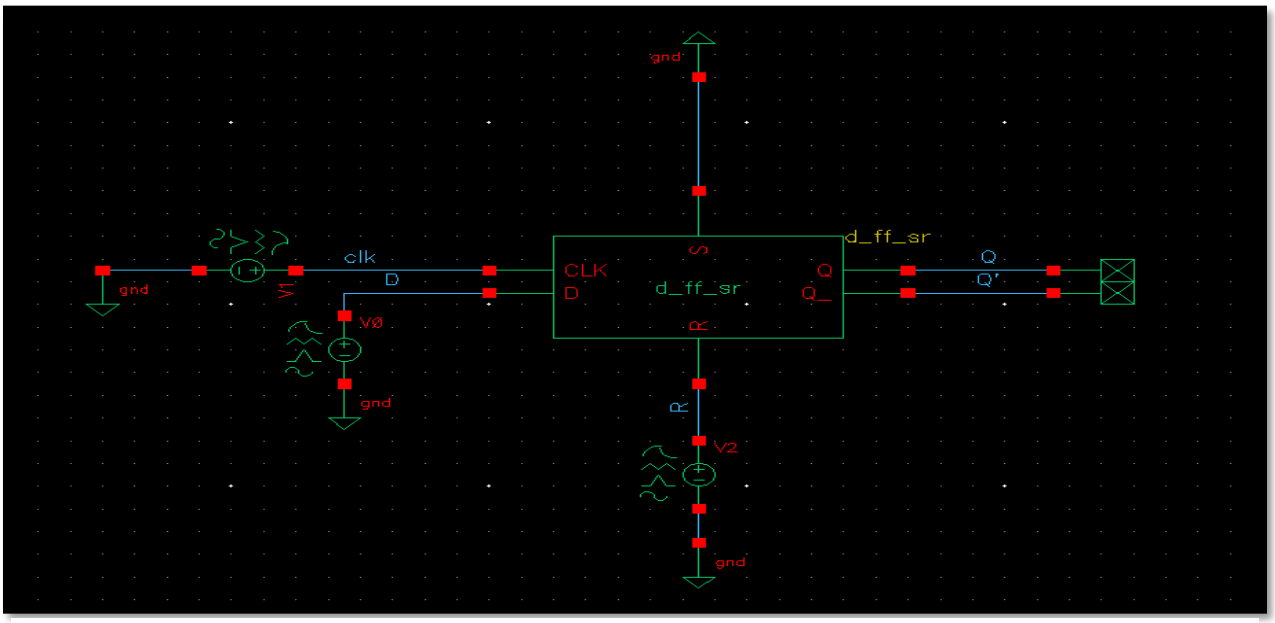

Figure 9-schematic of D_ff

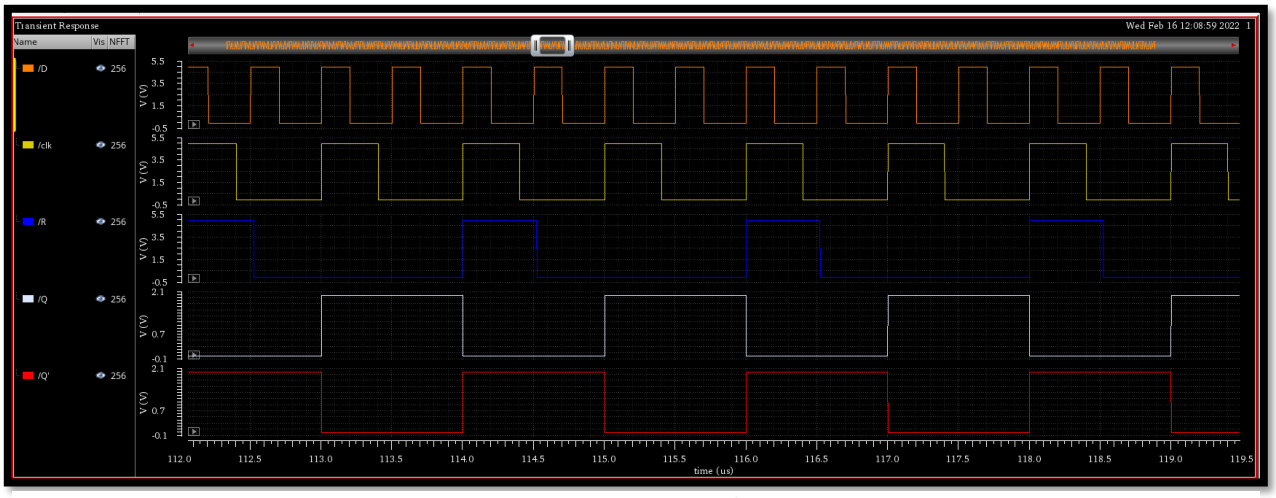

Figure 10-Transient analysis

Comment: We clearly see the proper operation of the D_ff with set and reset but I put the set equals zero forever as set and reset together gives undesired behavior .

- Sample&Hold:

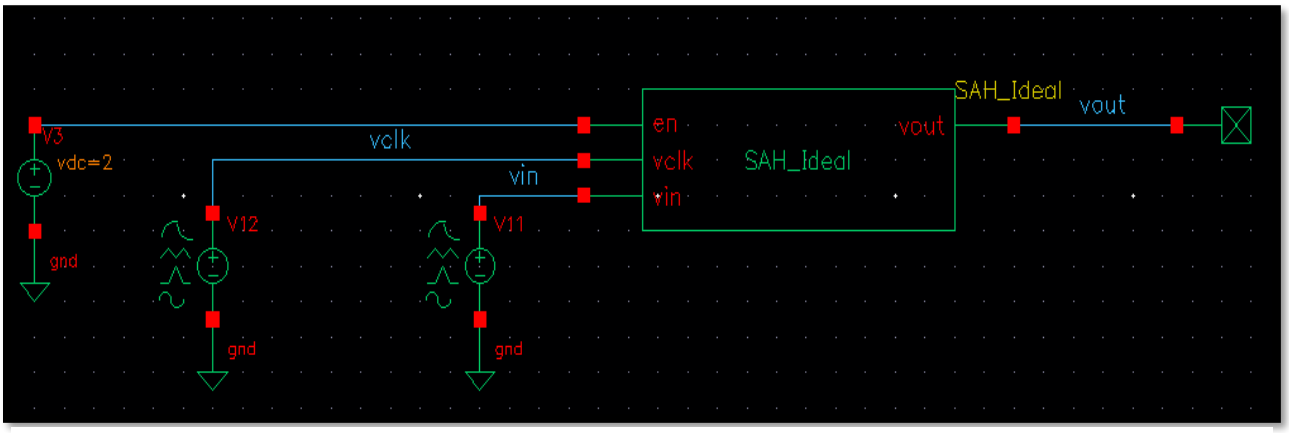

Figure 11-Schematic of S&H Circuit

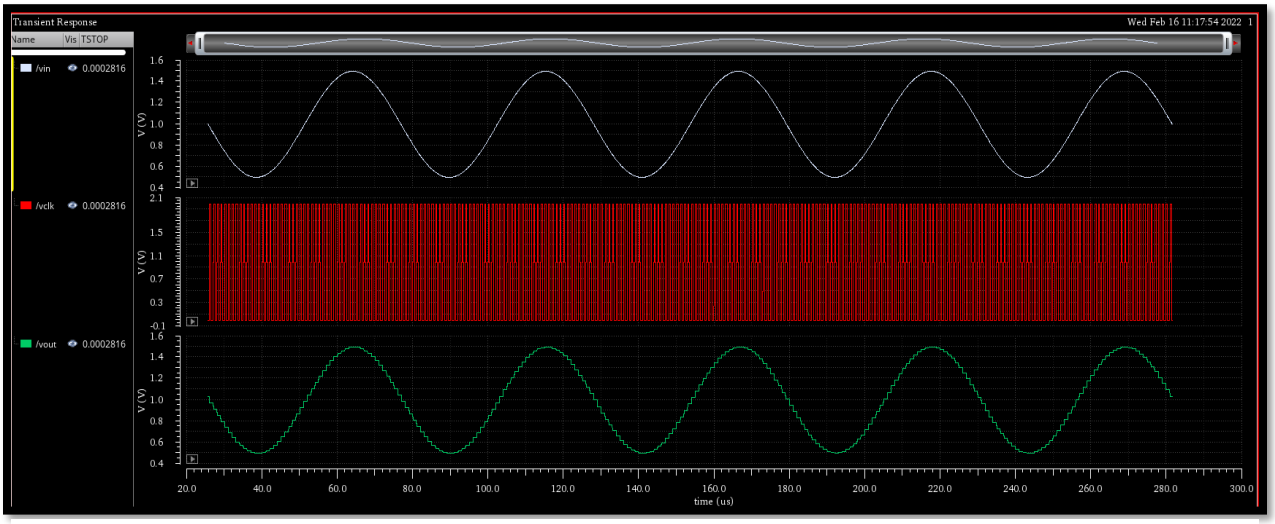

Figure 12-Transient analysis

Comment: We clearly see the proper operation of the S&H Circuit as we take a sample from the input signal and hold on it each clock cycle.

Part II:SAR Logic:

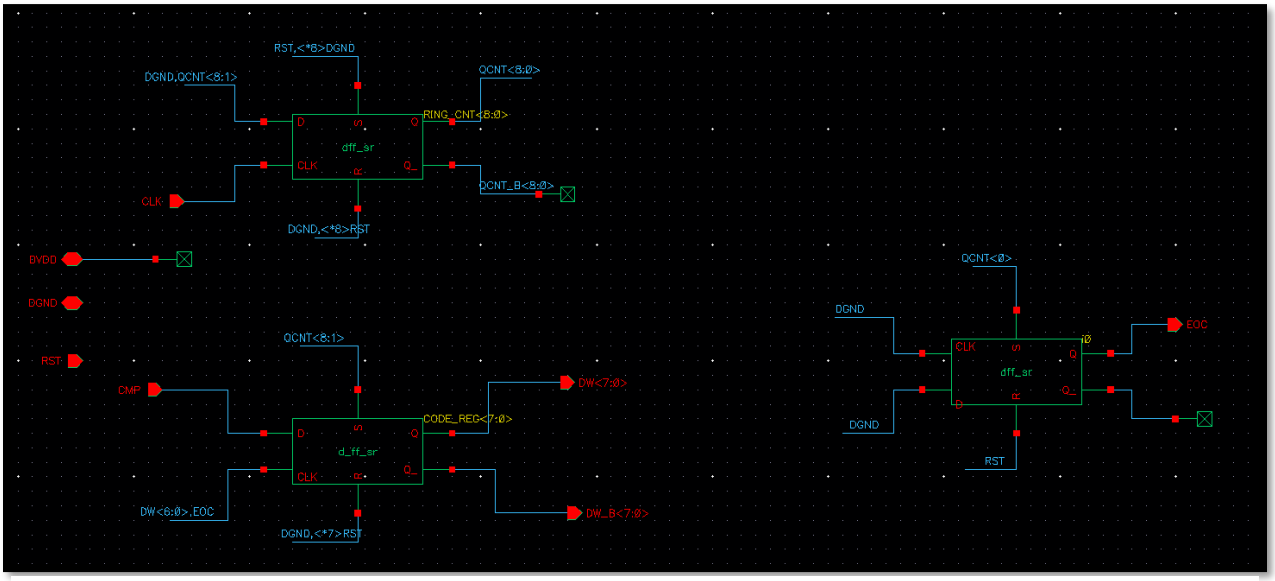

Figure 13-SAR_Logic Schematic

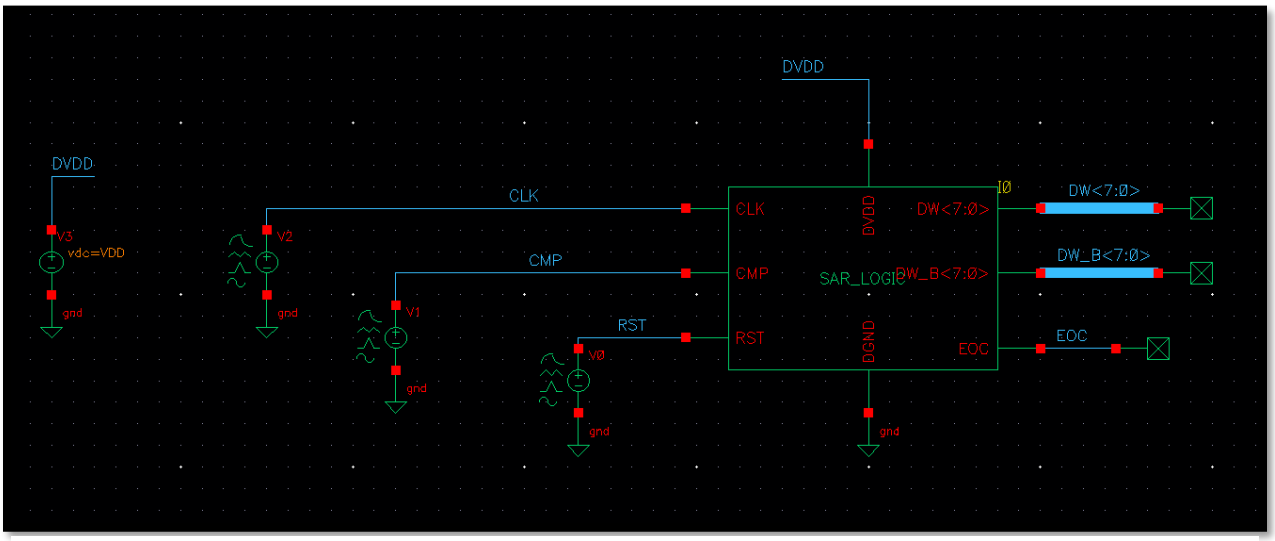

Figure 14-SAR_Logic Testbench Schematic

Outputs of different input cases:

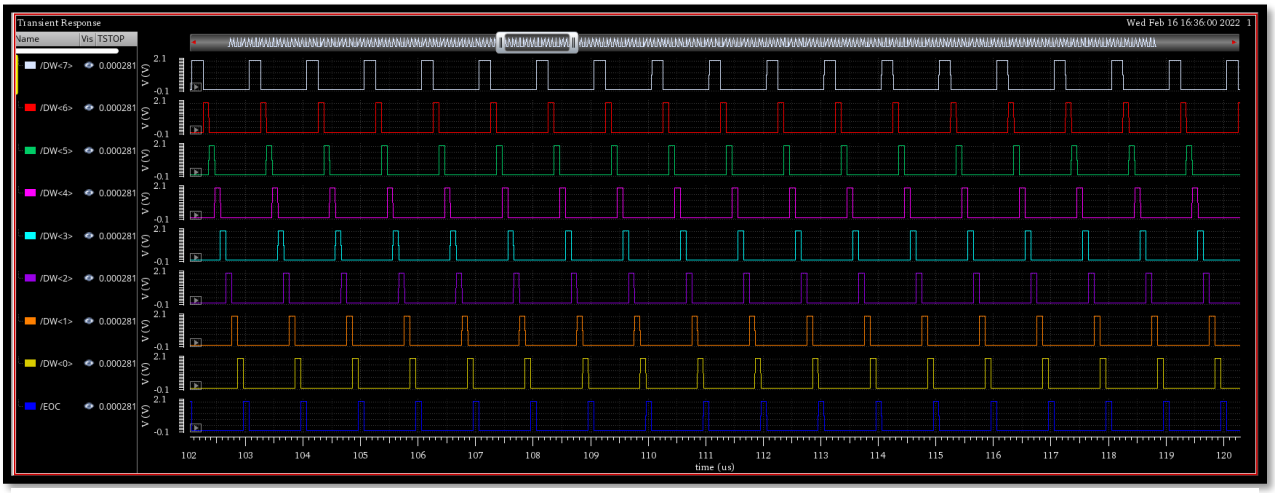

Figure 15-output at CMP is all zeroes

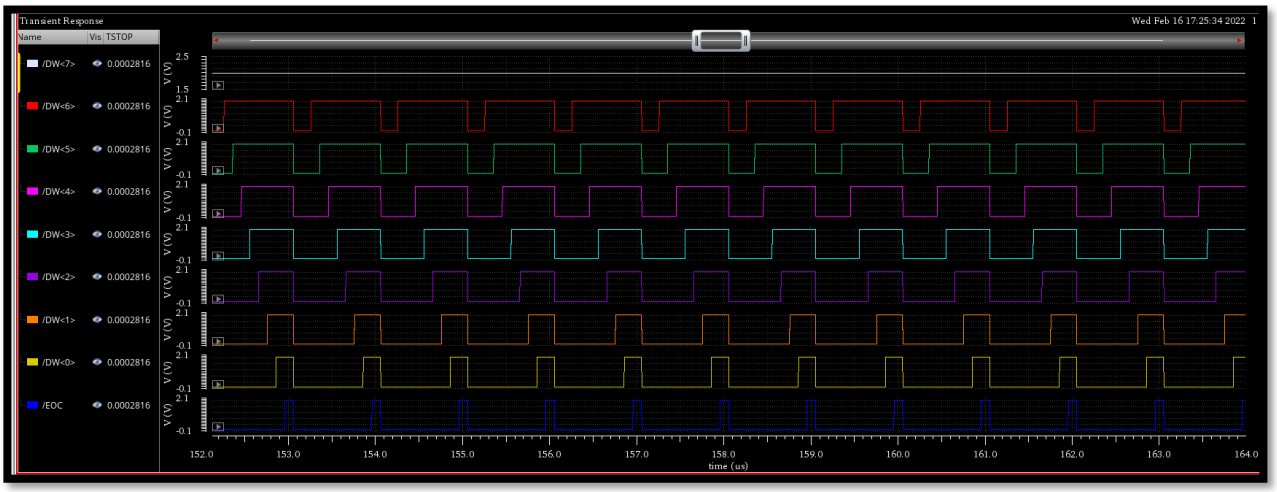

Figure 16-output at CMP is all Ones

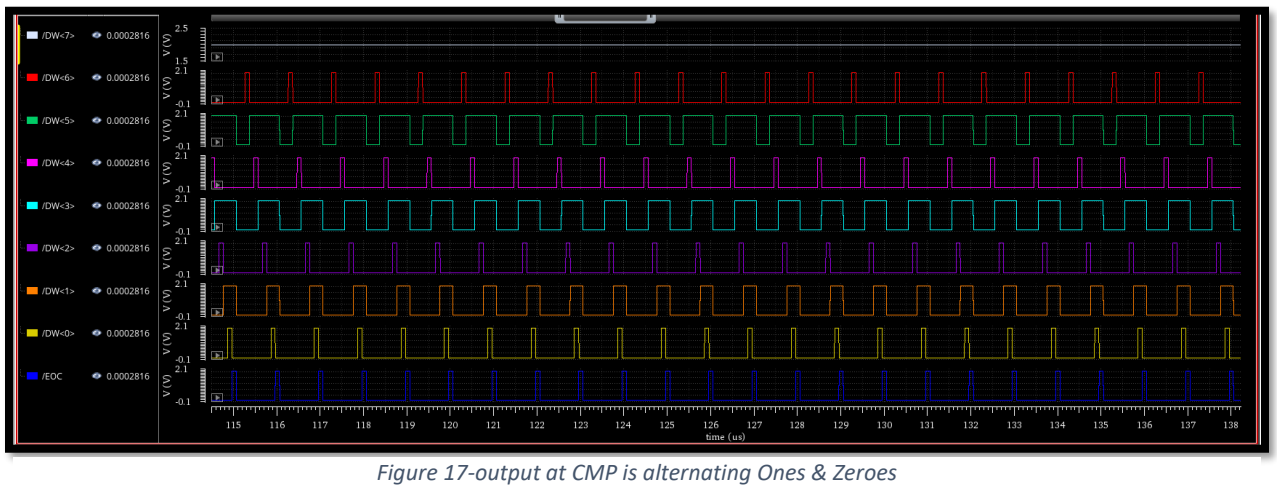

Figure 17-output at CMP is alternating Ones & Zeroes

How the design Works:

clk cycle	DW<7>	DW<6>	DW<5>	DW<4>	DW<3>	DW<2>	DW<1>	DW<0>	CMP	EOC
1(reset)	1	0	0	0	0	0	0	0	X	0
2	1	0	0	0	0	0	0	0	B7	0
3	B7	1	0	0	0	0	0	0	B6	0
4	B7	B6	1	0	0	0	0	0	B5	0
5	B7	B6	B5	1	0	0	0	0	B4	0
6	B7	B6	B5	B4	1	0	0	0	B3	0
7	B7	B6	B5	B4	B3	1	0	0	B2	0
8	B7	B6	B5	B4	B3	B2	1	0	B1	0
9	B7	B6	B5	B4	B3	B2	B1	1	B0	0
10	B7	B6	B5	B4	B3	B2	B1	B0	X	1

Discussing the logic and commenting on the o/p of the 3 cases:

Our logic is consisting of 3 main blocks, 2 chains of D flipflops, and single D flipflop to read the EOC, the 2chains of D flipflops are 9bits counter and 8bits code regs.

The ring counter consists of 9 flipflops, with reset to 8 of them, which reset them whenever reset signal is High , and the last one is it's reset connected to set which reset it to high instead.

We notice that the output of each flipflop is connected to the input of numerically preceding ones , starting from the MSB towards LSB but the LSB is grounded, and in each clock cycle the high state transfers from the MSB to the next and so on, till the LSB is high that till us that the 8bits digital data is now ready as there is 8 Clocks have been passed , and we use the state of the flip flop to trigger the EOC.
so the output from the MSB to bit number 1 fed into the code reg respectively.

Our cases : at the case of all Zeroes, as the comparator always find that his calculation is below the input so it will make each bit zero consequently until the EOC we find that all bits turned to Zero.

at case of all ones: we find the inverse of the previous case as the comparator will make each bit equals to one in order to achieve the input, until the EOC we find that all bits turned to one .

at case of alternating between ones and zeroes when the output of the comparator is one the bit will be one and vice versa so the output will alternate also between one and zero.

Part III: ADC Test Bench:

Screen shots for Schematics:

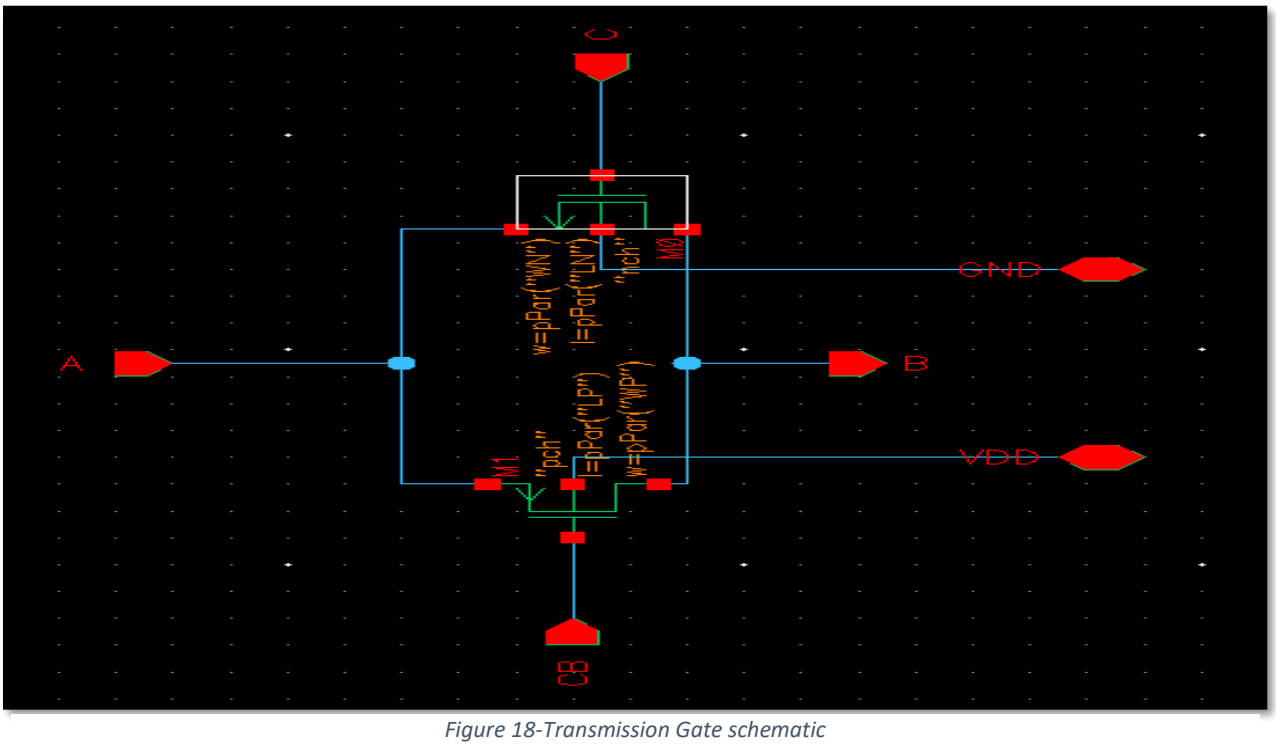

Figure 18-Transmission Gate schematic

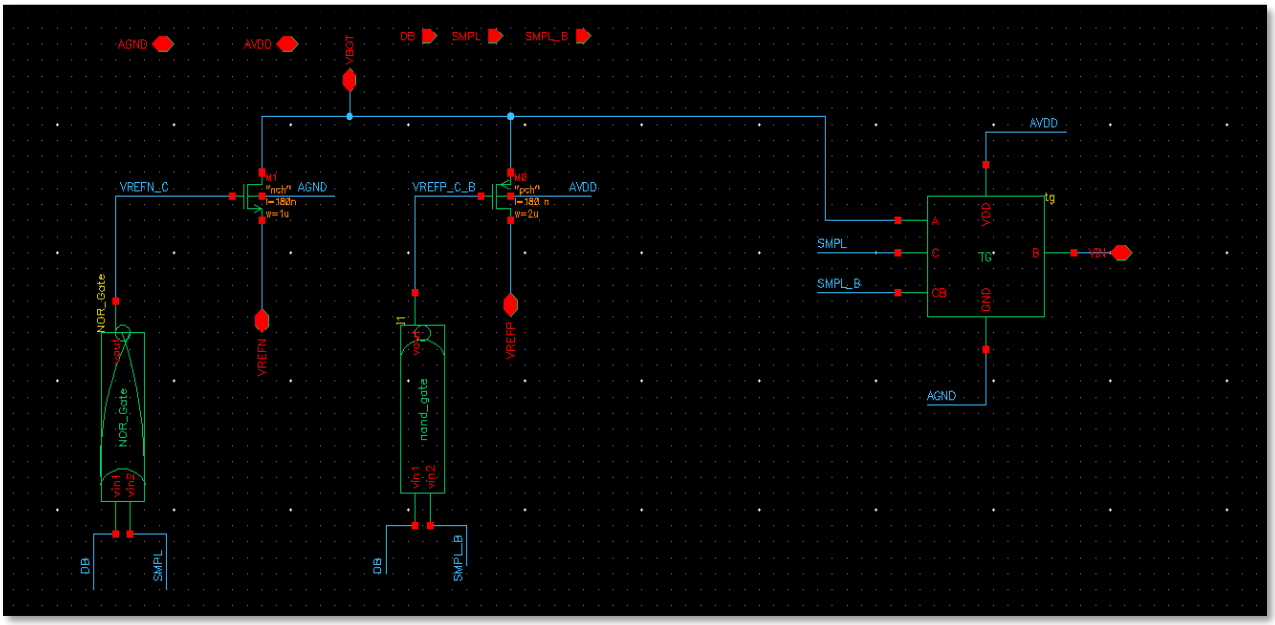

Figure 19-Bottom Plate sampling Switch schematic

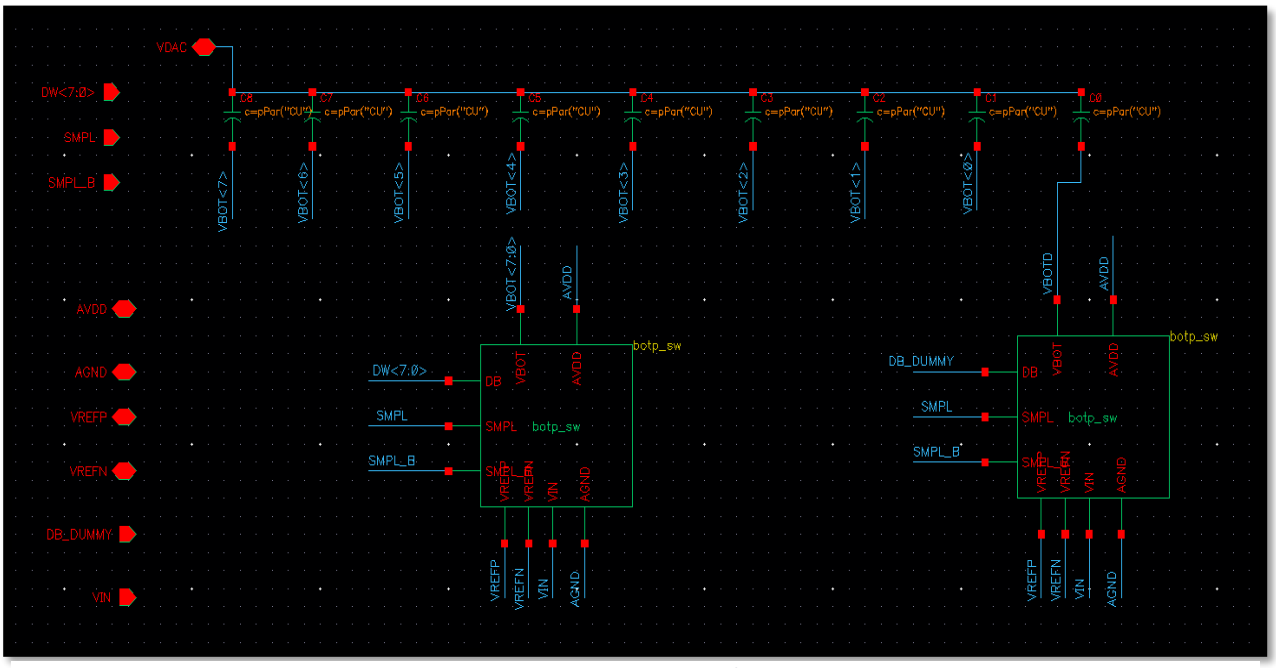

Figure 20-Capacitive DAC Schematic

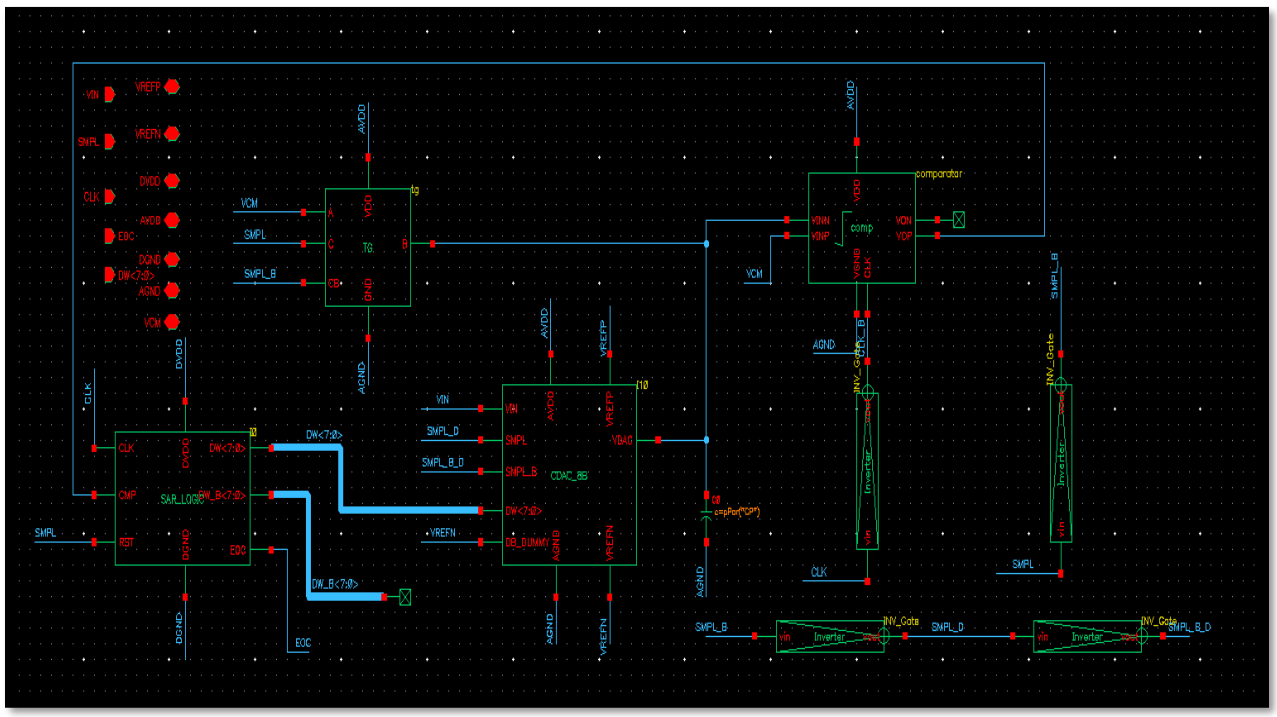

Figure 21-SAR ADC Schematic

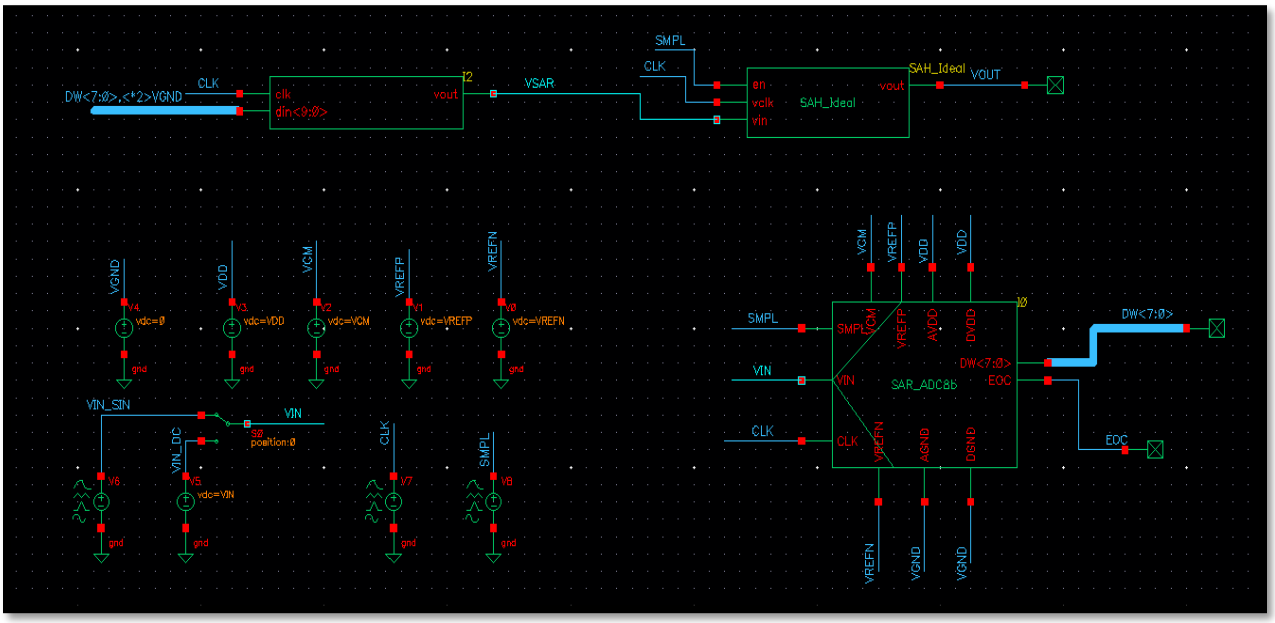

Figure 22-SAR ADC Test Bench

Part IV: DC Functional Test:

Waveforms of VIN,VSAR&EOC:

1st Case: VIN =VREFN:

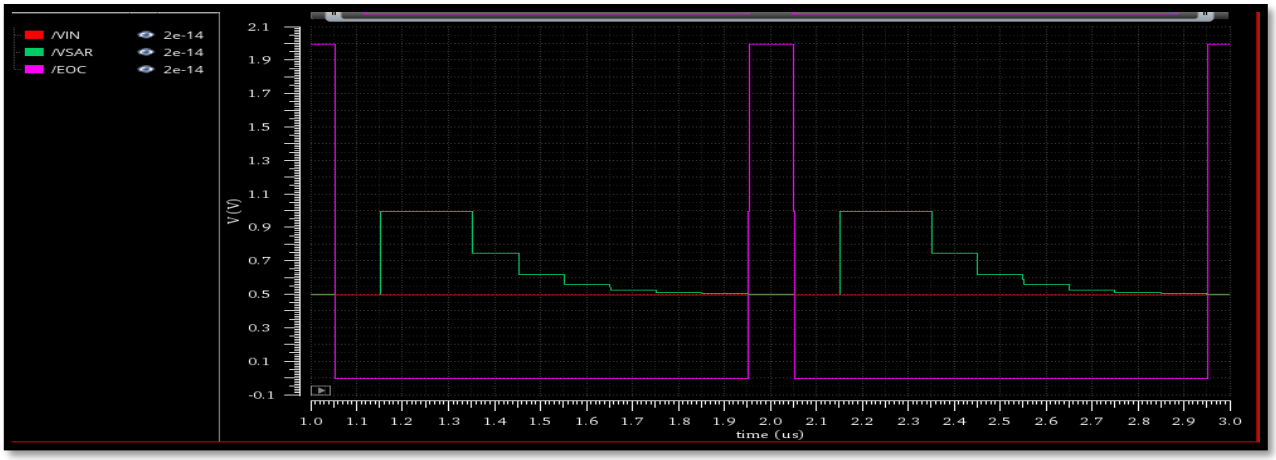

Figure 23-Case I VIN=VREFN

2nd Case: VIN=VREFN + (128+32+8+2+0.5)*VLSB:

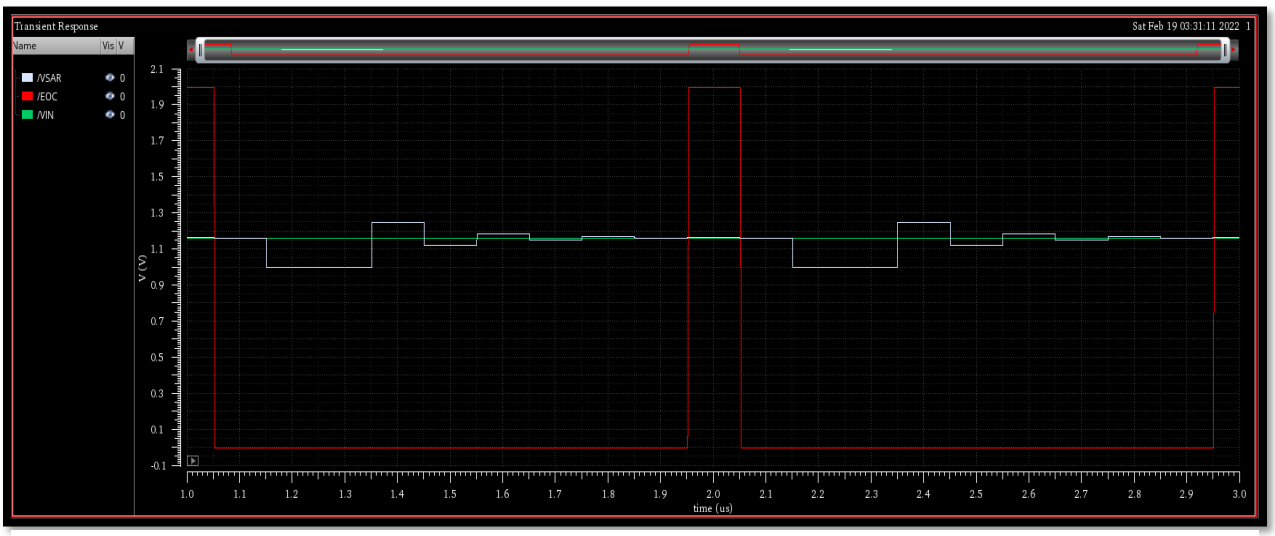

*Figure 23-Case II: VIN=VREFN + (128+32+8+2+0.5)*VLSB:*

Comment: in the 1st Case we see clearly the algorithm of the binary search as the output when see that the o/p is larger than the i/p will make one bit zero and so on till it settles at zero with no offset errors .

And in the 2nd Case as the i/p isn't totally larger or smaller than the o/p , the o/p will alternate between ones and zeroes as shown in the plot.

Case 3: VIN=VREFP:

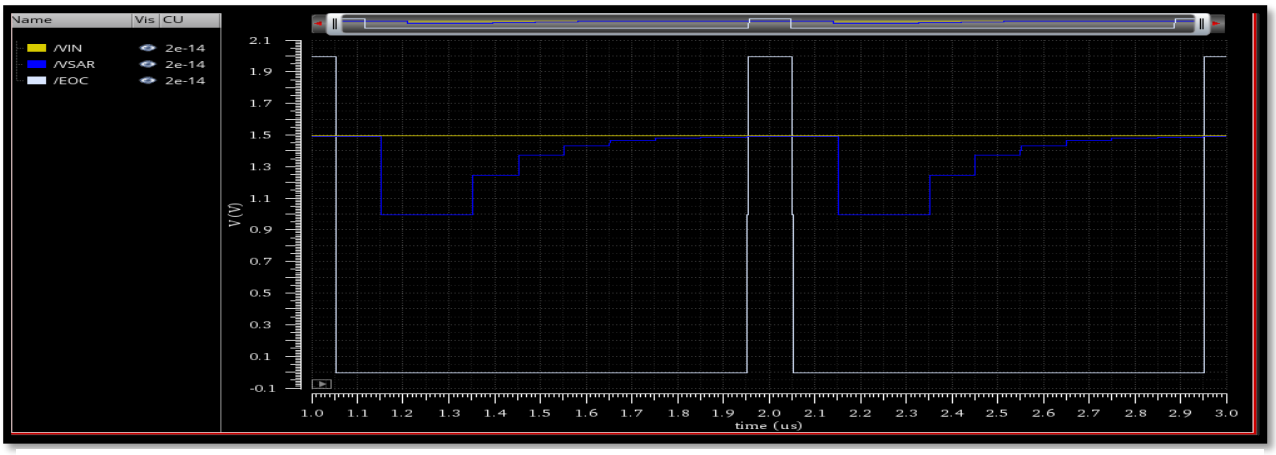

Figure 24-Case III : VIN=VREFP

The waveforms of SMPL, CLK, CMP, and EOC for the second case:

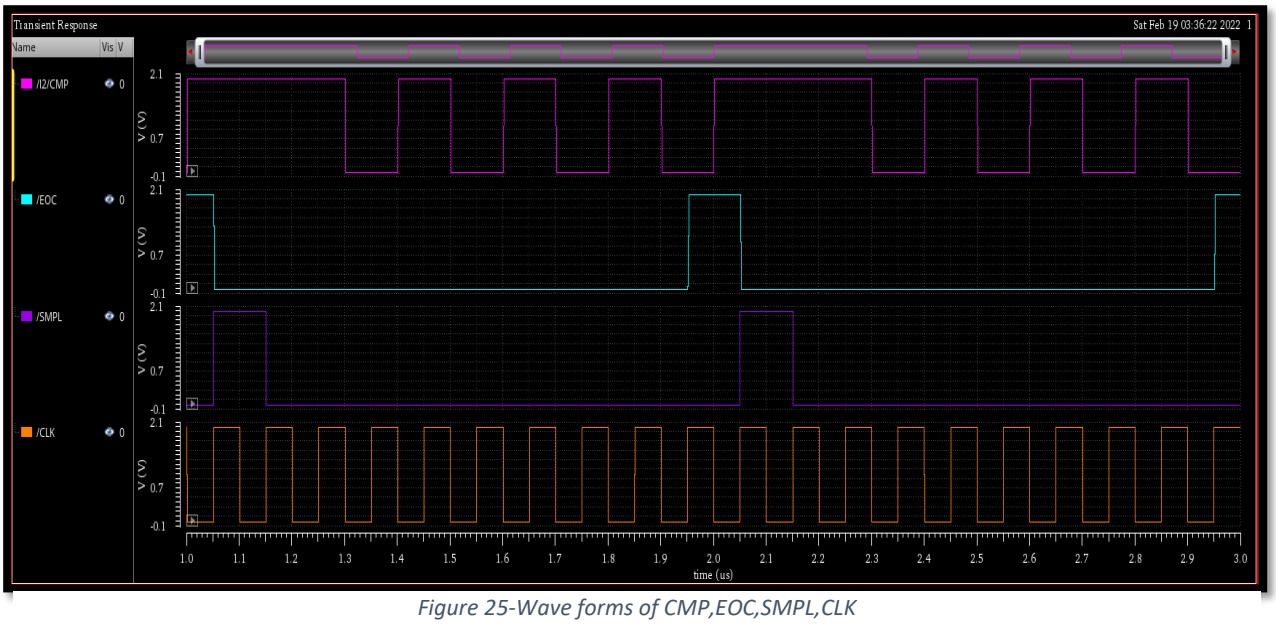

Figure 25-Wave forms of CMP,EOC,SMPL,CLK

Comment: in the 3rd Case we see clearly the algorithm of the binary search as the output when see that the o/p is smaller than the i/p will make one bit equals to one and so on till it settles at one with no offset errors .

We see in the plots of CMP & SMPL &CLK &EOC , that the comparator alternates between ones and zeroes as the i/p isn't fixed as larger or smaller positions , till the reset then it will repeat the same cycle.

Part V: sine wave Test:

Time Domain & FFT Plots :

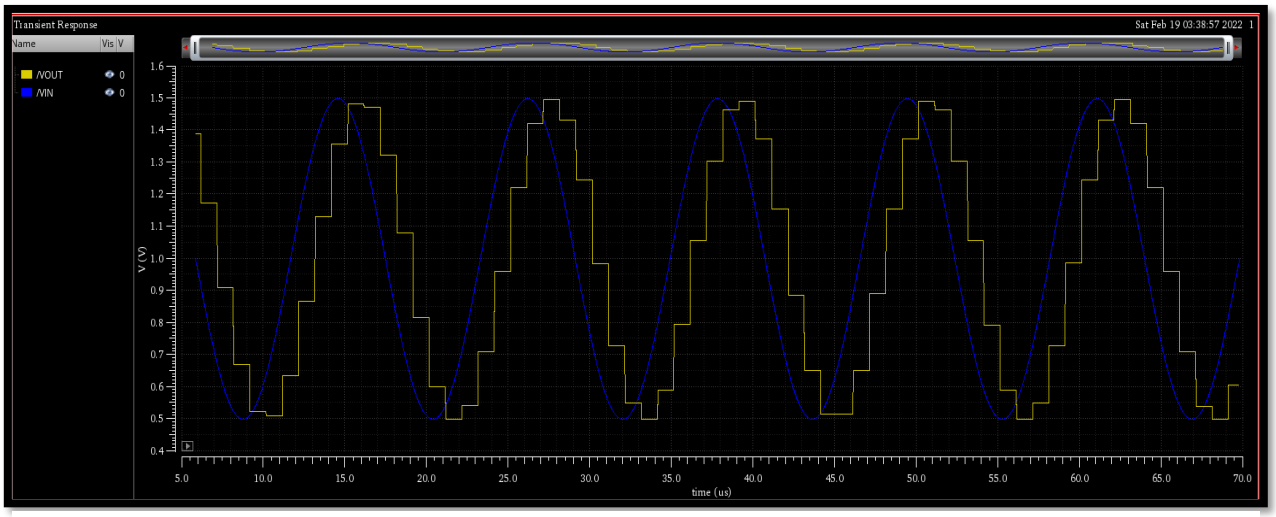

Figure 26-plot of VIN&VOUT

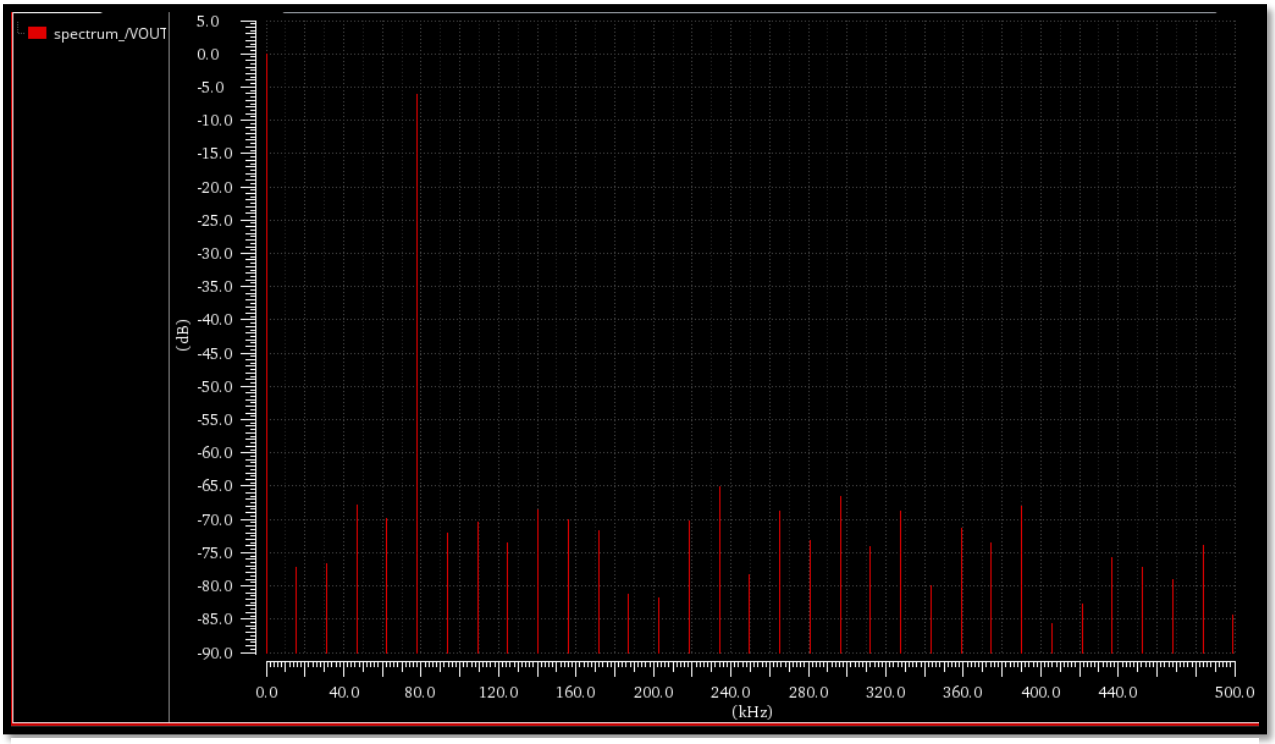

Figure 27-FFT of VOUT

Measured performance Parameters:

Measured Parameter	Measured value from Simulator
ENOB	8.06 bits
SNR	50.85 dB
SINAD	50.329 dB
SFDR	59.02 dB
THD	-57.4 dB
Signal Power	-6.02 dB
DC Power	-0.0185 dB
Noise Floor	-71.92 dB

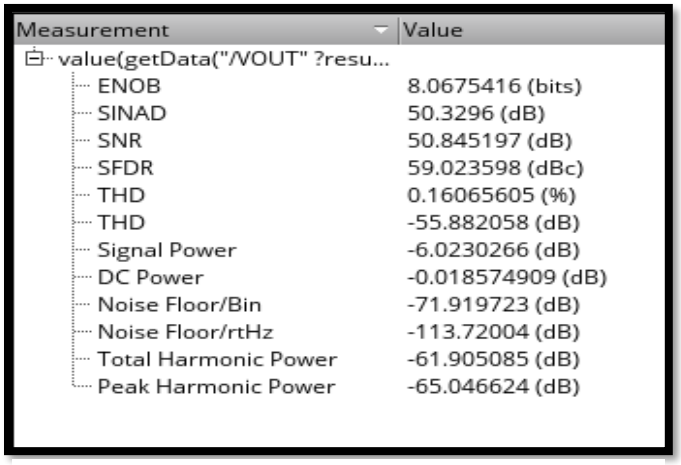

Figure 28-all Parameters from schematic

Comments: In this Case we make our test using sine wave , we see clearly that the output is tracking the input continuously, and we that the FFT of the output is very good and this is expected as all our blocks are behavioral models so there are no errors so we see from measured values that ENOB is almost 8 as expected and also all other parameters are very good such as SNR &THD , so our design is very good but if we used actual gates and blocks with errors and delays these measured values will degrade, but overall this design is very good .

Note : I used different model file for the transistor which is “ee214b_hspice” , which maybe make the ENOB little bit larger than 8 bits(ideal ENOB) in addition to little errors and differences between different processors that make this little shift.