W2022 Siemens ADCs

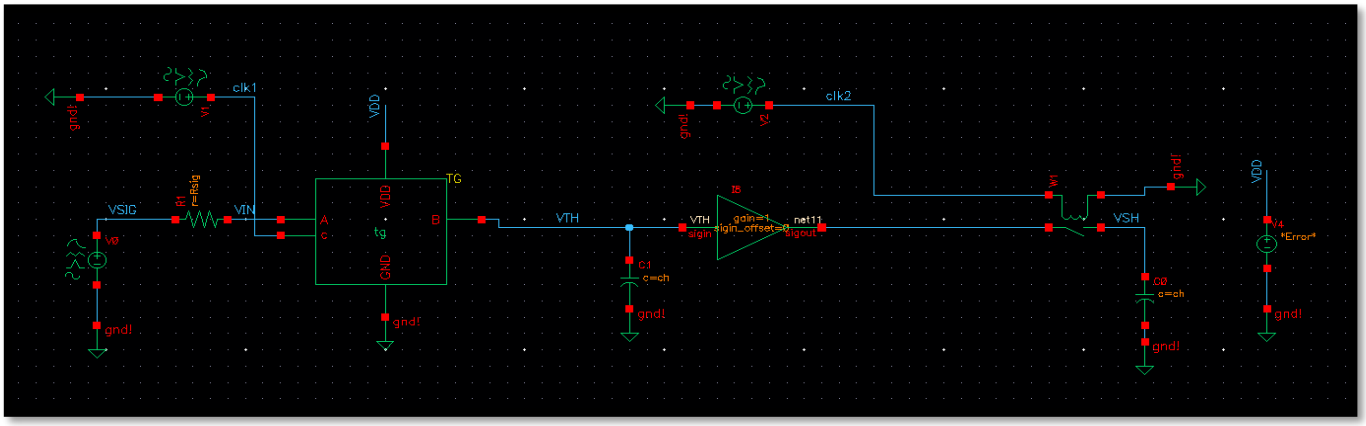
Lab 4

Sample&Hold circuits in Cadence Virtuoso

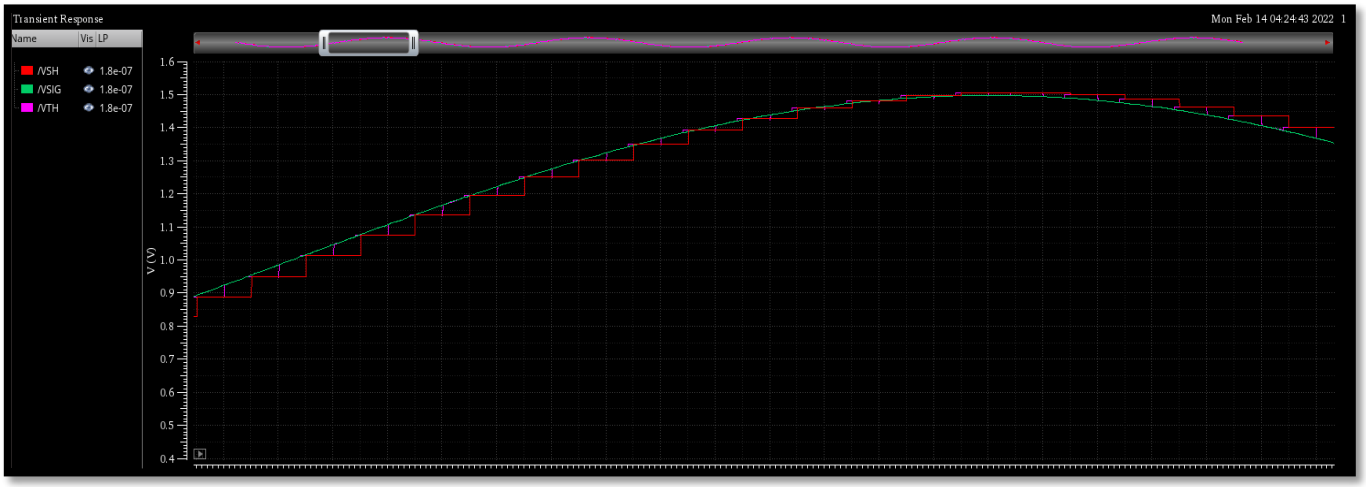
Contents

Part I:S&H Artifacts:

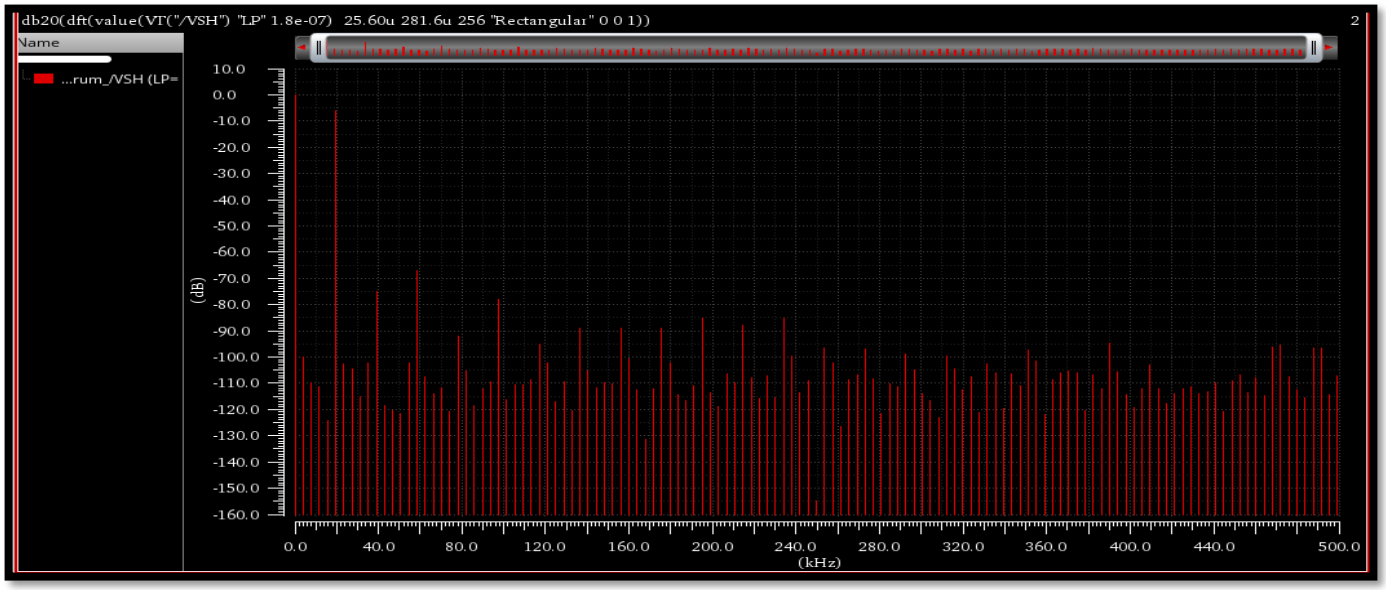
The schematic:



Timing diagram of VSIG,VTH&VSH:



FFT for VSH:



Comparing between results :

P.O.C	With TG(lab 4)	With Ideal witch (lab 2)
ENOB	9.627	27.61
SINAD(dB)	59.71	168.004
SNR(dB)	71.83	169.95
SFDR(dBF)	60.933	175.288
THD(dB)	-59.984	-172.07718
Signal Power(dB)	-5.898	-6.02
DC Power(dB)	0.0228	7.02e-13

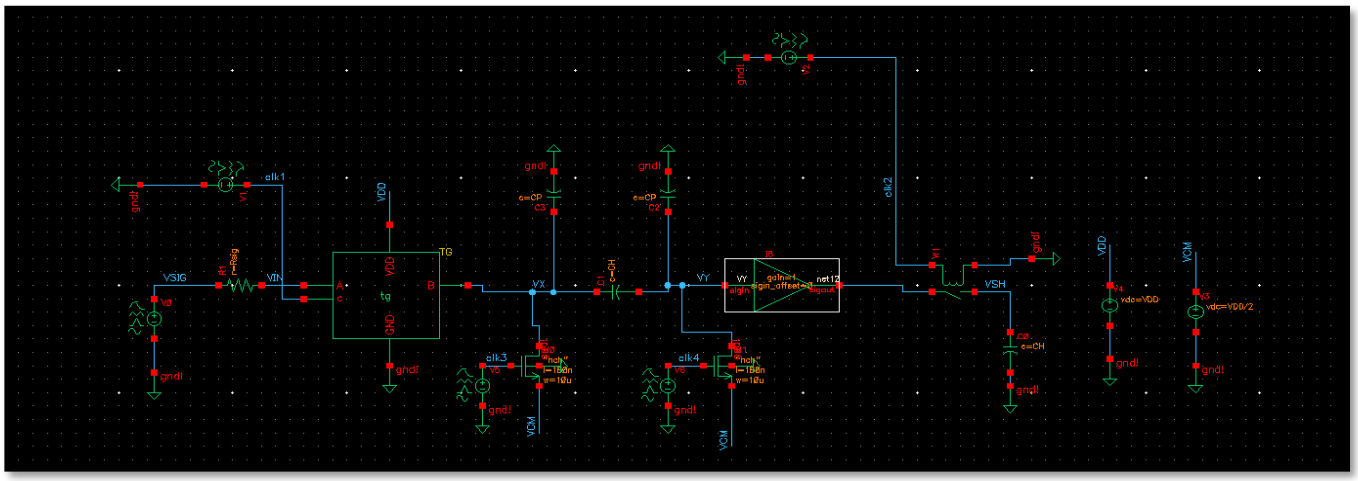
Commenting on the results :

We notice that the ENOB has been toughly degraded when we use practical switch rather the ideal switch, also SNR,SFDR,SINADand THD have been degraded but the signal power is almost the same but the DC Power has been increased ,all these bad effects are due to the non-ideality of the transmission gate and we will try to reduce these effects with some techniques as Bottom Plate Sampling .

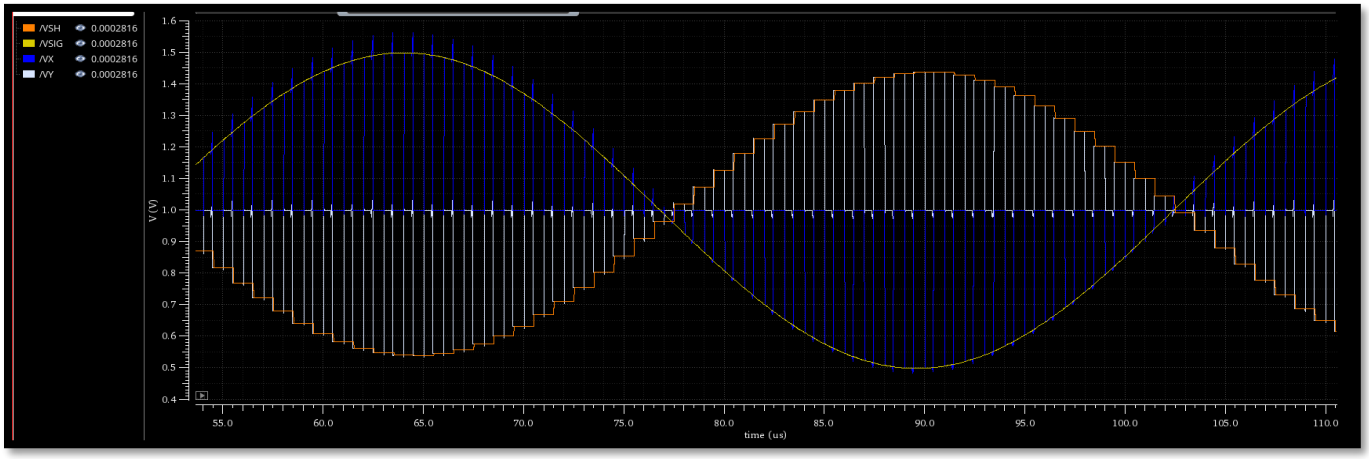
Note: signal and DC powers are in Amplitude values not rms.

Part II:Bottom Plate Sampling :

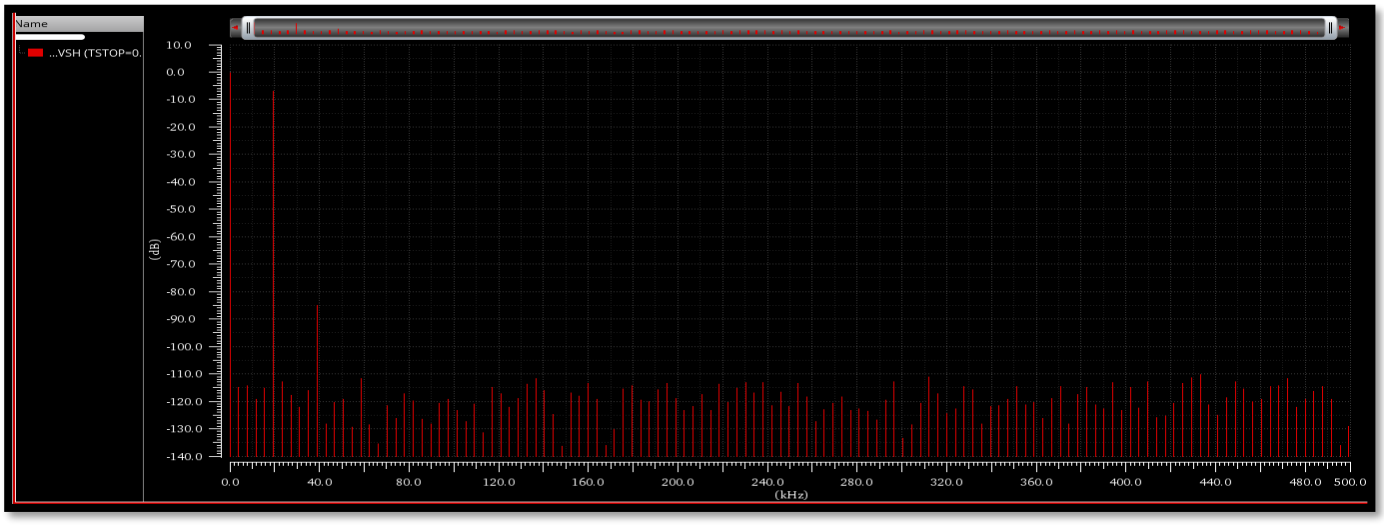
The schematic :



Timing Diagram between VSIG,VX,VY&VSH:



FFT of VSH:



Comparing between results :

P.O.C	With TG(part 1)	With Bottom plate (part 2)
ENOB	9.627	12.59
SINAD(dB)	59.71	77.601
SNR(dB)	71.83	89.188
SFDR(dBF)	60.933	77.91
THD(dB)	-59.984	-77.901
Signal Power(dB)	-5.898	-6.94
DC Power(dB)	-0.0228	-0.0886

Commenting on the results :

We notice that the ENOB has been improved significantly when we use the technique of Bottom Plate Sampling rather the Transmission Gate, also SNR,SFDR,SINADand THD have been improved.

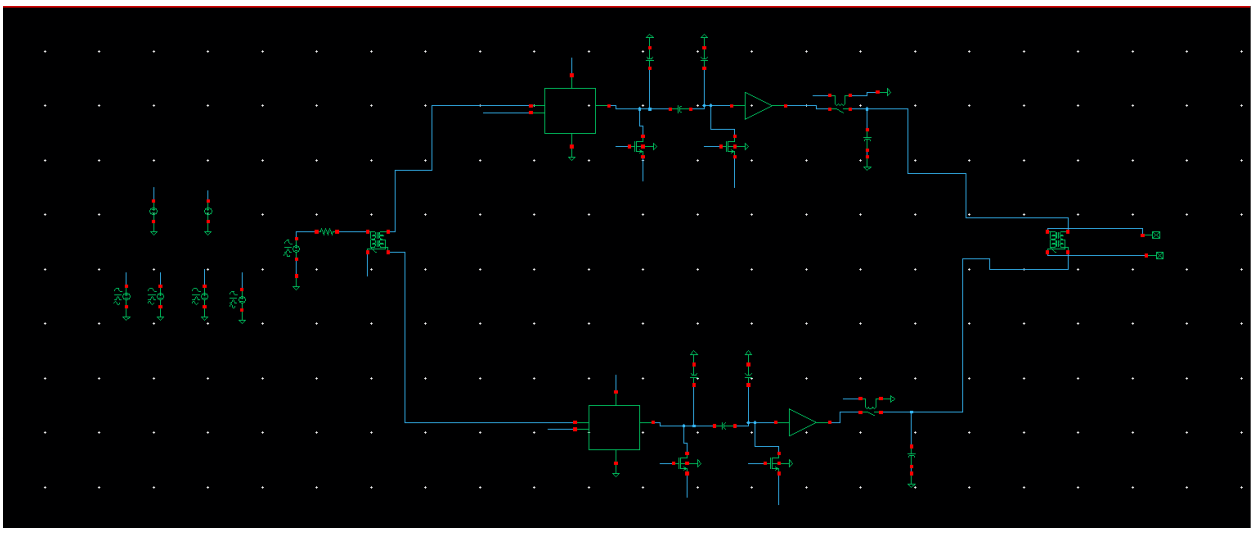
All this improvement of the specs is due to improvement the Non-Linearity as the error of bottom Plate Sampling is independent on V_{in} so the error isn't no more toughly non-linear so our specs has been improved except for that the input signal has been attenuated due to this

technique .

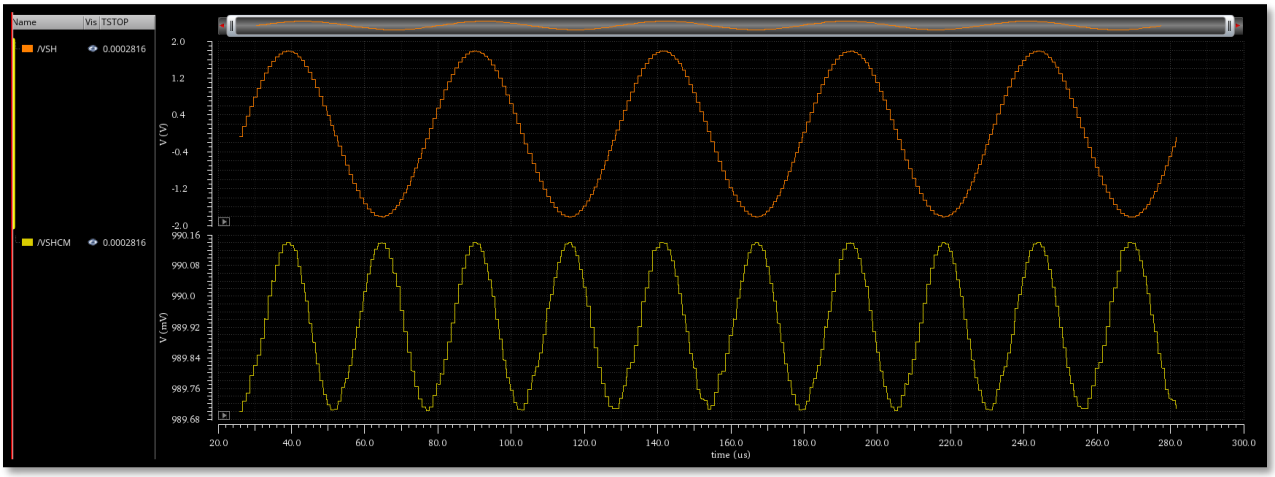
Note: signal and DC powers are in Amplitude values not rms.

Part III: Fully Differential Operation:

The Schematic :



Output of VSH&VSHCM vs time:

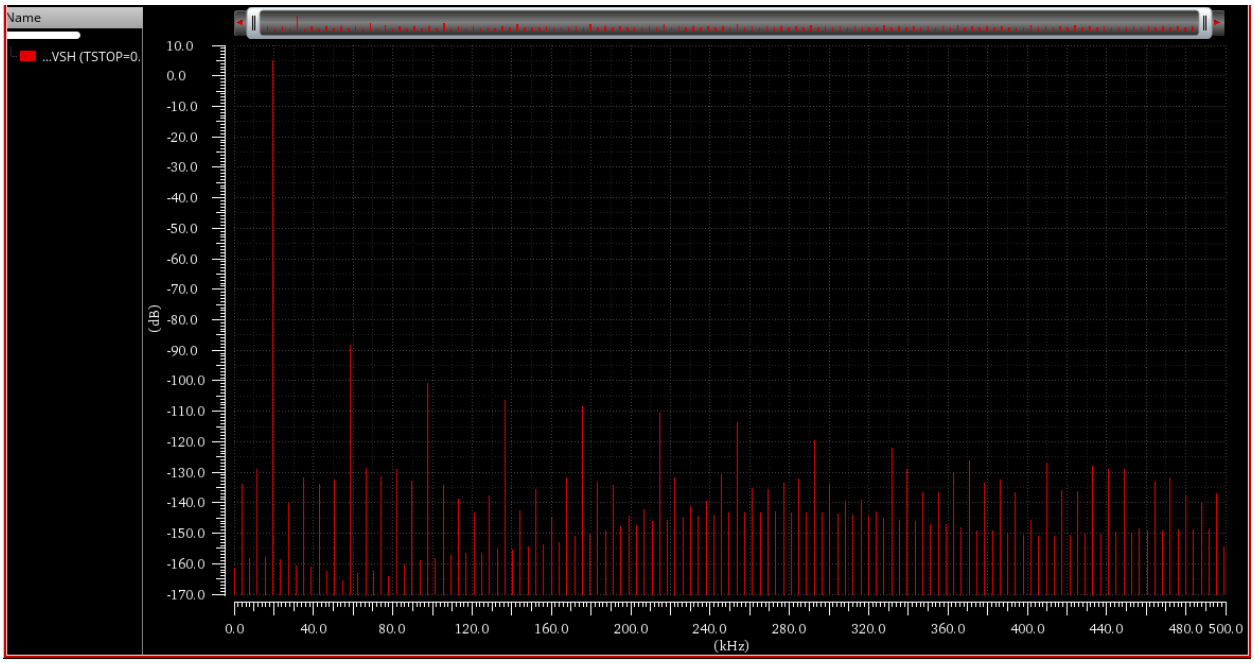


Commenting on the output:

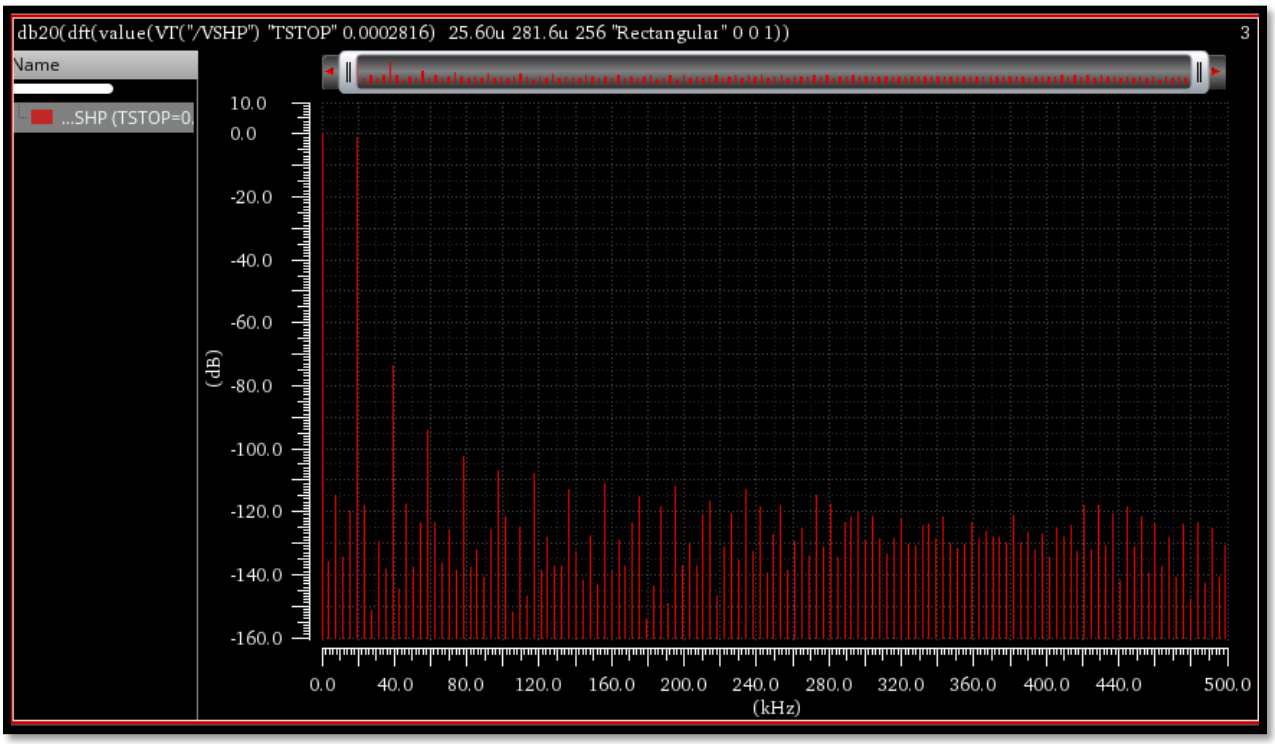
We notice from the output that in V_{outd} the Swing has been doubled and this is a property of differential circuit, also the swing of the Common Mode output is very small, this is another advantage of fully differential circuit as it rejects the common mode signals so the effect of common mode noise is reduced .

FFT of VSHP &VSH:

1: for VSH



2: for VSHP :



Comparing between results :

P.O.C	VSH	VSPH
ENOB	15.119	11.7
SINAD(dB)	92.779	72.429
SNR(dB)	109.788	100.506
SFDR(dBF)	93.156885	72.4831
THD(dB)	-92.8629	-72.4361
Signal Power(dB)	-5.099	-0.921
DC Power(dB)	-161.385	-0.087
2^{nd} harmonic Power(dB)	-88.05	-73.4

Commenting on the Results:

We notice that the specs in VSH has been improved more than that in VSPH as after we output the fully differential ENOB improved and the Common mode noise rejected so every specs improved.

Note :Part VI is optionally …