Folded Cascode OP-Amp

Reported by:

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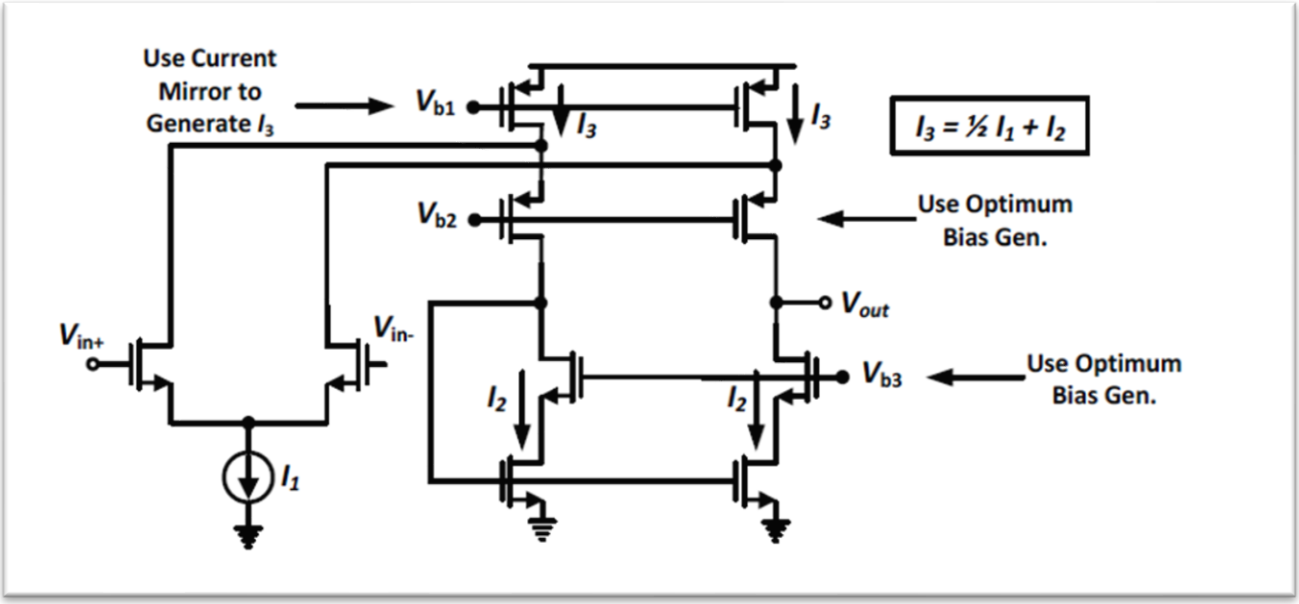
➢ Design procedure (hand calculations):



❖ ***Specifications:***

-ADC > 55 dB (DC differential gain)
-GBW > 100 MHz for a load capacitance of CL=2pF
-Slew Rate > 100 V/μsec
-Output Swing > 1.5Vpp
-Input referred thermal noise density < $\sqrt{hz}$
-PM > 60°

❖ ***The methodology we used:***

We didn't use the square law method as it's very approximated so the results wouldn't be exact, we used $\frac{g_m}{I_D}$ method.

In first, we made a dc sweep for $V_{GS}\ Vs\ \frac{g_m}{I_D}$ to determine the range of $\frac{g_m}{I_D}$.

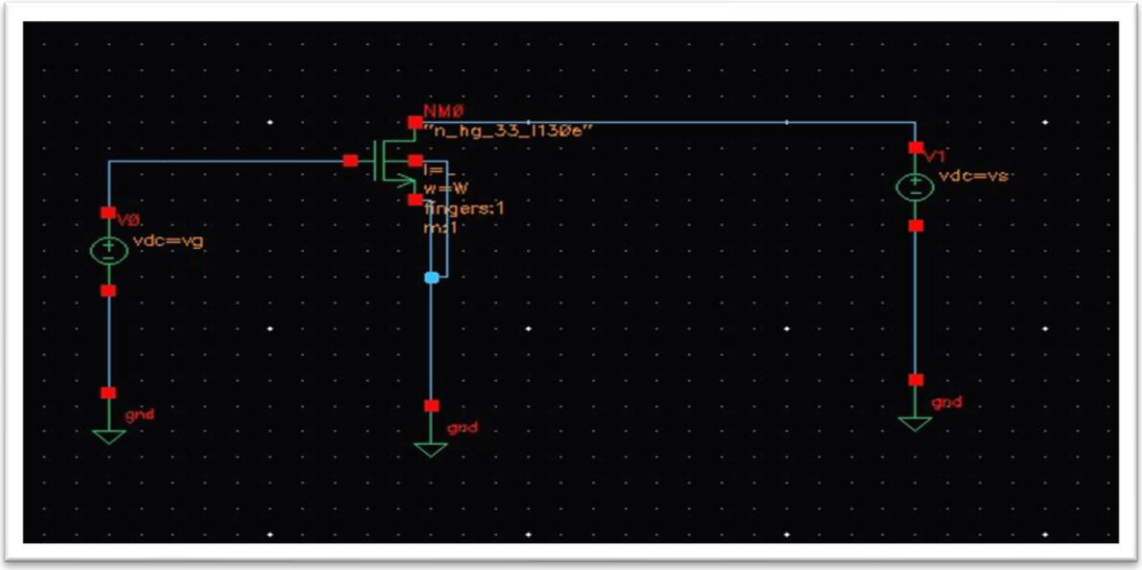
Then from the range of $\frac{g_m}{I_D}$ we generated the following relations (graphs):

- $\frac{g_m}{I_D}\ Vs\ g_m r_o$ → to determine the required gain.
- $\frac{g_m}{I_D}\ Vs\ \frac{I_D}{W}$ → to determine the required width
- $\frac{g_m}{I_D}\ Vs\ v_{sg}$ → to determine the required biasing.

- Note: we did that for both NMOS & PMOS.
- Note: graphs are for different L to make variety to choose the suitable L.

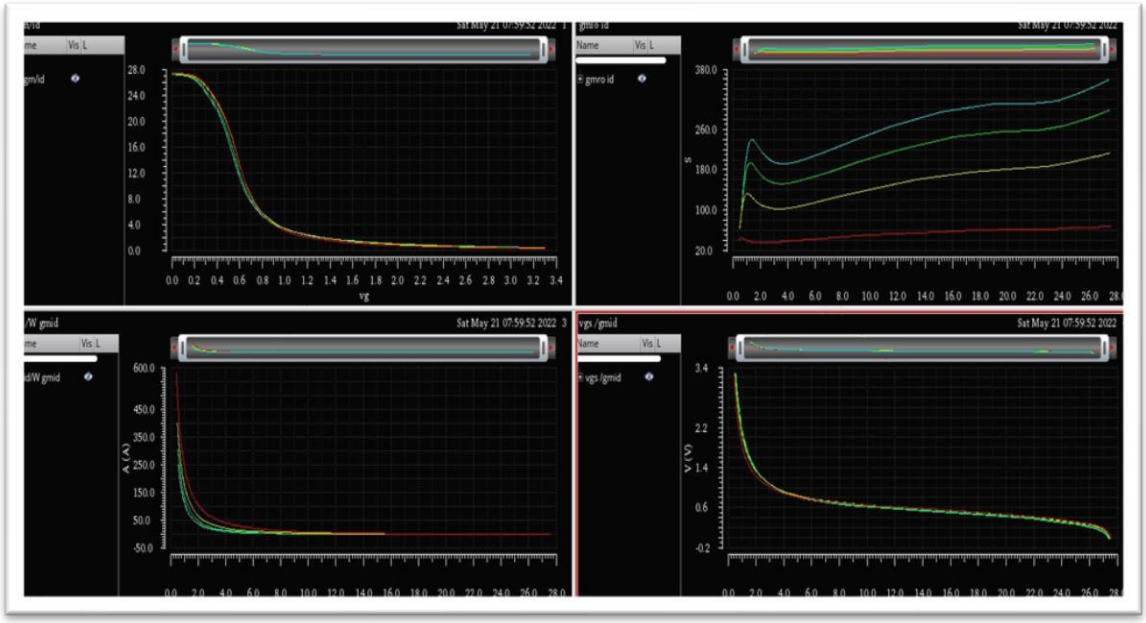
➢ ***For the NMOS:***

- ***NMOS test to get $\frac{g_m}{I_D}$ range:***



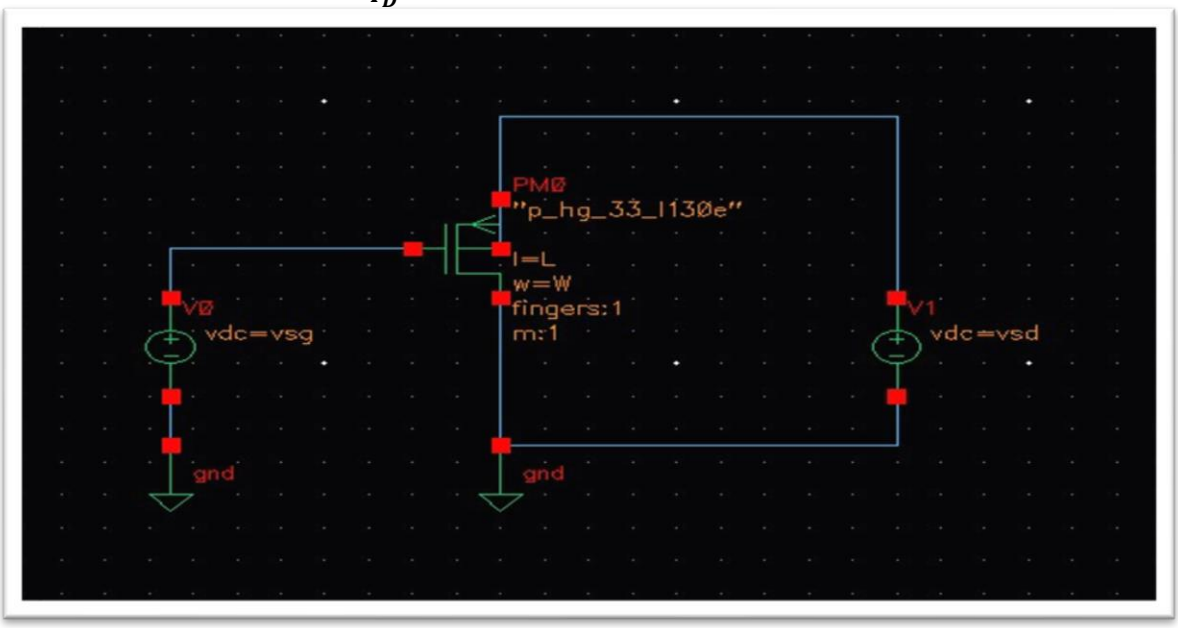
-In this test we made V_{DS} constant and sweeped the V_{GS} from 0 to V_{DD} then we get $\frac{g_m}{I_D}$ range.

❖ ***Figure of the DC sweep:***



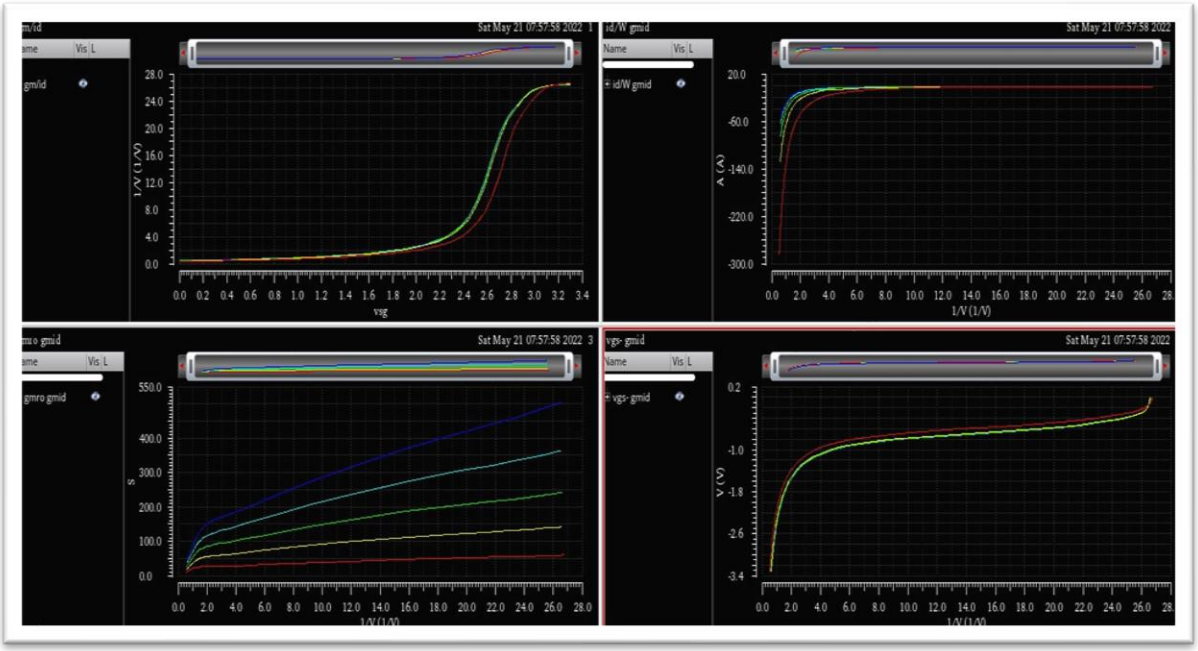
➢ ***For the PMOS:***

- ***PMOS test to get $\frac{g_m}{I_D}$ range:***



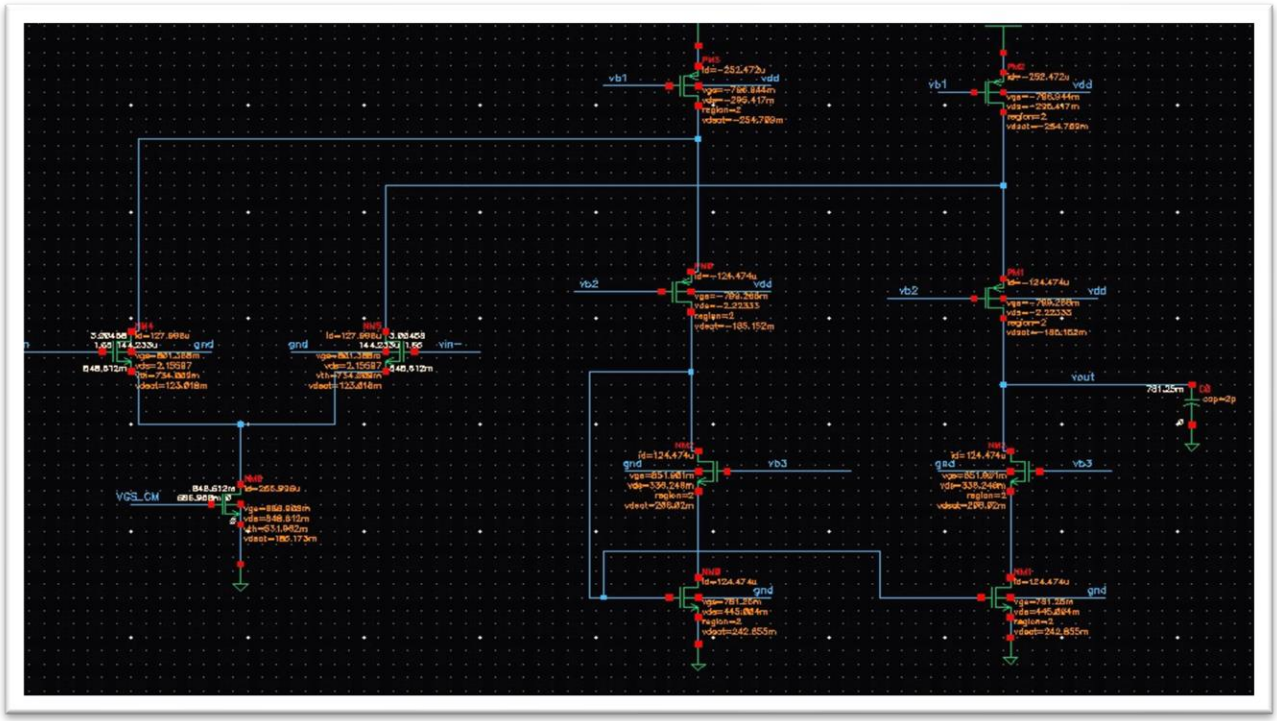
- We did the same thing here also.

❖ ***Figure of the DC sweep:***

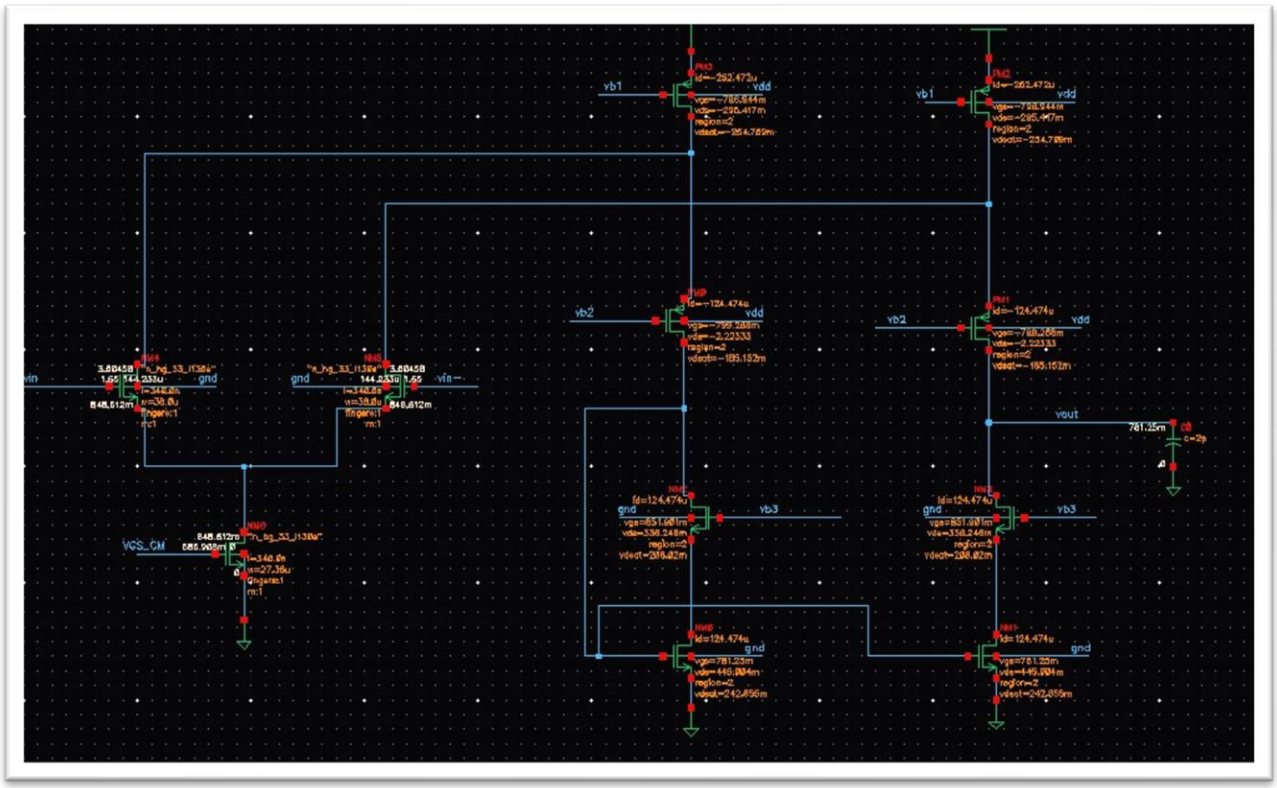


➢ ***Sizing & DC operating point:***

- DC operating point:



- Component parameters:



❖ ***For the input pair transistors:***

We know that slew rate $= \frac{I_{SS}}{C_L}$,minimum Iss to achieve this slew rate is 200μA, to maximize this ratio we increase I_{SS} to $250\ \mu A$.
To minimize the error, we assumed $I_2 = 125\ \mu A$
$\therefore I_3 = 0.5\ I_1 + I_2 = 250\ \mu A.$

$GBW = \frac{g_m}{c_l}$, as we want it to be 100 MHZ
$\therefore \frac{g_m}{c_l} > 100 * 2\pi * 10^6 \rightarrow g_m \geq 1.25 * 10^{-3}$ → $\therefore \frac{g_m}{I_D}$ **= 5**
To maximize the GBW , and as the input pair is essential in the gain and reducing the noise we maximized the ratio of $\frac{g_m}{I_D}$ and assumed it's =15.

For I_{SS} (I_1) :
For $I_{SS} = 250\ \mu A$ we made $\frac{w2}{w1} = 10$ (L1=L2=L_{min}=340nm), and we increased the value of $V_{DS}\ Vs\ V_{eff}$ by about 100 mv so that will reduce the variations and make the biasing in deep saturation.

❖ ***For the two upper PMOS transistors:***
To assume the value of $\frac{g_m}{I_D}$ we know that this pair doesn't participate in the gain so we made $\frac{g_m}{I_D} = 7$ to and also to minimize the noise.
We used L=340 nm
From $\frac{I_D}{W}\ vs\ \frac{g_m}{I_D}$ graph → w=46u
From $V_{Sg}\ vs\ \frac{g_m}{I_D}$ graph → $V_{sg} = 0.752\ v$
From $V_{eff}\ vs\ \frac{g_m}{I_D}$ graph → $V_{eff} = 251\ mv$
$\therefore V_{b1} = V_{DD} - V_{GS} = 2.54\ v$

❖ ***<u>For the two cascaded PMOS transistors:</u>***

To assume the value of $\frac{g_m}{I_D}$ we know that this pair participate in the gain so we made $\frac{g_m}{I_D} = \mathbf{9}$ to maximize the gain and minimize the noise.

We used L=340 nm

From $\frac{I_D}{W}\ vs\ \frac{g_m}{I_D}$ graph → w=39.5u

From $V_{Sg}\ vs\ \frac{g_m}{I_D}$ graph → $V_{sg} = 0.690\ v$

From $V_{eff}\ vs\ \frac{g_m}{I_D}$ graph → $V_{eff} = 189\ mv$

$\therefore V_{b2} = V_{DD} - (V_{eff1} + 100mv) - V_{sg2} = 2.26\ v$

- We added 100 mv to V_{eff1} to insure the saturation.

❖ ***<u>For the lower two NMOS transistors:</u>***

To assume the value of $\frac{g_m}{I_D}$ we know that this pair doesn't participate in the gain so we made $\frac{g_m}{I_D} = \mathbf{7}$ to minimize the noise.

We used L=340 nm

From $\frac{I_D}{W}\ vs\ \frac{g_m}{I_D}$ graph → w=7 u

From $V_{gs}\ vs\ \frac{g_m}{I_D}$ graph → $V_{gs} = 0.737\ v$

From $V_{eff}\ vs\ \frac{g_m}{I_D}$ graph → $V_{eff} = 228\ mv$

❖ ***<u>For the two cascaded NMOS transistors:</u>***

To assume the value of $\frac{g_m}{I_D}$ we know that this pair participate in the gain so we made $\frac{g_m}{I_D} = \mathbf{9}$ to maximize the gain and minimize the noise.

We used L=340 nm

From $\frac{I_D}{W}\ vs\ \frac{g_m}{I_D}$ graph → w=10.7u

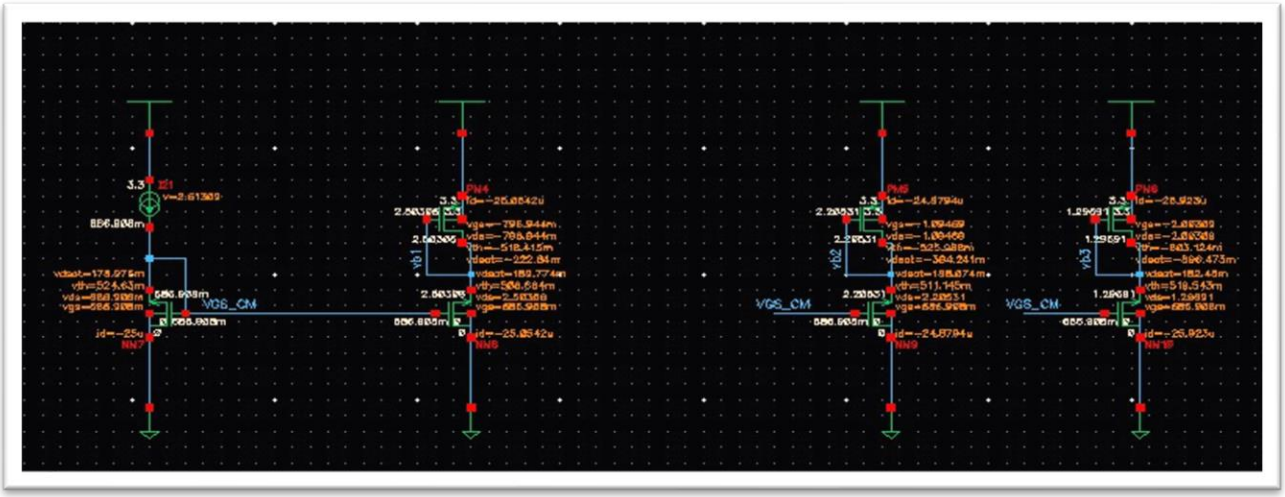
From $V_{gs}\ vs\ \frac{g_m}{I_D}$ graph → $V_{gs} = 0.681\ v$

From $V_{eff}\ vs\ \frac{g_m}{I_D}$ graph → $V_{eff} = 172\ mv$

$\therefore V_{b3} = V_{eff} + 100mv + V_{GS} = 1.2\ v$

- We added 100 mv to V_{eff} to ensure the saturation, and to increase r_0.

➢ ***Biasing:***



❖ ***Biasing V_{b1}:***

to get $V_{b1} = 2.54\ v$

$V_{DD} - V_{sg} = 2.54\ v$ → $\therefore V_{sg} = 750\ mv$

For $\frac{g_m}{I_D} = \mathbf{7}$ & L=340 nm

From $\frac{I_D}{W}\ vs\ \frac{g_m}{I_D}$ graph → w=4.6u

❖ ***Biasing V_{b2}:***

to get $V_{b2} = 2.26\ v$

$V_{DD} - V_{sg} = 2.26\ v$ → $\therefore V_{sg} = 1.04\ v$

For $\frac{g_m}{I_D} = \mathbf{3.21}$ & L=340 nm

From $\frac{I_D}{W}\ vs\ \frac{g_m}{I_D}$ graph → w=1.34u

❖ ***Biasing V_{b3}:***

to get $V_{b3} = 1.2\ v$

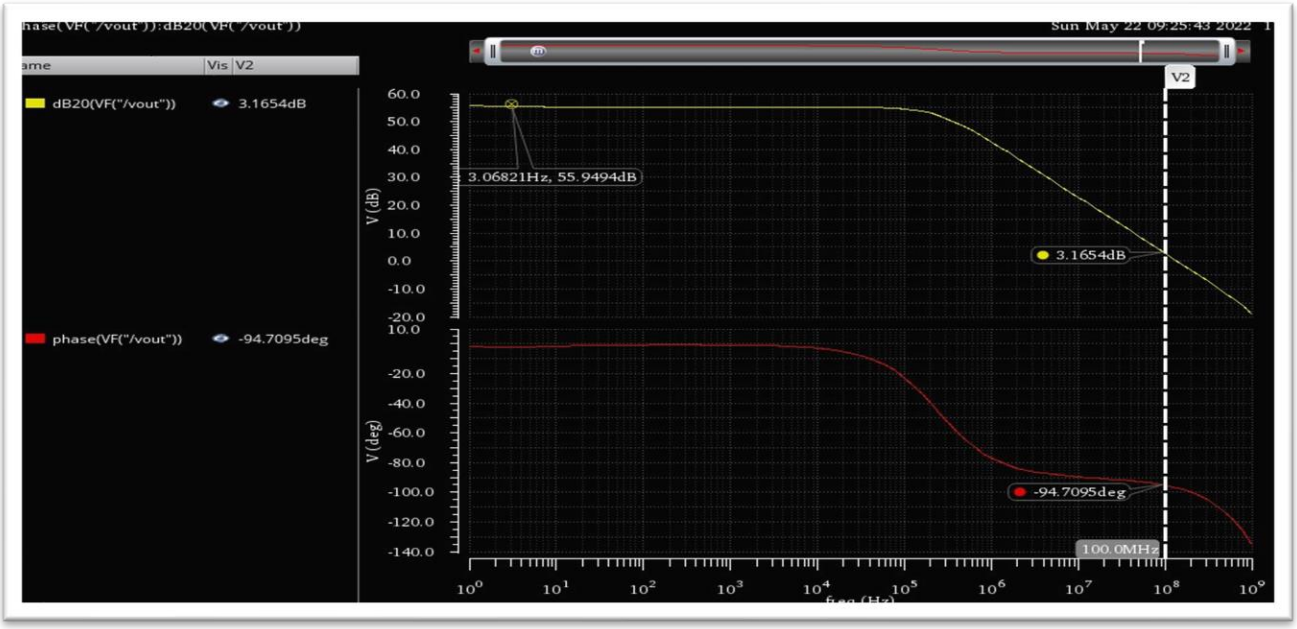
$V_{DD} - V_{sg} = 1.2\ v$ → $\therefore V_{sg} = 2.1\ v$

For $\frac{g_m}{I_D} = \mathbf{1.1267}$ & L=600 nm.

From $\frac{I_D}{W}\ vs\ \frac{g_m}{I_D}$ graph → w= 0.7 u

➢ ***Simulation results:***

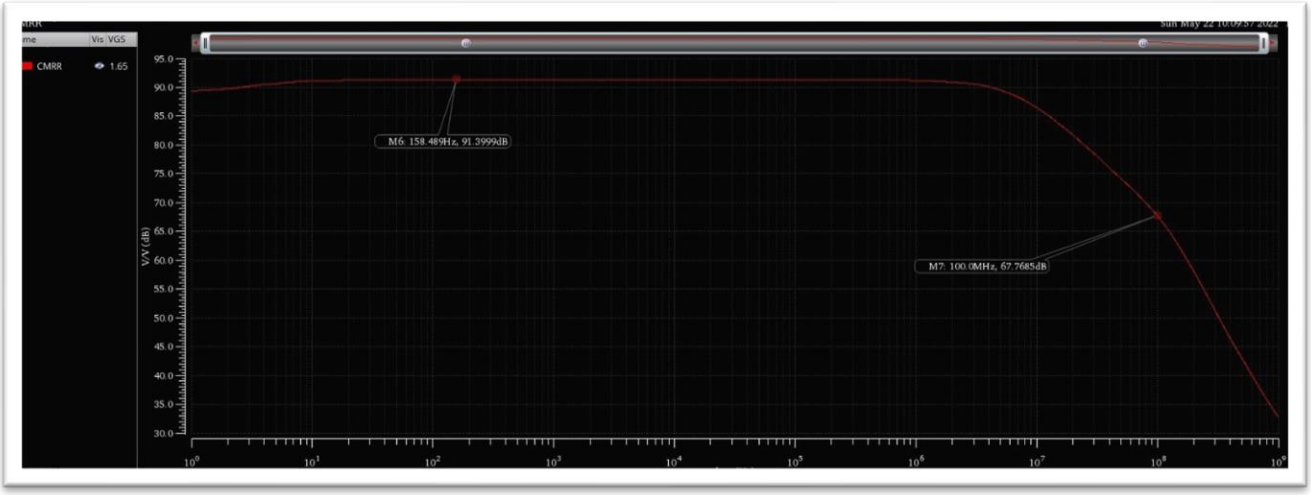
❖ ***the gain and phase versus frequency (AC)***



- ***open-loop gain and PM***
  - open loop gain $A_{DC} \approx 56\ db$
  - PM =180 – 94.7 = 85.3°

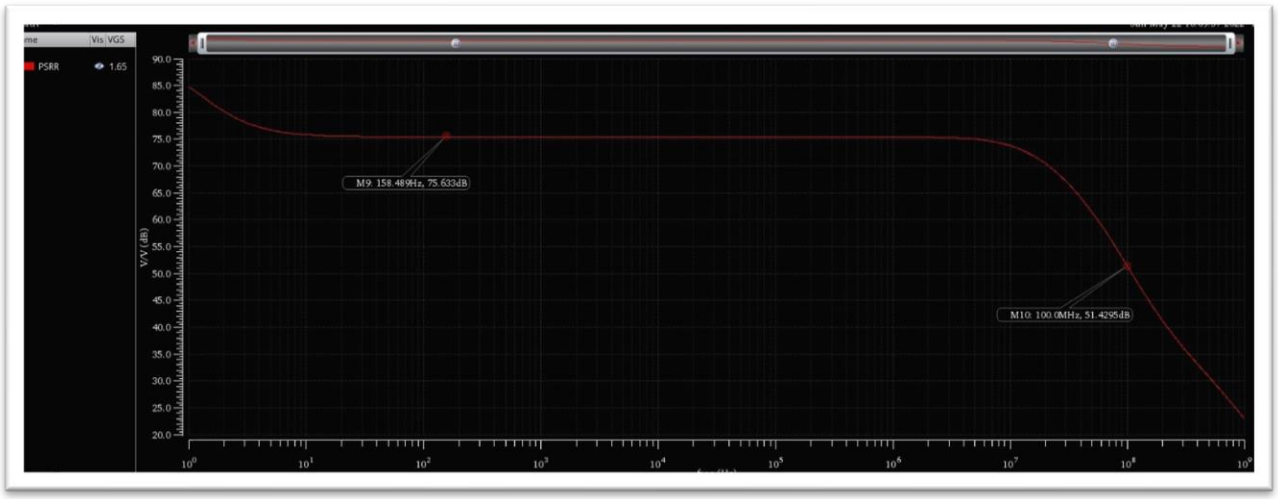
    GBW is much higher than 100 MHZ , so we achieved all specs required at this point.

❖ ***the common-mode rejection ratio (CMRR)***



- CMRR = $20 * \log\left(\frac{A_{DM}}{A_{CM}}\right)$ → from the figure we can see that CMRR is high enough.

❖ ***the power supply rejection ratio (PSRR):***

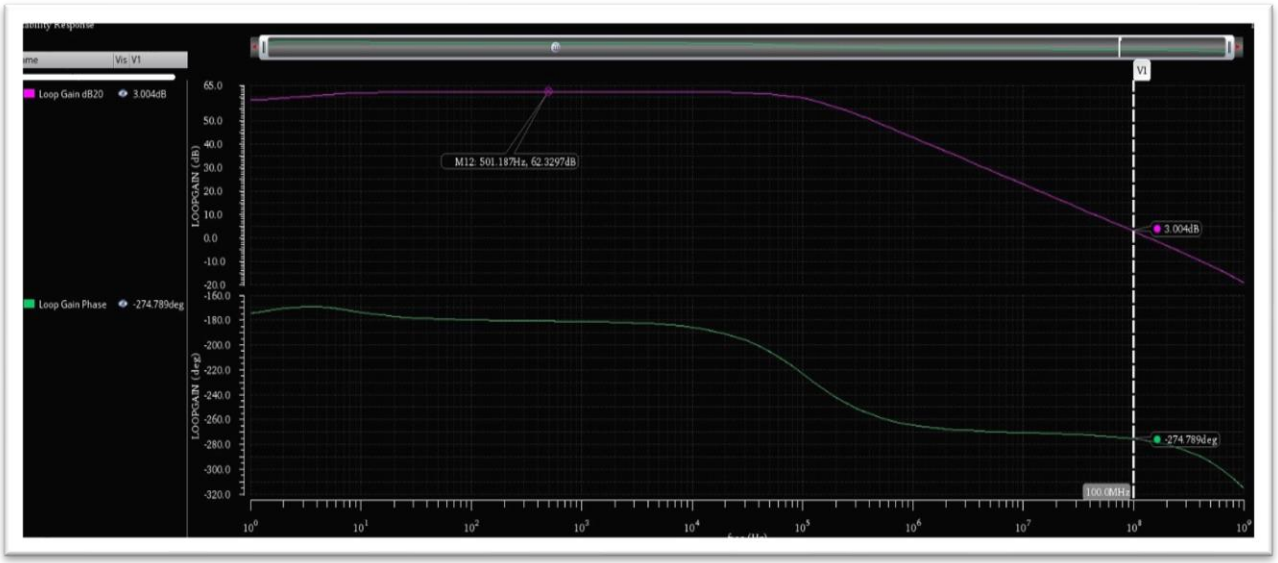


- power supply rejection ratio is high as we can see from the figure so the variations in power supply are not of significant effect.

➢ ***the op-amp in a unity feedback (Buffer) configuration:***

❖ ***stability using STB analysis and IPROBE:***

- ***STB gain and phase versus frequency (AC):***



-We can see that the gain is slighty different from the open loop gain as the biasing of the circuit has changed and also the output now is seeing the input capacitance of the op-amp in addition to CL , but still achieving the specs (gain & GBW & PM).

-the PM had slightly changed also due to loading effect of $C_{in}$and changingR_{out} .

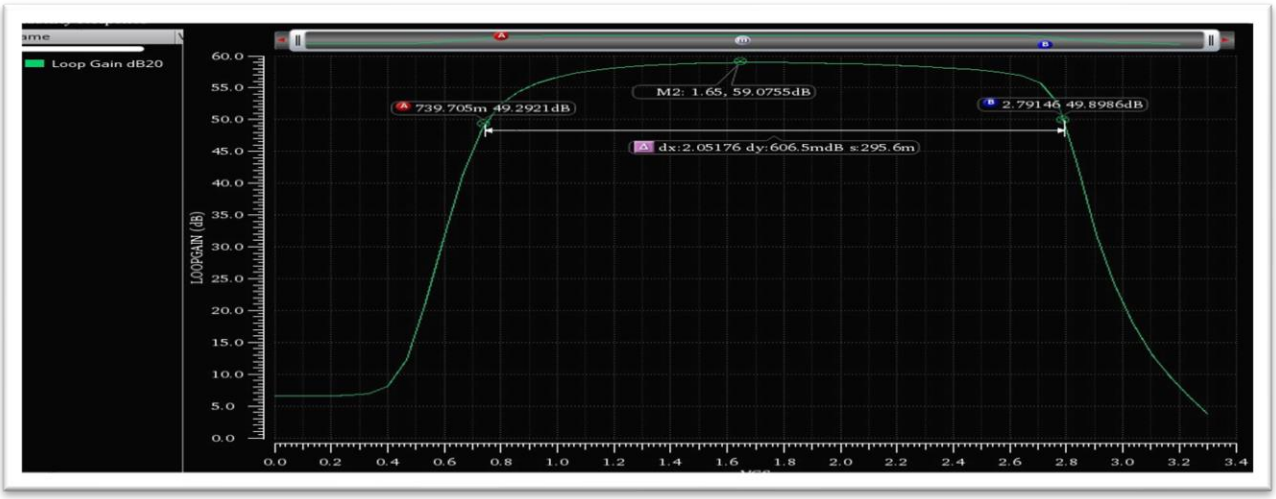
❖ *calculate open-loop gain and PM*

- open loop gain $A_{DC} \approx 62.3\ db$
- pm = 83.21°
- from stability summary we can see that the GM is equal to ∞ as the op-amp has been approximated to single pole so the phase never achieve -180° , and as the PM is very high it seems that we don't have to care about stability issues.

❖ *the difference between those results and previous open-loop AC results*

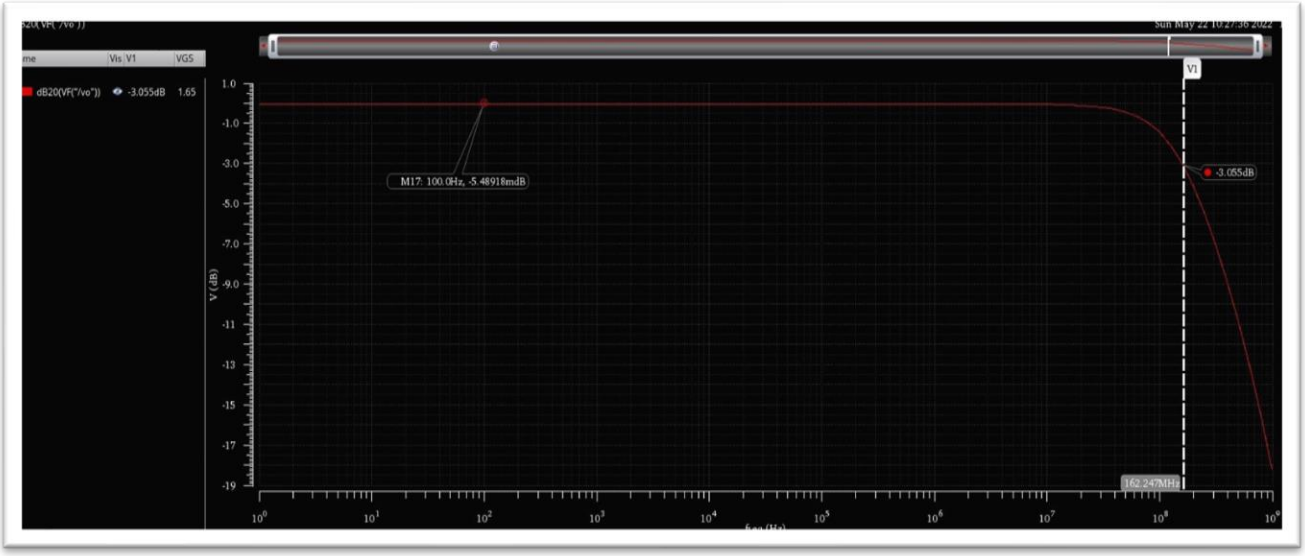
	open loop gain A_{DC}	phase margin PM
STB Analysis	$62.3\ db$	83.21°
Previous open-loop AC results	56 db	85.3°

❖ *the DC-gain versus Vout:*



-We see from the graph that o/p Swing≈ 2 , which is much larger than required.

❖ ***closed-loop (CL) frequency response:***



- Closed Loop gain $A_{cl} \approx 0\ db$
- Closed loop Bandwidth BW_{cl} = 162.24 MHz

- ***comment:*** we can notice from these results that BW_{cl} value is much greater than BW_{ol}, it's almost near to GBW and this makes sense as the op-amp is supposed to work as a buffer so the gain is equal to 0 dB

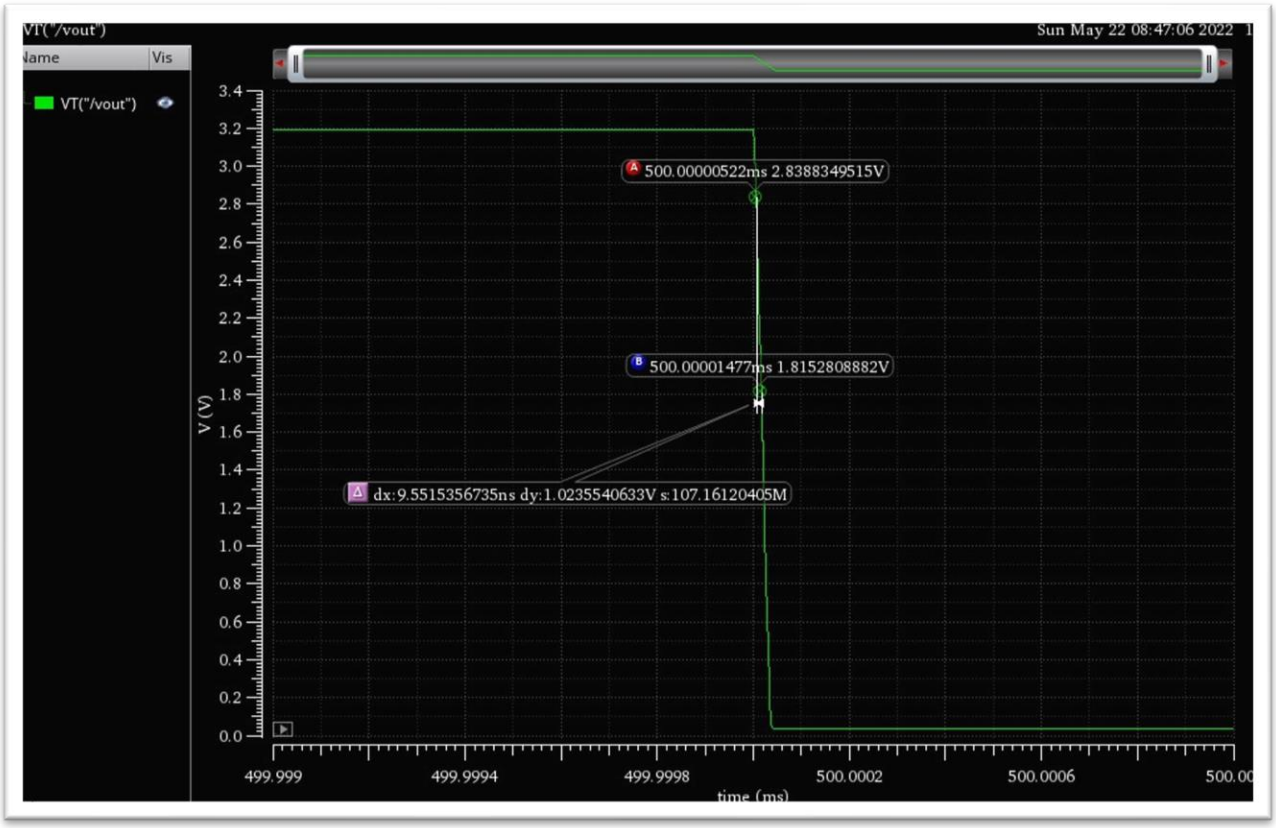
❖ ***input-referred noise and tabulate top 4 contributors @10MHz***

```
/I2/NM5     fn        4.10912e-09          20.42
/I2/NM4     fn        4.10318e-09          20.36
/I2/NM5     id        3.10839e-09          11.68
/I2/NM4     id        3.09194e-09          11.56

Spot Noise Summary (in V/sqrt(Hz)) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 9.09353e-09
Total Input Referred Noise = 9.1101e-09
The above noise summary info is for noise data
```

- We can see that the first 4 contributors we have 2 thermal contributors only which seems very good as the thermal noise with low percentage in total input referred noise .
- We also see that the total input referred noise <10$nv/\sqrt{Hz}$ which achieving the spec not only thermal noise but also total input referred noise .

❖ ***<u>the slew rate</u>***:

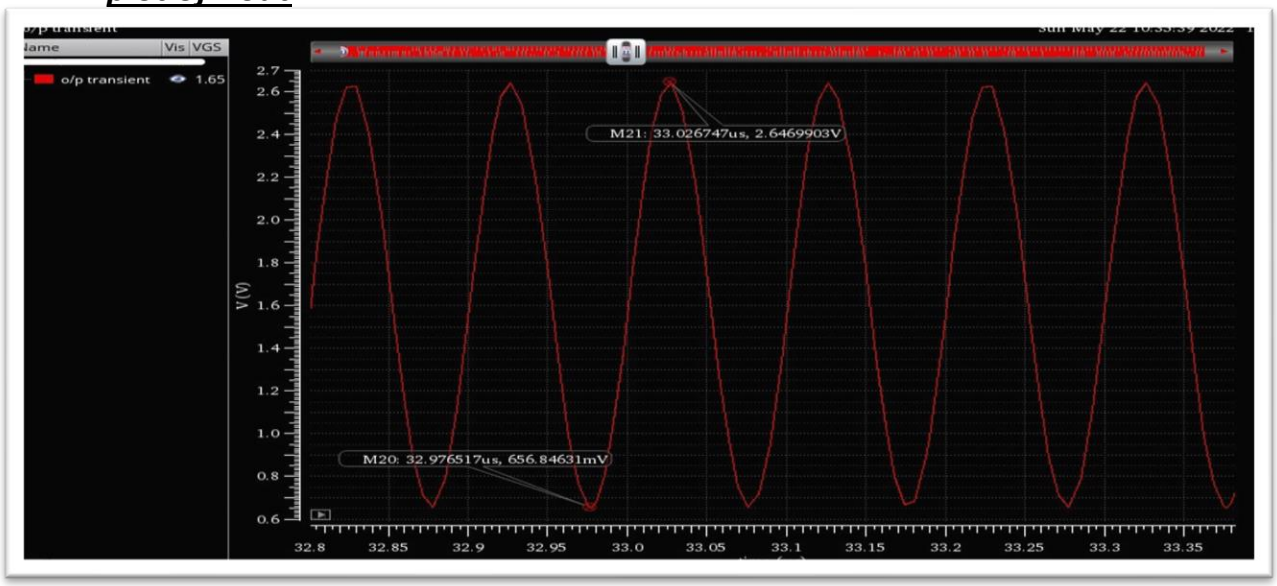


- ***<u>verifying the specifications:</u>***

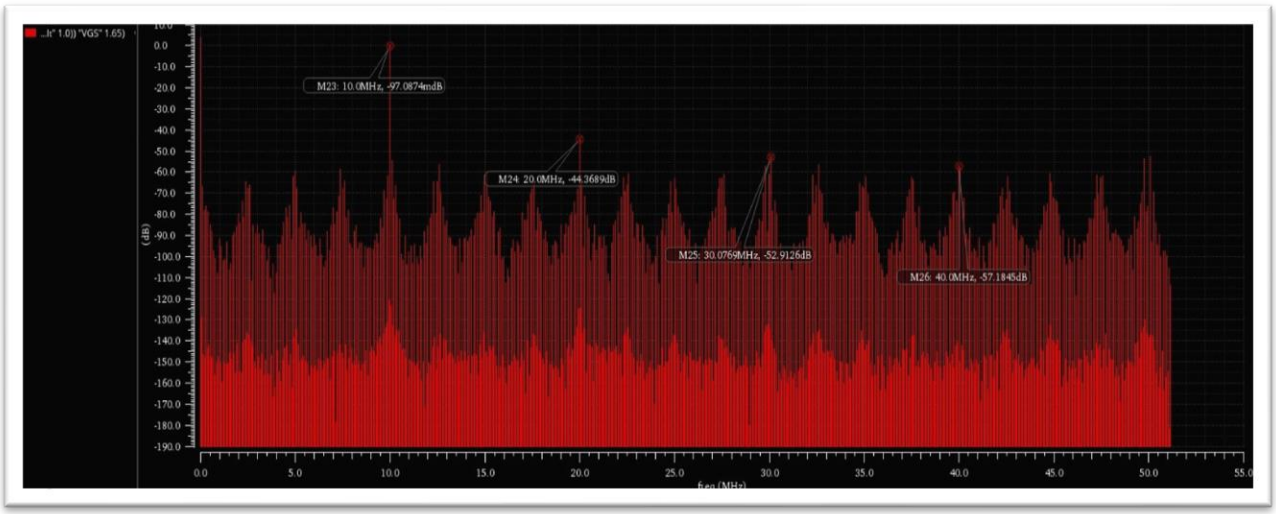
  - slew rate = $\frac{dy}{dx} = \frac{1.0255}{0.0095515\mu s} = 107.36\,\frac{v}{\mu s}$
  - slew rate >$100\,\frac{v}{\mu s}$
  - The design Acheives this specification.

❖ ***Applying a sine input signal of 1Vpp @ 10 MHz:***

- ***plot of Vout***



- ***Plot of DFT (in dB):***



- ***calculation of harmonic distortion:***

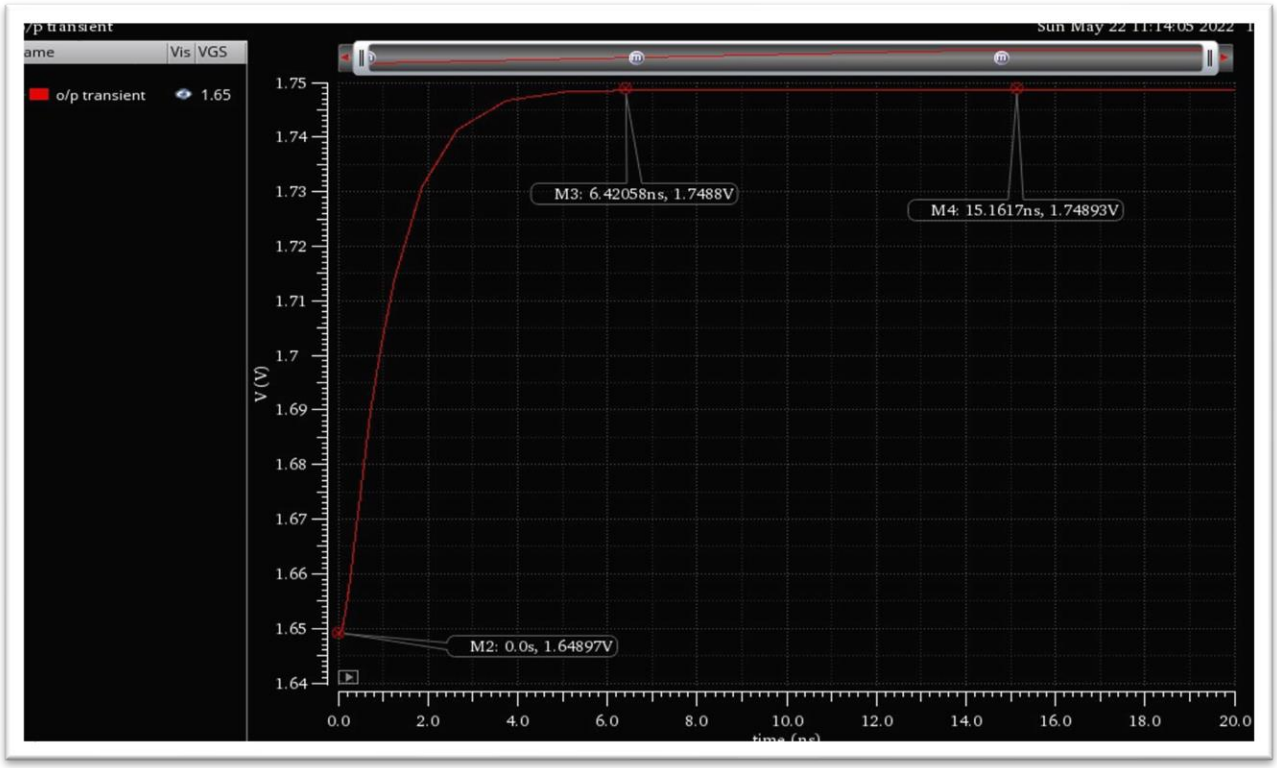
→ HD2 = -44.3689 - (-0.097) = -44.2719

→ HD3 = -52.9126 - (-0.097) = -52.8156

→ THD = 0.9792

- comment: the value of THD is very small so that the output signal will not suffer from the distortion.

❖ ***Plot of Vout for a small step input of 100mV:***



- ***Calculate the fractional gain error (FGE) and 1% settling time:***

  - FGE $= \frac{Ideal\ gain - actual\ gain}{ideal\ gain} = \frac{1-(\frac{1.74893-1.64897}{0.1})}{1} = 0.0004$
  - 1% settling time $T_S = 6.42\ ns$

- ***Comparing the results with hand analysis:***

  - FGE $= \frac{Ideal\ gain - actual\ gain}{ideal\ gain} = \frac{1-(\frac{A_0}{1+A_0})}{1} = 0.00016$
    as $A_0 = 56dB = 630v/v$.
  - settling time $T_S = \frac{4}{\mathrm{BW_{CL}} * 2\pi} = 3.92\ ns$.
  - Note that results from simulation and hand analysis are very close.

➢ conclusion:

- using $\frac{gm}{ID}$ methodology makes the design easier and more accurate than the square law model.
- We had to care about all design trade offs together when starting the design to avoid achieving some specs and lose others.
- Using slight more current than that is the minimum amount to achieve required slew rate is such a good choice to avoid slewing due to errors in some calculations or undesired behavior of some parts of the circuit.
- The gain trade off wasn't the challenging spec as even we use theL_{min} it gives high gmr_o , the challenging specs was the slew rate, GBW and o/p swing.
- Beside the major specs of the design we had to care about some minor tricks as biasing the transistors in CM deep in sat. to have high r_o to reduce variation in current due to changing the v_{out} .
- Note : We have changed our all design another time as after we designed the circuit it didn't achieve the slew rate spec although we chose relatively high I_{ss} , but it seems the mistake we did that we assumed I_2 significantly low , about 0.1 from I_{ss} in order to minimize the power consumption and increase the gain , but reducing the current to this value forced us to choose high W&L for many transistor to achieve the desired behavior for those transistors , this largened cgg which became parallel to C_L so it has degraded the slew rate and even with the attempt to increase I_{ss} it hasn't a very good effect to improve the slew rate as the output capacitance already became very high , so the only is to reassume the current to have reasonable capacitances that don't largens the output capacitance much , to can achieve the required slew rate without affecting the another specs , however , increasing I_2 reduced the gain as expected as it was (73 dB) , but it still achieving the requirements but we have improved the PM more than the previous design also the output swing , so these are many trade offs between those specs and the current and it makes sense that if you tried to improve on spec you degrade another one but trying to still achieving the specs .