RISC-V Pipeline Hazard Architecture (STA & Synthesis)

Name: Khaled Mahoud Taher Fathallah Mohamed Elkorany

Track: Digital IC Design New Capital

Number: 12

Run Script

```
set design_name "Top"
file mkdir ../${design_name}
file mkdir ../${design_name}/outputs/
file mkdir ../${design_name}/reports/
analyze -library WORK -format verilog "../src/${design_name}.v"
elaborate ${design_name} -library WORK
link
source ../cons/const.tcl
write -f ddc -hierarchy -output ../${design_name}/outputs/unmapped_${design_name}.ddc
compile_ultra -exact_map
report_area > ../${design_name}/reports/synth_area.rpt
report_cell > ../${design_name}/reports/synth_cells.rpt
report_qor  > ../${design_name}/reports/synth_qor.rpt
report_resources > ../${design_name}/reports/synth_resources.rpt
report_timing -max_paths 10 > ../${design_name}/reports/synth_timing.rpt
report_qor > ../${design_name}/reports/synth_qor.rpt
write_sdc  ../${design_name}/outputs/${design_name}.sdc
define_name_rules  no_case -case_insensitive
change_names -rule no_case -hierarchy
change_names -rule verilog -hierarchy
set verilogout_no_tri    true
set verilogout_equation  false
write -f ddc -hierarchy -output ../${design_name}/outputs/${design_name}.ddc
write_sdf "../${design_name}/outputs/${design_name}.sdf"
write -hierarchy -format verilog -output ../${design_name}/outputs/syn_${design_name}.v
```

Constrain File

```
set_max_delay .1 -from [all_inputs] -to [all_outputs]
create_clock -name clk -period 1.6 [get_ports clk]
set_clock_uncertainty 0.1 [get_clocks ]
set_input_delay -max 0.05 -clock [get_clocks clk] [remove_from_collection [all_inputs] [get_ports clk]]
set_output_delay -max 0.1 -clock clk [all_outputs]
```

Setup File

```
set library_name "NangateOpenCellLibrary_ss0p95vn40c"
set search_path "/home/IC/Desktop/khaled_taher/library"
set link_library  "* /home/IC/Desktop/khaled_taher/library/${library_name}.db"
set target_library  "/home/IC/Desktop/khaled_taher/library/${library_name}.db"

```

Time Report

```
16
17  Startpoint: DataPath_inst/ff_m2w_instance/RdW_reg[0]
18              (rising edge-triggered flip-flop clocked by clk)
19  Endpoint: DataPath_inst/Register_File_instance/rom_reg[19][0]
20            (rising edge-triggered flip-flop clocked by clk')
21  Path Group: clk
22  Path Type: max
23
24  Des/Clust/Port     Wire Load Model       Library
25  ------------------------------------------------
26  Top                5K_hvratio_1_1        NangateOpenCellLibrary_ss0p95vn40c
27
28  Point                                                   Incr       Path
29  ---------------------------------------------------------------------------
30  clock clk (rise edge)                                   0.00       0.00
31  clock network delay (ideal)                             0.00       0.00
32  DataPath_inst/ff_m2w_instance/RdW_reg[0]/CK (DFF_X1)
33                                                          0.00       0.00 r
34  DataPath_inst/ff_m2w_instance/RdW_reg[0]/Q (DFF_X1)     0.09       0.09 r
35  DataPath_inst/Register_File_instance/Addr3[0] (Register_File)
36                                                          0.00       0.09 r
37  DataPath_inst/Register_File_instance/U310/Z (BUF_X1)
38                                                          0.04       0.13 r
39  DataPath_inst/Register_File_instance/U2126/ZN (NAND3_X1)
40                                                          0.05       0.19 f
41  DataPath_inst/Register_File_instance/U302/ZN (OR2_X1)
42                                                          0.08       0.26 f
43  DataPath_inst/Register_File_instance/U164/ZN (INV_X1)
44                                                          0.08       0.34 r
45  DataPath_inst/Register_File_instance/U2141/ZN (AOI22_X1)
46                                                          0.05       0.40 f
47  DataPath_inst/Register_File_instance/U612/ZN (NAND3_X1)
48                                                          0.03       0.43 r
49  DataPath_inst/Register_File_instance/U526/ZN (NOR2_X1)
50                                                          0.02       0.45 f
51  DataPath_inst/Register_File_instance/U524/ZN (AND3_X1)
52                                                          0.04       0.49 f
53  DataPath_inst/Register_File_instance/U611/ZN (NAND2_X1)
54                                                          0.02       0.51 r
55  DataPath_inst/Register_File_instance/U273/ZN (AOI22_X1)
56                                                          0.03       0.54 f
57  DataPath_inst/Register_File_instance/U436/Z (BUF_X2)
58                                                          0.06       0.61 f
59  DataPath_inst/Register_File_instance/U2165/ZN (AOI22_X1)
60                                                          0.05       0.65 r
61  DataPath_inst/Register_File_instance/rom_reg[19][0]/D (DFF_X2)
62                                                          0.01       0.66 r
63  data arrival time                                                      0.66
64
65  clock clk' (rise edge)                                  0.80       0.80
66  clock network delay (ideal)                             0.00       0.80
67  clock uncertainty                                      -0.10       0.70
68  DataPath_inst/Register_File_instance/rom_reg[19][0]/CK (DFF_X2)
69                                                          0.00       0.70 r
70  library setup time                                     -0.04       0.66
71  data required time                                                     0.66
72  ---------------------------------------------------------------------------
73  data required time                                                     0.66
74  data arrival time                                                     -0.66
75  ---------------------------------------------------------------------------
76  slack (MET)                                                            0.00
77
```

Area Report

```
****************************************
Report : area
Design : Top
Version: K-2015.06
Date   : Wed Oct  4 20:26:20 2023
****************************************

Library(s) Used:

    NangateOpenCellLibrary_ss0p95vn40c (File: /home/IC/Desktop/khaled_taher/library/NangateOpenCellLibrary_ss0p95vn40c.db)

Number of ports:                          276
Number of nets:                          8470
Number of cells:                         7333
Number of combinational cells:           5796
Number of sequential cells:              1536
Number of macros/black boxes:               0
Number of buf/inv:                        842
Number of references:                      39

Combinational area:               6568.072115
Buf/Inv area:                      564.984001
Noncombinational area:            6947.919748
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                 13515.991863
Total area:                 undefined
1
dc_shell>
```

Power Reoprt

```
Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =   3.5706 mW   (69%)
  Net Switching Power  =   1.6197 mW   (31%)
                         ---------
Total Dynamic Power    =   5.1903 mW  (100%)

Cell Leakage Power     =  66.1635 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      5.1929        1.0616e+03           22.2033         1.0668e+03  (  20.29%)
register       3.2016e+03           70.7734         2.5558e+04         3.2979e+03  (  62.74%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational    363.8040          487.3552         4.0583e+04           891.7450  (  16.96%)
--------------------------------------------------------------------------------------------------
Total          3.5706e+03 uW     1.6197e+03 uW     6.6164e+04 nW     5.2565e+03 uW
1
dc_shell>
```

Qor Report

```
48  ----------------------------------
49  Cell Area:              13515.991863
50  Design Area:            13515.991863
51
52
53  Design Rules
54  ----------------------------------
55  Total Number of Nets:          8357
56  Nets With Violations:             0
57  Max Trans Violations:             0
58  Max Cap Violations:               0
59  ----------------------------------
60
61
62  Hostname: IC
63
64  Compile CPU Statistics
65  ----------------------------------------
66  Resource Sharing:                   0.96
67  Logic Optimization:                 5.14
68  Mapping Optimization:              62.37
69  ----------------------------------------
70  Overall Compile Time:              85.15
71  Overall Compile Wall Clock Time:   86.37
72
73  --------------------------------------------------------------------
74
75  Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0
76
77
78  Design (Hold)  WNS: 0.02  TNS: 5.63  Number of Violating Paths: 916
79
80  --------------------------------------------------------------------
81
82
```