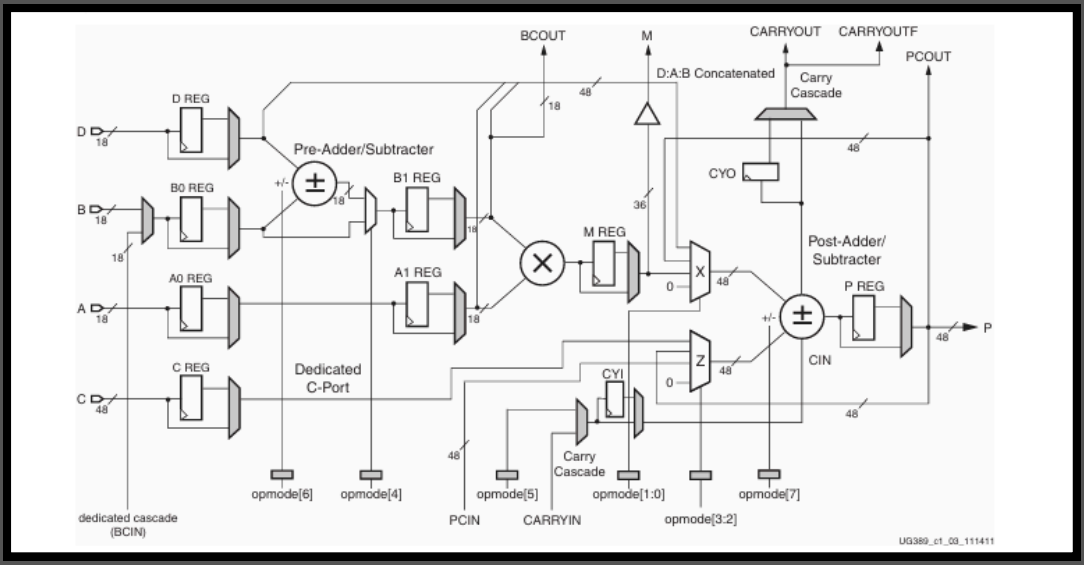
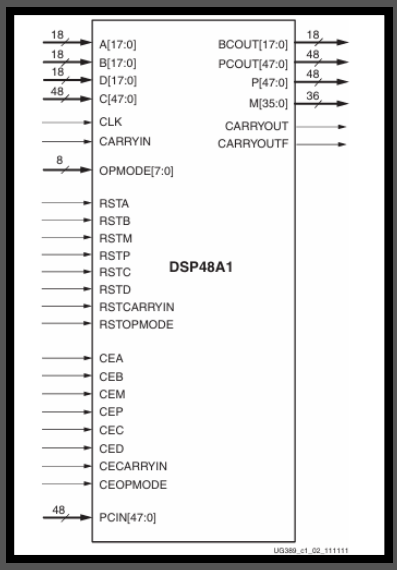
Spartan6_DSP48A1_Project





Name: Khaled Ali Elsayed Ali

Spartan6 - DSP48A1

- **Code:**

```
module DSP(A, B, C, D, CARRYIN, M, P, CARRYOUT, CARRYOUTF, CLK, OPMODE, BCIN,
CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP, RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP, BCOUT, PCIN, PCOUT);
localparam SYNC = 0, ASYNC = 1, OPMODE5 = 0, CARRYIn = 1, CASCODE = 1, DIRECT = 0;
parameter A0REG = 0, A1REG = 1, B0REG = 0, B1REG = 1;
parameter CREG = 1, DREG = 1, MREG = 1, PREG = 1, CARRYINREG = 1, CARRYOUTREG = 1, OPMODEREG = 1;
parameter CARRYINSEL = OPMODE5;
parameter B_INPUT = DIRECT;
parameter RSTTYPE = SYNC;
parameter A_WIDTH = 18, B_WIDTH = 18, C_WIDTH = 48, D_WIDTH = 12, M_WIDTH = 36, P_WIDTH = 48, OPMODE_WIDTH = 8;
input [17:0] A, B, BCIN;
input [11:0] D;
input [47:0] C, PCIN;
input CARRYIN, CLK, CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP;
input RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP;
input [7:0] OPMODE;
output [35:0] M;
output [47:0] P, PCOUT;
output CARRYOUT, CARRYOUTF;
output [17:0] BCOUT;
wire [7:0] OPMODE_out;
wire [17:0] A_mux_out, B_mux_out, MUX0B_out;
wire [11:0] D_mux_out;
wire [47:0] C_mux_out, X_mux_out, Z_mux_out, PRE_ADDER_SUB_2;
wire [17:0] PRE_ADDER_SUB_1, MUX_OP4, MULTI_1, MULTI_2;
wire [35:0] MULTI;
wire [47:0] M_ex;
wire Carry_Cascode_in, CIN, Carry_Cascode_out;
REG_MUX #(OPMODE_WIDTH,RSTTYPE,OPMODEREG) x0 (OPMODE, CLK, RSTOPMODE, CEOPMODE, OPMODE_out);
REG_MUX #(D_WIDTH,RSTTYPE,DREG) x1 (D, CLK, RSTD, CED, D_mux_out);
REG_MUX #(A_WIDTH,RSTTYPE,A0REG) x2 (A, CLK, RSTA, CEA, A_mux_out);
REG_MUX #(C_WIDTH,RSTTYPE,CREG) x3 (C, CLK, RSTC, CEC, C_mux_out);
assign MUX0B_out = (B_INPUT == DIRECT)? B : (B_INPUT == CASCODE)? BCIN : 0;
REG_MUX #(B_WIDTH,RSTTYPE,B0REG) x5 (MUX0B_out, CLK, RSTB, CEB, B_mux_out);
assign PRE_ADDER_SUB_1 = (OPMODE_out[6])? D_mux_out-B_mux_out : D_mux_out+B_mux_out;
assign MUX_OP4 = (OPMODE_out[4])? PRE_ADDER_SUB_1 : B_mux_out;
REG_MUX #(B_WIDTH,RSTTYPE,B1REG) x6 (MUX_OP4, CLK, RSTB, CEB, MULTI_1);
REG_MUX #(A_WIDTH,RSTTYPE,A1REG) x7 (A_mux_out, CLK, RSTA, CEA, MULTI_2);
assign BCOUT = MULTI_1;
assign MULTI = MULTI_1 * MULTI_2;
REG_MUX #(M_WIDTH,RSTTYPE,MREG) x8 (MULTI, CLK, RSTM, CEM, M);
assign Carry_Cascode_in = (CARRYINSEL==OPMODE5)? OPMODE_out[5] : (CARRYINSEL==CARRYIn)? CARRYIN : 0;
REG_MUX #(1,RSTTYPE,CARRYINREG) x9 (Carry_Cascode_in, CLK, RSTCARRYIN, CECARRYIN, CIN);
assign M_ex = {{12{1'b0}},M};
assign X_mux_out = (OPMODE_out[1:0]==3)? {D,A,B} : (OPMODE_out[1:0]==2)? P : (OPMODE_out[1:0]==1)? M_ex : 0;
assign Z_mux_out = (OPMODE_out[3:2]==3)? C_mux_out : (OPMODE_out[3:2]==2)? P : (OPMODE_out[3:2]==1)? PCIN : 0;
assign {Carry_Cascode_out,PRE_ADDER_SUB_2} = (OPMODE_out[7]==0)? (X_mux_out + Z_mux_out + CIN) : (Z_mux_out-(X_mux_out+CIN));
REG_MUX #(1,RSTTYPE,CARRYOUTREG) x10 (Carry_Cascode_out, CLK, RSTCARRYIN, CECARRYIN, CARRYOUT);
REG_MUX #(P_WIDTH,RSTTYPE,PREG) x11 (PRE_ADDER_SUB_2, CLK, RSTP, CEP, P);
assign CARRYOUTF = CARRYOUT;
assign PCOUT = P;
endmodule
```

```
module REG_MUX(in, CLK, RST, CE, out);
localparam SYNC = 0, ASYNC = 1;
parameter WIDTH = 18;
parameter RSTTYPE = SYNC, REG = 1;
input CLK, RST, CE;
input [WIDTH-1:0] in;
reg [WIDTH-1:0] in_reg;
output reg [WIDTH-1:0] out;
generate
    if(RSTTYPE==SYNC)begin
always @(posedge CLK) begin
    if(RST)
    in_reg<=0;
    else begin
    if(CE)
    in_reg<=in;
    end
end
always@(*)begin
    case(REG)
    1: out=in_reg;
    default:out=in;
    endcase
end
    end
```

```
    if(RSTTYPE==ASYNC)begin
always @(posedge CLK or posedge RST) begin
    if(RST)
    in_reg<=0;
    else begin
    if(CE)
    in_reg<=in;
    end
end
always@(*)begin
    case(REG)
    1:out=in_reg;
    default:out=in;
    endcase
end
    end
endgenerate
endmodule
```

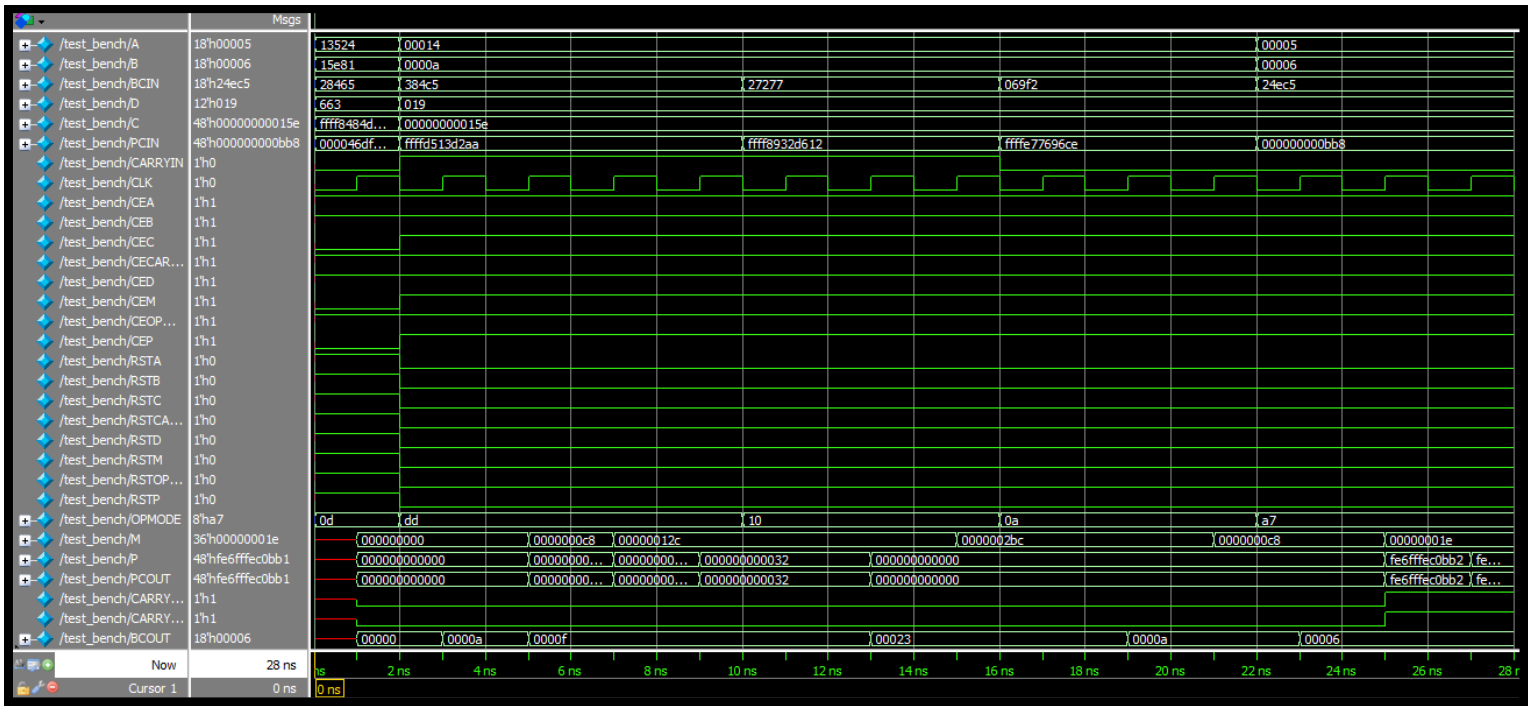
Spartan6 - DSP48A1

- **Code test_bench:**

```
module test_bench();
reg [17:0] A, B, BCIN;
reg [11:0] D;
reg [47:0] C, PCIN;
reg CARRYIN, CLK, CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP;
reg RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP;
reg [7:0] OPMODE;
wire [35:0] M;
wire [47:0] P, PCOUT;
wire CARRYOUT, CARRYOUTF;
wire [17:0] BCOUT;
DSP48A1 x1(A, B, C, D, CARRYIN, M, P, CARRYOUT, CARRYOUTF, CLK, OPMODE, BCIN,
CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP, RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP, BCOUT, PCIN, PCOUT);
initial begin
    CLK=0;
    forever begin
        #1CLK=~CLK;
    end
end
initial begin
    RSTA = 1;
    RSTB = 1;
    RSTC = 1;
    RSTCARRYIN = 1;
    RSTD = 1;
    RSTM = 1 ;
    RSTOPMODE = 1;
    RSTP = 1;
    A = $random;
    B = $random;
    C = $random;
    D = $random;
    OPMODE = $random;
    PCIN = $random;
    BCIN = $random;
    CARRYIN = $random;
    CEA = $random;
    CEB = $random;
    CEC = $random;
    CECARRYIN = $random;
    CED = $random;
    CEM = $random;
    CEOPMODE = $random;
    CEP = $random;
    @(negedge CLK);
    if(M!=0 || P!=0 || PCOUT!=0 || CARRYOUT!=0 || CARRYOUTF!=0 || BCOUT!=0)begin
        $display("Error");
        $stop;
    end
    RSTA = 0;
    RSTB = 0;
    RSTC = 0;
    RSTCARRYIN = 0;
    RSTD = 0;
    RSTM = 0 ;
    RSTOPMODE = 0;
    RSTP = 0;
    CEA = 1;
    CEB = 1;
    CEC = 1;
    CECARRYIN = 1;
    CED = 1;
    CEM = 1;
    CEOPMODE = 1;
    CEP = 1;

    OPMODE = 8'b11011101;
    A = 20;
    B = 10;
    C = 350;
    D = 25;
    BCIN = $random;
    PCIN = $random;
    CARRYIN = $random;
    repeat(4)@(negedge CLK);
    if(BCOUT!=18'hf || M!=36'h12c || PCOUT!=48'h32 || P!=48'h32 || CARRYOUTF!=0 || CARRYOUT!=0)begin
        $display("Error");
        $stop;
    end


    OPMODE = 8'b00010000;
    A = 20;
    B = 10;
    C = 350;
    D = 25;
    BCIN = $random;
    PCIN = $random;
    CARRYIN = $random;
    repeat(3)@(negedge CLK);
    if(BCOUT!=18'h23 || M!=36'h2bc || PCOUT!=48'h0 || P!=48'h0 || CARRYOUTF!=0 || CARRYOUT!=0)begin
        $display("Error");
        $stop;
    end

    OPMODE = 8'b00001010;
    A = 20;
    B = 10;
    C = 350;
    D = 25;
    BCIN = $random;
    PCIN = $random;
    CARRYIN = $random;
    repeat(3)@(negedge CLK);
    if(BCOUT!=18'ha || M!=36'hc8 || PCOUT!=48'h0 || P!=48'h0 || CARRYOUTF!=0 || CARRYOUT!=0)begin
        $display("Error");
        $stop;
    end

    OPMODE = 8'b10100111;
    A = 5;
    B = 6;
    C = 350;
    D = 25;
    BCIN = $random;
    PCIN = 3000;
    CARRYIN = $random;
    repeat(3)@(negedge CLK);
    if(BCOUT!=18'h6 || M!=36'h1e || PCOUT!=48'hfe6fffec0bb1 || P!=48'hfe6fffec0bb1 || CARRYOUTF!=1 || CARRYOUT!=1)begin
        $display("Error");
        $stop;
    end

    $stop;
end
endmodule
```

Spartan6 - DSP48A1

- **Waveform:**




```
104         repeat(3)@(negedge CLK);
105         if(BCOUT!=18'ha || M!=36'hc8 || PCOUT!=48'h0 || P!=48'h0 || CARRYOUTF!=0 || CARRYOUT!=0)begin
106             $display("Error");
107             $stop;
108         end
109
110         OPMODE = 8'b10100111;
111         A = 5;
112         B = 6;
113         C = 350;
114         D = 25;
115         BCIN = $random;
116         PCIN = 3000;
117         CARRYIN = $random;
118         repeat(3)@(negedge CLK);
119         if(BCOUT!=18'h6 || M!=36'hle || PCOUT!=48'hfe6fffec0bbl || P!=48'hfe6fffec0bbl || CARRYOUTF!=1 || CARRYOUT!=1)begin
120             $display("Error");
121             $stop;
122         end
123
124         $stop;
125     end
126     endmodule
```

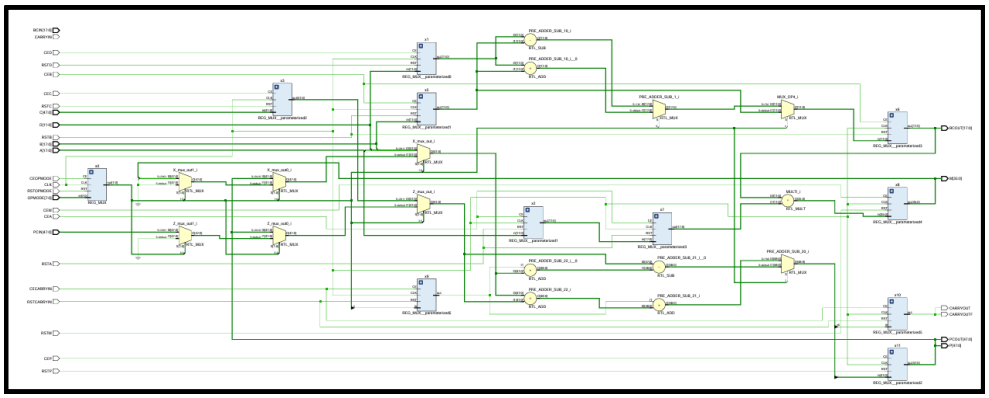
```
# ** Note: $stop    : test_bench.v(124)
#    Time: 28 ns  Iteration: 1  Instance: /test_bench
# Break in Module test_bench at test_bench.v line 124
```

```
vlib work
vlog DSP48A1.v REG_MUX.v test_bench.v
vsim -voptargs=+acc work.test_bench
add wave *
run -all
#quit -sim
```

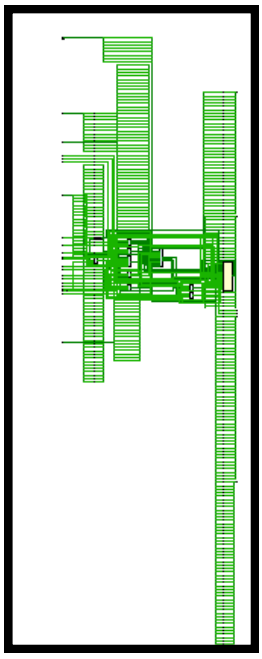
```
## Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports CLK]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports CLK]
```

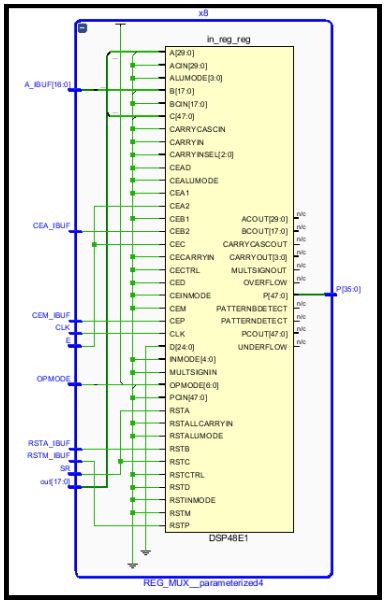
Spartan6 - DSP48A1

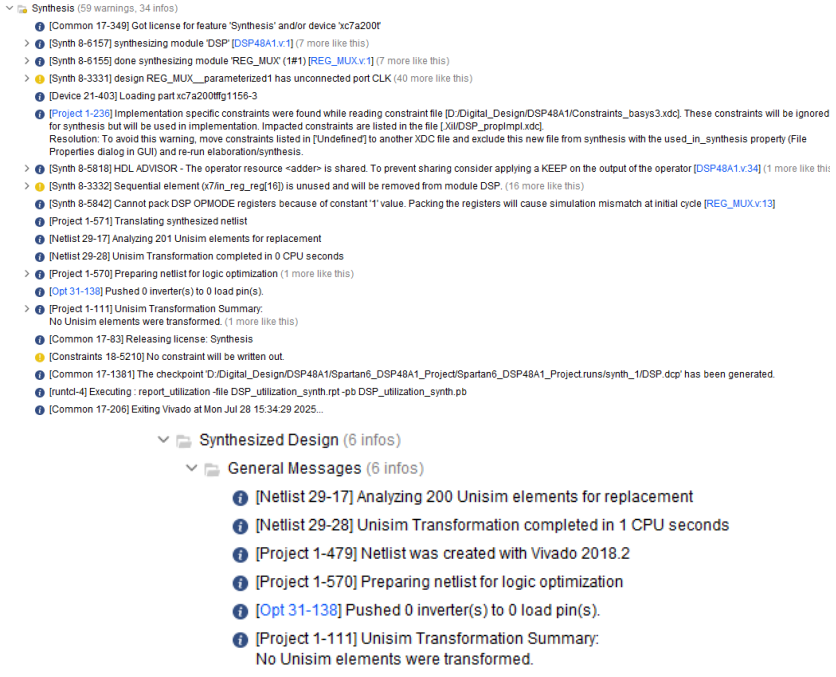
- **Vivado:**
  - **Elaboration:**



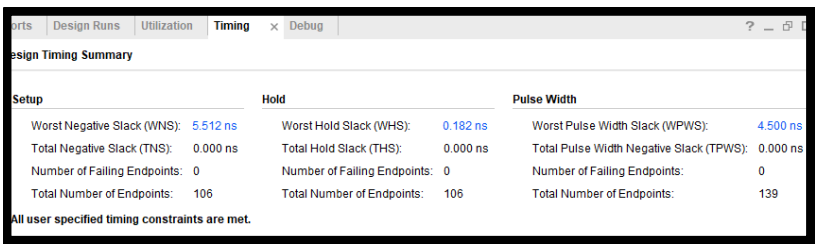
  - **Synthesis:**





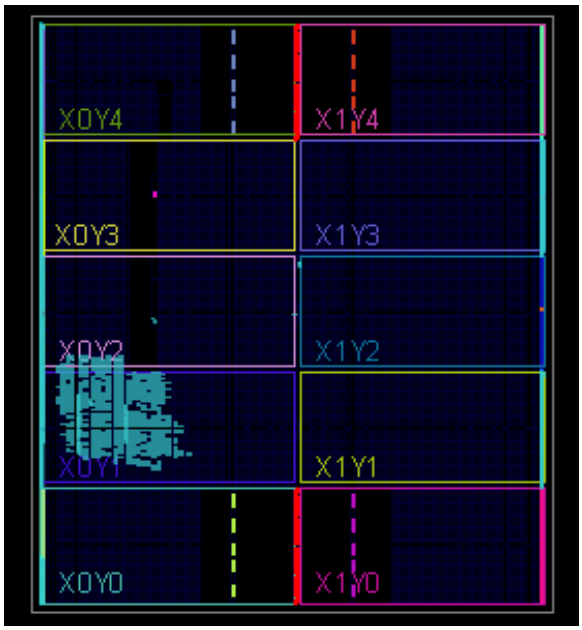


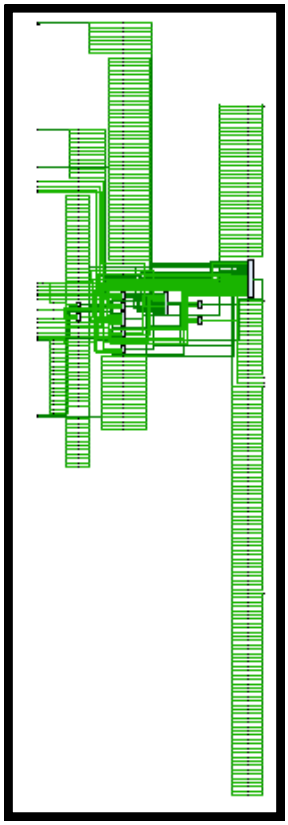
Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
N DSP	201	137	1	321	1
dbg_hub (dbg_hub_CV)	0	0	0	0	0
u_ila_0 (u_ila_0_CV)	0	0	0	0	0
x0 (REG_MUX)	200	8	0	0	0
x1 (REG_MUX__para...	12	12	0	0	0
x3 (REG_MUX__para...	0	48	0	0	0
x6 (REG_MUX__para...	0	18	0	0	0
x7 (REG_MUX__para...	0	1	0	0	0
x8 (REG_MUX__para...	0	0	1	0	0
x9 (REG_MUX__para...	2	1	0	0	0
x10 (REG_MUX__para...	0	1	0	0	0
x11 (REG_MUX__para...	0	48	0	0	0



Spartan6 - DSP48A1

- **Vivado:**
  - **Implementation:**





Name	Slice LUTs (133800)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)	LUT Flip Flop Pairs (133800)	Block RAM Tile (365)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	BSCANE2 (4)
N DSP	2663	4178	96	6	1291	2197	466	1601	8	1	321	2	1
dbg_hub (dbg_hub)	474	727	0	0	230	450	24	308	0	0	0	1	1
u_ila_0 (u_ila_0)	1988	3314	96	6	1008	1546	442	1224	8	0	0	0	0
x0 (REG_MUX)	200	8	0	0	60	200	0	0	0	0	0	0	0
x1 (REG_MUX__para...	12	12	0	0	6	12	0	0	0	0	0	0	0
x3 (REG_MUX__para...	0	48	0	0	16	0	0	0	0	0	0	0	0
x6 (REG_MUX__para...	0	18	0	0	5	0	0	0	0	0	0	0	0
x7 (REG_MUX__para...	0	1	0	0	1	0	0	0	0	0	0	0	0
x8 (REG_MUX__para...	0	0	0	0	0	0	0	0	0	1	0	0	0
x9 (REG_MUX__para...	2	1	0	0	2	2	0	1	0	0	0	0	0
x10 (REG_MUX__para...	0	1	0	0	1	0	0	0	0	0	0	0	0
x11 (REG_MUX__para...	0	48	0	0	12	0	0	0	0	0	0	0	0

Log | Reports | Design Runs | Power | DRC | Methodology | Timing

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.551 ns	Worst Hold Slack (WHS):	0.057 ns	Worst Pulse Width Slack (WPWS):	3.950 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	8023	Total Number of Endpoints:	8007	Total Number of Endpoints:	5075

All user specified timing constraints are met.

Transcript

```
# -- Compiling module DSP
#
# -- Compiling module REG_MUX
#
#
# Top level modules:
#
#           DSP
#
# End time: 16:21:22 on Jul 28,2025, Elapsed time: 0:00:00
#
# Errors: 0, Warnings: 0
#
```

Transcript

```
# vlog D:/Digital_Design/DSP48A1/DSP48A1.v -work work
#
# -- Compiling module DSP
#
#
# Top level modules:
#
#           DSP
#
# End time: 16:23:37 on Jul 28,2025, Elapsed time: 0:00:00
#
# Errors: 0, Warnings: 0
#
Visualizer>
```

Filter: Type here | Waived | Fixed | Pending | Uninspected | Bug | Verified | Total : 8 | Selected : 0

Severity	Status	Check	Alias	Message	Module	Category
	?	condition_const		Condition expression is a constant. Module DSP, File D:/Digital_Design/DSP48A1/DSP48A1.v, Line 32.	DSP	Rtl Design Style
	?	condition_const		Condition expression is a constant. Module DSP, File D:/Digital_Design/DSP48A1/DSP48A1.v, Line 41.	DSP	Rtl Design Style
	?	parameter_name_duplicate		Same parameter name is used in more than one module. Parameter ASYNC, Total count 2, First mod...	DSP	Nomenclature Style
	?	parameter_name_duplicate		Same parameter name is used in more than one module. Parameter SYNC, Total count 2, First modul...	DSP	Nomenclature Style
	?	parameter_name_duplicate		Same parameter name is used in more than one module. Parameter RSTTYPE, Total count 2, First mo...	DSP	Nomenclature Style