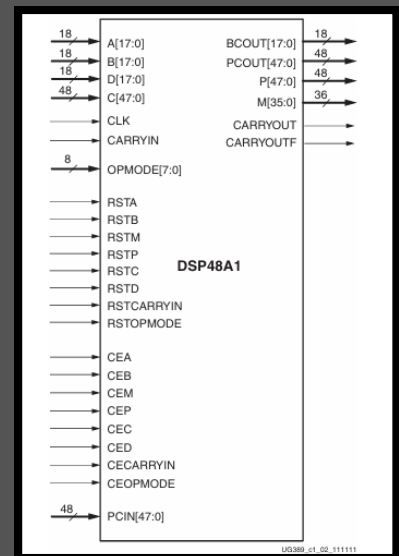
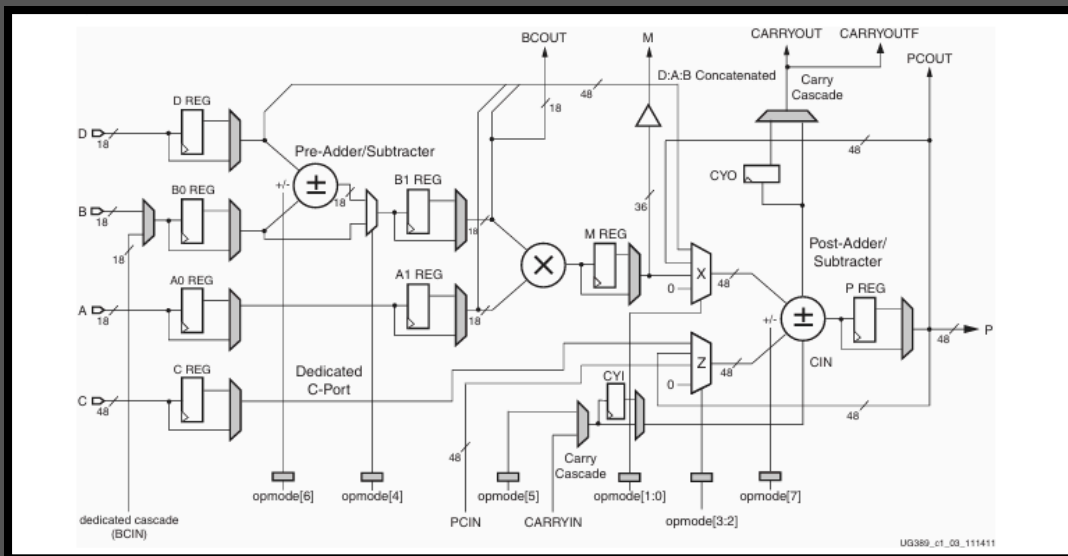




Spartan6_DSP48A1_Project



Name: Khaled Ali Elsayed Ali

Spartan6 - DSP48A1

- **Code:**

```
1 module DSP(A, B, C, D, CARRYIN, M, P, CARRYOUT, CARRYOUTF, CLK, OPMODE, BCIN,  
2 CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP, RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP, BCOUT, PCIN, PCOUT);  
3 localparam SYNC = 0, ASYNC = 1, OPMODE5 = 0, CARRYIN = 1, CASCODE = 1, DIRECT = 0;  
4 parameter A0REG = 0, A1REG = 1, B0REG = 0, B1REG = 1;  
5 parameter CREG = 1, DREG = 1, MREG = 1, PREG = 1, CARRYINREG = 1, CARRYOUTREG = 1, OPMODEREG = 1;  
6 parameter CARRYINSEL = OPMODE5;  
7 parameter B_INPUT = DIRECT;  
8 parameter RSTTYPE = SYNC;  
9 parameter A_WIDTH = 18, B_WIDTH = 18, C_WIDTH = 48, D_WIDTH = 12, M_WIDTH = 36, P_WIDTH = 48, OPMODE_WIDTH = 8;  
10 input [17:0] A, B, BCIN;  
11 input [11:0] D;  
12 input [47:0] C, PCIN;  
13 input CARRYIN, CLK, CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP;  
14 input RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP;  
15 input [7:0] OPMODE;  
16 output [35:0] M;  
17 output [47:0] P, PCOUT;  
18 output CARRYOUT, CARRYOUTF;  
19 output [17:0] BCOUT;  
20 wire [7:0] OPMODE_out;  
21 wire [17:0] A_mux_out, B_mux_out, MUX0B_out;  
22 wire [11:0] D_mux_out;  
23 wire [47:0] C_mux_out, X_mux_out, Z_mux_out, PRE_ADDER_SUB_2;  
24 wire [17:0] PRE_ADDER_SUB_1, MUX_OP4, MULTI_1, MULTI_2;  
25 wire [35:0] MULTI;  
26 wire [47:0] M_ex;  
27 wire Carry_Cascode_in, CIN, Carry_Cascode_out;  
28 REG_MUX #(OPMODE_WIDTH,RSTTYPE,OPMODEREG) x0 (OPMODE, CLK, RSTOPMODE, CEOPMODE, OPMODE_out);  
29 REG_MUX #(D_WIDTH,RSTTYPE,DREG) x1 (D, CLK, RSTD, CED, D_mux_out);  
30 REG_MUX #(A_WIDTH,RSTTYPE,A0REG) x2 (A, CLK, RSTA, CEA, A_mux_out);  
31 REG_MUX #(C_WIDTH,RSTTYPE,CREG) x3 (C, CLK, RSTC, CEC, C_mux_out);  
32 assign MUX0B_out = (B_INPUT == DIRECT)? B : (B_INPUT == CASCODE)? BCIN : 0;  
33 REG_MUX #(B_WIDTH,RSTTYPE,B0REG) x5 (MUX0B_out, CLK, RSTB, CEB, B_mux_out);  
34 assign PRE_ADDER_SUB_1 = (OPMODE_out[6])? D_mux_out-B_mux_out : D_mux_out+B_mux_out;  
35 assign MUX_OP4 = (OPMODE_out[4])? PRE_ADDER_SUB_1 : B_mux_out;  
36 REG_MUX #(B_WIDTH,RSTTYPE,B1REG) x6 (MUX_OP4, CLK, RSTB, CEB, MULTI_1);  
37 REG_MUX #(A_WIDTH,RSTTYPE,A1REG) x7 (A_mux_out, CLK, RSTA, CEA, MULTI_2);  
38 assign BCOUT = MULTI_1;  
39 assign MULTI = MULTI_1 * MULTI_2;  
40 REG_MUX #(M_WIDTH,RSTTYPE,MREG) x8 (MULTI, CLK, RSTM, CEM, M);  
41 assign Carry_Cascode_in = (CARRYINSEL==OPMODE5)? OPMODE_out[5] : (CARRYINSEL==CARRYIN)? CARRYIN : 0;  
42 REG_MUX #(1,RSTTYPE,CARRYINREG) x9 (Carry_Cascode_in, CLK, RSTCARRYIN, CECARRYIN, CIN);  
43 assign M_ex = {{12{1'b0}},M};  
44 assign X_mux_out = (OPMODE_out[1:0]==3)? {D,A,B} : (OPMODE_out[1:0]==2)? P : (OPMODE_out[1:0]==1)? M_ex : 0;  
45 assign Z_mux_out = (OPMODE_out[3:2]==3)? C_mux_out : (OPMODE_out[3:2]==2)? P : (OPMODE_out[3:2]==1)? PCIN : 0;  
46 assign {Carry_Cascode_out,PRE_ADDER_SUB_2} = (OPMODE_out[7]==0)? (X_mux_out + Z_mux_out + CIN) : (Z_mux_out-(X_mux_out+CIN));  
47 REG_MUX #(1,RSTTYPE,CARRYOUTREG) x10 (Carry_Cascode_out, CLK, RSTCARRYIN, CECARRYIN, CARRYOUT);  
48 REG_MUX #(P_WIDTH,RSTTYPE,PREG) x11 (PRE_ADDER_SUB_2, CLK, RSTP, CEP, P);  
49 assign CARRYOUTF = CARRYOUT;  
50 assign PCOUT = P;  
51 endmodule
```

```
1 module REG_MUX(in, CLK, RST, CE, out);  
2 localparam SYNC = 0, ASYNC = 1;  
3 parameter WIDTH = 18;  
4 parameter RSTTYPE = SYNC, REG = 1;  
5 input CLK, RST, CE;  
6 input [WIDTH-1:0] in;  
7 reg [WIDTH-1:0] in_reg;  
8 output reg [WIDTH-1:0] out;  
9 generate  
10     if(RSTTYPE==SYNC)begin  
11         always @(posedge CLK) begin  
12             if(RST)  
13                 in_reg<=0;  
14             else begin  
15                 if(CE)  
16                     in_reg<=in;  
17             end  
18         end  
19         always@(*)begin  
20             case(REG)  
21                 1: out=in_reg;  
22                 default:out=in;  
23             endcase  
24         end  
25     end
```

```
26     if(RSTTYPE==ASYNC)begin  
27         always @(posedge CLK or posedge RST) begin  
28             if(RST)  
29                 in_reg<=0;  
30             else begin  
31                 if(CE)  
32                     in_reg<=in;  
33             end  
34         end  
35         always@(*)begin  
36             case(REG)  
37                 1:out=in_reg;  
38                 default:out=in;  
39             endcase  
40         end  
41     end  
42 endgenerate  
43 endmodule
```

Spartan6 - DSP48A1

- Code test bench:

```
1  module test_bench();
2  reg [17:0] A, B, BCIN;
3  reg [11:0] D;
4  reg [47:0] C, PCIN;
5  reg CARRYIN, CLK, CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP;
6  reg RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP;
7  reg [7:0] OPMODE;
8  wire [35:0] M;
9  wire [47:0] P, PCOUT;
10 wire CARRYOUT, CARRYOUTF;
11 wire [17:0] BCOUT;
12 DSP48A1 x1(A, B, C, D, CARRYIN, M, P, CARRYOUT, CARRYOUTF, CLK, OPMODE, BCIN,
13 CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP, RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP, BCOUT, PCIN, PCOUT);
14 initial begin
15     CLK=0;
16     forever begin
17         #1CLK=~CLK;
18     end
19 end
20 initial begin
21     RSTA = 1;
22     RSTB = 1;
23     RSTC = 1;
24     RSTCARRYIN = 1;
25     RSTD = 1;
26     RSTM = 1 ;
27     RSTOPMODE = 1;
28     RSTP = 1;
29     A = $random;
30     B = $random;
31     C = $random;
32     D = $random;
33     OPMODE = $random;
34     PCIN = $random;
```

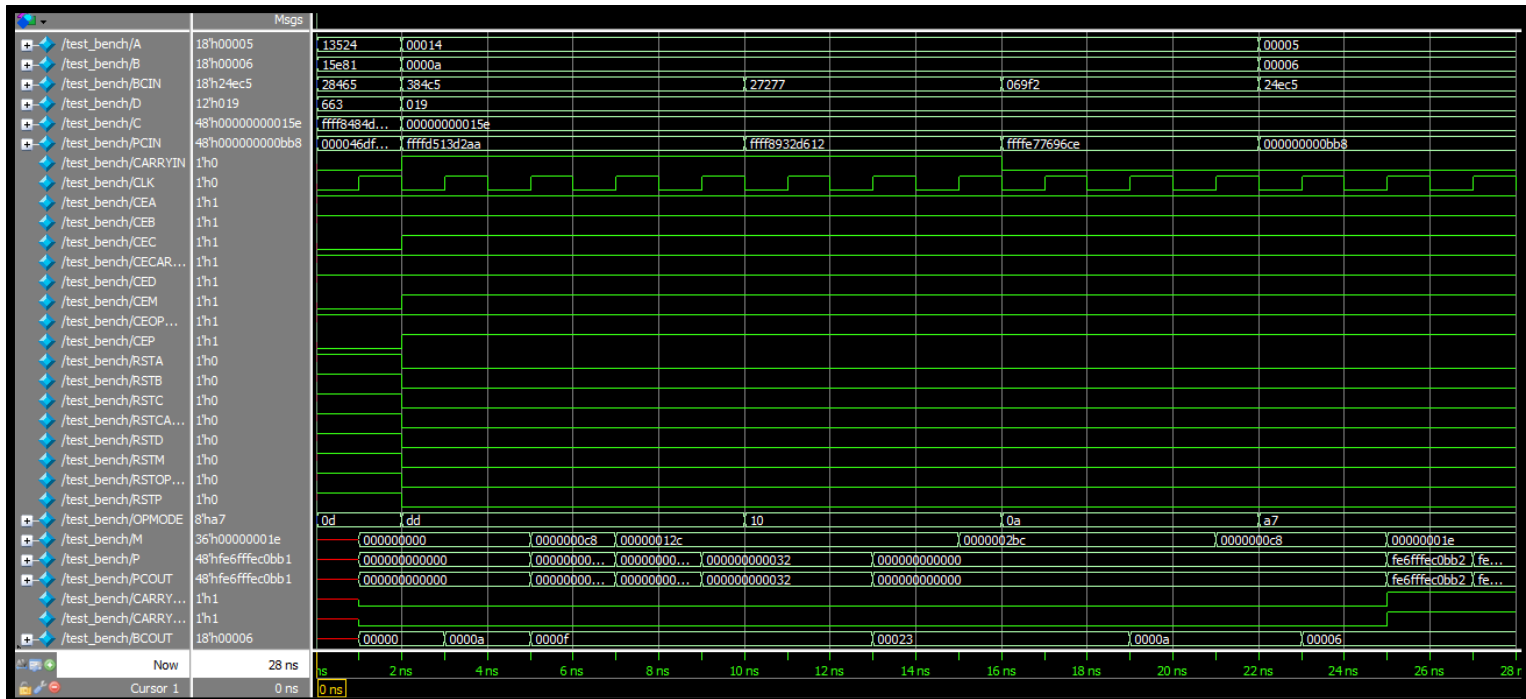
```
35     BCIN = $random;
36     CARRYIN = $random;
37     CEA = $random;
38     CEB = $random;
39     CEC = $random;
40     CECARRYIN = $random;
41     CED = $random;
42     CEM = $random;
43     CEOPMODE = $random;
44     CEP = $random;
45     @(negedge CLK);
46     if(M!=0 || P!=0 || PCOUT!=0 || CARRYOUT!=0 || CARRYOUTF!=0 || BCOUT!=0)begin
47         $display("Error");
48         $stop;
49     end
50     RSTA = 0;
51     RSTB = 0;
52     RSTC = 0;
53     RSTCARRYIN = 0;
54     RSTD = 0;
55     RSTM = 0 ;
56     RSTOPMODE = 0;
57     RSTP = 0;
58     CEA = 1;
59     CEB = 1;
60     CEC = 1;
61     CECARRYIN = 1;
62     CED = 1;
63     CEM = 1;
64     CEOPMODE = 1;
65     CEP = 1;
66
67     OPMODE = 8'b11011101;
```

```
68     A = 20;
69     B = 10;
70     C = 350;
71     D = 25;
72     BCIN = $random;
73     PCIN = $random;
74     CARRYIN = $random;
75     repeat(4)@(negedge CLK);
76     if(BCOUT!=18'hf || M!=36'h12c || PCOUT!=48'h32 || P!=48'h32 || CARRYOUTF!=0 || CARRYOUT!=0)begin
77         $display("Error");
78         $stop;
79     end
80
81
82     OPMODE = 8'b00010000;
83     A = 20;
84     B = 10;
85     C = 350;
86     D = 25;
87     BCIN = $random;
88     PCIN = $random;
89     CARRYIN = $random;
90     repeat(3)@(negedge CLK);
91     if(BCOUT!=18'h23 || M!=36'h2bc || PCOUT!=48'h0 || P!=48'h0 || CARRYOUTF!=0 || CARRYOUT!=0)begin
92         $display("Error");
93         $stop;
94     end
95
96     OPMODE = 8'b00001010;
97     A = 20;
98     B = 10;
99     C = 350;
100    D = 25;
```

```
101    BCIN = $random;
102    PCIN = $random;
103    CARRYIN = $random;
104    repeat(3)@(negedge CLK);
105    if(BCOUT!=18'h6 || M!=36'hc8 || PCOUT!=48'h0 || P!=48'h0 || CARRYOUTF!=0 || CARRYOUT!=0)begin
106        $display("Error");
107        $stop;
108    end
109
110    OPMODE = 8'b10100111;
111    A = 5;
112    B = 6;
113    C = 350;
114    D = 25;
115    BCIN = $random;
116    PCIN = 3000;
117    CARRYIN = $random;
118    repeat(3)@(negedge CLK);
119    if(BCOUT!=18'h6 || M!=36'h1e || PCOUT!=48'hfe0ffec0bb1 || P!=48'hfe0ffec0bb1 || CARRYOUTF!=1 || CARRYOUT!=1)begin
120        $display("Error");
121        $stop;
122    end
123
124    $stop;
125 end
126 endmodule
```

Spartan6 - DSP48A1

- Waveform:**



```

104 repeat(3)@(negedge CLK);
105 if(BCOUT!=18'ha || M!=36'hc8 || PCOUT!=48'h0 || P!=48'h0 || CARRYOUTF!=0 || CARRYOUT!=0)begin
106     $display("Error");
107     $stop;
108 end
109
110 OPMODE = 8'b10100111;
111 A = 5;
112 B = 6;
113 C = 350;
114 D = 25;
115 BCIN = $random;
116 PCIN = 3000;
117 CARRYIN = $random;
118 repeat(3)@(negedge CLK);
119 if(BCOUT!=18'h6 || M!=36'h1e || PCOUT!=48'hfe6fffec0bb1 || P!=48'hfe6fffec0bb1 || CARRYOUTF!=1 || CARRYOUT!=1)begin
120     $display("Error");
121     $stop;
122 end
123
124 $stop;
125 end
126 endmodule

```

```

# ** Note: $stop : test_bench.v(124)
# Time: 28 ns Iteration: 1 Instance: /test_bench
# Break in Module test_bench at test_bench.v line 124

```

```

vlib work
vlog DSP48A1.v REG_MUX.v test_bench.v
vsim -voptargs=+acc work.test_bench
add wave *
run -all
#quit -sim

```

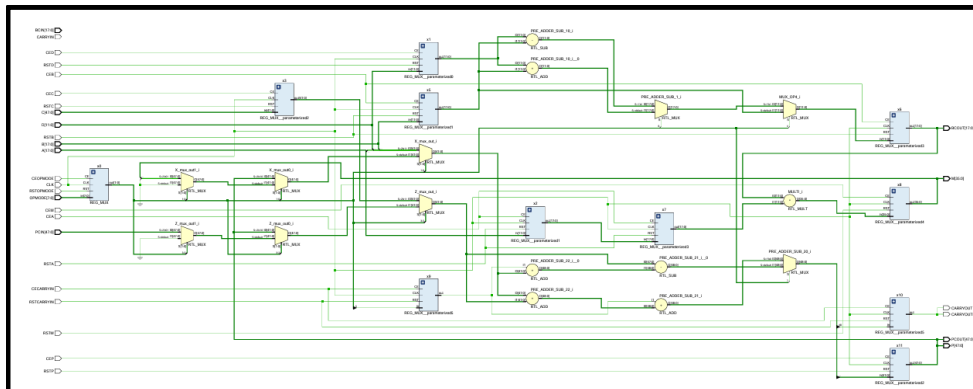
```

## Clock signal
set_property -dict { PACKAGE_PIN W5 IOSTANDARD LVCMOS33 } [get_ports CLK]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports CLK]

```

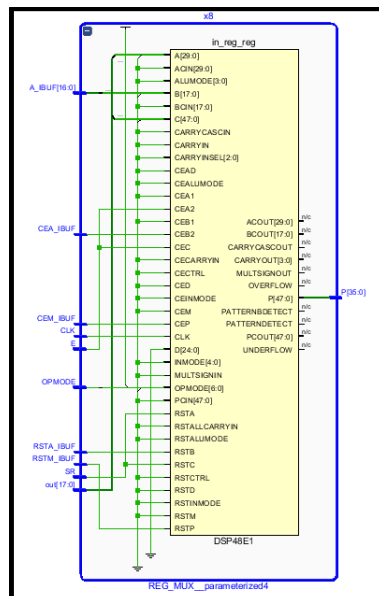
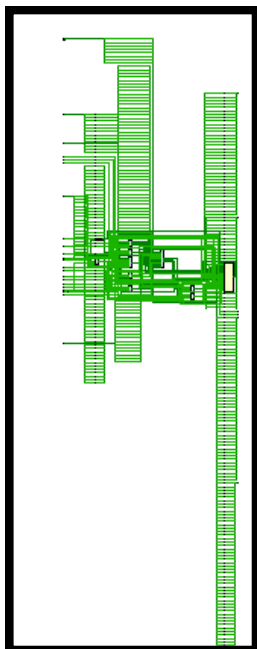
Spartan6 - DSP48A1

- Vivado:
- Elaboration:



- Elaborated Design (22 warnings, 19 infos)
- General Messages (22 warnings, 19 infos)
- [Synth 8-6157] synthesizing module 'DSP' [DSP48A1.v1] (7 more like this)
 - [Synth 8-6155] done synthesizing module 'REG_MUX' (#1) [REG_MUX.v1] (7 more like this)
 - [Synth 8-3331] design REG_MUX__parameterized1 has unconnected port CLK (21 more like this)
 - [Project 1-570] Preparing netlist for logic optimization
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.
- [Synth 8-3331] design REG_MUX__parameterized1 has unconnected port CLK (21 more like this)
- [Synth 8-3331] design REG_MUX__parameterized1 has unconnected port RST
 - [Synth 8-3331] design REG_MUX__parameterized1 has unconnected port CE
 - [Synth 8-3331] design DSP has unconnected port CARRYIN
 - [Synth 8-3331] design DSP has unconnected port BCIN[17]
 - [Synth 8-3331] design DSP has unconnected port BCIN[16]
 - [Synth 8-3331] design DSP has unconnected port BCIN[15]
 - [Synth 8-3331] design DSP has unconnected port BCIN[14]
 - [Synth 8-3331] design DSP has unconnected port BCIN[13]
 - [Synth 8-3331] design DSP has unconnected port BCIN[12]

- Synthesis:



- Synthesis (59 warnings, 34 infos)
- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200f'
 - [Synth 8-6157] synthesizing module 'DSP' [DSP48A1.v1] (7 more like this)
 - [Synth 8-6155] done synthesizing module 'REG_MUX' (#1) [REG_MUX.v1] (7 more like this)
 - [Synth 8-3331] design REG_MUX__parameterized1 has unconnected port CLK (40 more like this)
 - [Device 21-403] Loading part xc7a200fpg1156-3
 - [Project 1-236] Implementation specific constraints were found while reading constraint file D:/Digital_Design/DSP48A1/Constraints_basys3.xdc. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [XIU/DSP_proprietary.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
 - [Synth 8-5818] HDL ADVISOR - The operator resource '<adder>' is shared. To prevent sharing consider applying a KEEP on the output of the operator [DSP48A1.v34] (1 more like this)
 - [Synth 8-3332] Sequential element (x7/in_reg[16]) is unused and will be removed from module DSP. (16 more like this)
 - [Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [REG_MUX.v13]
 - [Project 1-571] Translating synthesized netlist
 - [Netlist 29-17] Analyzing 201 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-570] Preparing netlist for logic optimization (1 more like this)
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed. (1 more like this)
 - [Common 17-83] Releasing license: Synthesis
 - [Constraints 18-5210] No constraint will be written out.
 - [Common 17-1381] The checkpoint D:/Digital_Design/DSP48A1/Spartan6_DSP48A1_Project/Spartan6_DSP48A1_Project/runs/synth_1/DSP.dcp has been generated.
 - [runtcl-4] Executing : report_utilization -file DSP_utilization_synth.rpt -pb DSP_utilization_synth.pb
 - [Common 17-206] Exiting Vivado at Mon Jul 28 15:34:29 2025...

Synthesized Design (6 infos)

General Messages (6 infos)

- [Netlist 29-17] Analyzing 200 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 1 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Project 1-570] Preparing netlist for logic optimization
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.

| Name | Slice LUTs (134600) | Slice Registers (269200) | DSPs (740) | Bonded IOB (500) | BUFCTRL (32) |
|------------------------|---------------------|--------------------------|------------|------------------|--------------|
| DSP | 201 | 137 | 1 | 321 | 1 |
| dbg_hub (dbg_hub_CV) | 0 | 0 | 0 | 0 | 0 |
| u_ila_0 (u_ila_0_CV) | 0 | 0 | 0 | 0 | 0 |
| x0 (REG_MUX) | 200 | 8 | 0 | 0 | 0 |
| x1 (REG_MUX__para...) | 12 | 12 | 0 | 0 | 0 |
| x3 (REG_MUX__para...) | 0 | 48 | 0 | 0 | 0 |
| x6 (REG_MUX__para...) | 0 | 18 | 0 | 0 | 0 |
| x7 (REG_MUX__para...) | 0 | 1 | 0 | 0 | 0 |
| x8 (REG_MUX__para...) | 0 | 0 | 1 | 0 | 0 |
| x9 (REG_MUX__para...) | 2 | 1 | 0 | 0 | 0 |
| x10 (REG_MUX__para...) | 0 | 1 | 0 | 0 | 0 |
| x11 (REG_MUX__para...) | 0 | 48 | 0 | 0 | 0 |

| Setup | Hold | Pulse Width |
|--------------------------------------|----------------------------------|---|
| Worst Negative Slack (WNS): 5.512 ns | Worst Hold Slack (WHS): 0.182 ns | Worst Pulse Width Slack (WPWS): 4.500 ns |
| Total Negative Slack (TNS): 0.000 ns | Total Hold Slack (THS): 0.000 ns | Total Pulse Width Negative Slack (TPWS): 0.000 ns |
| Number of Failing Endpoints: 0 | Number of Failing Endpoints: 0 | Number of Failing Endpoints: 0 |
| Total Number of Endpoints: 106 | Total Number of Endpoints: 106 | Total Number of Endpoints: 139 |

All user specified timing constraints are met.

- Vivado:
- Implementation:



| | Name | Slice LUTs (13380) | Slice Registers (26760) | F7 Muxes (66900) | F8 Muxes (33450) | Slice (3345 0) | LUT as Logic (13380) | LUT as Memory (4620) | LUT Flip Flop Pairs (13380) | Block RAM Tile (365) | DSP (740) | Bonded IOB (500) | BUFCCTRL (32) | BSCAN#2 (4) |
|---------------------------|------|-----------------------|----------------------------|------------------------|------------------------|----------------------|-------------------------|-------------------------|--------------------------------|-------------------------|------------------|---------------------|------------------|----------------|
| ▼ DSP | | 2663 | 4178 | 96 | 6 | 1291 | 2197 | 466 | 1601 | 8 | 1 | 321 | 2 | 1 |
| > ▣ dbg_hub (dbg_hub) | | 474 | 727 | 0 | 0 | 230 | 450 | 24 | 308 | 0 | 0 | 0 | 1 | 1 |
| > ▣ u_ila_0 (u_ila_0) | | 1988 | 3314 | 96 | 6 | 1008 | 1546 | 442 | 1224 | 8 | 0 | 0 | 0 | 0 |
| ▢ x0 (REG_MUX) | | 200 | 8 | 0 | 0 | 60 | 200 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ▢ x1 (REG_MUX__para_...) | | 12 | 12 | 0 | 0 | 6 | 12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ▢ x3 (REG_MUX__para_...) | | 0 | 48 | 0 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ▢ x6 (REG_MUX__para_...) | | 0 | 18 | 0 | 0 | 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ▢ x7 (REG_MUX__para_...) | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ▢ x8 (REG_MUX__para_...) | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| ▢ x9 (REG_MUX__para_...) | | 2 | 1 | 0 | 0 | 2 | 2 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| ▢ x10 (REG_MUX__para_...) | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ▢ x11 (REG_MUX__para_...) | | 0 | 48 | 0 | 0 | 12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

```

# Transcript
# -- Compiling module DSP
#
# -- Compiling module REG_MUX
#
#
# Top level modules:
#
#     DSP
#
# End time: 16:21:22 on Jul 28,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
#

```

| Severity | Status | Check | Alias | Message | Module | Category |
|----------|--------|--------------------------|-------|---|--------|--------------------|
| | | condition_const | | Condition expression is a constant. Module DSPF, File D:\Digital_Design\GSPF4A\GSPF4A.v, Line 32 | DSP | Re Design Style |
| | | condition_const | | Condition expression is a constant. Module DSPF, File D:\Digital_Design\GSPF4A\GSPF4A.v, Line 41 | DSP | Re Design Style |
| | | parameter_name_duplicate | | Same parameter name is used in more than one module. Parameter ASYNC, Total count: 2, First mod. | DSP | Nomenclature Style |
| | | parameter_name_duplicate | | Same parameter name is used in more than one module. Parameter SYNC, Total count: 2, First mod. | DSP | Nomenclature Style |
| | | parameter_name_duplicate | | Same parameter name is used in more than one module. Parameter RSTTYPE, Total count: 2, First mo. | DSP | Nomenclature Style |