Op codes:

NO SRCs or DSTs					
NOP	000000	000	000	000	0
RET	100000	000	000	000	0
One Operands					
NOT Rdst	000001	Rdst	Rdst	XXX	0
INC Rdst	000010	Rdst	Rdst	XXX	0
DEC Rdst	000011	Rdst	Rdst	XXX	0
OUT Rdst	000100	XXX	Rdst	XXX	0
IN Rdst	000101	Rdst	XXX	XXX	0
2 operands					
SWAP Rsrc,Rdst	000110	Rdst	Rdst	Rsrc	0
ADD Rsrc1,Rsrc2,Rdst	000111	Rdst	Rsrc1	Rsrc2	0
SUB Rsrc1,Rsrc2,Rdst	001000	Rdst	Rsrc1	Rsrc2	0
AND Rsrc1,Rsrc2,Rdst	001001	Rdst	Rsrc1	Rsrc2	0
OR Rsrc1,Rsrc2,Rdst	001010	Rdst	Rsrc1	Rsrc2	0

Memory Operations					
PUSH Rdst	001011	XXX	Rsrc	XXX	0
POP Rdst	001100	Rdst	XXX	XXX	0
JZ Rsrc	001101	XXX	Rsrc	XXX	0
JMP Rsrc	001110	XXX	Rsrc	XXX	0
CALL Rsrc	001111	XXX	Rsrc	XXX	0
IMMEDIATE VALUE					
SHL Rsrc,Imm	010000	Rsrc	Rsrc	Immediate Value	0000
SHR Rsrc,Imm	010001	Rsrc	Rsrc	Immediate Value	0000
LDM Rdst,Imm	010010	Rdst	XXX	Immediate Value	0000
IADD Rsrc,Rdst,Imm	010011	Rdst	Rsrc	Immediate Value	0000
EFFECTIVE ADDRESS					
LDD Rdst,EA	010100	Rdst	XXX	Effective Address	
STD Rsrc,EA	010101	XXX	Rsrc	Effective Address	

Instructions ALU equivalent: -

Instruction	ALU OPcode
ADD (IADD)	1011
SUB	0001
AND	0010
OR	0011
NOT	0100
INC	0101
DEC	0110
SHL	0111
SHR	1000
Res = D1	1001
Res = D2	1010
Jz	1011

* Res = D1 and Res = D2 instructions **do not** change the values of the CCR

Instructions Control signals: -

		Decode		execute					Memory			writeBack					
	6 bits	1 bit		1 bit	4 bits	1bit	1 bit	1 bit	1 bit	1 bit	1 bit	1 bit	1 bit	2 bit	1 bit	1 bit	1 bit
Instruction	OP	IN?		IMM?	ALUOp	lw_ex	JZ?	JMP?	PC_or_d1	EA?	MemWrite	MemtoReg	OUT?	regWrite	PCWB	SP_SL	SP_enable
NOP	000000	0		0	1001	0	0	0	0	0	0	0	0	00	0	0	0
RET	100000	0		0	1001	1	0	0	0	0	0	0	0	00	1	1	1
NOT	000001	0		0	0100	0	0	0	0	0	0	1	0	01	0	0	0
INC	000010	0		0	0101	0	0	0	0	0	0	1	0	01	0	0	0
DEC	000011	0		0	0110	0	0	0	0	0	0	1	0	01	0	0	0
OUT	000100	0		0	1001	0	0	0	0	0	0	0	1	00	0	0	0
IN	000101	1		0	1001	0	0	0	0	0	0	1	0	01	0	0	0
SWAP	000110	0		0	1010	0	0	0	0	0	0	1	0	11	0	0	0
ADD	000111	0		0	1011	0	0	0	0	0	0	1	0	01	0	0	0
SUB	001000	0		0	0001	0	0	0	0	0	0	1	0	01	0	0	0
AND	001001	0		0	0010	0	0	0	0	0	0	1	0	01	0	0	0
OR	001010	0		0	0011	0	0	0	0	0	0	1	0	01	0	0	0
PUSH	001011	0		0	1001	1	0	0	1	0	1	0	0	00	0	0	1
POP	001100	0		0	1001	1	0	0	0	0	0	0	0	01	0	1	1
JZ	001101	0		0	1011	0	1	0	0	0	0	1	0	00	0	0	0
JMP	001110	0		0	1001	0	0	1	0	0	0	1	0	00	0	0	0
CALL	001111	0		0	1001	1	0	1	0	0	1	1	0	00	0	0	1
SHL	010000	0		1	0111	0	0	0	0	0	0	1	0	01	0	0	0
SHR	010001	0		1	1000	0	0	0	0	0	0	1	0	01	0	0	0
LDM	010010	0		1	1010	0	0	0	0	0	0	1	0	01	0	0	0
IADD	010011	0		1	1011	0	0	0	0	0	0	1	0	01	0	0	0
LDD	010100	0		0	1001	1	0	0	0	1	0	0	0	01	0	0	0
STD	010101	0		0	1001	0	0	0	1	1	1	0	0	00	0	0	0