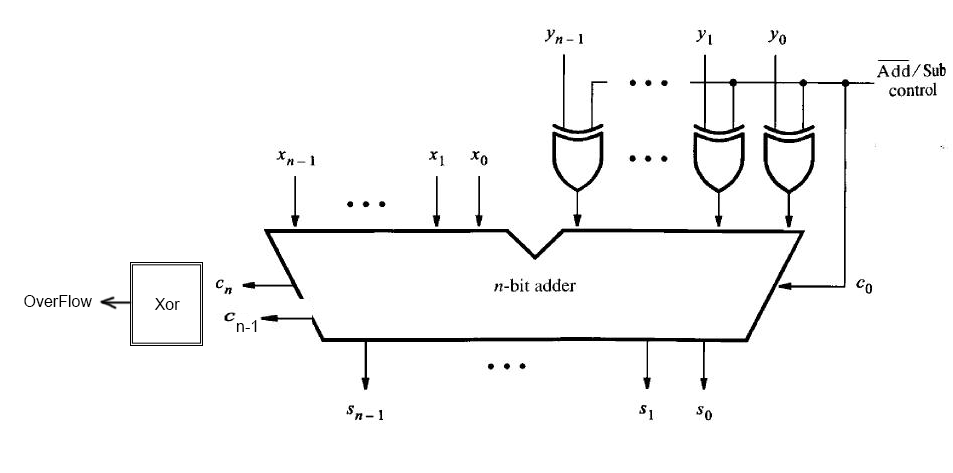
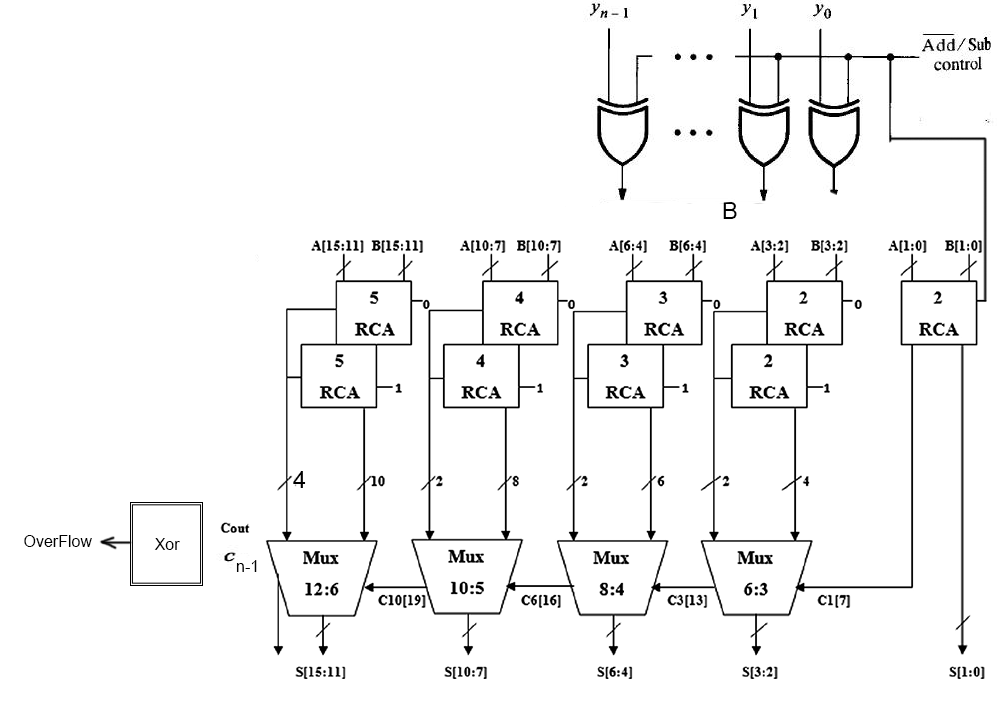
**First : Mini Modules**

**Design:**

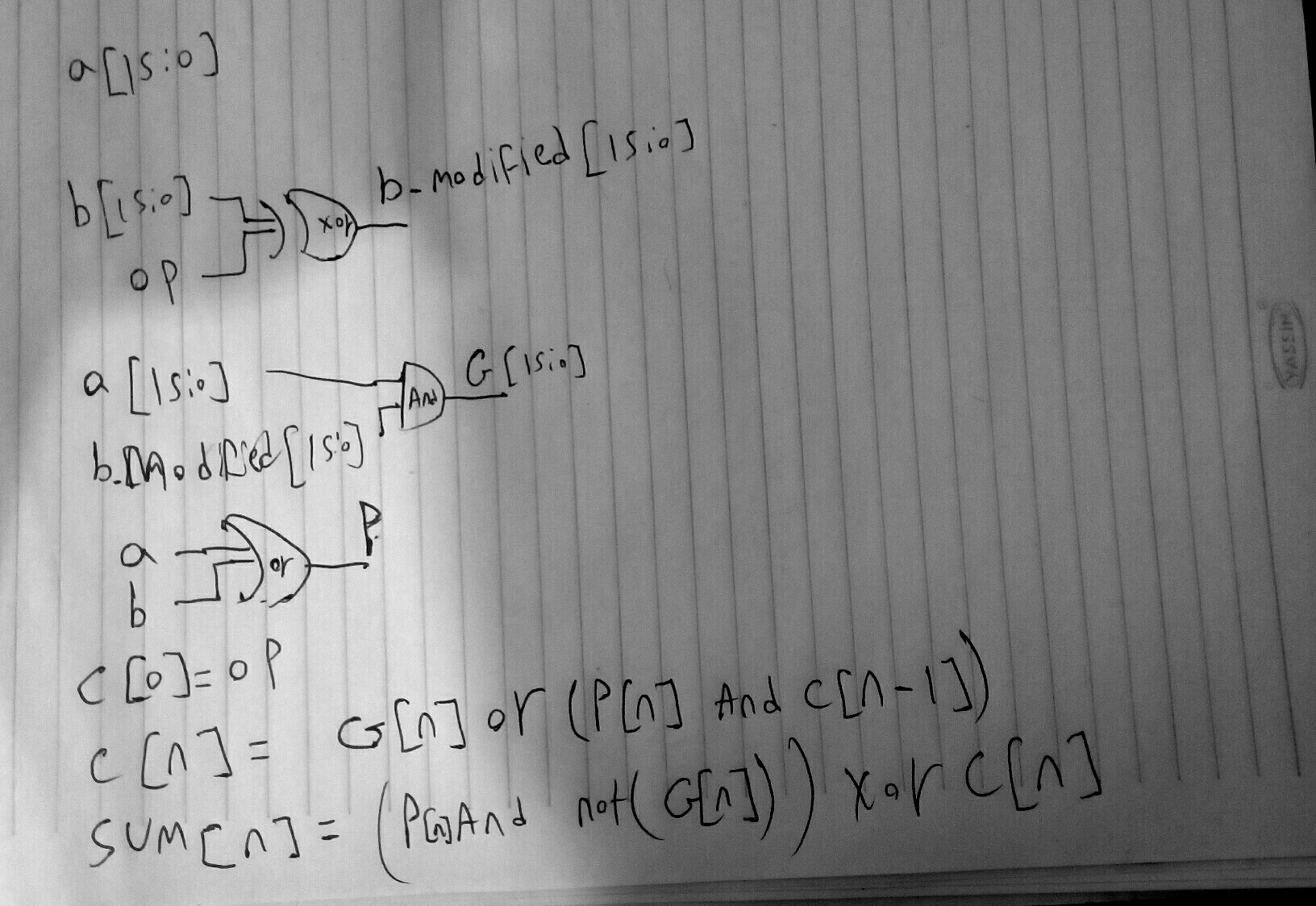
**1- Add/Sub Baseline**

****

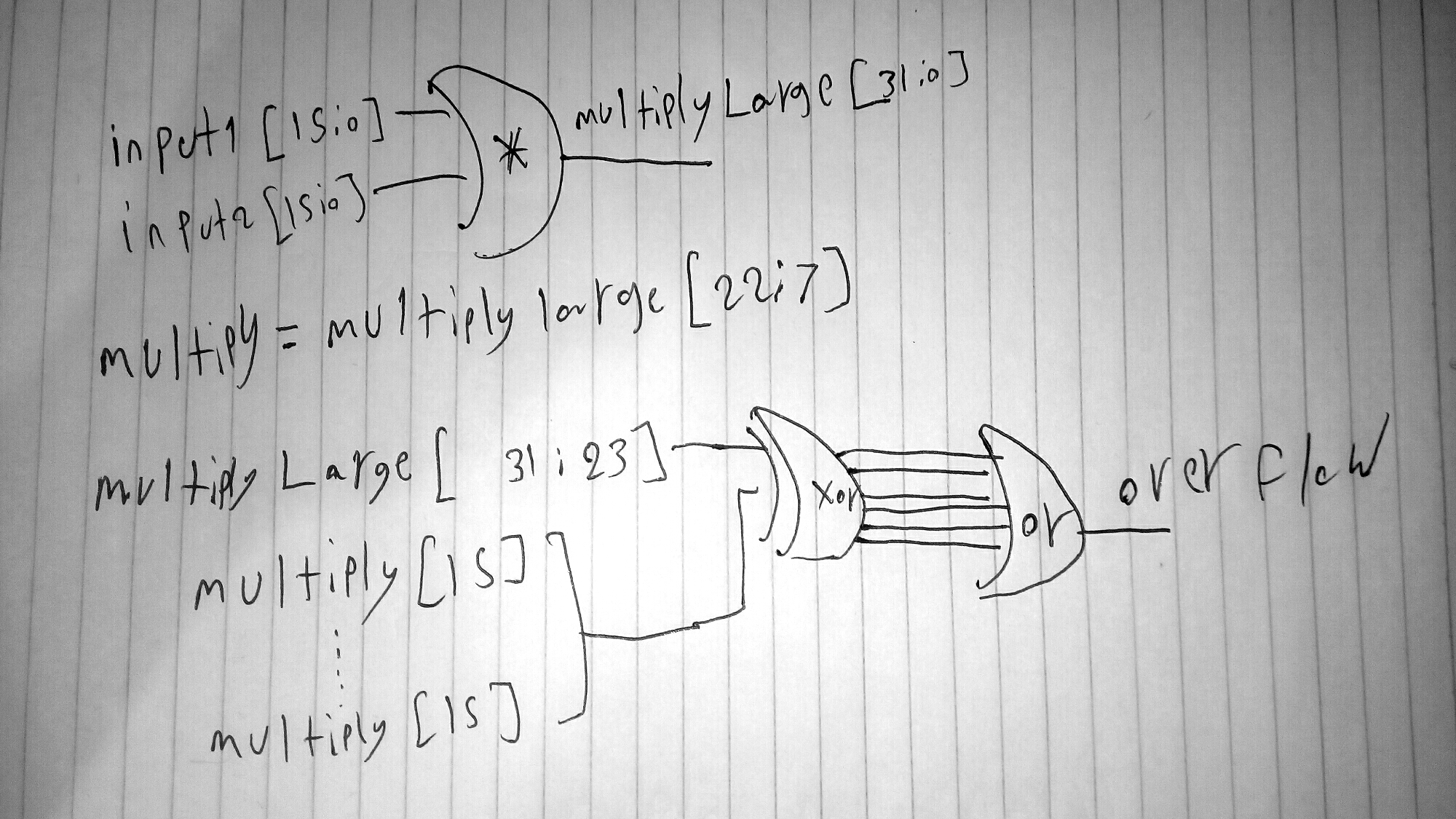
**1- Add/Sub Carry Select**

****

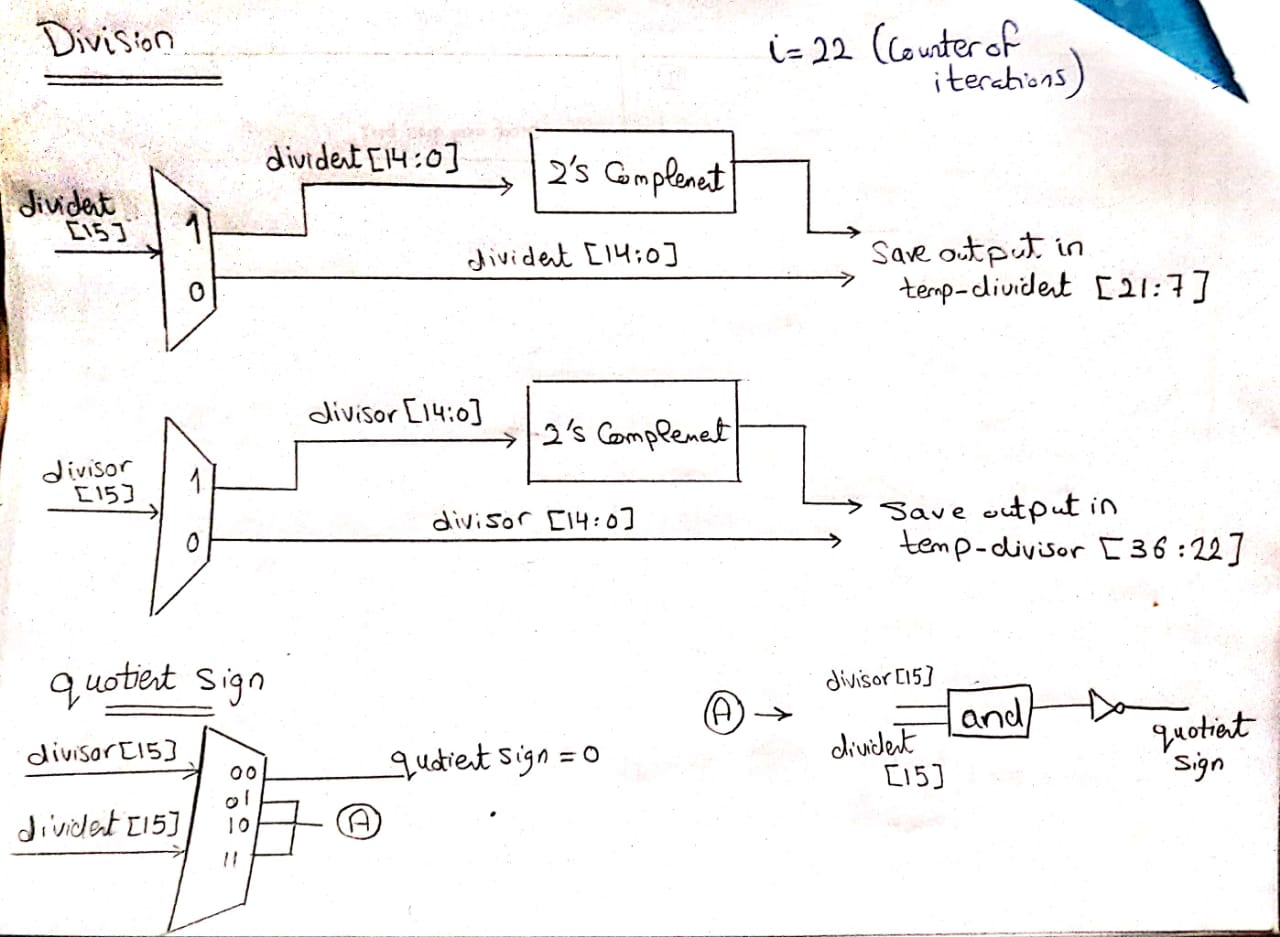
**1- Add/Sub Carry Lookahead**

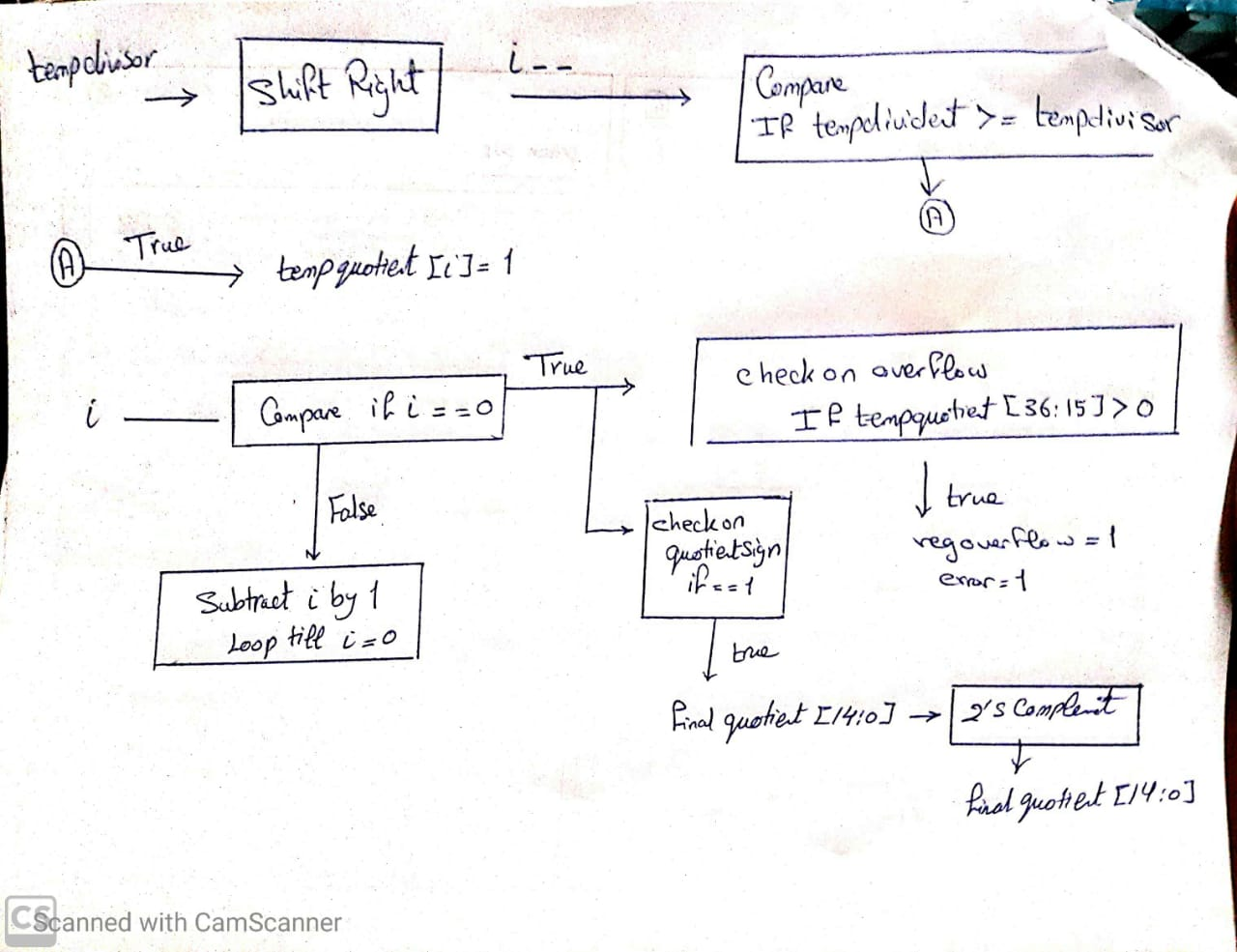
****

**2- Multiply Baseline**

****

**3- Division**

****

****

**Readme : Mini modules**

**1- Add/Sub**

Run FixedPoint\_Adder\_Baseline\_TB.do file

It will test all add/sub algorithms

**2- Multiply**

Run FixedPoint\_Multiply\_Baseline\_TB.do file

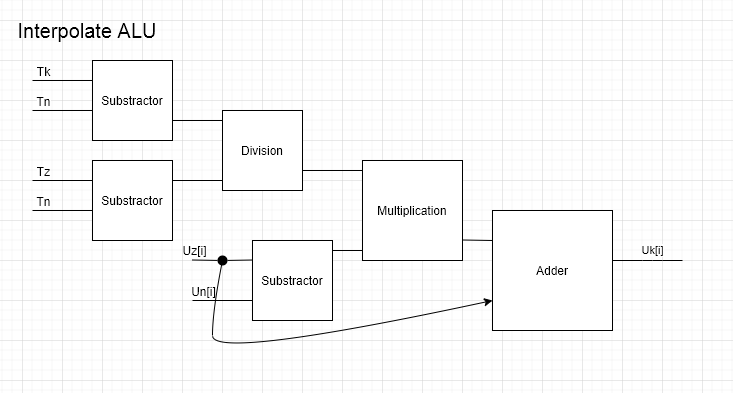
**3- Divison**

Run Division.do file

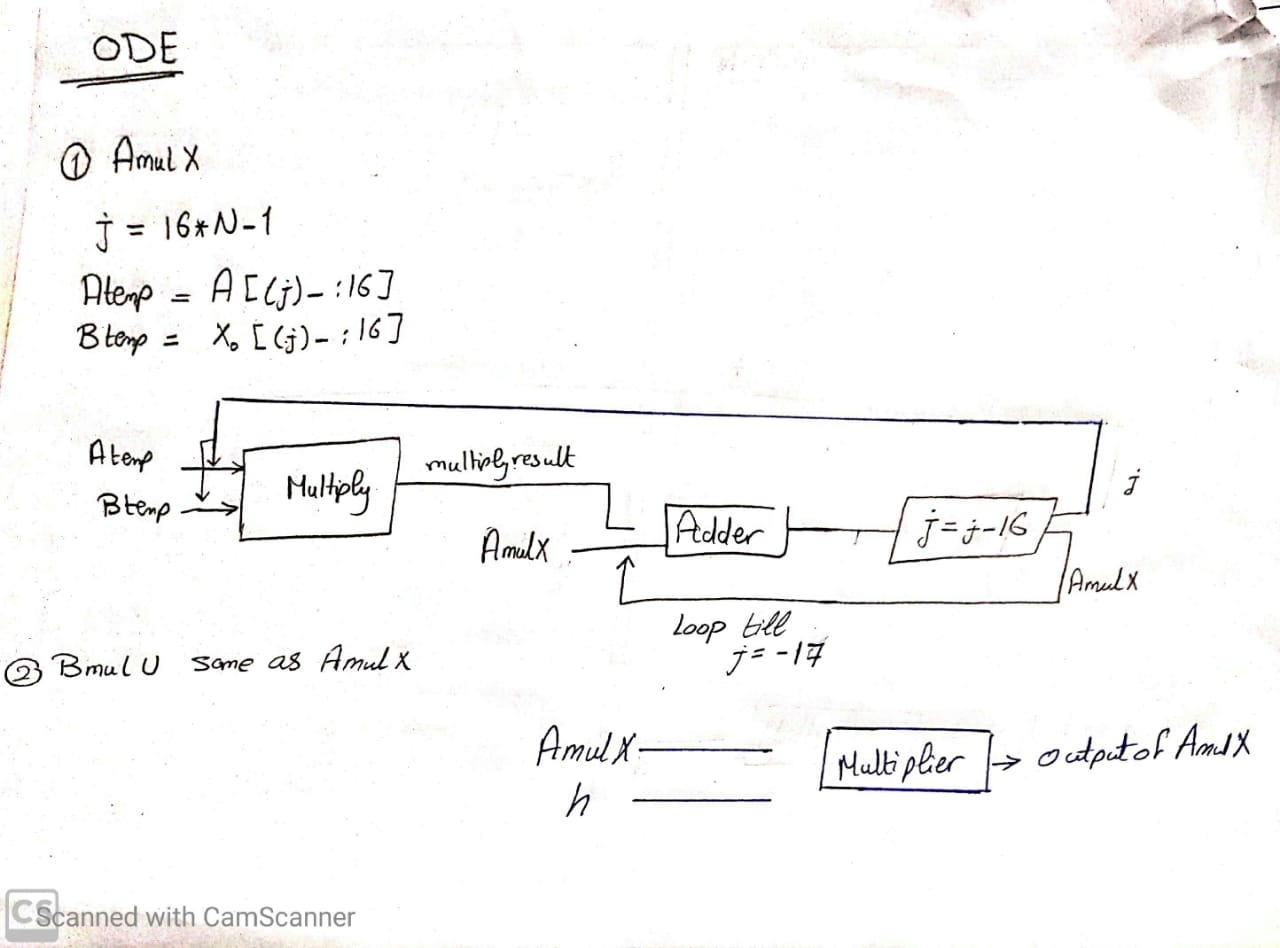
**Second: Macro Modules**

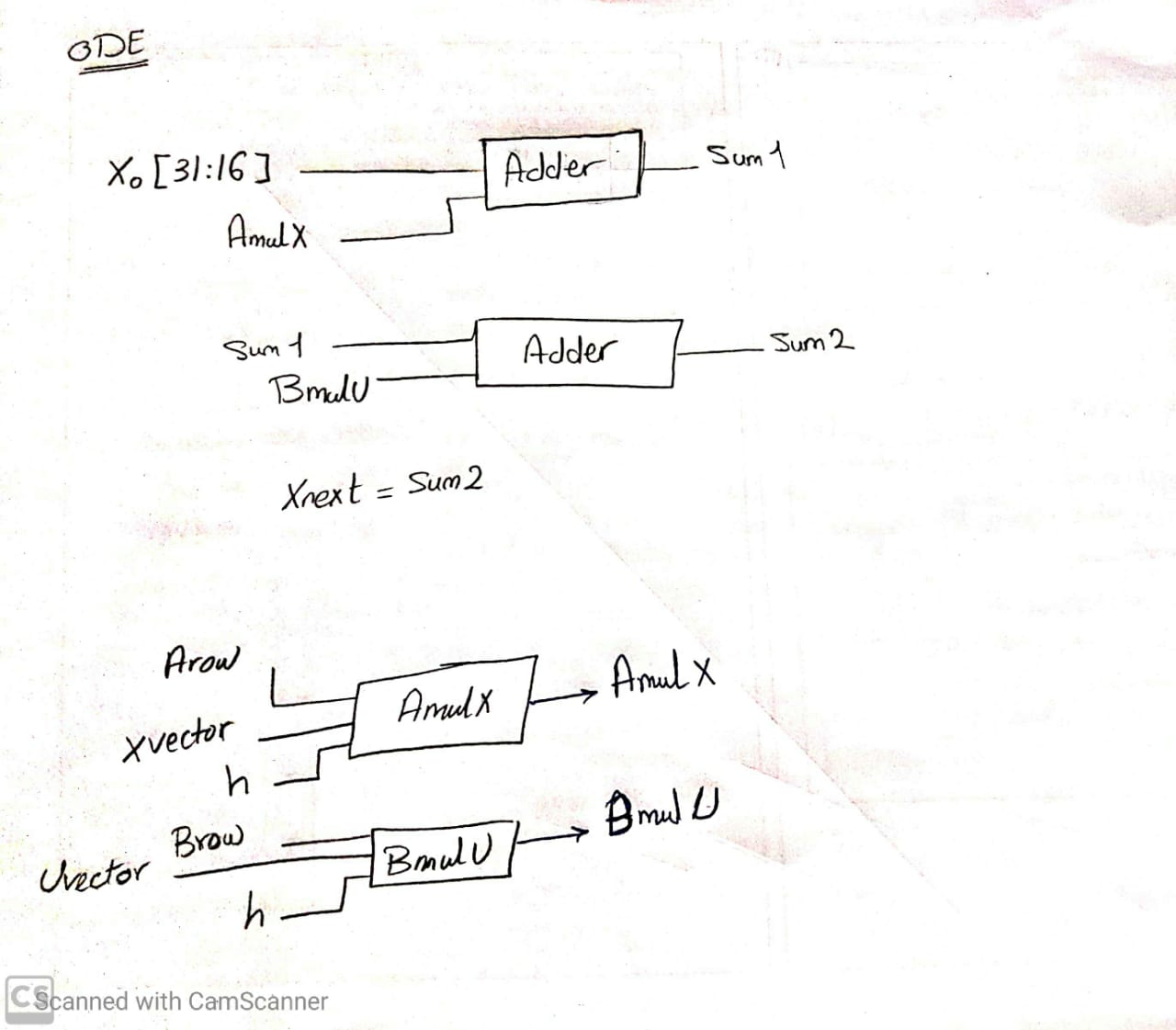
**Design**

**2- Interpolate**

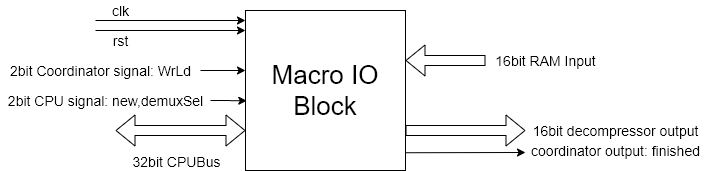
****

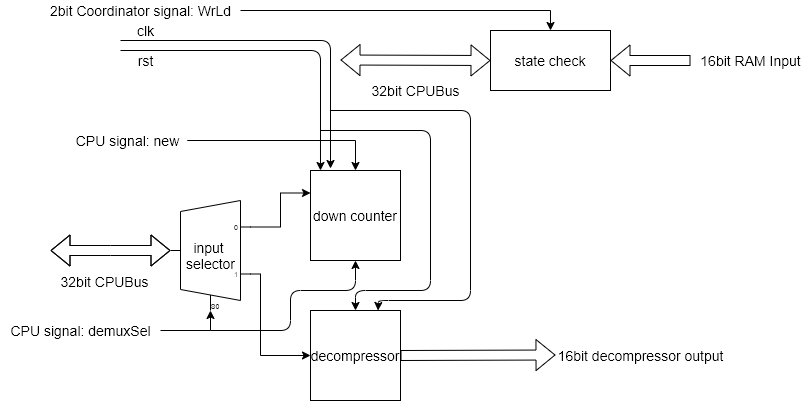
**3- ODE**

****

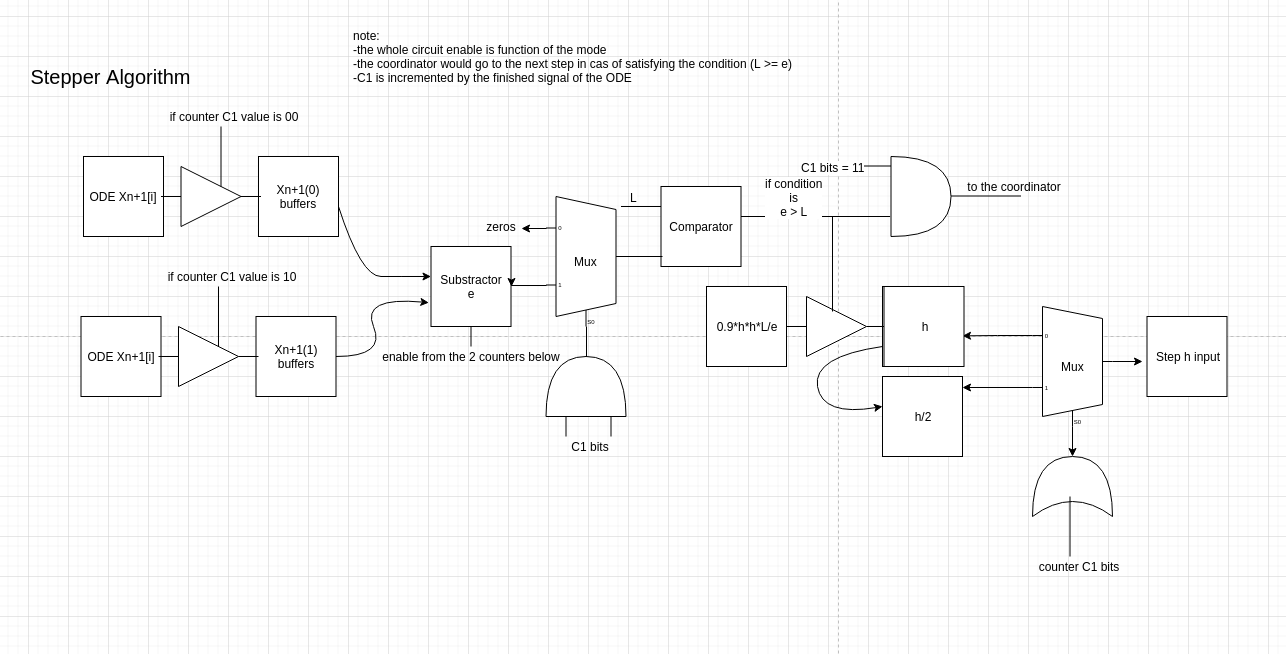
****

**4- I/O**

****

****

**5- Step**

****

**Readme : Macro modules**

**2- Interpolate**

Run interpolateALU\_TB.do file.

**3- ODE**

Run ODE.do file.

**4- I/O**

Run testiodo.do file.

**5- Step**

Run stepDo.do file.

**Task Distribution Table**

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Tasks** | **Time spent** | **Problems Faced** |
| Amira Ahmed Reda | 1.Cpu  Readjson  2.Synthesize all the files | 2 days continued (about 6~8 hours aday)  1 day (more than 6 hrs) | Too much problems on searching and errors and problems with understanding  Synthesize was hard because every edit they made i re synthesize again and again too many times |
| Khaled Amgad | 1- adder/sub baseline  2- adder/sub carry select  3- adder/sub carry lookahead  4- adder/sub testbench to test all of them  5- Software equivalent for adder/sub.  6- Multiply baseline  7- Multiply testbench  8- Software equivalent for Multiply.  9- Interpolator  10- Interpolator testbench  11- Software equivalent for Interpolator .  12- handle overflow(error) in adder/sub , Multiply and Interpolator  13- Division baseline  14- Division baseline testbench | 1 hour  2 hours  2 hours  4 hours  0.5 hour  0.5 hour  0.5 hour  0.5 hour  1 hour  4 hour  1 hour  4 hour | 1-adder/sub( overflow )  2- Multiply (overflow ) |
| Sarah Mohamed Ahmed Lotfy | 1- Division  2- Division test bench  3- ODE  4- ODE test bench  5- Software equivalent for division.  6- Software equivalent for ODE. | 4 days  3 hours  1 day  4 hours  1 day  3 hours | 1- Searching for Division algorithm and understanding the long division of fixed points.  2- Handling signed fixed in division.  3- Handling overflow in division.  4- Handling how to get vector as input in verilog.  5- In software equivalent handling sign of quotient. |
| Sherif Essam | postponed | postponed | postponed |
| Kareem Omar | 1- I/O micro modules 2- I/O macro design  3- I/O block integration | 1 day  1 week  3 days (joint effort) | -macro design was difficult due to uncertainties in the overall design flow |
| Marc Nagui | 1- decompression block in I/O  2- I/O block integration | 2 days  3 days (joint effort) | -the decompression took a lot of thinking time  -putting results in the same reg |
| Muhammed Ayman | 1-Ram (ram module,testbench)  2-Step Circuit (step module, do file , software equivalent) | 5 days average 8 hours/day | -synthesis |

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Time**  Data arrival time: | **Power**  Total Power(uw): | **Area**  Chip Size (mm x mm) |
| FixedPoint AdderSub Baseline | 868.7 | 146.196686 | 0.073 x 0.073 |
| FixedPoint AdderSub CarrySelect | 786.1 | 280.766724 | 0.075 x 0.075 |
| FixedPoint AdderSub CarryLookAhead | 796.1 | 258.536224 | 0.074 x 0.074 |
| FixedPoint Multiply Baseline | 1021.7 | 1989.856812 | 0.106 x 0.106 |
| down\_counter |  | 222.692322 | 0.086 x 0.086 |
| Demux |  | 401.339539 | 0.077 x 0.077 |
| Decom |  | 357.306244 | 0.086 x 0.086 |
| ODE |  | 5063.750488 | 0.158 x 0.158 |
| FixedPoint Division Baseline | 4500.2 | 7620.921875 | 0.135 x 0.135 |
| InterpolateALU | 4773.8 | 11297.319336 | 0.152 x 0.152 |