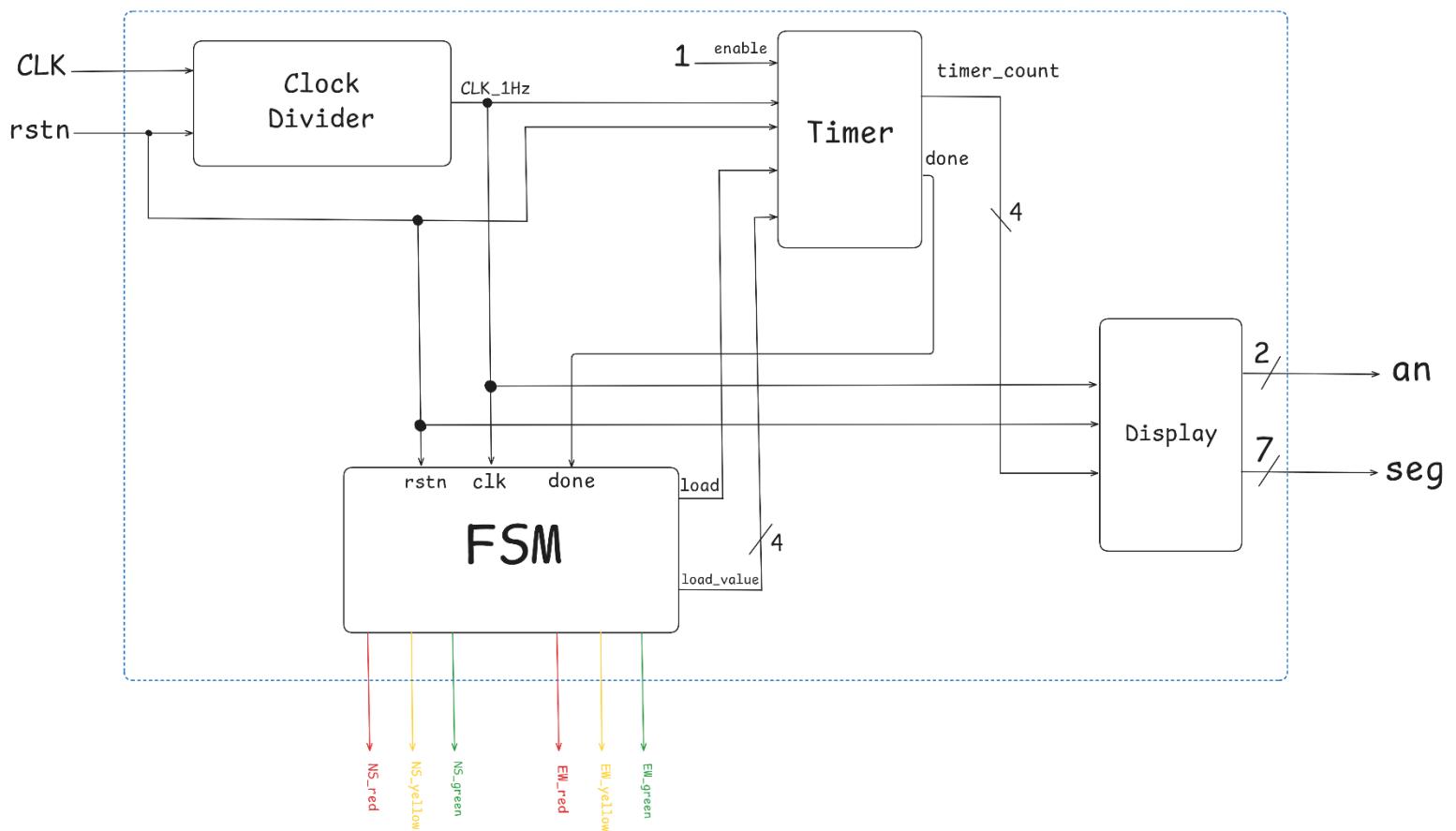
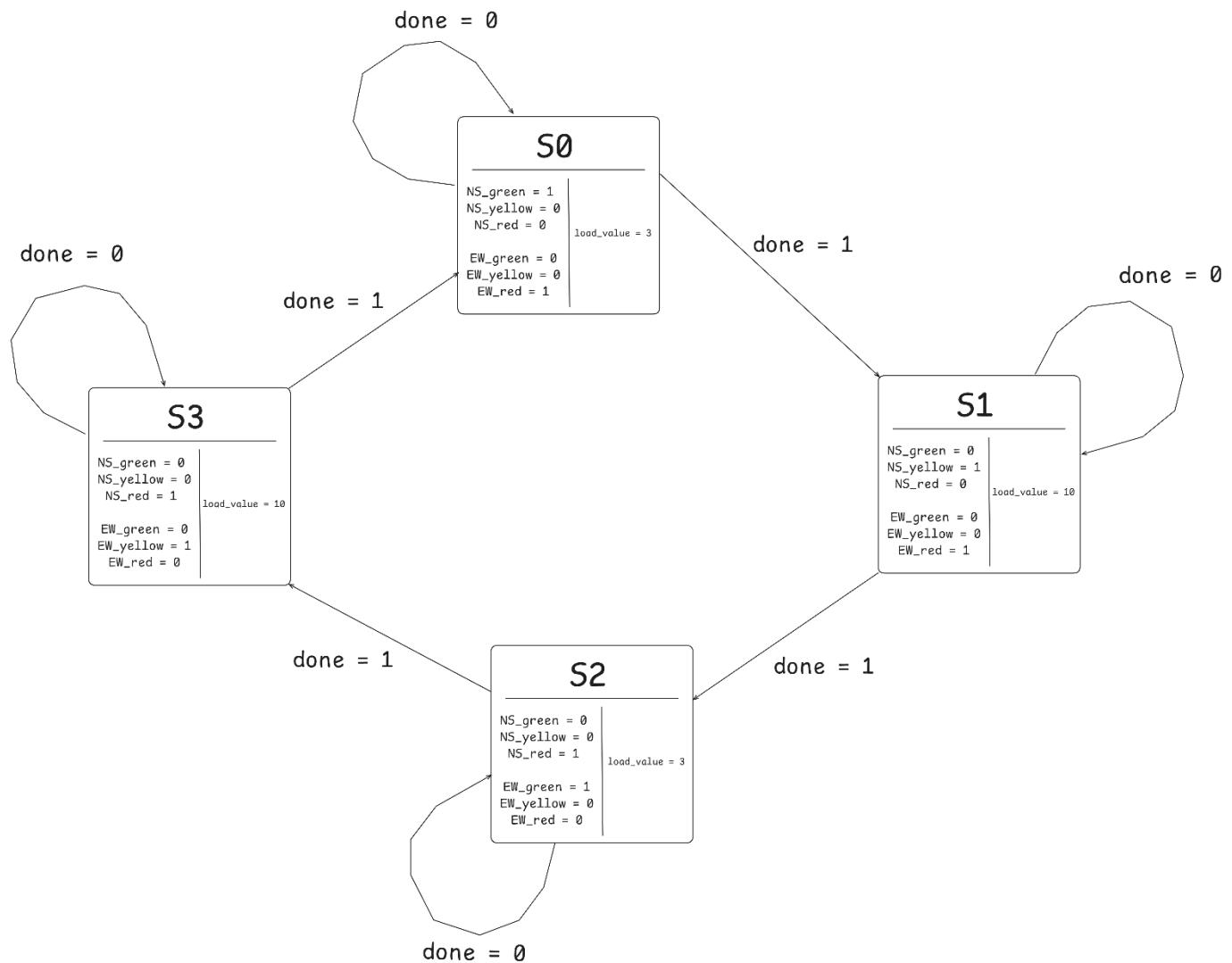


Traffic Light Controller

1- Block Diagram:



2- FSM state diagram:



3- Timing Diagram:



4- Pin mapping table:

Port	Description
clk	100 MHz clock signal
Clk_1Hz	1 Hz clock signal Note: used 10 times divided clock for the simulation purpose
rstn	Active low reset signal
Load	Signal to load the value into the timer
load_value	Loading value to the timer
Timer_count	Counting down values in decimal
State_reg	Current state
NS_red	North-South traffic lights
NS_yellow	
NS_green	
EW_red	East-West traffic lights
EW_yellow	
EW_green	
Seg	FPGA's 7-segment inputs
an	Select which 7-segment is active

5- Simulation explanation:

At the beginning, the reset signal is asserted, which forces the controller into state 0.

- **State 0:**

In this state, the North–South (NS) green light is ON, while East–West (EW) remains red. At the same time, the timer is loaded with a value of 10, and it begins counting down at the 1 Hz clock rate.

When the countdown finishes, the controller transitions to state 1.

- **State 1:**

Here, the timer is loaded with 3, and the NS yellow light is turned ON. The timer counts down again until it reaches 0.

After this, the controller moves to state 2.

- **State 2:**

The timer reloads with 10, the EW green light turns ON, and the NS light turns red. The timer continues to count down to 0.

Once the countdown completes, the system enters state 3.

- **State 3:**

The timer is loaded with 3, and the EW yellow light is turned ON. After the timer reaches 0, the system returns to state 0, where NS green is ON, EW red is ON, and the cycle repeats.

Notes:

- **Timer_loaded & initial_load signals:** are used for fixing the initial reset and load signal for not toggling to state1.
- Merged North with South and East with West each into one signal and with every light color for simplification.

6- FPGA test results:

- Using Nexys4DDR_Master FPGA kit.

- Utilization reports:

Tcl Console | Messages | Log | Reports | Design Runs | **Utilization** x Timing |

Hierarchy

- Summary
- > Slice Logic
- Memory
- DSP
- > IO and GT Specific
- ▽ Clocking
 - BUFGCTRL (3%)
- Specific Feature

Utilization

Name	1	Slice LUTs (63400)	Slice Registers (126800)	Bonded IOB (210)	BUFGCTRL (32)
Top_module	23	22	17	1	
clk_div_inst (clk_divider)	3	5	0	0	
display (two_digit_disp...)	1	9	0	0	
fsm (Traffic_light_contr...	9	4	0	0	
timer_inst (timer)	10	4	0	0	

Tcl Console | Messages | Log | Reports | Design Runs | **Utilization** x Timing |

Summary

Hierarchy

- Summary
- > Slice Logic
- Memory
- DSP
- > IO and GT Specific
- ▽ Clocking
 - BUFGCTRL (3%)
- Specific Feature
- Primitives
- Black Boxes
- Instantiated Netlists

Utilization

Resource	Utilization	Available	Utilization %
LUT	23	63400	0.04
FF	22	126800	0.02
IO	17	210	8.10

Utilization (%)

- **Timing Summary:**

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | **Timing** |

Q | X | ▲ | ● |

General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (70)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 8.582 ns	Worst Hold Slack (WHS): 0.295 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 5	Total Number of Endpoints: 5	Total Number of Endpoints: 6

All user specified timing constraints are met.