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Experiment in Electrical engineering, ET061G

by Khaled Hamza

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Purpose

The purpose of this experiment is to simplify the understanding of logic gates and develop the ability to derive equations and construct circuits based on given input and output lists.

Theory

Task1: Datasheets for IC are widely available, but knowing the IC number makes it easier to find the right information quickly without unnecessary searching.

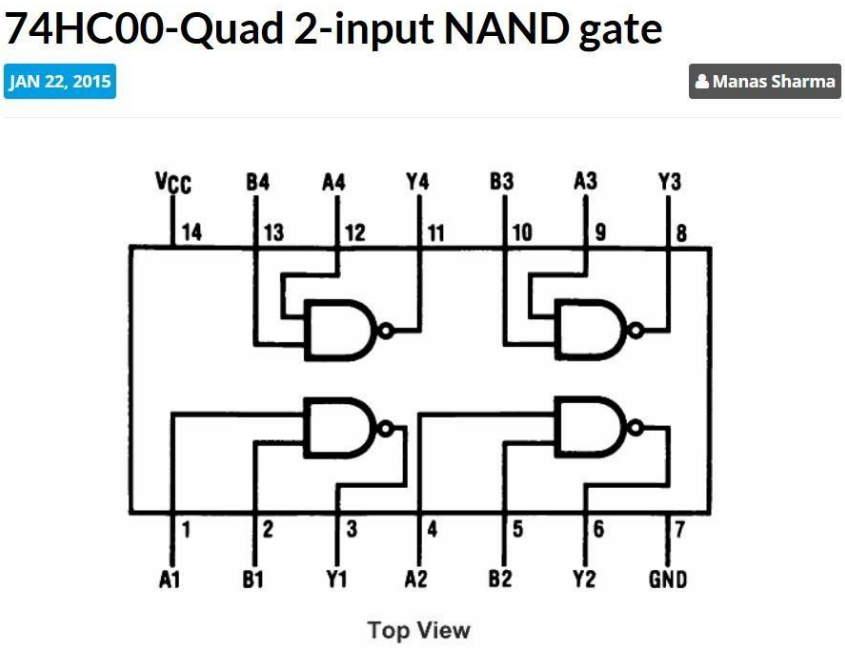

Figure 1: A sketch of a logical NAND gate (74x00) [1]

IC:s have different properties based on their designation. For instance, the 74x00 (refer to the image above) is a Quad 2-input NAND circuit, meaning it contains 4 separate NAND gates. Each gate has 2 inputs and 1 output. In contrast, the 74x10 has 3 outputs and 3 inputs for each output. The circuit depicted in the image contains 14 pins numbered from 1 to 14. Pins labeled A and B serve as the inputs corresponding to the number that follows, while Y indicates the result of A and B. Since this is a transistor-transistor logic circuit, a power source is required; in this case, the source should be connected to pin 14, and the ground should be connected to pin 11.
[2]

Task2: through 5 must be solved step by step to ensure the correct answer for each task. Task 2 requires finding the minimal function for the following:

$$f(A, B, C, D) = \sum (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$$

The function was simply found by using a Karnaugh-diagram:

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$F(A,B,C,D) = \Sigma(0,1,2,4,5,6,8,9,12,13,14)$

we have four variables $2^4 = 16$, two choices (0 or 1)

A	B	C	D	Binary	Decimal
0	0	0	0	0000	0
0	0	0	1	0001	1
0	0	1	0	0010	2
0	1	0	0	0100	4
0	1	0	1	0101	5
0	1	1	0	0110	6
1	0	0	0	1000	8
1	0	0	1	1001	9
1	1	0	0	1100	12
1	1	0	1	1101	13
1	1	1	0	1110	14

Karugh-diagram of (A, B, C, D)

A and B → control the rows

C and D → control the columns

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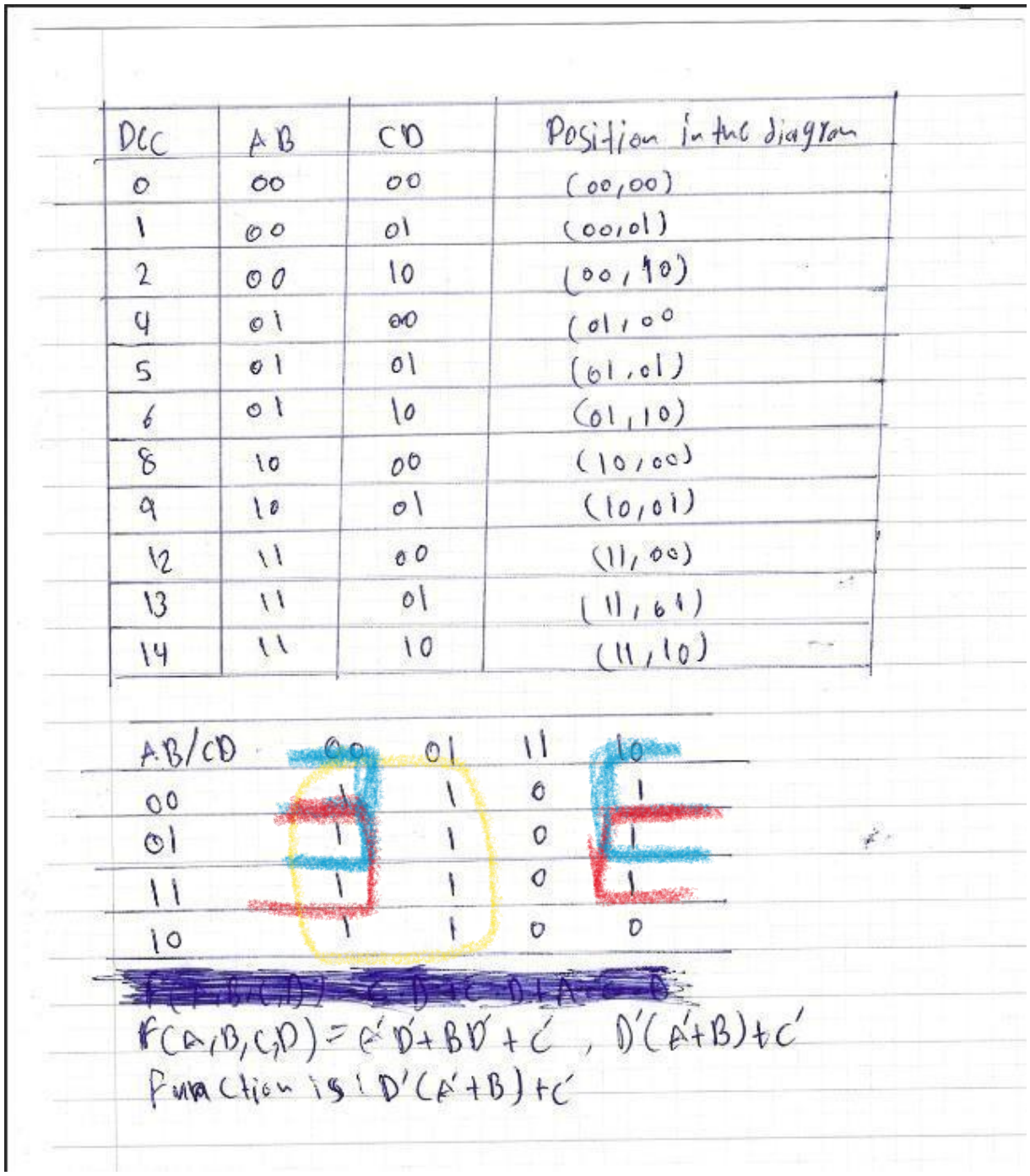

DCC	AB	CD	Position in the diagram
0	00	00	(00,00)
1	00	01	(00,01)
2	00	10	(00,10)
4	01	00	(01,00)
5	01	01	(01,01)
6	01	10	(01,10)
8	10	00	(10,00)
9	10	01	(10,01)
12	11	00	(11,00)
13	11	01	(11,01)
14	11	10	(11,10)

AB/CD	00	01	11	10
00	1	1	0	1
01	1	1	0	1
11	1	1	0	1
10	1	1	0	0

F(A,B,C,D) = A'D'+BD'+C' , D'(A'+B)+C'
Function is: D'(A'+B)+C'

The function was: D´(A´+ B) + C´.

1. **Gul grupp** (C=0): Ger termen C'.
2. **Blå grupp** (D=0, A=0): Ger termen D'A'.
3. **Röd grupp** (D=0, B=1): Ger termen D'B.

Dessa två sista termer kombineras till D'(A'+B) och tillsammans med C', får vi den minimerade funktionen F=D'(A'+B)+C'

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Task3: The circuit will appear as shown in the image below after being implemented in Logic.ly.

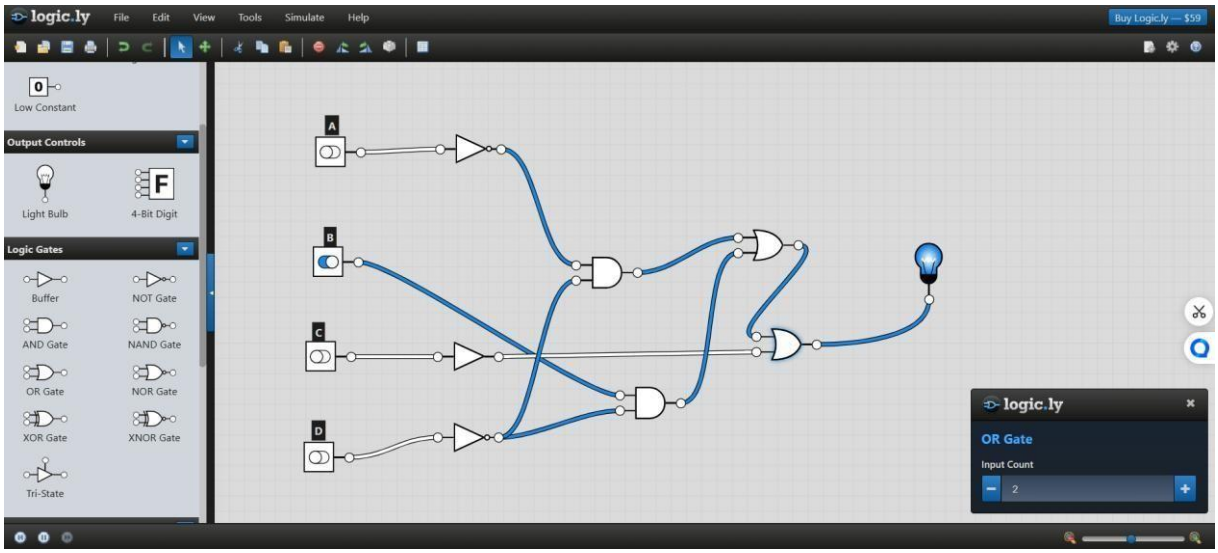

Figure 2: Implementation of the function in logic.ly [3]

Task4: The following figure presents a circuit diagram for the function.

The circuit is constructed using the following TTL chips:

1. 74x04 (NOT gate)
2. 74x08 (AND gate)
3. 74x32 (OR gate)

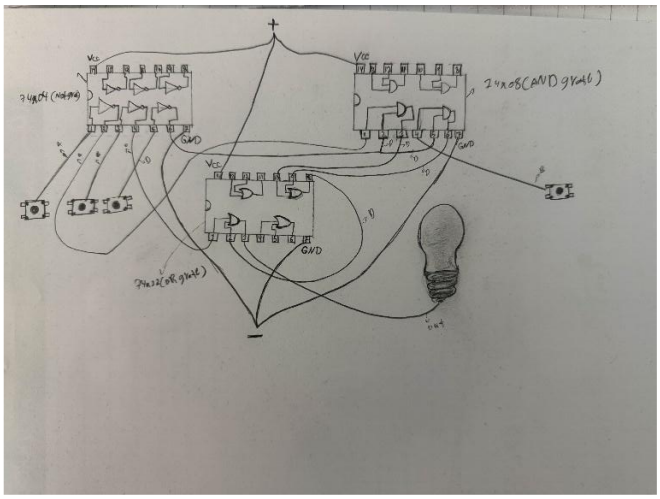

Figure 4: Circuit diagram for the function

Task 5: The last task involved implementing the circuit on a breadboard using the ICs 74x04 (NOT), 74x08 (AND), and 74x32 (OR). Only one circuit of each logical gate was necessary since each IC has multiple outputs—specifically, the NOT gate has 6 outputs while the AND and OR gates have 4

outputs each. This allows for the same IC to be reused in different parts of the circuit. It's important to know that the breadboard had certain pins connected together both vertically and horizontally, which facilitated easier connections throughout the circuit. The following image illustrates how the circuit appeared after all connections were made:

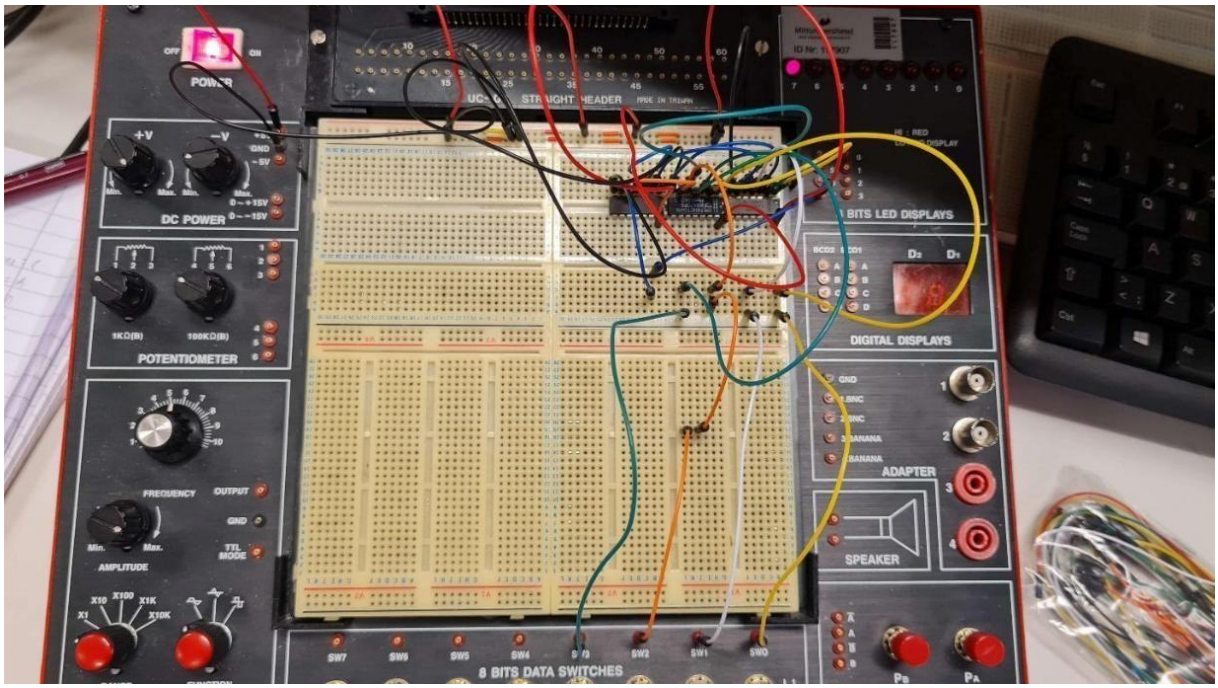

Figure 5: Implementation of the function on a breadboard

References:

[1] https://www.bragitoff.com/2015/01/74hc00-quad-2-input-nand-gate/

[2] https://en.wikipedia.org/wiki/List_of_7400-series_integrated_circuits

[3] https://logic.ly/demo/